Increasing DG Penetration in Multiphase Distribution Networks Considering Grid Losses, Maximum Loading Factor and Bus Voltage Limits

Journal:	*IET Generation, Transmission & Distribution*
Manuscript ID:	GTD-2011-0841.R1
Manuscript Type:	Research Paper
Date Submitted by the Author:	10-May-2012
Complete List of Authors:	Juanuwattanakul, Parachai; Sripatum University, Electrical Engineering Masoum, Mohammad; Curtin University of Technology , Electrical and Computer Engineering
Keyword:	DISTRIBUTION NETWORKS, POWER SYSTEMS, POWER SYSTEM STABILITY

Increasing DG Penetration in Multiphase Distribution Networks Considering Grid Losses, Maximum Loading Factor and Bus Voltage Limits

Parachai Juanuwattanakul[1] and Mohammad A.S. Masoum[2]

parachai.ju@spu.ac.th m.masoum@curtin.edu.au

[1]Department of Electrical Engineering, Sripatum University, Bangkok, Thailand.

[2]Department of Electrical and Computer Engineering, Curtin University, Perth, WA, Australia.

Abstract- This paper proposes a new iterative algorithm to improve the performance of multiphase distribution networks by proper placement and sizing of DG units and single-phase capacitors. The approach consists of utilizing the positive-sequence voltage ratio $V_{collapse}/V_{no\text{-}load}$ to identify the weakest three-phase and single-phase buses for the installation of DG units and shunt capacitors, respectively. DG penetration levels are increased by evaluating their impacts on voltage profile, grid losses, and voltage stability margin while considering the voltage limits at all buses. Detailed simulations are performed for the placement and sizing of a doubly-fed induction generator (DFIG) and single-phase capacitors in the IEEE multiphase 34 node test feeder using the DIgSILENT PowerFactory software. The impacts of DFIG on voltage profile, active power loss, maximum loading factor and voltage unbalance factor are highlighted.

Index Terms- Multiphase network, weakest bus, DG, DFIG, voltage profile, voltage limit, grid loss, and maximum loading factor.

1. INTRODUCTION

The present integration of Distributed Generation (DG) units in power systems has many advantages, but also challenges the performance of the old networks. Integration of DGs at low penetration levels can have a variety of benefits such as loss reduction, voltage regulation improvement, and voltage stability enhancement [1-4]. The main challenges are determination of optimal locations and penetration levels of DG units which can easily be absorbed in the system without major structural changes while keeping all bus voltage levels within permissible limits. Even though DGs offer a variety of benefits, they may also impose some problems and limitations at high penetration levels such as overvoltage conditions and increased grid losses [2, 5]. Most studies confirm that about 10 to 50% penetration of DG can be safely absorbed in the electricity network [6-8]. Therefore, it seems reasonable to expect that adequate integration of DG to the utility grid at appropriate locations improves the voltage profile and enhances the voltage stability while reducing active and reactive losses [9].

As the penetration level of DG increases, the above mentioned problems become highly significant. This will eventually require voltage stability analysis to ensure a proper and reliable operation of the power system with large amounts of DG [10-11]. When the power system becomes stressed (e.g., as a result of load increasing), voltage instability can easily occur. This type of voltage instability mostly occurs at the weakest bus [12]. Therefore, both the location and the penetration level of DG become a challenging task for system planning and operation. Several methods for DG placement in balanced three-phase networks have been proposed including voltage sensitivity analysis [11], continuation power flow for determination of the most sensitive bus to voltage collapse [13], voltage stability index [3], and artificial intelligence based optimization approaches [3, 14]. There are only two approaches for DG placement in multiphase networks based on the voltage profile and grid loss calculations [15] and the unbalanced voltage variance index is utilized in [16]. However, these references do not consider the maximum loading factor (MLF) and

bus voltage limits in their approaches. References [11, 14, 17] show that the sizes and locations of DG units can significantly influence the voltage profile and should be well planned to maintain the node voltages within permissible limits.

Detailed analyses of unbalanced/multiphase networks based on continuation three-phase power flow show that the three PV curves on each phase for the unbalanced networks are different [18-20]. Therefore, to determine the voltage stability margins, the method of symmetrical components has been applied to merge the three PV curves to one PV curve based on the positive-sequence voltage. In addition, to extend and generalize the conventional definition of bus voltage ranking index for multiphase networks, symmetrical components are also applied to the three-phase voltages resulting from three-phase power flow [21].

Furthermore, the degree of unbalance is influenced primarily by loads. As the variation in loads and DG (wind) are non-deterministic in nature, optimization approaches for DG placement and sizing should also focus on the stochastic aspect of the nature of the problem. There have been interesting research work on modeling stochastic nature of wind generators in optimal power flow setting and statistically characterizing the demand for network state estimation computation through Gaussian expectation measurement [22-24].

This paper expands the well-known voltage index V/V_0 for balanced three-phase systems [25-26] and defines an improved positive-sequence voltage index of $V_{collapse}/V_{no\text{-}load}$ to identify the weakest buses in multiphase distribution networks. For the first time an iterative algorithm is proposed to accurately increase the DG penetration in unbalanced multiphase networks in order to improve grid losses while considering MLF and bus voltage limits. The proposed iterative algorithm for the placement and sizing of DG units and single-phase capacitors in multiphase networks will reduce grid losses, increase MLF and decrease the voltage unbalance factor (VUF) [27] while keeping all bus voltage within acceptable limits. Simulation results including locations and the maximum penetration levels of DG units as well as the locations and sizes of single-phase capacitors are presented for the IEEE multiphase 34 node test feeder [28] using the DIgSILENT PowerFactory software [29].

2. BUS RANKING OF MULTIPHASE DISTRIBUTION NETWORKS

The approach taken in this study is utilizing the bus voltage ranking index to identify the weakest buses in multiphase distribution networks. This section starts with the definition and derivation of the conventional voltage ranking index (VRI) V/V_o using the two bus balanced network of Fig. 1 and continues to extend its application to multiphase networks using symmetrical components [21].

The conventional VRI is defined for balanced three-phase networks [25-26]:

$$VRI_j^{conventional} = \frac{V}{V_o} = \frac{V_{j,base-load}}{V_{j,no-load}} \tag{1}$$

where j is the bus number, $V_{j,based-load}$ and $V_{j,no-load}$ are the bus voltages for the base-load and no-load operating conditions, respectively.

Balanced three-phase load flow can be used to compute $V_{j,based-load}$. From Fig. 1, the complex power at bus j can be computed as:

$$S_j = f(\delta,V) = P_j - jQ_j = (V_j\angle\delta_j)^* \left(\frac{V_i\angle\delta_i - V_j\angle\delta_j}{R_{ij} + jX_{ij}} \right) \tag{2}$$

where $V_i\angle\delta_i$ and $V_j\angle\delta_j$ are the voltages at buses i and j, respectively; R_{ij} and X_{ij} are the resistance and reactance between buses i and j, respectively; while P_j and Q_j are the active and reactive flowing at bus j. Separating real and imaginary parts of (2) results in:

$$\begin{cases} W_{real}(\delta_{ij},V_j) = [P_jR_{ij} + Q_jX_{ij}] = V_iV_jcos\delta_{ij} - (V_j)^2 \\ W_{imag}(\delta_{ij},V_j) = [P_jX_{ij} - Q_jR_{ij}] = V_iV_jsin\delta_{ij} \end{cases} \tag{3}$$

where $\delta_{ij} = \delta_i - \delta_j$. The voltage V_j is computed by squaring and adding the real and imaginary parts of (3):

$$V_j^4 + 2(P_jR_{ij} + Q_jX_{ij} - 0.5V_i^2)V_j^2 + (P_j^2 + Q_j^2)(R_{ij}^2 + X_{ij}^2) = 0. \tag{4}$$

There are four solutions to (4),

$$V_j = \pm\sqrt{\frac{1}{2}[-b \pm \sqrt{(b^2 - 4c)}]} \tag{5}$$

where $b = -(V_i^2 - 2P_j R_{ij} - 2Q_j X_{ij})$ and $c = (P_j^2 + Q_j^2)(R_{ij}^2 + X_{ij}^2)$. However, $-(b)$ is always positive because the term $(-2P_j R_{ij} - 2Q_j X_{ij})$ is small as compared to (V_i^2) and also $(4c)$ is small as compared to (b^2); therefore, the unique positive and stable solution of (5) is

$$V_j = V_{j,based-load} = \pm\sqrt{\frac{1}{2}[-b + \sqrt{(b^2 - 4c)}]}. \quad (6)$$

Substituting (6) in (1) results in

$$VRI_j^{conventional} = \frac{V}{V_o} = \frac{\sqrt{(0.5V_i^2 - P_j R_{ij} - Q_j X_{ij}) + A}}{V_i} \quad (7)$$

where A = $\sqrt{0.25(V_i^2 - 2P_j R_{ij} - 2Q_j X_{ij})^2 - (P_j^2 + Q_j^2)(R_{ij}^2 + X_{ij}^2)}$.

The propose index in balanced network is defined as:

$$VRI_j^{balanced} = \frac{V_{j,collapse}}{V_{j,no-load}}. \quad (8)$$

To compute the proposed VRI for balanced three-phase networks, $V_{j,collapse}$ is computed based on the Newton-Raphson load flow by forcing (3) to zero. The Jacobian corresponding to (3) is defined as follows:

$$J = \begin{bmatrix} -V_i V_j \sin\delta_{ij} & V_i V_j \cos\delta_{ij} - 2V_j \\ V_i V_j \cos\delta_{ij} & V_i \sin\delta_{ij} \end{bmatrix}. \quad (9)$$

At the collapse point, the Jacobian matrix is singular, therefore:

$$det(J) = 0 \Rightarrow \frac{V_j \cos\delta_{ij}}{V_i} = \frac{1}{2} \Rightarrow V_{j,collapse} = \frac{0.5V_j}{\cos\delta_{ij}}. \quad (10)$$

Substituting (6) and (10) in (8) results in

$$VRI_j^{balanced} = \frac{V_{j,collapse}}{V_{j,no-load}} = \frac{0.5}{\cos\delta_{ij}}. \quad (11)$$

where the angle is computed from (12):

$$\delta_{ij} = tan^{-1}\left(\frac{[P_j X_{ij} - Q_j R_{ij}]}{[P_j R_{ij} + Q_j X_{ij}] + (V_j)^2} \right) \quad (12)$$

To extend and generalize the conventional definition of VRI for multiphase networks, symmetrical components are applied to the three-phase voltages resulting from three-phase power flow. The new index for multiphase applications is defined as the ratio of the positive-sequence voltage at the collapse point to the positive-sequence voltage at the no-load:

$$VRI_j^{multiphase} = \frac{V_{j,collapse}^{+}}{V_{j,no-load}^{+}}. \quad (13)$$

Equation (13) can be used to identify the weakest buses of both balanced and unbalanced multiphase networks. The node with the lowest bus voltage ranking index value is classified as the weakest bus.

3. IMPACTS OF DG PLACEMENT ON VOLTAGE PROFILE, GRID LOSS, AND MAXIMUM LOADING FACTOR (MLF)

3.1 Impact of DG on Voltage Profiles

In balanced three-phase networks, voltage profiles are usually plotted using the average bus voltage values. For unbalanced networks, system unbalanced voltage variance index [15] has been proposed for considering voltage profiles instead of using the system average voltage [13, 16]. However, for multiphase networks, voltage magnitudes in some phases are missing. Therefore, in this paper, the voltage profiles of all phases will be plotted in the range of 0.95-1.05p.u. (see Figs. 4(c), 5(c) and 7(b)).

3.2 Impact of DG on Grid Losses

Grid losses associated with the placement and the penetration level of a DG unit (e.g., at the weakest bus) are computed and compared with the losses without any compensation device. The active power loss reduction (ALR) (for example due to the installation of DG units or compensation devices) is defined as:

$$ALR = \frac{P_{loss} - P_{loss}^{DG}}{P_{loss}} \times 100\% \quad (14)$$

where P_{loss}^{DG} and P_{loss} are the total active power loss with and without DG units, respectively.

The DG penetration level is defined as

$$DG\,Penetration\;\;Level = \frac{P_{DG}}{P_{load}} \times 100\% \quad (15)$$

where P_{DG} and P_{load} are the total active power of the DG units and system loads, respectively.

3.3 Impact of DG on MLF

Using a continuation three-phase power flow, PV curves for multiphase distribution networks will be plotted. The method of symmetrical components will then be applied to merge the three individual PV curves into a single PV curve based on the positive-sequence voltage. Finally, MLF will be determined using the single PV curve based on the positive-sequence voltage [21]. MLF is defined as the ratio of the maximum system load (at the voltage collapse point) to the base load.

$$MLF = \frac{P_{collapse}}{P_{base\,load}} \quad (16)$$

3.4 Impact of DG on Voltage Unbalance Factor (VUF)

The voltage unbalance factor (VUF) is defined as the ratio of the negative-sequence voltage component to the positive-sequence voltage component [27]:

$$\%\;VUF = \frac{negative-sequence\;\;voltage\;\;component}{positive-sequence\;\;voltage\;\;component} \times 100\%. \quad (17)$$

4 Proposed Iterative Algorithm for DG Placement in Unbalanced Multiphase Networks

The proposed iterative algorithm of Fig. 2 is designed to increase the penetration level of DG units in multiphase networks in order to reduce total active power loss and enhance voltage stability margins

considering voltage limits at all buses. In addition, single-phase shunt capacitors are also utilized to further improve the performance of the systems.

Stage one of the algorithm consists of an iterative procedure to properly place and increase the penetration of DG units in multiphase system. DG units are located one at a time and their corresponding sizes are increased until a voltage violation is detected in the system. To find the best location and rate of the first DG, a small DFIG is temporary placed at the weakest three-phase bus as identified by the calculated VRI (Eq. 13). The size of DFIG is then increase (to reduce total system loss and increase MLF) until one of the bus voltages is increased above the permissible level. The first iteration terminates by permanently connecting the first DG at Bus_{DG} with PL_{DG}. This procedure is repeated to place more DG units as long as no voltage violations are noticed and there are improvements in the total system loss and MLF.

Stage two of the proposed algorithm is similar to stage one with the exception of selecting the weakest single-phase buses (identified by VRI) and connecting single-phase capacitor banks to the single-phase sections of the multiphase network.

5 SIMULATION RESULTS

For the analysis of this paper, the IEEE multiphase 34 node test feeder of Fig. 3 [28] is considered. The network has been simulated using the DIgSILENT PowerFactory software [29]. The system data and parameters are available in [28]. This unbalanced multiphase feeder consists of three-phase and single-phase sections with unbalanced spot loads (Y-PQ, D-PQ, Y-I, D-I, Y-Z, and D-Z), distributed loads (Y-PQ, Y-I, Y-Z, D-I, D-Z, and D-PQ), three-phase shunt capacitors (at buses 844 and 848), and an in-line transformer (between buses 832 and 688). There are also two automatic voltage regulators.

Bus 800 is treated as a slack bus with a voltage set point of 1.05 p.u. At a base-case load condition, the voltage at bus 890 is lower than the permissible voltage limit because the line between buses 888 and 890 is relatively long. However, other bus voltages are in the acceptable range of 0.95p.u. to 1.05p.u.

5.1 Bus Voltage Ranking Based on Proposed VRI Index

Figure 4a shows the bus voltage ranking for the base-case load with two automatic voltage regulators which regulate the voltages in the range of 0.95-1.05p.u. The weakest three-phase and single-phase buses are 890 and 864, respectively.

5.2 Placement and Sizing of DG Units to Improve Voltage Profile, Grid Loss, and MLF

Stage one of the proposed iterative algorithm (Fig. 2) consists of the installation of DFIG wind turbines.

- ***Iteration One-*** A DFIG wind turbine with power factor control is installed at the weakest three-phase bus (bus 890) through a 4.16kV/0.69kV transformer. The size of DFIG is gradually increased to determine its impacts on loading factor, active power loss reduction, and voltage profile. Simulations results are presented in Fig. 4b indicating that active power loss is lowest (ALR = 62.31%) at a DG penetration level of 40% while the loading factor escalates as the DG penetration increases. However, there will be a voltage violation (at bus 890, all phases) for a DG penetration of 40%. According to the algorithm of Fig. 2, with 30% DG penetration at bus 890, all the bus voltage profiles are in the permissible range of 0.95-1.05p.u. (Fig. 4c). Notice that the voltage profile of phase c at bus 890 is 1.0499p.u., which is very close to the upper voltage limit of 1.05p.u. Any further increase in the DG penetration level at this bus beyond 30% will cause an overvoltage condition at bus 890. Therefore, the maximum penetration of the first DFIG that can be safely installed at bus 890 is 30% (600kW, 666.66kVA). Furthermore, the total active power loss is reduced from 0.2641MW to 0.1053MW and MLF is increased from 2.518 to 3.150. These results indicate that voltage limits should be considered as a constraint in the DG placement problem.
- ***Iteration Two-*** With 30% DFIG connected at bus 890, a similar procedure is implemented in the second iteration to properly locate and size the second DFIG and increase the penetration of DG units.

According to Fig. 5a, the four weakest buses are now 890, 852, 888, and 814. That is the weakest three-phase bus is still bus 890. However according to the results of the first iteration, the DG penetration level is restricted at this bus due to a voltage violation at bus 890. As a result, the most appropriate position for the second DFIG is bus 852. The algorithm continues by increasing the size of DG while considering MLF, active power loss (Fig. 5b) and voltage profiles (Fig. 5c). Iteration two is terminated at a maximum DG penetration of 30% at bus 852. This will result in a further active power loss reduction of 76.92% and MLF will be increased to 3.519.

- ***Iteration Three-*** With the two DFIGs in service at buses 890 and 852, the four weakest three-phase buses are buses 890, 814, 888, and 848 (Fig. 6). As there is already a DG unit in service at bus 890, the best location for the third DFIG connection is bus 814. However, with only 1% penetration of DG at bus 814, there will be a voltage violation at bus 808 (e.g., phase c voltage is increased to 1.050142p.u.). The first stage of the algorithm (Fig. 2) will be terminated as any further DFIG connection will result in a voltage violation. Therefore according to the results of iterations 1-3, the maximum DG penetration can be safely increased to 60% without any voltage violations.

5.3 Placement and Sizing of Single-Phase Capacitor Banks to Further Improve Voltage Profile, Grid Loss, and MLF

Stage two of the proposed algorithm (Fig. 2) aims at further improvements in VUF, total power loss, MLF, and voltage profiles through the installation of capacitor banks in the single-phase sections of the multiphase network.

- ***Iteration One-*** The first capacitor bank is connected at the weakest single-phase bus and its size is increased until a voltage violation is spotted. According to Fig. 6, the weakest single-phase location is bus 822 and the capacitor size can be safely increased to 273kVar while all bus voltage profiles are kept in the range of 0.95-1.05p.u. (Fig. 7a). Note that any further increase of this capacitor size

beyond 273kVar will cause an overvoltage condition at bus 802 (phase c). The inclusion of the two DFIGs (at busses 890 and 852) and a single-phase capacitor (at bus 822) has increased the total active power loss from 0.0610MW to 0.0778MW while MLF is further increased to 3.575.

- ***Iteration Two***- The iterative procedure is repeated to install more single-phase shunt capacitors. According to Fig. 7a, the four weakest single-phase locations are buses 822, 820, 864, and 818. The next location for capacitor placement is bus 820. However, installation of a 3kVar (1% of Q_{load}) single-phase shunt capacitor at this bus 820 will cause an overvoltage condition at bus 802 (phase a). Therefore, the second stage of the algorithm terminates with only one capacitor bank connected to bus 822.

5.4 Summary and Analysis of Simulation Results

Simulation results for increasing the penetration of DFIG and single-phase capacitors in the IEEE multiphase 34 node test feeder of Fig. 2 based on the proposed algorithm (Fig. 3) are summarized and compared in Table 1. The impacts of DG and capacitor installations on the performance (total active power loss, MLF, and VUF) of the multiphase network are highlighted in rows 3-6 and 9-11 of Table 1, respectively. With the proposed algorithm, a total DG penetration level of 60% (30% at bus 890 and 30% at bus 852) is achieved and a 0.273MVar shunt capacitor is placed at bus 822 without any voltage violations which will reduced the total active power loss to 0.0778MW and increased MLF to 3.575. In addition, the percentage of VUF at the weakest three-phase bus has been considerably improved from 2.99 to 0.36 as shown in Fig. 8. Simulations have also been performed without the two voltage regulators and summarized in Table 2. Without the voltage regulators, the algorithm will only locate 36% DG at bus 890; however, the overall system performance is considerably deteriorated as the losses and VUF have increased while the MLF is decreased from 3.575 to 3.014.

5.5 Comparison of Simulation Results with Voltage Sensitivity Approach of [13] for Balanced Three-Phase Networks

Reference [13] has presented a method for DG placement in balanced three-phase distribution networks based on voltage sensitivity analysis without voltage requlators. In order to check the validity and accurcay of the proposed algorithm of Fig. 2 for balanced three-phase networks, we have simplfied Fig. 3 by removing the single-phase buses and the voltage regulators. Simulation results based on the voltage sensitivity approach of [13] and the proposed iterative algorithm of this paper are presented and compared in Table 3. As expected, the two approaches arrive at an identical solution (Table 3; rows 4 and 9) with the same DG location, DG penetration, losses and MLF. These results demonstrate the legitimacy and accuracy of the proposed solution for balanced three-phase operation. It should be emphasize that the voltage sensitive approach of [13] can only be applied to balanced three-phase networks while the proposed algorithm of this paper can also be used in unbalanced three-phase and unbalanced multiphase systems.

5.6 Comparison of Simulation Results with DG Placement Approaches of [15] and [16] for Unbalanced Multiphase Networks

To demonstrate the performance and accuracy of the proposed algorithm (Fig. 2) under multiphase operating conditions, simulation results are also compared with those generated based on the approaches of [15] and [16]. The DG placement approach of [15] is based on the voltage profile and grid loss calculations, while the system unbalanced voltage variance index is utilized in [16]. According to Table 4, the proposed algorithm provides a better solution with lower grid losses, larger MLF and smaller VUF values. Furthermore, the DG placement method of [16] results in overvoltage conditions at 24 out of the 34 buses. For example, the worse overvoltage condition is at bus 840 with per unit voltage magnitudes of 1.068, 1.086, and 1.094 at phases a, b, and c, respectively.

6 CONCLUSION

This paper has extended the definition of the conventional bus voltage ranking index (VRI) of V/V_o defined for balanced three-phase systems to identify the weakest buses of the multiphase networks. The new VRI is utilized through a proposed iterative algorithm to properly increase the penetration levels of DG and single-phase capacitors in order to improve the performance of the multiphase networks. The proposed algorithm is relatively simple and can effectively reduce total active power loss, increase MLF and decrease VUF while keeping all bus voltages within the designated lower and higher limits. Main conclusions are:

- The proposed bus ranking approach based on the positive-sequence voltage ratio $V_{collapse}/V_{no\text{-}load}$ can effectively identify the weakest three-phase and single-phase buses for DG and shunt capacitors placements, respectively.
- Compared to the previously proposed DG placement approaches of [13], [15] and [16], the proposed algorithm provides better solutions with lower grid losses, larger MLF and smaller VUF values
- Analysis of simulation results indicates that the penetration level of DG is limited by considering not only the line losses and/or MLF as conventionally practiced in the literature, but also the bus voltage limits. Therefore, at high penetration levels of DG, it is necessary to also take voltage limits into consideration.
- Placements of shunt capacitors at the weakest single-phase buses will not only increase MLF, but also further improve VUF.
- The future scope of the work could include application of artificial intelligence optimization in the DG placement and sizing problem to arrive at near global solutions and the inclusion of DG (wind) non-deterministic nature.

7 REFERENCES

[1] Vinothkumar, K., Selvan, M.P., and Srinath, S.; 'Impact of DG model and load model on placement of multiple DGs in distribution system'. Proc. Int. Conf. Industrial and Information Systems, July 2010, pp. 508-513

[2] Quezada, V.H.M., Abbad, J.R., and Roman, T.G.S.; 'Assessment of energy distribution losses for increasing penetration of distributed generation', IEEE Trans. Power Syst., 2006, 21, (2), pp. 533- 540

[3] Kumar, K. V., and Selvan M. P.: 'Planning and operation of Distributed Generations in distribution systems for improved voltage profile'. Proc. IEEE PES Power Syst. Conf. and Exposition, March 2009, pp. 1-7

[4] Vittal, E., O'Malley, M., and Keane, A.; 'A Steady-State Voltage Stability Analysis of Power Systems With High Penetrations of Wind', IEEE Trans. Power Syst., 2010, 25, (1), pp. 433-442

[5] Ayres, H.M., Freitas, W., De Almeida, M.C., and Da Silva, L.C.P., 'Method for determining the maximum allowable penetration level of distributed generation without steady-state voltage violations', IET Gen. Trans. Dist., 2010, 4, (4), pp. 495-508

[6] Enslin, J.H.R.: 'Interconnection of distributed power to the distribution network'. Proc. IEEE PES Power Syst. Conf. and Exposition, October 2004, pp. 726- 731

[7] Van Thong, V., Van Dommelen, D., Driesen, J., and Belmans, R.; 'Using dynamic simulation to study the penetration level of distributed energy resources'. Proc. IEEE Russia Power Tech., June 2005, pp. 1-6

[8] Celli, Gianni., Ghiani, Emilio., Mocci, Susanna., and Pilo, Fabrizio.; 'Multi-objective programming to maximize the penetration of distributed generation in distribution networks'. Proc. CIRED Elect. Dist. Int. Conf., June 2009, pp. 8-11

[9] Ramesh, L., Chowdhury, S.P., Chowdhury, S., Song, Y.H., and Natarajan, A.A.: 'Voltage stability analysis and real power loss reduction in distributed distribution system'. Proc. IEEE PES Trans. Dist. Conf. and Exposition, April 2008, pp. 1-6

[10] Hasani, M., and Parniani, M.: 'Method of combined static and dynamic analysis of voltage collapse in voltage stability assessment'. Proc. IEEE PES Trans. Dist. Conf. and Exhibition: Asia and Pacific, 2005, pp. 1-6

[11] Ayres, H.M., Freitas, W., De Almeida, M.C., and Da Silva, L.C.P.: 'Method for determining the maximum allowable penetration level of distributed generation without steady-state voltage violations', IET Gen. Trans. Dist., 2010, 4, (4), pp. 495-508

[12] Hong, Y.-Y., and Gau, C.-H.; 'Voltage stability indicator for identification of the weakest bus/area in power systems', IET Gen. Trans. Dist., 1994, 141, (4), pp. 305-309

[13] Hedayati, H., Nabaviniaki S. A., and Akbarimajd A.: 'A Method for Placement of DG Units in Distribution Networks', IEEE Trans. Power Del., 2008, 23, (3), pp. 1620-1628

[14] Alonso, M., and Amaris, H.: 'Voltage stability in distribution networks with DG'. Proc. IEEE Bucharest PowerTech, June 2009, pp. 1-6

[15] Jones, G. W., and Chowdhury B. H.: 'Distribution system operation and planning in the presence of distributed generation technology'. Proc. IEEE PES Trans. Dist. Conf. and Exposition, April 2008, pp. 1-8

[16] Baohua, D., Asgarpoor, S., and Wei, Q.: 'Voltage analysis of distribution systems with DFIG wind turbines'. Proc. IEEE Power Electronics and Machines in Wind Applications, June 2009, pp. 1-5

[17] Nuroglu, F. M., and A. B. Arsoy.: 'Voltage profile and short circuit analysis in distribution systems with DG'. Proc. IEEE Canada Electric Power Conf., October 2008, pp. 1-5

[18] Juanuwattanakul, P., and Masoum, M.A.S.; 'Analysis and comparison of bus ranking indices for balanced and unbalanced three-phase distribution networks'. Proc. AUPEC. Uni. Power Eng. Conf., September 2011, pp.1-5

[19] Mori, H., and Seki, K.: 'Non-linear-predictor-based continuation power flow for unbalanced distribution systems'. Proc. Trans. Dist. Conf. and Exposition: Asia and Pacific, October 2009, pp. 1-4

[20] Zhang, X. P., Ju, P., and Handschin, E.: 'Continuation three-phase power flow: A tool for voltage stability analysis of unbalanced three-phase power systems', IEEE Trans. Power Syst., 2005, 20, (3), pp. 1320-1329

[21] Juanuwattanakul, P., and Masoum, M.A.S.: 'Voltage stability enhancement for unbalanced multiphase distribution networks'. Proc. IEEE PES General Meeting, July 2011, pp.1-6

[22] Jabr, R.A., and Pal, B.C., 'Intermittent wind generation in optimal power flow dispatching', IET Gen. Trans. Dist., 2009, 3, (1), pp. 66-74

[23] Jabr, R.A., and Pal, B.C., 'Ordinal optimisation approach for locating and sizing of distributed generation', IET Gen. Trans. Dist., 2009, 3, (8), pp. 713-723

[24] Singh, R., Pal, B.C., and Jabr, R.A.; 'Statistical Representation of Distribution System Loads Using Gaussian Mixture Model', IEEE Trans. Power Syst., 2010, 25, (1), pp. 29-37

[25] Phadke, A. R., Bansal, S. K., and Niazi, K. R.: 'A comparison of voltage stability indices for placing shunt FACTS controllers'. Proc. Int. Conf. Emerging Trends in Engineering and Technology, July 2008, pp. 939-944

[26] IEEE/PES Power System Stability Subcommittee.: 'Voltage stability assessment: Concepts, practices and tools', IEEE Catalog Number SP101PSS, August 2002

[27] Dugan, R.C., McGranaghan, M.F., and Beaty, H.W.: '*Electrical Power Systems Quality*' (McGraw-Hill, 1996)

[28] http://ewh.ieee.org/soc/pes/dsacom/testfeeders/index.html, accessed August 2011

[29] DIgSILENT PowerFactory Manual, 14.0 ed., 2009

Parachai Juanuwattanakul received his B.Eng (2nd Class Hons.), M.Eng and Ph.D. degrees in Electrical Engineering from Mahanakorn University of Technology, Bangkok, Thailand, Kasetsart University, Bangkok, Thailand and Curtin University, Perth, WA, Australia in 1994, 1998 and 2012, respectively. His research interests include voltage stability, smart grid and distributed generation. Currently, he is a lecturer at the Electrical Engineering Department, Sripatum University, Bangkok, Thailand and a member of IEEE.

Mohammad A.S. Masoum received his B.S., M.S. and Ph.D. degrees in Electrical and Computer Engineering in 1983, 1985, and 1991, respectively, from the University of Colorado, Boulder, USA. His research interests include optimization, power quality and stability of power systems/electric machines and distributed generation. Dr. Masoum is the co-author of "*Power Quality in Power Systems and* Electrical *Machines"* (Elsevier, 2008) and *"Power Conversion of Renewable Energy Systems*" (Springer, 2011). Currently, he is an Associate Professor and the discipline leader for electrical power engineering at the Electrical and Computer Engineering Department, Curtin University, Perth, Australia and a senior member of IEEE.

Table Captions

Table 1. Detailed solution for DFIG and capacitor placement and sizing in the IEEE multiphase 34 node test feeder (Fig. 3) with voltage regulators using the proposed algorithm of Fig. 2.

Table 2. Detailed solution for DG (DFIG) and capacitor placement and sizing in the IEEE multiphase 34 node test feeder of Fig. 3 without any voltage regulators using the proposed iterative algorithm of Fig. 2.

Table 3. Comparison of simulation results based on the proposed algorithm of Fig. 2 and the voltage sensitive approach of [13] for DG (DFIG) placement and sizing in the modified IEEE multiphase 34 node test feeder of Fig. 3 (without single-phase buses and voltage regulators) under balanced three-phase operating conditions.

Table 4. Comparison of simulation results based on the proposed algorithm of Fig. 2, the voltage profile approach and grid loss calculations of [15], and the system unbalanced voltage variance index of [16] for DG (DFIG) placement and sizing in the IEEE multiphase 34 node test feeder of Fig. 3.

Table 1

Multiphase Network (Fig. 3) With Voltage Regulators

Stage One: Placement and Sizing of DFIGs						
iteration	weakest three-phase bus	penetration of DFIG [%]	total loss [MW]	MLF	VUF at bus 890 [%]	Fig.
0	-	-	0.2641	2.518	2.985	-
1	890	30	0.1053	3.150	0.492	4
2	852	30	0.0610	3.519	0.361	5
3	814	-	-	-	-	6
Stage Two: Placement and Sizing of Single-Phase Shunt Capacitors						
iteration	weakest single-phase bus	capacitor size [kVar]	total loss [MW]	MLF	VUF at bus 890 [%]	Fig.
0	-	-	0.0610	3.519	0.361	-
1	822	273	0.0778	3.575	0.356	7
2	820	-	-	-	-	-
Final Solution: 30% DFIG penetration at bus 890, 30% DFIG penetration at bus 852 and 273kVar capacitor at bus 822.						

Table 2

Multiphase Network (Fig. 3) Without Voltage Regulators

Stage One: Placement and Sizing of DFIGs					
iteration	weakest three-phase bus	penetration of DFIG [%]	total loss [MW]	MLF	VUF at bus 890 [%]
0	-	-	0.2284	1.895	1.428
1	890	36	0.0965	3.014	0.404
2	888	-	-	-	-
Stage Two: Placement and Sizing of Single-Phase Shunt Capacitors					
iteration	weakest single-phase bus	capacitor size [kVar]	total loss [MW]	MLF	VUF at bus 890 [%]
0	-	-	0.0965	3.014	0.404
1	864	120	0.1010	3.014	0.376
2	822	-	-	-	-
Final Solution: 36% DFIG penetration at bus 890 and 120kVar capacitor at bus 864.					

Table 3

Balanced Three-Phase Network Without Voltage Regulators

Method One: The Proposed DG Placement Algorithm of Fig. 2				
iteration	weakest three-phase bus	penetration of DFIG [%]	total loss [MW]	MLF
0	-	-	0.1877	2.022
1	890	45	0.0737	3.814
2	888	-	-	-
Final Solution: 45% DFIG penetration at bus 890.				
Method Two: The Voltage Sensitive Approach of [13]				
iteration	weakest single-phase bus	penetration of DFIG [%]	total loss [MW]	MLF
0	-	-	0.1877	2.022
1	890	45	0.0737	3.814
2	888	-	-	-
Final Solution: 45% DFIG penetration at bus 890.				

Table 4

Multiphase Network (Fig. 3) Without Voltage Regulators*					
method	**DG location(s)**	**DG penetration [%]**	**total loss [MW]**	**MLF**	**VUF at worst bus [%]**
the proposed algorithm (Fig. 2)	890	59	0.2125	3.534	0.457 (bus 890)
[15]	890	25	0.2824	2.790	0.833 (bus 890)
Multiphase Network (Fig. 3) With Voltage Regulators					
the proposed algorithm (Fig. 2)	890, 852	30, 30	0.0778	3.575	0.356 (bus 890)
[16]**	840	85	0.1556	2.994	0.680 (bus 890)

*) In order to compare the results with [15], all loads are increased to 150%.

**) This approach causes overvoltage conditions at 24 out of 34 buses.

Figure Captions

Figure 1. Equivalent circuit of a two bus balanced network.

Figure 2. The proposed algorithm for the placement and sizing of DG units and single-phase capacitors in multiphase networks.

Figure 3. The IEEE multiphase 34 node test feeder.

Figure 4. Simulation results for the first DG placement (stage one, iteration one); (a) voltage ranking index with no DFIG installation (base-case load), (b) loading factor and active power loss with different DG penetrations at bus 890, (c) voltage profile with 30% DFIG penetration at bus 890.

Figure 5. Simulation results for the second DG placement (stage one, iteration two); (a) voltage ranking index with 30% DFIG units installed at bus 890, (b) loading factor and active power loss with 30% DFIG penetration at bus 890 and different DFIG penetration at bus 852, (c) voltage profile with 30% DFIG penetration at bus 890 and 30% DFIG penetration at bus 852.

Figure 6. Simulation results for the third DG placement (stage one, iteration three) showing voltage ranking index with 30% DFIG units installed at bus 890 and 30% DFIG at bus 852.

Figure 7. Simulation results for the single-phase capacitor placement (stage two, iteration one); (a) voltage ranking index with 30% DG units installed at bus 890, 30% DG at bus 852, and single-phase shunt capacitor 0.273MVar at bus 822, (b) voltage profile with 30% DG penetration at bus 890, 30% DG penetration at bus 852, and single-phase 0.273MVar shunt capacitor at bus 822.

Figure 8. Comparison of %VUF at different iterations of the proposed algorithm (Fig. 2).

Figure 1

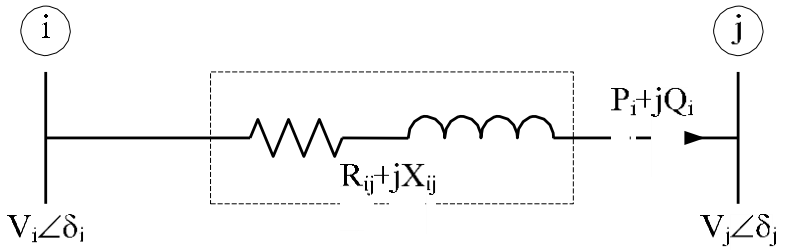


Figure 2

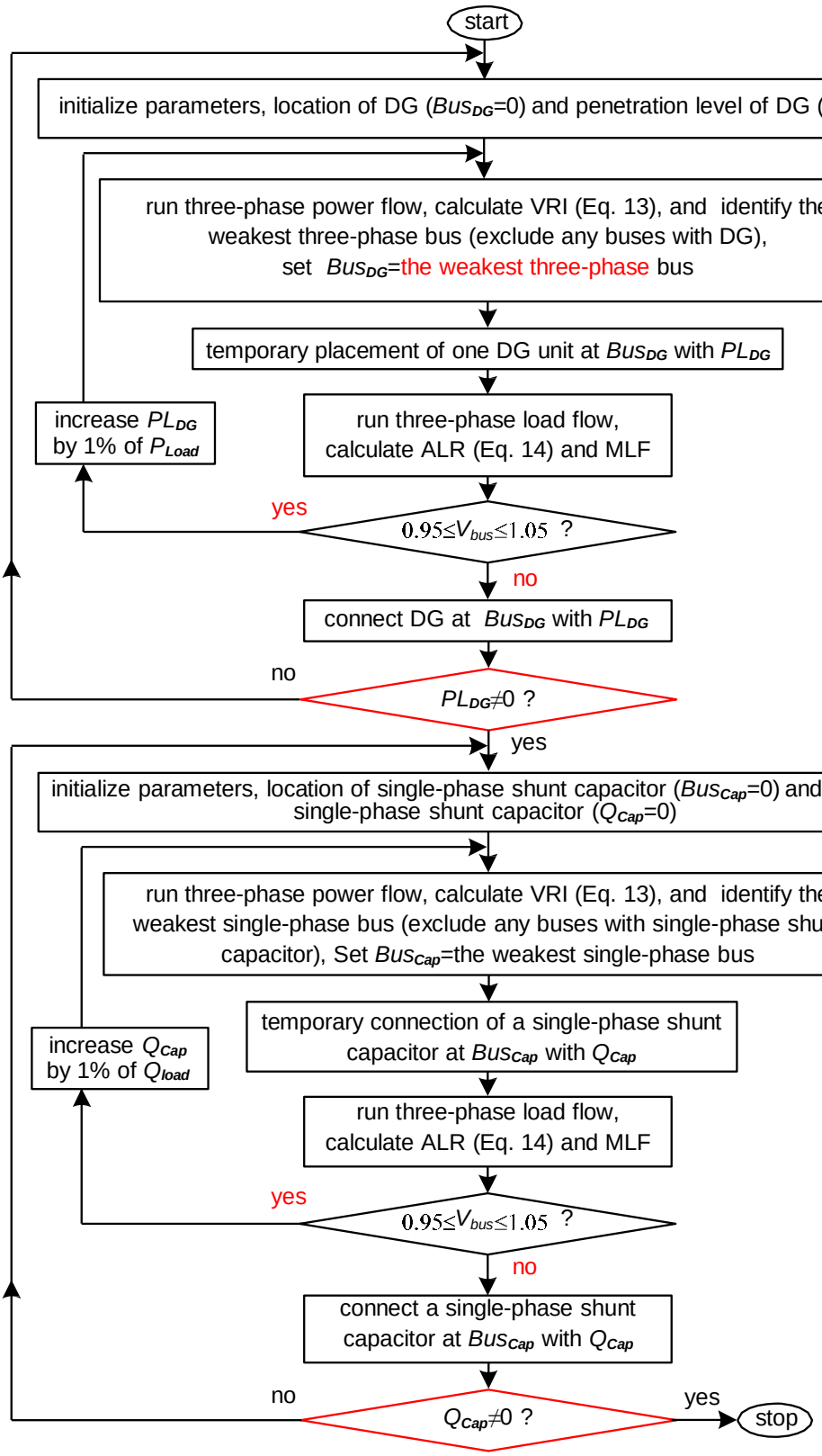

start
initialize parameters, location of DG (Bus_{DG}=0) and penetration level of DG (PL_{DG}=0)
run three-phase power flow, calculate VRI (Eq. 13), and identify the weakest three-phase bus (exclude any buses with DG), set Bus_{DG}=the weakest three-phase bus
temporary placement of one DG unit at Bus_{DG} with PL_{DG}
run three-phase load flow, calculate ALR (Eq. 14) and MLF
increase PL_{DG} by 1% of P_{Load}
yes
$0.95 \le V_{bus} \le 1.05$?
no
connect DG at Bus_{DG} with PL_{DG}
no
$PL_{DG} \neq 0$?
yes
Stage one: placement and sizing of DG units
initialize parameters, location of single-phase shunt capacitor (Bus_{Cap}=0) and sizing of single-phase shunt capacitor (Q_{Cap}=0)
run three-phase power flow, calculate VRI (Eq. 13), and identify the weakest single-phase bus (exclude any buses with single-phase shunt capacitor), Set Bus_{Cap}=the weakest single-phase bus
temporary connection of a single-phase shunt capacitor at Bus_{Cap} with Q_{Cap}
run three-phase load flow, calculate ALR (Eq. 14) and MLF
increase Q_{Cap} by 1% of Q_{load}
yes
$0.95 \le V_{bus} \le 1.05$?
no
connect a single-phase shunt capacitor at Bus_{Cap} with Q_{Cap}
no
$Q_{Cap} \neq 0$?
yes
stop
Stage two: placement and sizing of single-phase shunt capacitors

Figure 3

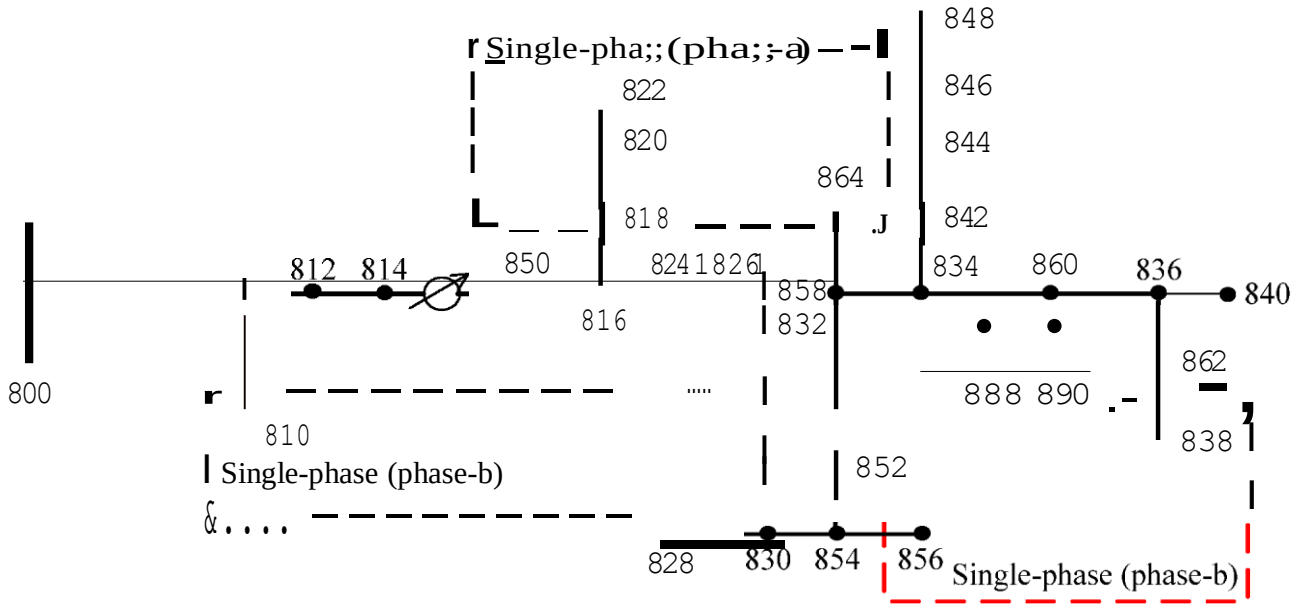
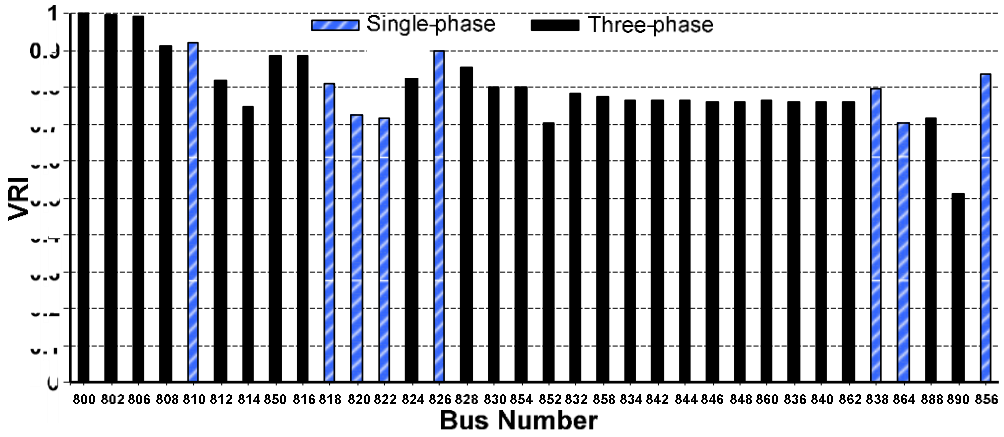
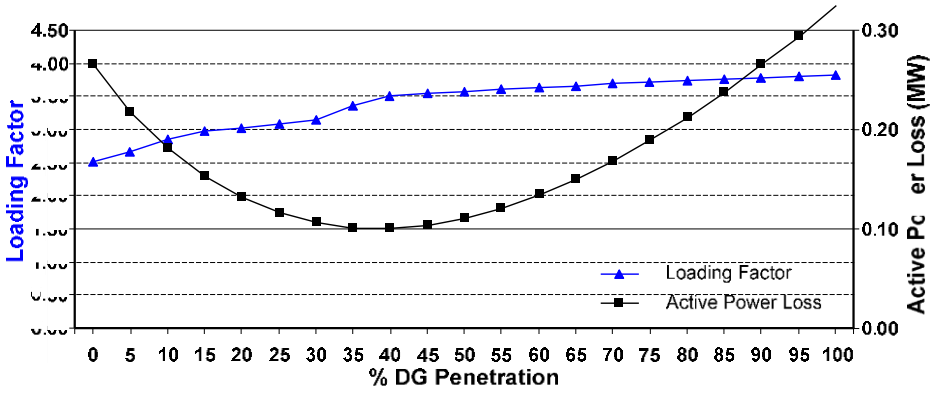

Single-pha;;(pha;;-a)
848
846
844
842
822
820
818
864
812
814
850
824
826
858
832
834
860
836
840
816
800
862
888
890
838
810
Single-phase (phase-b)
852
828
830
854
856
Single-phase (phase-b)

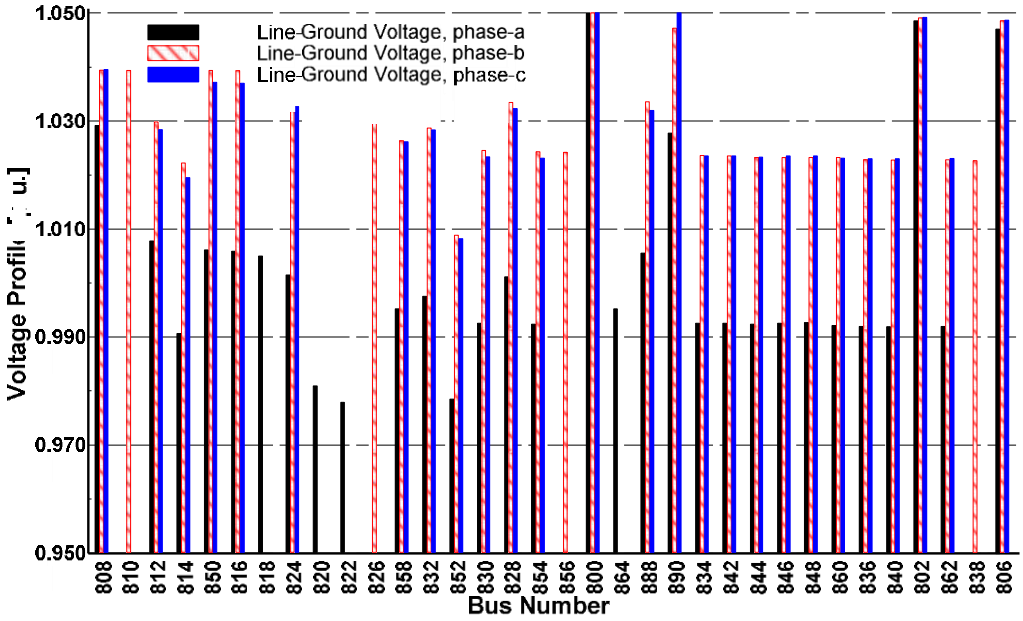
Figure 4


Single-phase
Three-phase
VRI
Bus Number

(a)

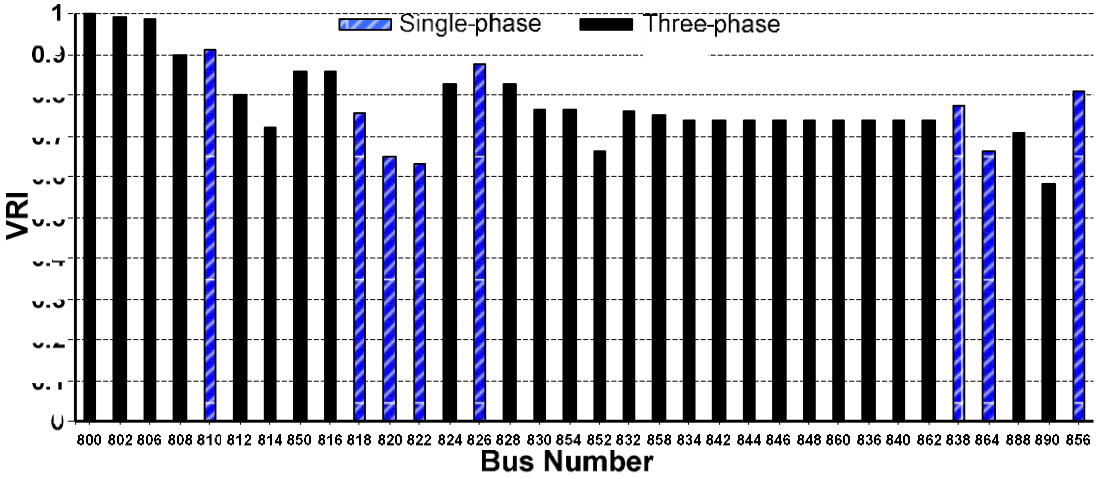

Loading Factor
Active Power Loss (MW)
Loading Factor
Active Power Loss
% DG Penetration

(b)

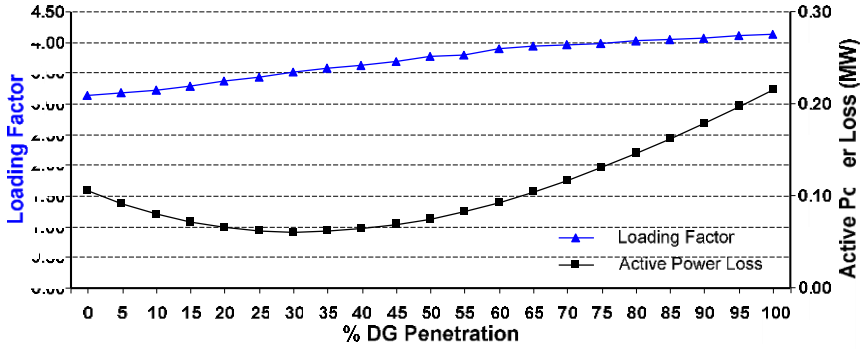

Line-Ground Voltage, phase-a
Line-Ground Voltage, phase-b
Line-Ground Voltage, phase-c
Bus Number

(c)

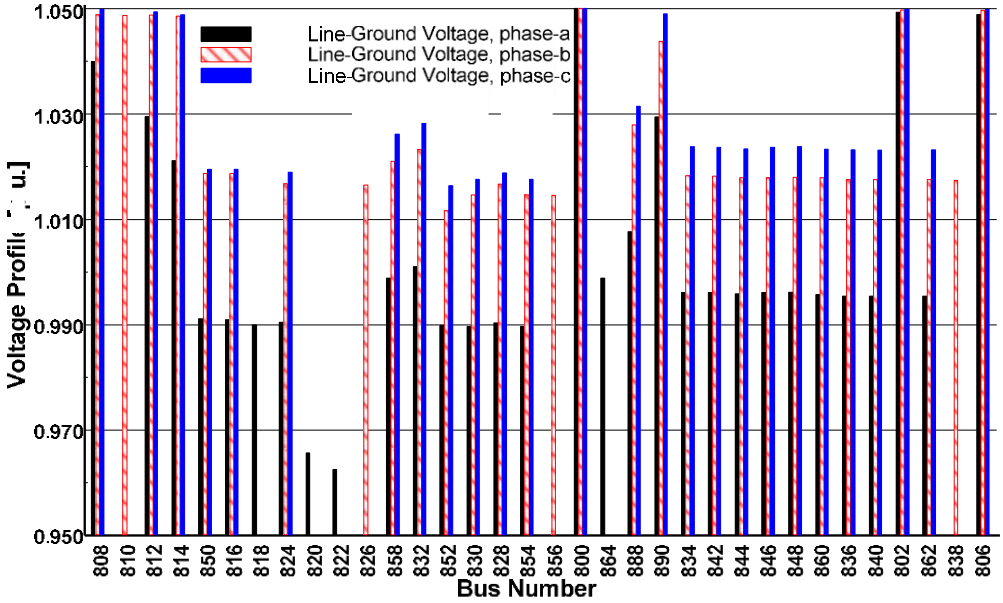
Figure 5


Single-phase
Three-phase
VRI
1
800 802 806 808 810 812 814 850 816 818 820 822 824 826 828 830 854 852 832 858 834 842 844 846 848 860 836 840 862 838 864 888 890 856
Bus Number

(a)


Loading Factor
Active Power Loss (MW)
4.50
0.30
0.20
0.10
0.00
0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100
% DG Penetration
Loading Factor
Active Power Loss

(b)


Line-Ground Voltage, phase-a
Line-Ground Voltage, phase-b
Line-Ground Voltage, phase-c
1.050
1.030
1.010
0.990
0.970
0.950
808 810 812 814 850 816 818 824 820 822 826 858 832 852 830 828 854 856 800 864 888 890 834 842 844 846 848 860 836 840 802 862 838 806
Bus Number

(c)

Figure 6

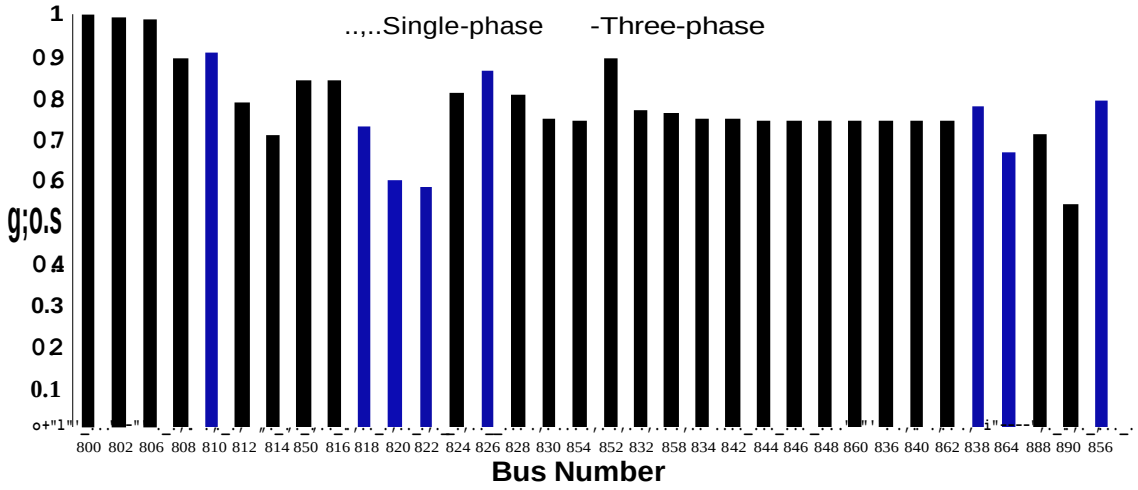
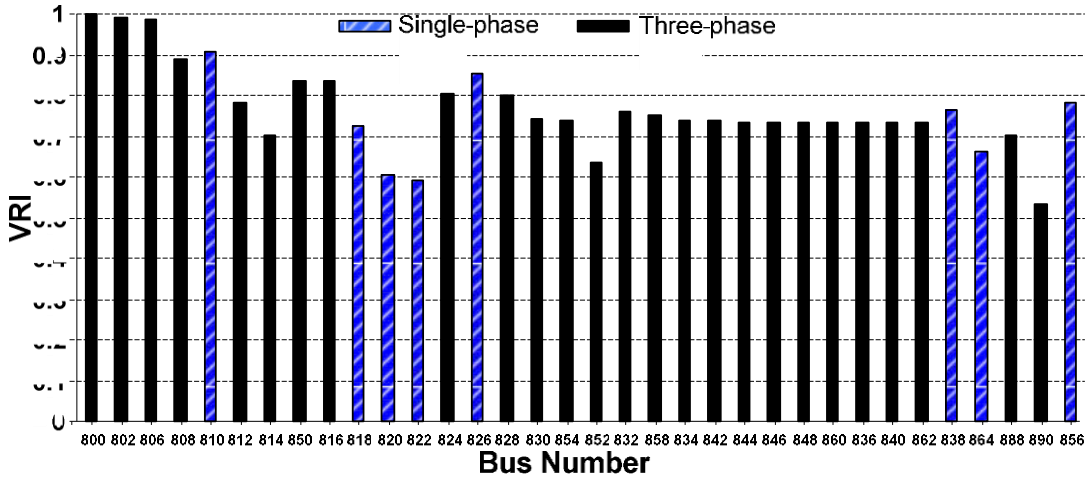
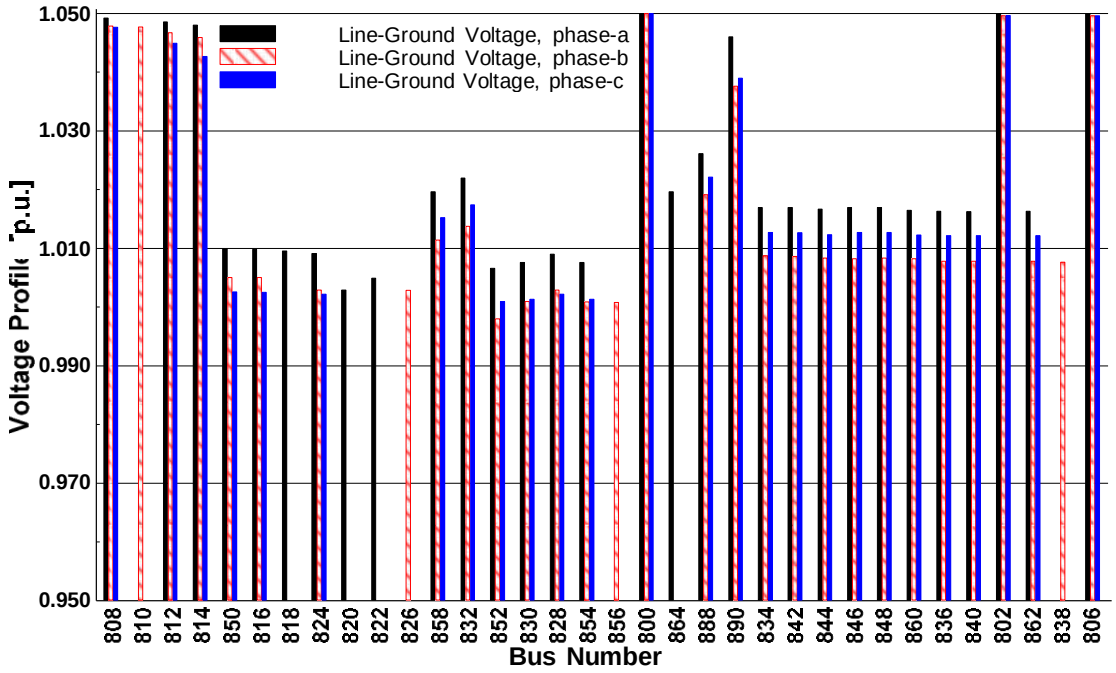

..,..Single-phase
-Three-phase
1
0 9
0 8
0 7
0 6
0.5
0 4
0.3
0 2
0.1
800 802 806 808 810 812 814 850 816 818 820 822 824 826 828 830 854 852 832 858 834 842 844 846 848 860 836 840 862 838 864 888 890 856
Bus Number

Figure 7

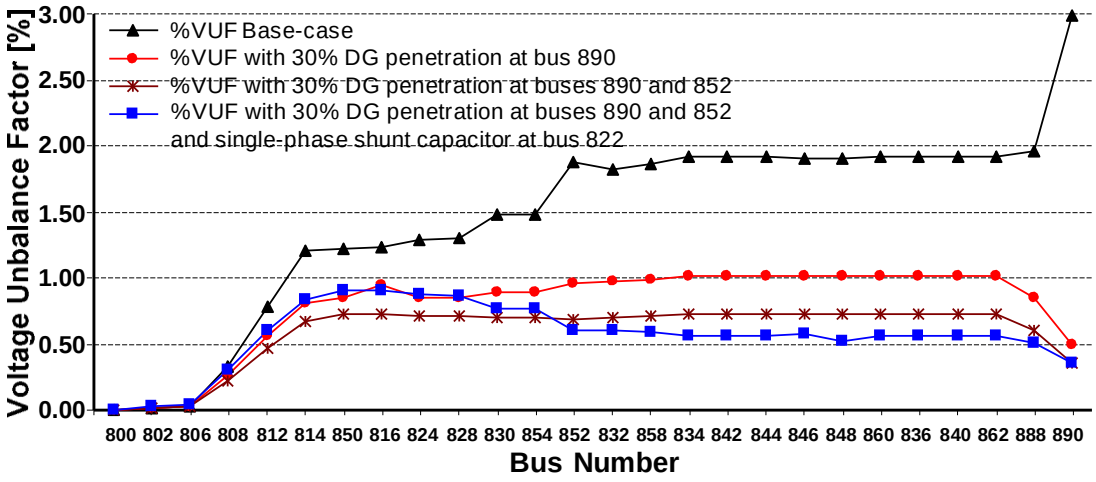

Single-phase
Three-phase
VRI
1
800 802 806 808 810 812 814 850 816 818 820 822 824 826 828 830 854 852 832 858 834 842 844 846 848 860 836 840 862 838 864 888 890 856
Bus Number

(a)


Line-Ground Voltage, phase-a
Line-Ground Voltage, phase-b
Line-Ground Voltage, phase-c
Voltage Profil [p.u.]
1.050
1.030
1.010
0.990
0.970
0.950
808 810 812 814 850 816 818 824 820 822 826 858 832 852 830 828 854 856 800 864 888 890 834 842 844 846 848 860 836 840 802 862 838 806
Bus Number

(b)

Figure 8


%VUF Base-case
%VUF with 30% DG penetration at bus 890
%VUF with 30% DG penetration at buses 890 and 852
%VUF with 30% DG penetration at buses 890 and 852
and single-phase shunt capacitor at bus 822
Voltage Unbalance Factor [%]
3.00
2.50
2.00
1.50
1.00
0.50
0.00
800 802 806 808 812 814 850 816 824 828 830 854 852 832 858 834 842 844 846 848 860 836 840 862 888 890
Bus Number