Department of Electrical and Computer Engineering

Design, Optimization and Implementation of a High Frequency Link Multilevel Cascaded Inverter

Md. Mubashwar Hasan

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Declaration

To the best of my knowledge and belief this thesis contains no material previously published by any other person except where due acknowledgment has been made.

This thesis contains no material which has been accepted for the award of any other degree in any university.

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Date: 07/03/2018

Abstract

Currently, multilevel inverter (MLI) is being used as a medium voltage power converter in several industrial applications such as liquefied natural gas (LNG), chemical, fuel and water plants, marine and electric vehicles, mining, power generation and power-quality improvement devices. Three MLI topologies, diode clamped or neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) MLI are considered as conventional MLI topologies for commercial applications. Among these topologies cascaded MLI is preferred for high power and voltage applications. The most attractive features of cascaded H-bridge inverter over the other conventional MLIs are modularity that facilitates simple and similar control to all H-bridge modules and utilizes cheap low-voltage switching devices in the CHB MLI to generate high voltage output. A number of new cascaded MLI (CMLI) topologies has been proposed in the the last few years aiming at reducing device counts while optimizing the number of levels in the inverter output voltage. Device reduction not only reduces the implementation cost, but also reduces the physical size and weight of the cascaded MLI.

This thesis presents a new concept of cascaded MLI device reduction by utilizing low frequency (50Hz) and high frequency (20kHz) transformer link. The transformer link not only overcomes the predominant CMLI problem of the need for multiple dc-power supplies, but also provides a galvanic isolation between the input and output sides of the inverter, which is essential for grid-connected applications. Two CMLI topologies, symmetric and asymmetric are proposed in this thesis. The asymmetric cascaded inverter is formed through the combination of any existing cascaded topology and a conventional three-phase, two-level inverter while a toroidal core is employed for the high frequency magnetic link to warrant compact size and high power density. On the other hand, the proposed symmetric cascaded MLI topology consists of series-connected half-bridge modules and a simple H-bridge module.

Compared with counterpart CMLI topologies available in the literatures, the proposed two inverter topologies in this thesis have the advantage of utilizing the least number of power electronic components without compromising the overall performance particularly when a high number of levels is required in the output voltage waveform. The feasibility and effectiveness of the proposed inverter topologies are confirmed through extensive simulation and experimental studies using a scaled down low-voltage laboratory prototype.

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List of Publications

It is acknowledged that most of the results from this work has been published in the following journal articles and conferences.

Journal articles

1. Md Mubashwar Hasan, Ahmed Abu-Siada, Syed M. Islam, and S. M. Muyeen. "A Novel Concept for Three-Phase Cascaded Multilevel Inverter Topologies." *Energies*, *11*(2), 268 (January 2018).
2. Md Mubashwar Hasan, Ahmed Abu-Siada, and Mohamed SA Dahidah. "A Three-Phase Symmetrical DC-Link Multilevel Inverter with Reduced Number of DC Sources." *IEEE Transactions on Power Electronics* (2018, In press)
3. Md Mubashwar Hasan, Ahmed Abu-Siada, and Md. Rabiul Islam. "Design and implementation of a novel three-phase cascaded half-bridge inverter." *IET Power Electronics* , Volume 9, Issue 8, June 2016, p. 1741 – 1752
4. Md Mubashwar Hasan, Ahmed Abu-Siada, Syed M. Islam, and Mohamed SA Dahidah. "A New Cascaded Multilevel Inverter Topology with Galvanic Isolation." IEEE Transactions on Industrial Applications (2018, In press)

Conference Papers

1. Md Mubashwar Hasan, and A. Abu-Siada. "A high frequency linked modular cascaded multilevel inverter." In 2016 IEEE I*ndustrial Electronics and Applications Conference (IEACon),* pp. 47-51., 2016.
2. Md Mubashwar Hasan, and A. Abu-Siada. "A novel three phase cascaded multilevel inverter topology." In 2016 IEEE *Industrial Electronics and Applications Conference (IEACon),* pp. 31-35.
3. Md Mubashwar Hasan, Ahmed Abu-Siada, and Md Rabiul Islam. "Investigation of low switching frequency control of a three phase cascaded H-bridge multilevel inverter." In 2016 IEEE *Electrical, Computer & Telecommunication Engineering (ICECTE), International Conference on*, pp. 1-5.
4. Md Mubashwar Hasan, A. Abu-Siada, Syed M. Islam, and S. M. Muyeen. "A Novel Generalized Concept for Three Phase Cascaded Multilevel Inverter Topologies." In *2017 IEEE Ninth Annual Green Technologies Conference (GreenTech),* pp. 110-117.

5. Md Mubashwar Hasan, A. Abu-Siada, Syed M. Islam, and S. M. Muyeen. “A three-phase half-bridge cascaded inverter with reduced number of input DC supply.”2017 Australasian Universities Power Engineering Conference (AUPEC)

Book chapters

1. Islam, Syed M., Chem V. Nayar, Ahmed Abu-Siada, and Md Mubashwar Hasan. "Power Electronics for Renewable Energy Sources." In *Power Electronics Handbook (Fourth Edition)*, pp. 783-827. 2018.

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List of Abbreviations

AC	Alternating Current
BD	Bi-directional
CHB	Cascaded H-bridge
CMLI	Cascaded Multilevel inverter
DC	Direct current
DSP	digital signal processor
FC	flying capacitor
GEEP	Green Electric Energy Park
HFML	High Frequency-Magnetic link
IGBT	Insulated Gate Bipolar Transistors
LNG	liquefied natural gas
MWT	multi-winding transformer
MLI	Multilevel inverter
NPC	Neutral point clamp
PV	photo-voltaic
SPWM	Pulse-Width Modulation
SWV	square wave voltage
THD	total harmonic distortion

Chapter One: Introduction

1.1. Motivation and background of the study

The consumption and demand of energy is gradually increasing due to the worldwide rapid industrial development. Owing to the significant consumption of conventional petroleum-based fuel, the world healthy environment is under vulnerable threat. The concept of alternative source of electrical energy or renewable energy sources has come to the attention of the global countries in the last two decades. These new sources are usually interfaced with the electricity grid through power electronic converters. The performance of renewable energy sources such as photo-voltaic and wind turbine is impacted by several environmental conditions including sun radiation, temperature and wind speed. In many cases, the renewable energy source is accomplished with a battery storage system connected to a DC-AC converter [1]. Multilevel inverter (MLI) is gaining its popularity as a DC-AC converter in renewable energy systems, industrial applications [2, 3], liquefied natural gas (LNG), chemical, fuel and water plants, marine and electric vehicles, mining [3, 4], power generation and power-quality improvement devices [1]. There is a significant worldwide research activity aiming at maximizing MLI efficiency while minimizing its cost. Power electronic device count reduction is considered as one of the cost minimizing techniques of voltage source inverters. Also, the control of the inverter switching pulses is a very important section in designing a MLI with reduced device counts. The simplicity in control algorithm is always expected. Moreover, galvanic isolation between the inverter input DC voltage side and output voltage side is essential for grid connected inverters.

1.2 Problem statement of the research

Three MLI topologies, diode clamped or neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) MLI are considered as conventional MLI topology for commercial applications [2, 3]. While all these conventional MLI topologies are utilized in in various industrial applications, cascaded MLI is preferred for high power and voltage applications (6.6-13.8kV, 500 MVA) [3, 4]. The most attractive features of cascaded H-bridge inverter over the other conventional MLIs are modularity, simple and similar control to all H-bridge modules and requirement for cheap-low voltage switching devices to generate high voltage output [5]. In spite of having a wide range of applications of conventional MLIs, a number of attractive new cascaded

MLI (CMLI) topologies are proposed in the recent few years. New multilevel inverter topologies are mainly developed to reduce device counts as it is directly related with cost and physical size of the converter. Three-phase CMLI has been widely used in large-scale renewable energy applications to comply with the high power conversion requirement. Although several topologies have been proposed in the literatures with reduced device count, majority of these topologies have not been extended to three phase structures yet. It is a common trend that the number of components of single phase topologies to be tripled when they are extended to three phase structures [6-10]. This thesis is aimed at resolving this issue as per the objectives listed below.

1.3 Research objectives

The key objectives of this research proposal are summarised below:

1. Developing a cascaded MLI topology with reduced device count.
2. Developing a high frequency multi-winding transformer to facilitate the connection of the proposed MLI to a single DC bus system.
3. Developing an appropriate control algorithm for the proposed MLI in order to enhance the system efficiency and to improve the power quality of the generated waveforms.
4. Investigating the performance of the proposed topology under different loading and operating conditions.
5. Building a scaled down laboratory prototype for the proposed MLI topology.

1.4 Methodology

The research goals were achieved in three stages as descripted bellow:

- **Literature review**: An in-depth literature survey is performed on different multilevel inverter topologies and their control algorithms. The pros and cons as well as challenges were recorded and utilised in the next stage of proposing a new MLI topology. The literature survey helped to achieve knowledge on device count reduction techniques in multilevel inverter. Besides, it gives a clear idea on the renewable applications of multilevel inverter.
- **Modelling and simulation**: At early stage of the research, a number of existing multilevel inverter topologies were investigated, verified and simulated in Matlab/Simulink. This stage helped in mastering the software used in all simulation analysis. Two new MLI topologies were then developed and simulated in Matlab/Simulink. Simulation results are

tested for a number of operating condition, e.g., dynamic load change and various switching frequencies.

- **Experimental prototyping**: Experimental prototyping includes equipment purchase, prototype building, programming in C++ language for DSP operation, and finally, testing and comparing experimental results with the simulation results were conducted.

1.5 Significance of the work

Significance of the work presented in this thesis can be summarised as below:

- The proposed three phase CMLI topology with reduced device count will cut down the implementation cost and physical size of existing three phase multilevel inverters.

- The high frequency magnetic link (HFML) in the proposed three phase CMLI system not only ensures galvanic isolation, but also allows the CMLI to operate with a single input DC power supply.

-The potential applications of the proposed HFML CMLI can be anticipated in grid-connected renewable energy conversion systems, electric vehicle and motor drive applications.

The Australian Government has a target to meet 20% of electricity demand from renewable energy sources by 2020 [11]. Around 383 MW of PV was installed in Australia in 2010, where 99% was grid connected [11]. This project will bolster the research on Australian grid connected PV systems and multiple or hybrid renewable energy based generation.

1.6 Thesis outline

The main goal of this thesis is to find a simplified way to reduce the device count of the existing three phase cascaded multilevel inverters in which the main components comprise power electronic switches and dc-voltage supplies. In order to achieve the research goal, the research was accomplished by developing two cascaded MLI topologies. A half-bridge CMLI is proposed in Chapter-3 that reduces 67% of the dc-voltage supplies required by a counterpart conventional three phase half-bridge CMLI. While the half-bridge CMLI in Chapter-3 is able to reduce only the dc-voltage supplies, the half-bridge CMLI topology proposed in Chapter-4 not only reduces the dc-voltage supplies, but also the power electronic switches. On the other hand, Chapter-5 demonstrates the device reduction technique in a generalised pattern, where the device count of any existing cascaded MLI can be reduced using this generalized technique. Furthermore, Chapter-5 explains how a cascaded MLI can be operated by a single dc-source. This thesis consists of six chapters and the outline of the remaining chapters are as follows:

- Chapter 2 presents in depth literature survey on the conventional MLI and state-of-the-art MLI current topologies. Operating principles and pros and cons of the existing MLI are clearly described in this chapter.
- In chapter 3, a new three phase half-bridge CMLI is presented with reduced dc-voltage supplies and three phase transformer. This topology utilizes non-isolated dc-voltage supplies. While this topology is able to reduce the number of dc-voltage supplies, it cannot reduce the number switching devices. Sine pulse width modulation (SPWM) is utilized as switching pulses generator of the proposed half-bridge CMLI.
- The new CMLI topology introduced in chapter 4 is a further device reduction of the half-bridge MLI topology proposed in chapter 3. A brief comparison with other MLIs is provided to show the superiority of the proposed CMLI topology in this chapter. Low frequency staircase modulation technique is adopted as switching controller of the CMLI topology.
- In chapter 5, a high frequency multi-winding transformer is utilized to reduce the dc-voltage supplies of the proposed CMLI in chapter 4 to a single dc-source. Also, the topology proposed in chapter 4 is presented as a generalized device reduction technique in chapter 5, which can be applied to any existing cascaded MLI. The performance of the proposed technique is demonstrated through a number of case studies.
- Finally, chapter 6 presents the key conclusions and recommendation for future work.

Chapter Two: Comprehensive literature review for Cascaded Multilevel Inverter

2.1 Introduction

In recent years, multilevel inverters (MLI) have drawn much attention in academic and industrial research. The applications of MLI are found from a few kVA to multi-MVA power conversion systems. Nowadays, utilisation of MLI in renewable energy systems (photovoltaic, wind and hybrid systems) to enhance overall system reliability and efficiency is getting more attention. Besides, the applications of MLI is found in several sophisticated industrial sectors, railway, aircraft, mining, motor drive, electric vehicle and power-quality improvement. This chapter presents a comprehensive literature review for different mutilevel inverter topologies and their pros and cons. Also, a number of control algorithms of MLI topologies are presented and discussed.

2.2 Cascaded Multilevel inverter

Figure 2.1 shows a basic generalized classification of MLI topologies in which conventional and reduced device count MLI are the two major branches. An extensive research to reduce the components and to simplify the control algorithm for MLIs can be found in the literatures. This thesis is written following an in-depth study on MLI with reduced device count.

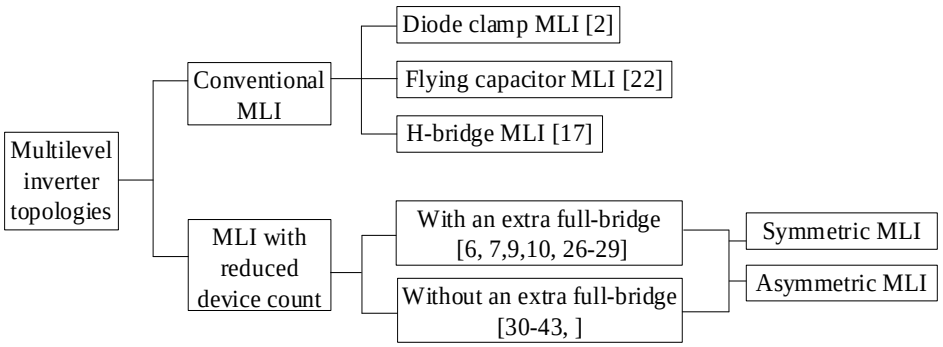


Figure 2. 1 Generalized classification of MLI

2.2.1 Basic concept of Multilevel inverter

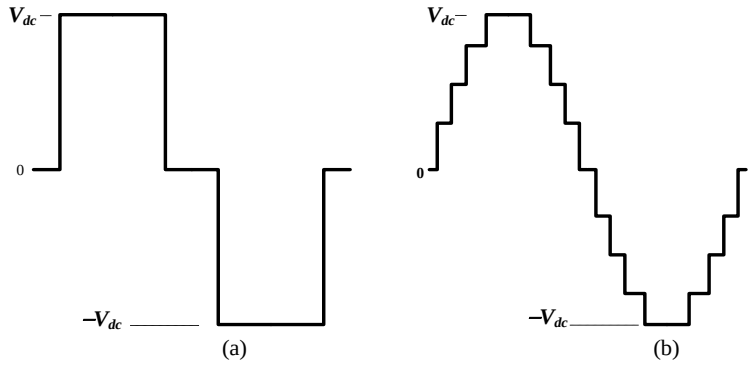


Figure 2. 2 voltage waveform (a) three level line voltage, (b) nine level line voltage

A conventional inverter contains three level (Fig. 2.2a) in its line voltage waveform, where as a multilevel inverter produces multiple steps (Fig. 2.2b) in its output voltage. Figure 2.2 shows a basic difference between the three level and nine level voltage waveforms. The multiple steps in the voltage waveform ensures reduction in total harmonic distortion (THD) and allows a multilevel inverter to be used in high power conversion.

2.2.2 Conventional MLI topologies

Three MLI topologies, diode clamped or neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) MLIs are considered as conventional MLI topologies for commercial applications [2, 3]. While all these conventional MLI topologies are utilized in commercial applications, cascaded MLI is preferred for high power, high voltage applications (6.6-13.8kV, 500 MVA) [3, 4]. The most attractive features of cascaded H-bridge inverter over the other conventional MLIs are modularity, simple and similar control to all H-bridge modules and the utilization of cheap-low voltage switching devices to generate high voltage output [5].

An extensive research has been conducted on CHB MLI aiming at simplifying the management of the input dc voltage sources. In [12], a 25-level CHB MLI is proposed as a wind energy converter (11kV, 1.8MW), which replaces the grid side step-up transformer. In this structure, H-bridge modules are connected with the multi-coil wind generator through active rectifiers. Similar multi-coil wind generator-based CHB MLI application is reported in [13], which is rated at 11kV, 2MW. In [14-16], a CHB MLI is proposed for different applications, e.g., electric vehicle, photo-voltaic

(PV), machine drive by utilizing single DC-supply. In these applications the output terminals of each H-bridge module is connected with a single phase transformers primary side while all secondary sides are connected in series with the load. The number of output voltage levels can be optimized by changing the turn ratio among of the single phase transformers. While this arrangement reduces the number of input DC power supplies and ensures galvanic isolation between load and inverter, it requires huge amount of single phase transformers which may increase the cost and size of the MLI.

In 2007, a high frequency (20kHz) linked toroidal transformer based modular CHB MLI is proposed for high voltage (6.6kV) applications [5]. Despite maintaining all features of modular CHB MLI, this design introduces a new concept of CHB that utilizes power electronic switches of low device rating (1.2 kV) and low voltage input, 350V to generate 6.6kV. Besides, ensuring galvanic isolation between load and MLI, it requires only one DC-source (which may be PV source, battery or rectified wind generator output). Such high frequency transformer based MLI has a potential application in electrical railways and renewable energy conversion as the size of the whole converter is lighter, more compact and cheaper than the 50/60Hz operated transformer based CHB [5, 17, 18].

In 2010, a step down high frequency transformer based asymmetrical CHB MLI is proposed for traction drives by utilizing single DC supply [19]. The concept proposed in [5] is utilized in [19] for designing high frequency toroidal transformer. While the topology in [19] optimizes the number of levels in the output voltage by utilizing reduced number of power electronic devices, it does not retain modular structure of CHB MLI and it is not suitable for high voltage applications due to its asymmetrical structure.

In 2014, a step-up high frequency transformer based modular CHB MLI is presented for grid connected renewable energy systems [17]. A number of amorphous alloy, *Metglas* 2605SA1, 2605S3A is utilized to build the high frequency transformer to investigate their performances. This MLI can be utilized as a grid side step-up (11kV) transformer-less inverter, which completely ensures galvanic isolation between inverter and grid [17].

2.2.3 Benefits of Multilevel inverter

The main advantages of multilevel inverter are:

- Requires low voltage switching device to produce high voltage inverter output.

- The output multilevel voltage waveform is very close to sine wave and hence, multilevel inverters require reduced size of filter.
- The switching devices in MLI gets less dv/dt stress, which reduces semiconductor isolation risk.
- Moreover, it eliminates common mode voltage, which reduces overcurrent issue in an inverter operated with induction motor.
- It has the ability of high voltage DC-AC conversion, which can facilitate a transformer less inverter for direct grid connection of renewable sources.

2.2.4 Shortcomings of MLI

Despite the several advantages listed above, MLI have some limitation too. The main drawback in MLI technology is the requirement of huge number of power electronic devices and dc supplies. The excessive amount of power electronic device count not only makes a MLI bulky in size, but it increases its cost as well. Moreover, the isolated DC supply voltage management and switching control become more complex.

2.3 Basic MLI topologies

While a wide range of MLI structures can be found in the literature, three circuital configurations are considered as basic topologies in MLI family. These are:

1. Diode clamp or Neutral point clamp (NPC) MLI
2. Flying capacitor (FC) MLI
3. Cascaded H-bridge (CHB) MLI

2.3.1 Diode clamp or Neutral point clamp (NPC) MLI

Diode clamp MLI consists of a common DC bus, a number of balancing capacitors, clamping diodes and semiconductor switches to generate multilevel AC voltage. A five level NPC MLI was first proposed in 1981 [2].

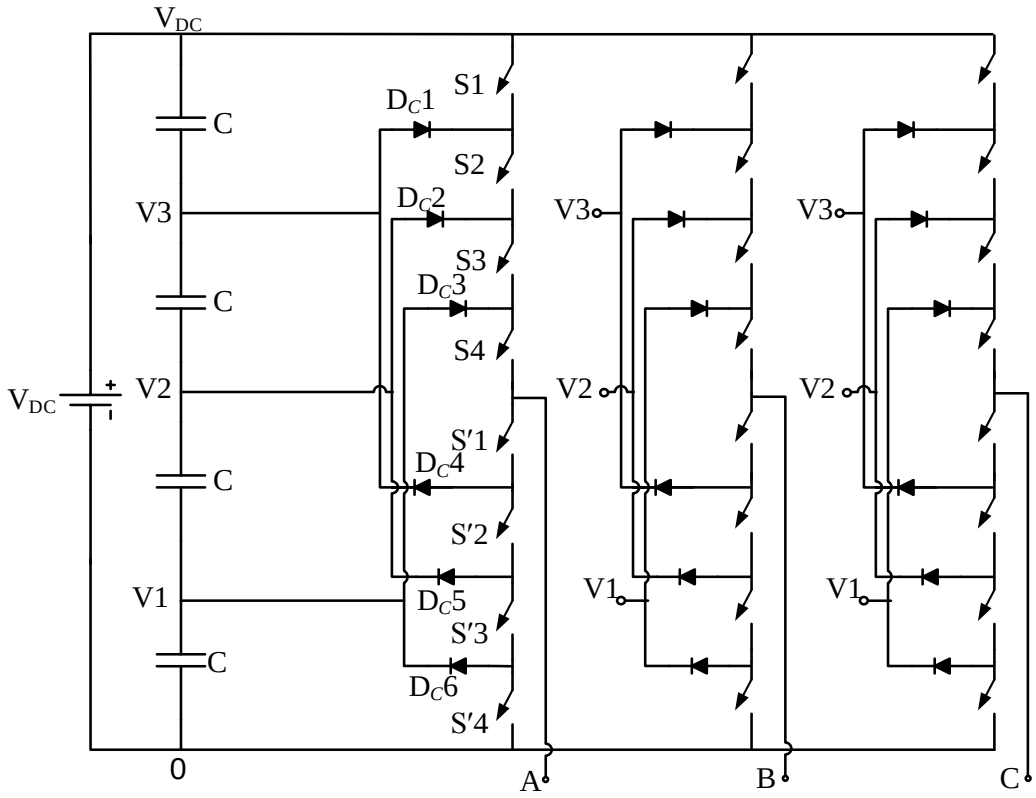


Figure 2. 3 A five level diode clam MLI [2]

Table 2. 1 Switching logic to generate 5-level output voltage

Phase voltage	Turn on switches
V_{DC}	S_1, S_2, S_3, S_4
V_3	S_2, S_3, S_4, S'_1
V_2	S_3, S_4, S'_1, S'_2
V_1	S_4, S'_1, S'_2, S'_3
0	S'_1, S'_2, S'_3, , S'_4

A five level diode clamp MLI is shown in Fig. 2.3, where each phase leg contains eight switches (S_1, S_2. S_3. S_4, S'_1, S'_2, S'_3, S'_4) and five clamped capacitors with equal capacitance C which create four node voltages, 0, V_1, V_2, V_3. The capacitors are fed by a dc bus voltage, V_{DC}. Table 2.1 shows the switching logics to generate the multilevel voltage in the MLI output by utilizing the capacitor nodal voltages.

Challenges in NPC MLI are listed below:

a. It requires excessive number of clamping diodes and switches, which may increase the cost.

b. The voltage balancing control of the clamped capacitors is very complex which limits the utilization of this inverter in high power applications [20].

Applications of NPC MLI are found in motor drive that is widely utilized in metals, mining, marine, and chemical, oil and gas industries [21].

2.3.2 Flying capacitor Multilevel inverter

Flying capacitor (FC) MLI was first proposed in 1992 [22]. While the circuital structure looks very similar to diode clamp MLI, the clamped diodes of NPC are replaced with clamped capacitors in FC MLI. Fig. 2.4 shows the phase leg-A of a five level FCMLI inverter. The clamping capacitors are arranged such a way that each capacitor gets the same voltage, e.g. $V_c=V_{dc}/4$. Table 2.2 shows the switching logics to generate five levels in the FCMLI output voltage. One of the main advantages of this topology is that it can be utilized easily in controlling real and reactive power flow. Besides, the clamped capacitors have a capability to sustain undistorted voltage output, while there might have a short time input power outage.

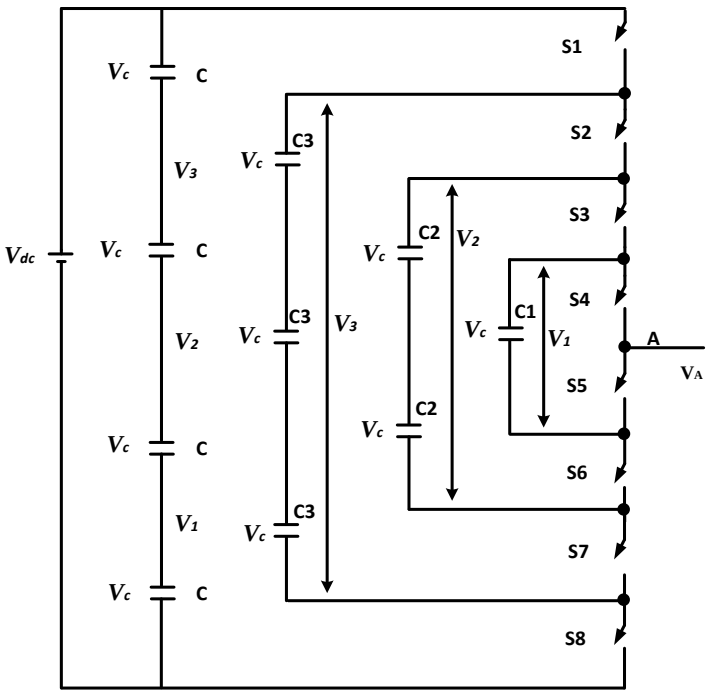


Figure 2.4 A phase leg of five level FC MLI [22]

Table 2.2 Switching logic to generate 5-level output voltage

Phase voltage	Turn on switches
V_{DC}	S_1, S_2, S_3, S_4
V_3	S_2, S_3, S_4, S_8
V_2	S_3, S_4, S_7, S_8
V_1	S_4, S_6, S_7, S_8
0	S_5, S_6, S_7, S_8

Unlike diode clamp MLI, FCMLI doesn't require any clamping diode that reduce power electronic device counts. Besides, more number of levels in the output line voltage can be achieved by utilizing FCMLI than a diode clamp MLI.

Challenges involved with NPC MLI are listed below:

a. While FCMLI is good for obtaining lower number of voltage levels, it becomes very complex when higher number of voltage levels is required. Capacitor voltage balancing becomes very difficult in case higher voltage level structure [20, 23].

b. This topology is not suitable for high voltage applications and a single input DC power supply manages full load in operation [20]

c. The utilization of a large number of capacitor arrangement makes the inverter bulky as well as expensive.

FCMLI is very attractive in industrial adjustable-speed drive (ASD) applications as it requires single input DC power supply. Besides, it has a potential application in electric vehicles.

2.3.3 Cascaded H-bridge (CHB) Multilevel inverter

A cascaded H-bridge MLI (CHBMLI) contains series connected H-bridge cells, where each H-bridge cell consists of four semiconductor switches and a DC-power supply as depicted in Fig. 2.5a. Fig. 2.5b shows a CHBMLI, which has two H-bridge cells in its structure.

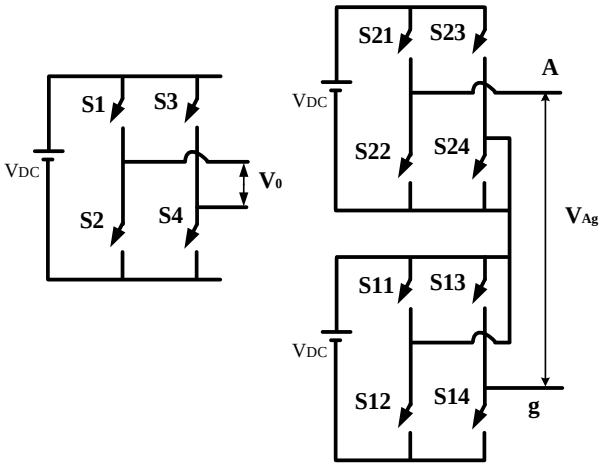


Figure 2.5 CHBMLI: (a) basic cell; (b) CHBMLI with two cascaded H-bridge cell [17]

Table 2. 3 Switching logic of basic H-bridge cell

Phase voltage	Turn on switches
V_{DC}	S_1, S_4
0	S_1, S_3 or S_2, S_4
- V_{DC}	S_2, S_3

Table 2.3 presents the switching functions for generating the voltage levels, V_{DC}, 0, - V_{DC} by a H-bridge cell. The most attractive features of CHBMLI include modularity, simple identical control, and it requires low voltage components to generate high voltage output. Fig. 4b shows phase-A of a three phase five level CHBMLI. It generates five levels in the inverter output voltage. The switching logic of the aforementioned five level CHBMLI is presented in Table 2.4.

Table 2. 4 Switching logic to generate 5-level output voltage

Phase voltage	Turn on switches
$2V_{DC}$	S_{11}, S_{14}, S_{21}, S_{24}
V_{DC}	S_{11}, S_{14}, S_{21}, S_{23}
0	S_{11}, S_{13}, S_{21}, S_{23}
$-V_{DC}$	S_{21}, S_{13}, S_{21}, S_{23}
$-2V_{DC}$	S_{12}, S_{13}, S_{22}, S_{24}

Along with symmetric CHBMLI [17], there are a number of asymmetric CHBMLI. Asymmetric methods are adopted to obtain more levels in the output voltage [14, 18, 19]. If any

aforementioned three conventional MLI generates m-number of voltage levels in the output voltage, the number of components and inverter efficiency in its three phase structure are listed in Table 2.5.

Table 2. 5 Comparison among the three conventional MLI

	Diode clamped	Flying Capacitor	CHB
Number of clamping diodes [7]	3*(*m*-1)*(*m*-2)	0	0
Number of clamping capacitors [7]	0	3(*m*-1)*(*m*-2)/2	0
Number of voltage divider capacitors [7]	3*(*m*-1)	3*(*m*-1)	0
Number of switching devices [7]	6*(*m*-1)	6*(*m*-1)	6*(*m*-1)
Number of DC supplies [7]	1	1	3(*m*-1)/2
Output Transformer [16]	1	1	1
Inverter Efficiency [17, 24, 25]	Up to 96%	Up to 97%	Up to 95%

This topology doesn't have any issue related with capacitor voltage balancing and hence, the switching control algorithm is very simple. Besides, modularity among the H-bridge modules brings more simplicity in its structure that allows fast replacement of the faulty module.

While CHBMLI doesn't require any balancing or clamping capacitor, it requires a number of isolated balanced dc supplies. The isolated DC-voltage supply management is considered a significant shortcoming of CHBMLI.

A wide range of applications of CHBMLI is found in the literature that include renewable energy, electric vehicles as a traction drive and electronic transformers.

2.4 Cascaded MLI topologies with reduced device counts

In this section, a number of cascaded MLI (CMLI) topologies with reduced device counts are reviewed thoroughly along with their operational principle and are classified under different sub-sections. While the switching logics of different cascaded MLI topologies are distinctive, the circuital shape of the topologies can be classified based on availability of an extra full-bridge.

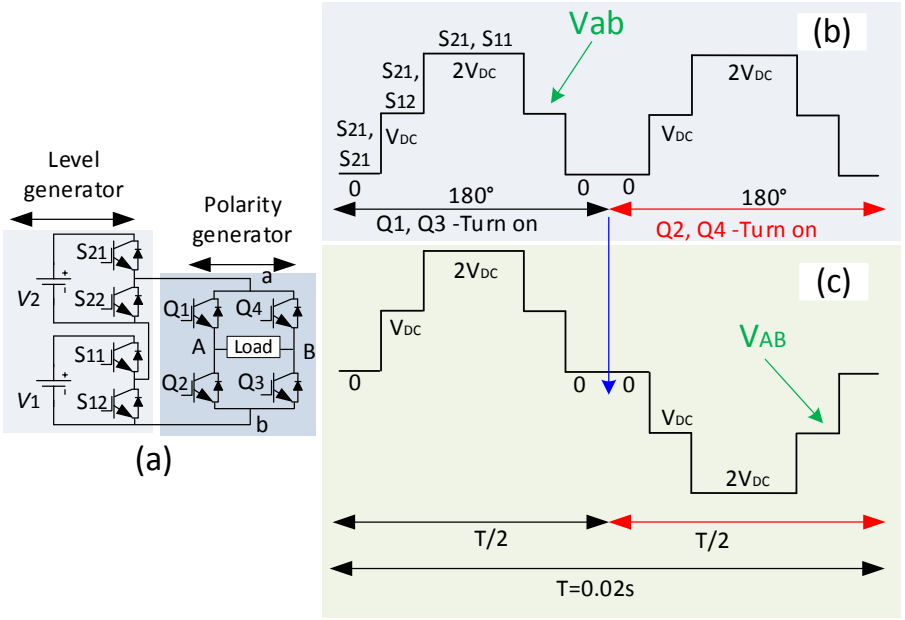


Figure 2. 6 Basic operation of level and polarity generator based CMLI: (a) cascaded half-bride topology, (b) level generator output voltage, (c) polarity generator output voltage [7, 9, 10]

2.4.1 Cascaded MLI topologies with an extra full-bridge

Most of the new CMLI topologies utilize a level generator and an extra Full-bridge as a polarity generator. The level generator is responsible to generate a unipolar multi-level voltage waveform for every 0.01 second (if intended AC voltage frequency is 50Hz). On the other hand, the extra Full-bridge is fed by the level generator stage output voltage and polarity generator changes the polarity of the unipolar multi-level voltage of level generator into bipolar AC voltage in every 0.01 second. While the level generator switching devices may operate with higher switching frequency than 50 Hz, the switching frequency of the extra Full-bridge in polarity generator is always 50Hz [8]. To elaborate the operational concept of level and polarity generator, an example is given in Fig. 2.6. Level generator and polarity generator in Fig. 2.6a consist of two half-bridge modules and a full-bridge, respectively. Two cascaded half-bridge modules in level generator are fed by equal voltage supplies, (V_1=V_2= V_{DC}) and produce three levels (0, V_{DC}, 2V_{DC}) in its unipolar output voltage, V_{ab} for 0.02s as shown Fig. 2.6b. The four switches, Q_1, Q_2, Q_3 and Q_4 in the polarity generator form two pairs and operate in complementary mode for every 0.01s to convert unipolar voltage, V_{ab} into bipolar voltage V_{AB} as shown in Fig. 2.6c.

2.4.1.1 New basic unit based CMLI

A new basic unit based MLI is proposed in [26]. The key features of this inverter are high modularity, ahievement of higher voltage levels in the output voltage, symmetric and asymetric input voltage among the inverter basic units and overall device count reduction.

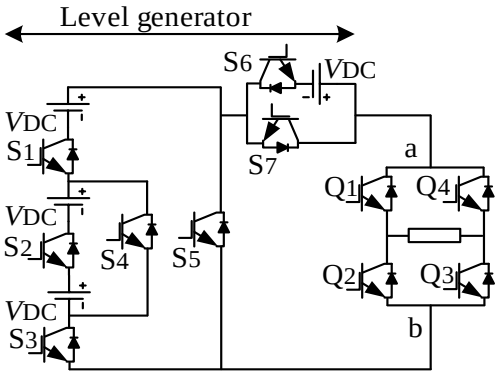


Table 2. 6 Switching operation

Voltage Level in V_{ab}	Turn on switches
0	Q_1, Q_4
V_{DC}	S_5, S_6
$2V_{DC}$	S_1, S_3, S_4, S_6
$3V_{DC}$	S_1, S_2, S_3, S_7
$4V_{DC}$	S_1, S_2, S_3, S_6

Figure 2. 7 Half-bridge CMLI with non-isolated DC supply

Fig. 2.7 shows a five level structure of the proposed topology in [26] and Table 4 shows the switching logics to generate the voltage levels in the inverter output.

2.4.1.2 Symmetric CMLI with bidirectional switches

A non-isolated DC supply based CMLI topology is proposed with reduced device counts in [6, 27]. This topology contains an innovative combination of unidirectional and bidirectional switches in the level generator part. This topology allows symmetrical DC supply only and exhibits minimum blocking voltage on the switches.

Table 2. 7 Switching operation

Voltage Level in V_{ab}	Turn on switches
0	Q_1, Q_4
V	S_{11}, S_{21}
2V	S_{12}, S_{21}
3V	S_{13}, S_{21}
4V	S_{14}, S_{21}
5V	S_{14}, S_{22}
6V	S_{14}, S_{23}
7V	S_{14}, S_{24}

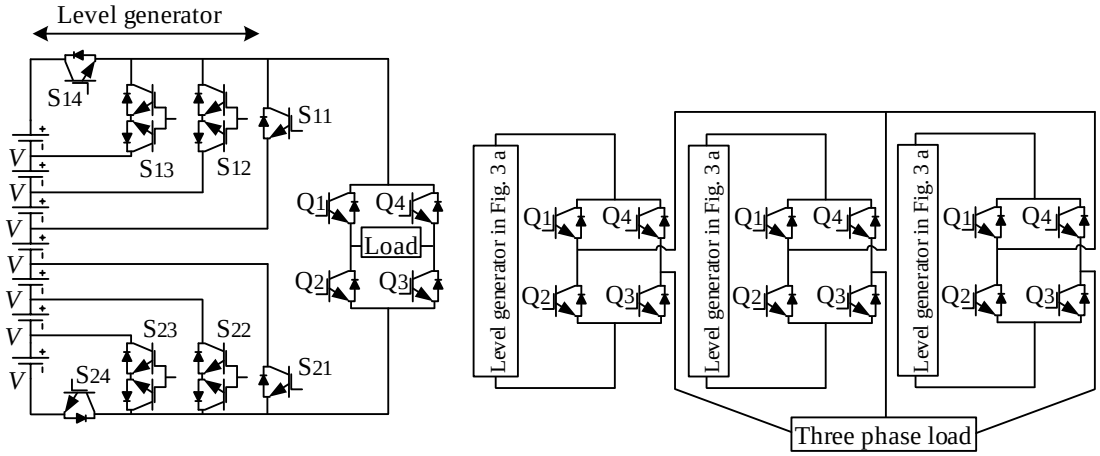


Figure 2. 8 Topology proposed in [6, 27] (a) single phase structure, (b) three phase structure

The single phase and three phase structures of the topology are as shown in Fig. 2.8a and 2.8b, respectively. The switching logics in level generation switches for different voltage levels is provided in Table 2.7.

2.4.1.3 CMLI topology with switched series/parallel DC voltage Sources

Table 2. 8 Switching operation

Voltage Level in V_{ab}	Turn on switches
V_1	S_{13}, S_{23}
V_2	S_{11}, S_{23}
V_3	S_{11}, S_{21}
V_1+V_2	S_{12}, S_{23}
V_2+V_3	S_{11}, S_{22}
V_3+V_1	S_{11}, S_{21}
$V_1+V_2+V_3$	S_{12}, S_{21}

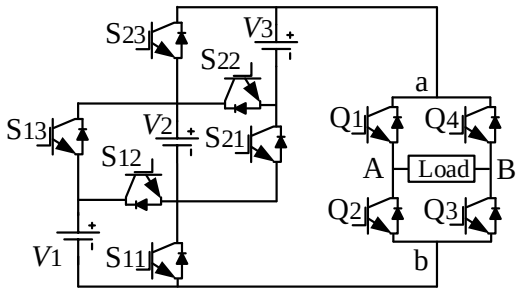


Figure 2. 9 CMLI topology with Switched Series/Parallel DC Voltage Sources [28]

A CMLI with reduced device count is proposed in [28]. This topology consists of a full-bridge in the polarity generator and a novel structure of switches along with DC-supplies. Fig. 2.9 shows the proposed CMLI topology with switched series/parallel DC voltage Sources. This inverter contains three DC supplies and can be extended to get more output voltage levels by connecting more DC supplies and switches in a similar pattern. Table 2.8 shows switching functions of the levels generation switches to get all the possible levels in the output voltage, V_{ab}. This topology allows symmetric and asymmetric input DC voltage supplies.

2.4.1.4 T-Type MLI

T-type MLI consists of an innovative level generation part and a polarity generator part [29]. A six level T-type MLI is shown in Fig. 2.10 and its switching operation is provided in Table 2.9. Level generation part in the T-type produces different voltage levels using multiple bidirectional switches.

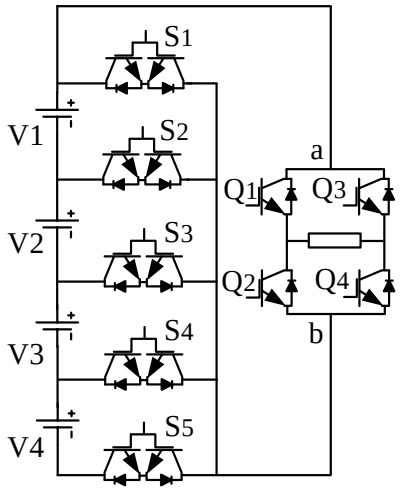


Figure 2. 10 T-type MLI [29]

Table 2. 9 Switching operation

Voltage Level in V_{ab}	Turn on switches
0	S_1
V1	S_2
V1+V2	S_3
V3+V4	S_4
V1+V2+V3	S_5
V1+V2+V3+V4+V5	S_1

2.4.2 Cascaded MLI topologies without extra full-bridge

There are many CMLI topologies, who don't require an extra Full-bridge to generate bi-polar AC voltage waveform. Some are listed below.

2.4.2.1 Cascaded Cross-switched CMLI

Cross-switched cascaded MLI consists of a number of semiconductor switches and isolated dc supplies in a cross shape arrangement as shown in Fig. 2.11a [30-34]. Table 2.10 shows the switching logics for generating different levels in the output voltage. This topology was extended for three phase voltage generation as presented in Fig. 2.11b.

Table 2. 10 Switching operation

Voltage Level in V_{ab}	Turn on switches
0	S_1, S_3, S_5, S_7
V_1	S_2, S_3, S_5, S_7
V_2	S_1, S_3, S_6, S_8
V_3	S_2, S_4, S_6, S_7
V_1+V_2	S_2, S_3, S_6, S_8
V_2+V_3	S_1, S_3, S_6, S_7
$V_1+V_2+V_3$	S_2, S_3, S_6, S_7
$-V_1$	S_1, S_4, S_6, S_8
$-V_2$	S_1, S_3, S_6, S_8
$-V_3$	S_1, S_3, S_5, S_8
$-(V_1+V_2)$	S_2, S_3, S_6, S_8
$-(V_2+V_3)$	S_2, S_4, S_5, S_8
$-(V_1+V_2+V_3)$	S_2, S_4, S_5, S_8

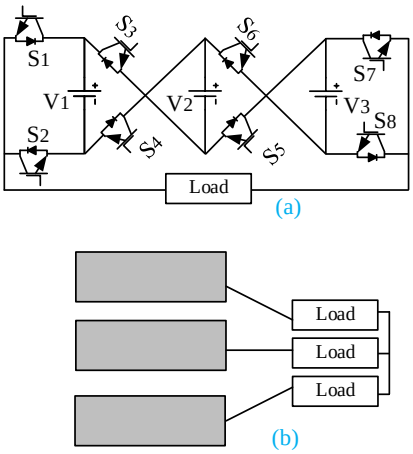


Figure 2. 11 crossed switched CMLI: (a) single phase structure, (b) three phase structure [30-34]

2.4.2.2 Cascade MLI with developed H-bridge

A new trend of Multilevel inverter was launched by the developed H-bridge based MLI in [35, 36]. It has six unidirectional switches and two isolated dc supplied in each basic unit as shown in Fig. 8. Basic units are able to generate positive and negative voltage levels by utilizing their innovative

switching arrangement, which is provided in Table 6. While the proposed topologies in [35, 36] present a successful implementation with different experimental results, the three phase structure of this topology is not demonstrated.

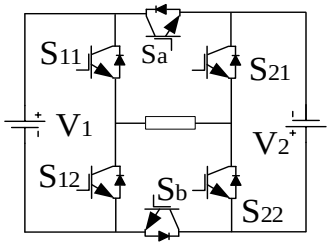


Figure 2. 12 Basic unit of developed H-bridge unit [35, 36]

Table 2. 11 Switching operation

Voltage Level in V_{ab}	Turn on switches
0	*S_{12}, S_b, S_{22}*
V_1	*S_{11}, S_{22}, S_b*
V_2	*S_{12}, S_b, S_{21}*
V_1+V_2	*S_{11}, S_b, S_{21}*
-V_1	*S_{12}, S_a, S_{21}*
-V_2	*S_{11}, S_a, S_{22}*
-(V_1+V_2)	*S_{12}, S_a, S_{22}*

2.4.2.3 U-cell CMLI

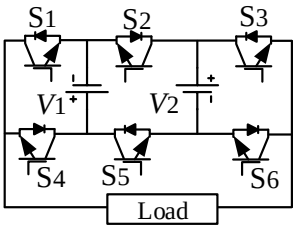


Figure 2. 13 A three level U-cell MLI [37-41]

Table 2. 12 Table Switching operation of U-cell

Voltage Level in V_{ab}	Turn on switches
0	*S_4, S_5, S_6*
V_1	*S_1, S_5, S_6*
V_2	*S_4, S_5, S_3*
V_1+V_2	*S_1, S_5, S_3*
-V_1	*S_4, S_2, S_3*
-V_2	*S_1, S_2, S_6*
-(V_1+V_2)	*S_2, S_4, S_6*

A four three level U-cell MLI is shown in Fig. 2.13 and its switching logics are presented in Table 2.12. Any U-cell in this topology contains two switches and an isolated dc-voltage supply. This topology is able to function under symmetric and asymmetric dc-voltage supply.

2.4.2.4 Envelope type (E-type) MLI

A new asymmetric E-type module based MLI is proposed in [42, 43]. A basic unit of E-type module is shown in Fig. 2.14 and Table 2.13 shows the switching function of that module. These modules can be connected in series to achieve higher number of voltage levels.

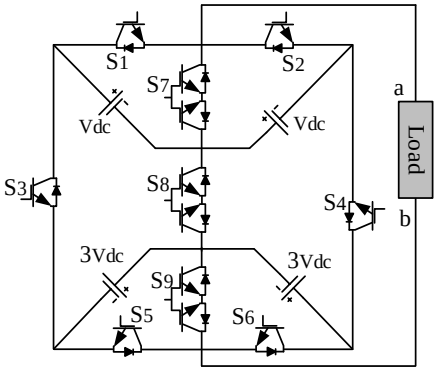


Figure 2. 14 A nine level E-type MLI topology [42, 43]

Table 2. 13 switching logic of E-type MLI

Voltage Level in V_{ab}	Turn on switches
$8V_{DC}$	S_1, S_4, S_5
$7V_{DC}$	S_4, S_5, S_7
$6V_{DC}$	S_2, S_4, S_5
$5V_{DC}$	S_1, S_4, S_9
$4V_{DC}$	S_1, S_5, S_8
$3V_{DC}$	S_5, S_7, S_8
$2V_{DC}$	S_2, S_5, S_8
V_{DC}	S_1, S_8, S_9
0	S_7, S_8, S_9
$-V_{DC}$	S_2, S_8, S_9
$-2V_{DC}$	S_1, S_6, S_8
$-3V_{DC}$	S_6, S_7, S_8
$-4V_{DC}$	S_2, S_6, S_8
$-5V_{DC}$	S_2, S_3, S_9
$-6V_{DC}$	S_1, S_3, S_6
$-7V_{DC}$	S_3, S_6, S_7
$-8V_{DC}$	S_2, S_3, S_6

Table 2.14 is provided to present the pros and cons of different reduced device count topologies described in the literature.

Table 2. 14 Pros and cons of different reduced device count topologies

Topology	Reference	Benefits	Shortcomings
Half-bridge	[7, 9, 10]	a. Modular structure and simple operation b. Able to work as a symmetric and asymmetric inverter c. Unidirectional switches are required only d. Homogeneous load sharing among the cells	a. Needs a number of isolated dc supplies b. Higher device rating in the extra full-bridge
Symmetric Bi-directional	[6, 27]	a. Minimum conduction losses b. Non-isolated dc supplies are required	a. Unequal load sharing b. Asymmetric structure is not possible c. High device voltage stress in the extra full-bridge
Switched series/parallel	[28]	a. Homogeneous load sharing among the cells b. Simple structure and accepts symmetric and asymmetric input voltage supplies	a. High device voltage stress
T-Type CMLI	[29]	a. Simple structure and needs non-isolated dc voltage supplies	a. Needs combination of uni-directional and bi-directional switches, which makes it expansive b. Unequal load sharing and High device voltage stress
developed H-bridge	[35, 36]	a. Optimizes the number of voltage levels	a. Lack of modularity b. Complex switching control design
U-cell CMLI	[37-41]	a. Reduced power loss and simple structure	a. Complex modulation technique b. Doesn't accept symmetric input dc voltage supplies
Envelope type (E-type) MLI	[42, 43]	a. Optimizes the number of voltage levels b. Simple operation c. Requires less number of switches and input voltage supplies	a. Three phase structure is not proposed b. Doesn't accept symmetric input dc supplies

2.5 Summary

An extensive research is found in the literature to develop new CMLI topologies complying with specific requirements and applications [44, 45]. Device count, simple structure, number of output voltage levels and cost effectiveness are crucial factors that should be considered while proposing a new CMLI topology [46, 47]. In the last few years a wide range of attractive CMLI topologies have been proposed and most of these topologies are only presented as a single-phase structure [26, 43, 48-50]. When extending such single phase topologies to three phase structure, the number of device counts is to be tripled which increases design complexity, cost and size of the three phase inverter [6, 10, 18, 29, 51-57].

Chapter Three: A Three-Phase Symmetrical DC-Link Multilevel Inverter with Reduced Number of DC Sources

3.1 Introduction

This chapter presents a novel three-phase DC-link multilevel inverter topology with reduced number of input DC power supplies. The proposed inverter consists of series-connected half-bridge modules to generate the multilevel waveform and a simple H-bridge module, acting as a polarity generator. The inverter output voltage is transferred to the load through a three-phase transformer, which facilitates a galvanic isolation between the inverter and the load. The proposed topology features many advantages when compared with the conventional multilevel inverters proposed in the literatures. These features include scalability, simple control, reduced number of DC voltage sources and less devices count. A simple sinusoidal pulse-width modulation technique is employed to control the proposed inverter. The performance of the inverter is evaluated under different loading conditions and a comparison with some existing topologies is also presented. The feasibility and effectiveness of the proposed inverter are confirmed through simulation and experimental studies using a scaled down low-voltage laboratory prototype.

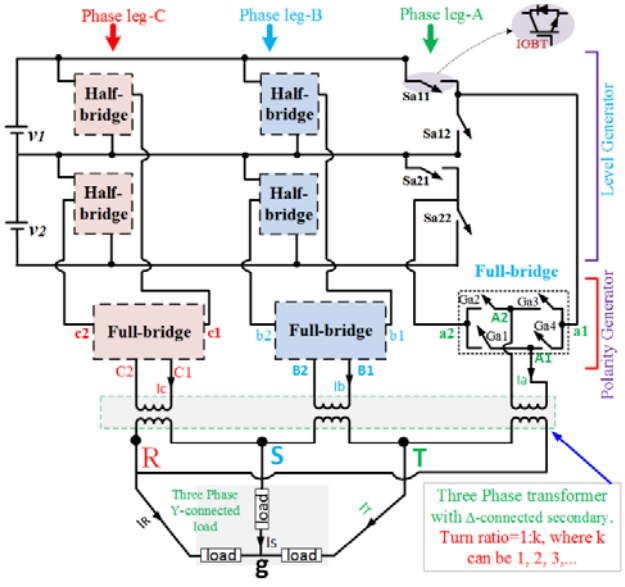


Figure 3. 1 The proposed three-phase CMLI with two half-bridge cells per phase leg

3.2 The proposed multilevel inverter and its modulation strategy

Figure 3.1 illustrates the proposed CMLI, which consists of two stages. The first stage is a level generator, which generates the unipolar multilevel voltage waveforms by utilizing the cascaded

half-bride modules. As shown in Fig. 3.1, each three half-bridge modules in the three-phase legs-A, B and C are fed from a non-isolated DC power supply. In reality, the DC-power supplies can be battery sources, or rectifier output terminals. Furthermore, the DC supplies can be equally obtained from photovoltaic (PV) output terminals or other renewable energy source. To realize constant output power and voltage for renewable energy sources of intermittent characteristics, some control algorithms such as constant voltage source mode can be employed [58]. It is worth noting that the half-bridge modules will have the same blocking voltage requirement since they are connected across the same DC-supply. This ensures modularity and simple control methods. The second stage is the polarity generator, which utilizes a simple full-bridge inverter to bipolarize the multilevel output voltage waveforms produced by the first stage.

A three-phase transformer couples the outputs of the polarity generator with the load, providing a galvanic isolation as well as boosting to the output voltage. It should be noted that although in Fig. 3.1 the transformer secondary windings are connected in Δ, it could be also connected in Y, if required. Furthermore, the CMLI presented in Fig. 3.1 can be easily expanded to generate higher number of levels in the output voltage waveform by adding more half-bridge modules into the level generator. The number of levels, *m* in the output voltage of each polarity generator by utilizing *n*-number of half-bridge modules in each phase leg is given by:

$$m=2n+1 \tag{3.1}$$

Considering equal input DC voltages ($v_1, v_2,\ldots,v_n$) to the *n*-number of the half-bridge modules in the level generator stage, the input DC voltages can be written as,

$$v_1= v_2,\ldots.=v_n=V_{DC}; \tag{3.2}$$

where V_{DC} represents a constant value

While the half-bridge modules in the level generator utilize low voltage, high switching frequency devices, the low frequency switches used in the full-bridge modules in the polarity generator experience a voltage stress of a magnitude equals to the summation of the input DC voltage sources [7]. Hence, the voltage stress or standing voltage, $V_{pg,\ stress}$ on the polarity generator switches can be expressed as,

$$V_{pg,\ stress}=nV_{DC} \tag{3.3}$$

It is to be noted that because they are operating at the fundamental switching frequency of 50 Hz, full-bridge modules do not exhibit significant switching losses. On the other side, state-of-the-art technology currently offers switching devices such as Insulated Gate Bipolar Transistors (IGBT)-module, FZ500R65KE3 that can withstand a collector to emitter voltage up to 6.5 kV [59]. Moreover, the operating voltage capacity of the switching devices can be extended by connecting

multiple switches in series. A number of CMLIs topologies utilizing half-bridge and H-bridge modules have been implemented for high voltage applications and can be found in the literatures [9, 60]. The rating of the switching devices in the proposed CMLI can be identified according to the voltage requirement of the intended application. It is worth mentioning that as the three-phase transformer is an essential component in the proposed topology, it will inherently fulfill the galvanic isolation requirement for renewable energy grid-connected applications [60].

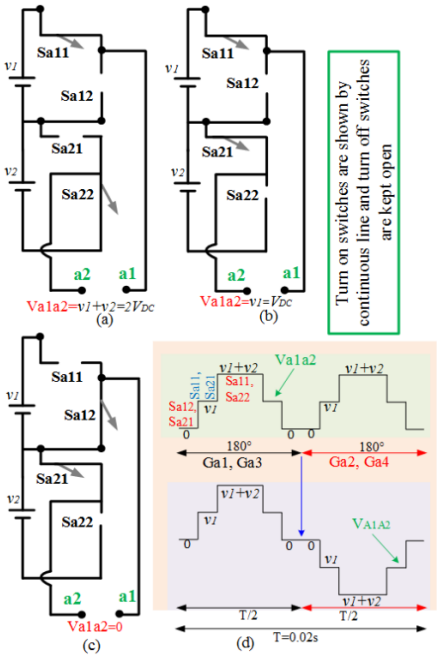


Figure 3. 2 Switching logics for generating different levels in the level generator output voltages: (a) logic for generating $2V_{DC}$, (b) logic for generating V_{DC}, (c) logic for generating 0, (d) desired output in the level generator and polarity generator output voltage

Figures 3.2(a)-(c) show the different switching states of the level generator, producing different output voltage levels (v_1+v_2, v_1, 0). Figure 2 (d) illustrates the generated AC output voltage in the polarity generator at phase leg-A, where the polarity generator flips the waveform in every 180^0.

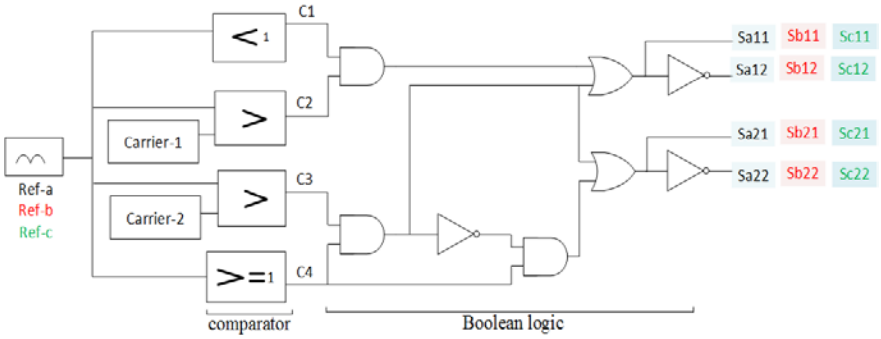


Figure 3. 3 Block diagram of the modulation technique

The main focus of this chapter is to develop a new inverter topology. Conventional Sinusoidal Pulse-Width Modulation (SPWM) technique is a well-known and easy to implement technique [61]. Hence, SPWM is adopted to demonstrate the effectiveness of the proposed topology. As shown in Fig. 3.3, the reference signals, Ref-a, Ref-b, Ref-c are the rectified sinusoidal waveforms with a 120^0 phase shift from each other. These are then compared with two carrier signals (carrier-1 and carrier-2) to generate the required gating signals. Same switching signals generation logic is utilized for each phase leg.

3.3 Semiconductor losses and converter efficiency

The semiconductor losses are considered as a crucial design and selection criterion for any converter circuit as they influence and define the required thermal management, which contributes to the estimation of the overall cost/volume/weight of the inverter. There are two dominant losses in the semiconductor devices; the static and the dynamic losses. The on-state resistance and the forward voltage drop of the semiconductor devices are responsible for the conduction losses, while the dynamic losses are produced during the turn on/off actions dictated by the switching frequency of the device.

The instantaneous conduction losses of a transistor $\left(\sigma_{c,T}\right)$ and a diode $(\sigma_{c,D})$ at any instant of time (t) can be expressed as,

$$\left.\begin{aligned}\sigma_{c,T}(t) &= [V_T + R_T\, i^{\beta}(t)]i(t)\\ \sigma_{c,D}(t) &= [V_D + R_D\, i(t)]i(t)\end{aligned}\right\} \tag{3.4}$$

Where, the on-state voltage drops of the transistor and diode are expressed by V_T and V_D, respectively. The on-state resistances of the transistor and diode, are given by R_T and R_D, respectively. β and $i(t)$ are the transistor amplification factor and a transistor or diode current at any instant of time, respectively.

Hence, the average conduction losses in both, the transistor and the diode, denoted by $P_{c,T}(t)$ and $P_{c,D}(t)$, respectively are given by:

$$\left.\begin{aligned}P_{c,T}(t) &= \tfrac{1}{2\pi}\textstyle\int_0^{2\pi}\big[\{V_T + R_T i^{\beta}(t)\}[72]ii(t)]\; d(\omega t)\\ P_{c,D}(t) &= \tfrac{1}{2\pi}\textstyle\int_0^{2\pi}[\{V_D + R_D\, i(t)\}i(t)]\; d(\omega t)\end{aligned}\right\} \tag{3.5}$$

The total average conduction losses can then be calculated from,

$$P_c(t) = \textstyle\int_0^{2\pi}[\{N_{Transistor}(t) * P_{c,T}(t)\} + \{N_{Diode}(t) * P_{c,D}(t)\}]d(\omega t) \tag{3.6}$$

where $N_{Transistor}$ and N_{Diode} are the number of transistors and diodes, respectively, in the same current path at any instant of time.

Similarly, the total switching power losses of the semiconductor devices are calculated by the energy losses during turn-on (t_{on}) and turn-off (t_{off}) periods. The switching energy losses during turn-on (E_{on}) and turn-off (E_{off}) can be derived from,

$$\left.\begin{aligned} E_{on} &= \int_0^{t_{on}} v(t)i(t)dt \\ &= \int_0^{t_{on}} \left[\left(\frac{V_{sw}}{t_{on}} * t\right)\left(-\frac{I}{t_{on}}\right) * (t - t_{on})\right] dt \\ &= \frac{1}{6} V_{sw} * I * t_{on} \\ E_{off} &= \int_0^{t_{off}} v(t)i(t)dt \\ &= \int_0^{t_{off}} \left[\left(\frac{V_{sw}}{t_{off}} * t\right)\left(-\frac{I'}{t_{off}}\right) * (t - t_{off})\right] dt \\ &= \frac{1}{6} V_{sw} * I' * t_{off} \end{aligned}\right\} \quad (3.7)$$

where V_{sw} and I, represent the off-state voltage and current of the device, respectively. I' represents the device current measured just before the device is turned off.

The total switching power losses (P_{sw}), for a time-period T can be calculated from,

$$P_{sw} = \frac{1}{T}\left[\sum_1^{N_{switch}}\{(N_{on} * E_{on}) + (N_{off} * E_{off})\}\right] \quad (3.8)$$

where the number of turn-on and off counts of a switch in a cycle is given by N_{on} and N_{off}, respectively.

The overall semiconductor losses of the proposed CMLI can be estimated by the total conduction and switching losses of all used semiconductors, expressed as:

$$P_{total\_loss} = P_c(t) + P_{sw} \quad (3.9)$$

If the output power is P_{out}, the inverter efficiency (η) can be calculated from:

$$\eta\% = \left(\frac{P_{out}}{P_{total\_loss} + P_{out}}\right) * 100\% \quad (3.10)$$

where the output power is calculated from:

$$P_{out} = \sqrt{3} * \frac{3V_{dc}}{\sqrt{2}} * \frac{I_{line}}{\sqrt{2}} * PF \quad (3.11)$$

If the power factor (PF) of the connected load is 0.79 lagging, when connecting a load of 20+j15.7Ω in each phase leg, the output power is 98.64 watts, which gives an overall efficiency of about 97%.

Table 3. 1 Properties System specifications of the proposed inverter

Input DC sources (v1, v2)	60V each
Carrier frequency	4 kHz
Switching controller	TMS320F2812
Ratings of IGBT	HGTG20N60B3D, 600V/40 A
Magnitudes of the line voltages	270V (peak)
Number of levels in line voltages	13

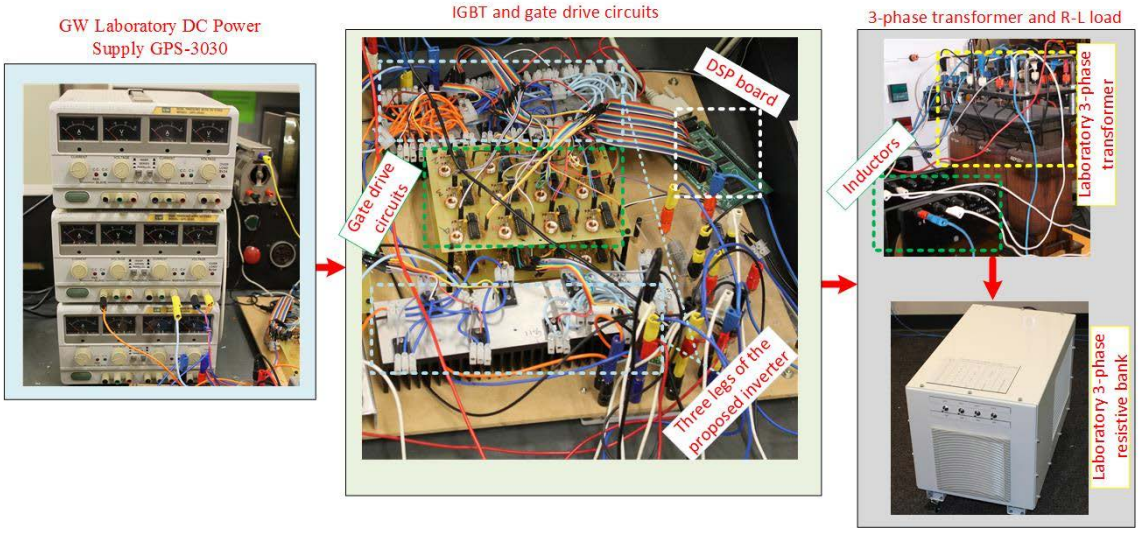


Figure 3. 4 Experimental test-rig setup

3.4 Simulation and experimental results

Fig. 3.4 illustrates the experimental test-rig of the proposed inverter, developed at the Green Electric Energy Park (GEEP), Curtin University [62]. On the other hand, simulation analysis is carried out using the Matlab/Simulink software package. The main parameters of the inverter prototype are summarized in Table 3.1. The input DC voltages from the 'GW Laboratory DC power supplies GPS-3030' are set to provide a constant DC voltage of 60V, i.e. (v_1=v_2=60 volts). Both, the level generator and polarity generator stages require twelve IGBTs, each. A digital signal processor (DSP), TMS320F2812 is used to generate the real time switching gate signals. The gate signals from the DSP are connected to the IGBT gates through 24-gate drive circuits. The role of gate drive circuits is to isolate the common ground of the DSP output gate pulses and boost-up their magnitudes to nearly 15 volts. As shown in Fig. 3.4, there are two printed circuit boards comprising 24-gate drive circuits for the 24 IGBTs in the level generator and polarity generator stages.

In this chapter, the conventional SPWM modulation strategy is considered with a carrier frequency of 4kHz for both, simulation and experimental studies. The modulation index M_i is expressed as [61].

$$M_i = \frac{A_m}{(N_p-1)A_c} \tag{3.12}$$

where A_m is the magnitude of the reference sine waveform and A_C is the magnitude of the carrier signal. Modulation index, M_i has an influence on the magnitude of the output line voltages and line currents [61]. The output of the polarity generator is connected to the primary of a three-phase isolation transformer with a turn ratio of 1:1, as shown in Fig. 3.4.

As previously mentioned, the secondary side of the transformer can be connected in either Δ or Y. The output line voltages can therefore be presented by (3.13) or (3.14) for Δ or Y connection, respectively.

$$\begin{bmatrix} V_{RS} \\ V_{ST} \\ V_{TS} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{C1C2} \\ V_{B1B2} \\ V_{A1A2} \end{bmatrix} \tag{3.13}$$

$$\begin{bmatrix} V_{RS} \\ V_{ST} \\ V_{TS} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}\begin{bmatrix} V_{C1C2} \\ V_{B1B2} \\ V_{A1A2} \end{bmatrix} \tag{3.14}$$

The performance of the proposed inverter under various loading conditions is assessed as elaborated in the following case studies.

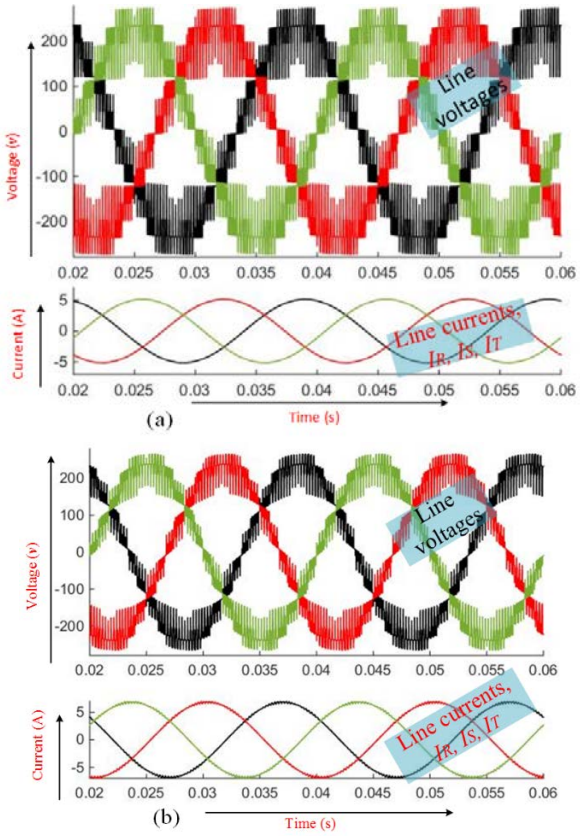


Figure 3. 5 Simulation results of the output line voltages and line currents for (a) load of 0.79 (lagging) power factor and (b) load of nearly unity power factor

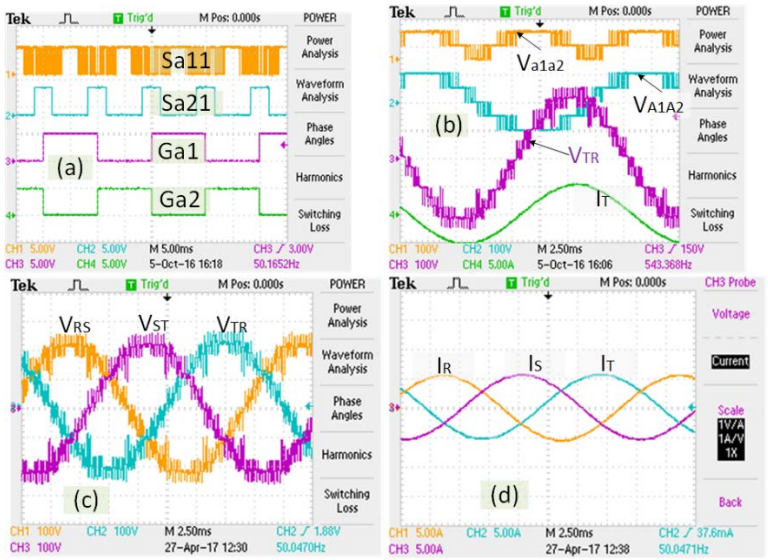


Figure 3. 6 Different experimental results for phase leg-A with a load of 0.79 lagging power factor: (a) gate pulses in half-bridge and full bridge module at phase leg-A, (b) level and polarity generator output voltages along with the line voltage and line current for phase leg-A, (c) three phase line voltages and (d) three phase line currents.

3.4.1 Case study 1: The impact of load power factor

Fig. 3.5 shows the simulation results of the line voltage and line current waveforms of the proposed inverter under load power factor of 0.79 (lagging) and 0.99 power factor, when each phase leg is connected with balanced inductive loads of (20+j15.7Ω) and (20+j1.57Ω), respectively.

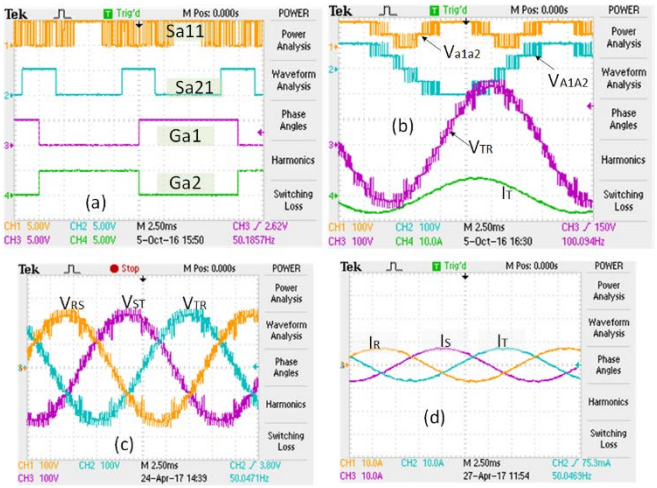


Figure 3. 7 Different experimental results for phase leg-A with a load of 0.99 power factor: (a) gate pulses in half-bridge and full bridge module at phase leg-A, (b) level and polarity generator output voltages along with the line voltage and line current for phase leg-A, (c) three phase line voltages and (d) three phase line currents.

On the other hand, Figs. 3.6 and 3.7 illustrate different experimental results for 0.79 (lagging) and 0.99 power factor loads, respectively.

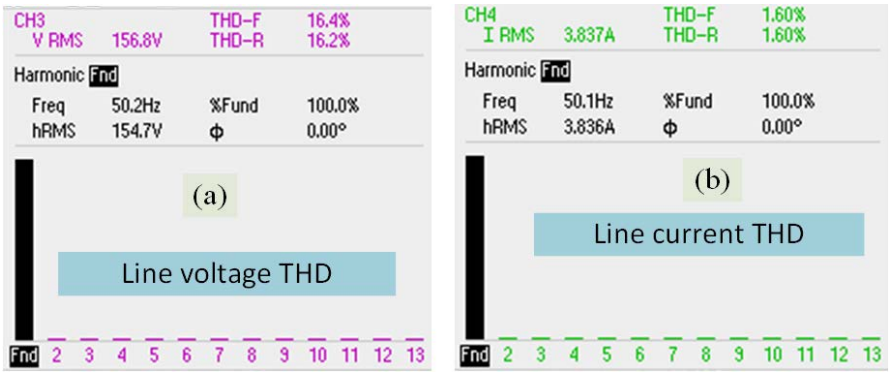


Figure 3. 8 THD results for 0.79 (lagging) PF load: (a) THD for line voltage waveform, (b) THD for line current waveform

Tektronix TPS2014B digital storage oscilloscope is utilized for capturing the experimental waveforms and displaying their harmonic spectrums. It is worth mentioning that, no harmonic filters were utilized while taking the results. Figs. 6(a) and 7(a) illustrate the experimental gating signals for both, the level generator and polarity generator switches, S_{a11}, S_{a21}, G_{a1}, G_{a2} in phase leg-A. The corresponding level generator output voltage (V_{a1a2}), the polarity generator output voltage (V_{A1A2}), line voltage (V_{TR}) and line current (I_T) are shown in Figs. 6(b) and 7(b). Moreover, Figs. 6(c), 6(d) and 7(c), 7(d) show the three-phase line voltages and line currents, respectively.

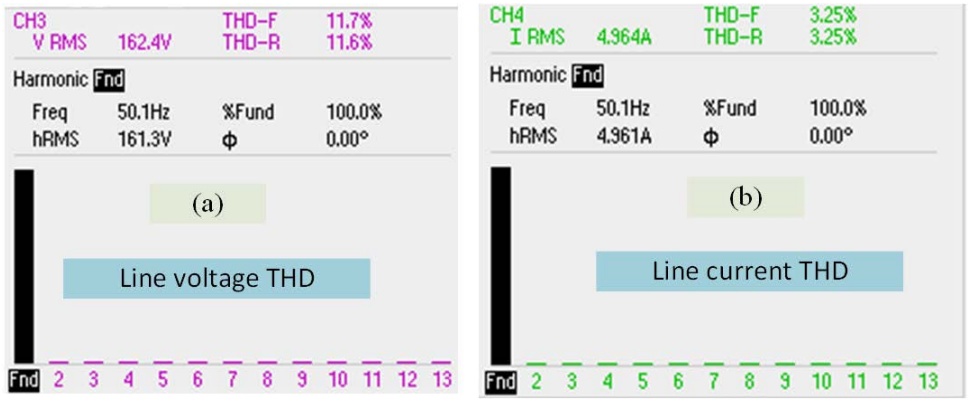


Figure 3. 9 THD results for nearly unity PF load: (a) THD for line voltage waveform, (b) THD for line current waveform

The total harmonic distortions (THD) of the line voltage and line current waveforms of the two cases above are shown in Figs. 3.8 and 3.9, respectively. It can be observed that the change of the load PF from 0.79 (lagging) to 0.99 does not influence the number of levels in the line voltage waveforms. However, the THD in the line voltage and line current waveforms is changed due to the change in the load PF.

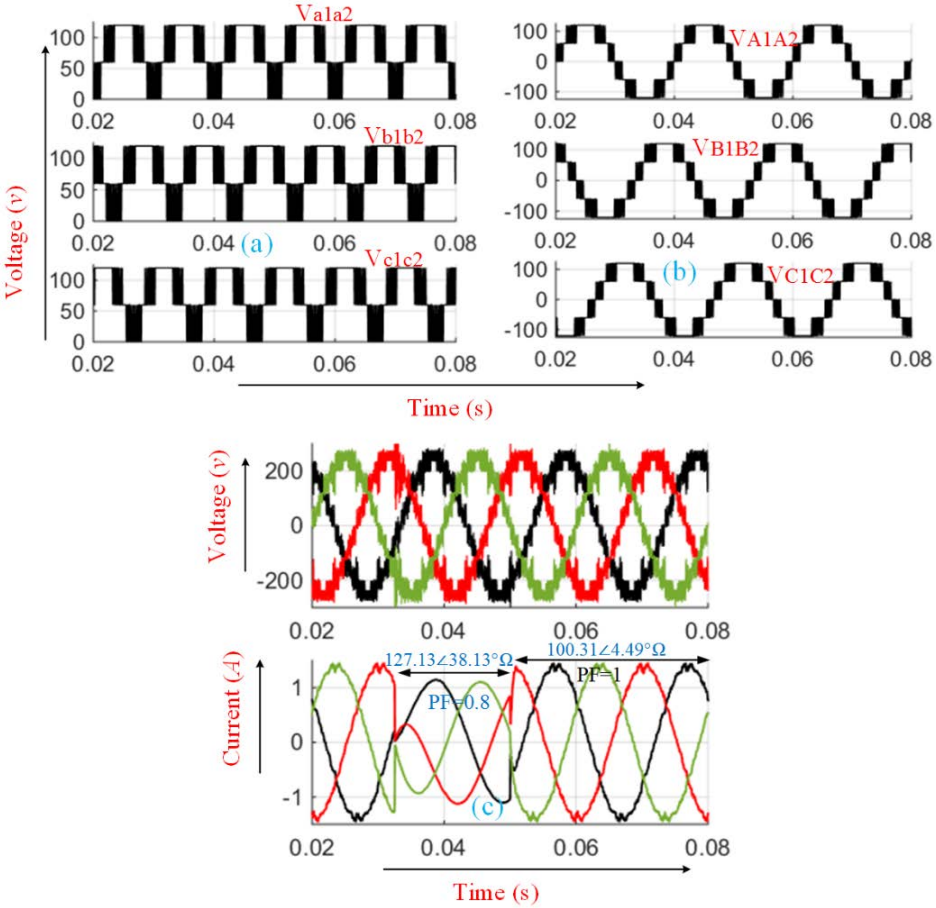


Figure 3. 10 Simulation results for a dynamic change in the load from 0.99 PF (100.31∠4.49°Ω) to 0.79 (lagging) PF (127.13∠38.13°Ω): (a) level generator output voltage, (b) polarity generator output voltage (phase voltage) and (c) line voltage and line current

It is worth mentioning that the inductance of an inductive load acts as a line current harmonic filter [63] , consequently, the line current comprises less harmonics in the case of 0.8 lagging PF load as opposed to unity PF load. The THD of the line current waveforms is less than 5% in both loading conditions, which satisfies the IEEE standard [64]. On the other hand, the value of voltage THD is less than the cascaded MLI proposed in [7, 9, 10, 65]. The line voltage THD can be kept within acceptable limit, if a small filter is connected at the output terminals or through increasing the number of levels in the line voltages by cascading more half-bridge cells in each phase leg.

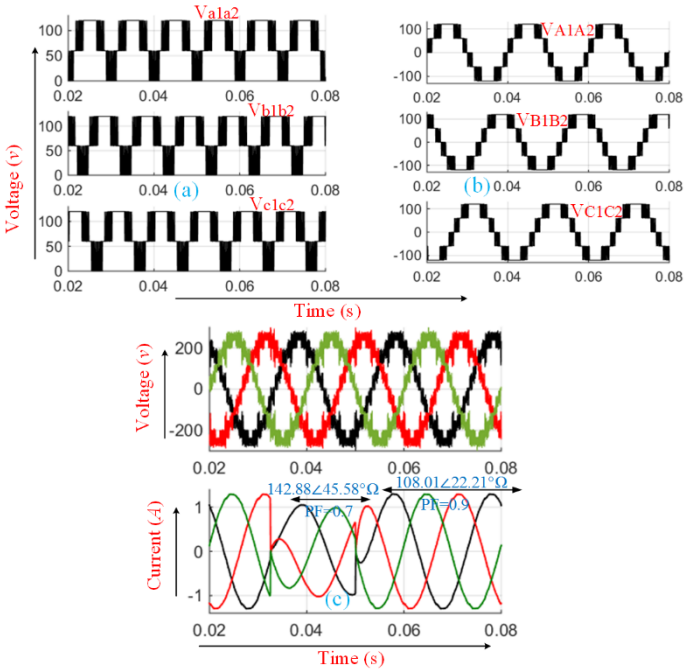


Figure 3. 11 Simulation results for a dynamic change in the load from nearly 0.9 lagging PF (108.01∠22.21°Ω) to 0.7 lagging PF (142.88∠45.58°Ω): (a) level generator output voltage, (b) polarity generator output voltage (phase voltage) and (c) line voltage and line current

3.4.2 Case study 2: The performance of inverter under load dynamics

Inverter output voltage and current waveforms are observed during load dynamic conditions. Fig. 3.10 shows the simulation results when a load of nearly unity power factor (100+j7.85Ω per phase leg) changed at t=0.0325s to 100+j78.5Ω per phase leg. It is assumed that this change lasts for a duration of 0.0175s after which the original load is retained.

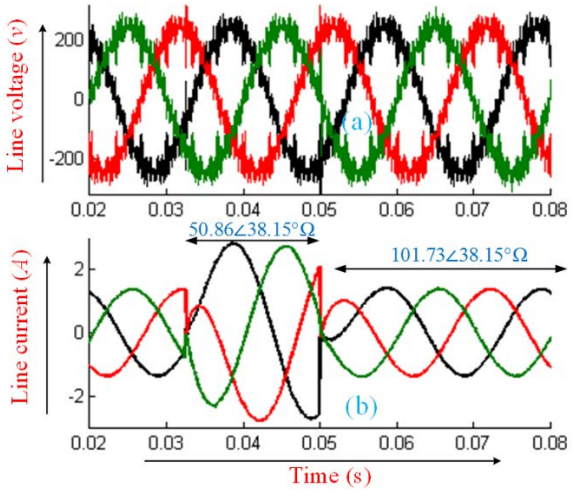


Figure 3. 12 Simulation results for a dynamic change in the load magnitude with the same PF: (a) Line voltage, (b) Line current

Although a little distortion can be observed in the line voltage waveforms in Fig. 3.10(c) during

the transition period, no effect is found on the level generator output voltages shown in Figs. 3.10(a) and 3.10(b). Similar observation can be seen in Fig. 3.11 when a load of 100+j40.82Ω per phase leg changes to 100+j102.05Ω per phase leg at t=0.0325s for a duration of 0.0175s.

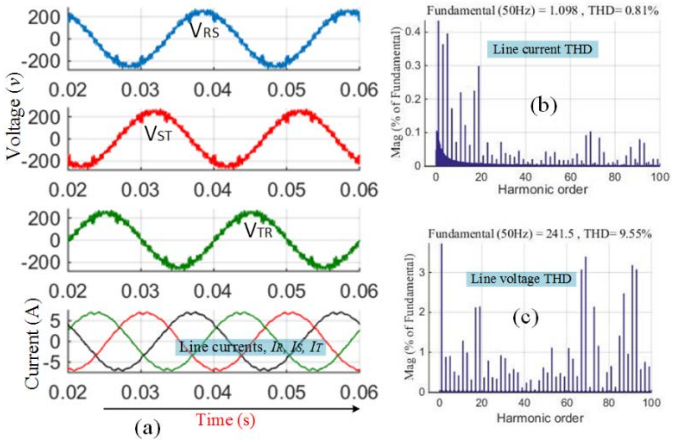


Figure 3. 13 Simulation results for carrier frequency of 8 kHz: (a) line voltages and currents, (b) line current THD, (c) line voltage THD

The performance of the proposed CMLI is also investigated with a change in the load magnitude with the same power factor. Fig. 3.12 shows the inverter line voltage and line current waveforms when the load is doubled (i.e. 40 +j31.42 Ω /phase leg to 80+j62.84 Ω /phase leg) at t=0.0325s for a duration of 0.0175s. Same observations in the above two cases can be noticed in this case study as well.

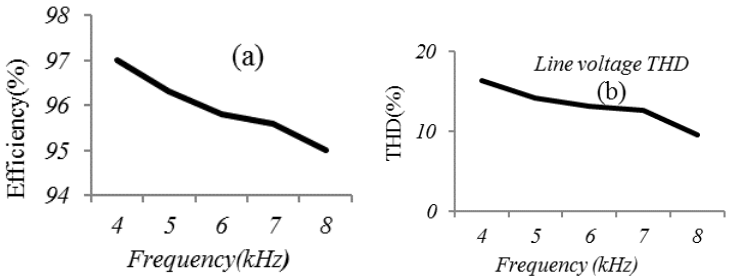


Figure 3. 14 Effect of carrier frequency on (a) Semiconductor efficiency, (b) Line voltage THD

3.4.3. Case study 3: Impact of changing the carrier frequency on the inverter performance

To assess the performance of the proposed inverter with high carrier frequency, the carrier frequency is increased from 4 kHz to 8 kHz. Fig. 3.13 shows the inverter's output line voltages and line currents at 8 kHz carrier frequency and a load of 20+j15.7Ω /phase leg. In this case, the THD of the line voltage and line current waveforms is reduced from 15.6% and 1.37% in case of 4 kHz carrier frequency to 9.55% and 0.81%; respectively in case of 8 kHz carrier frequency. The efficiency of the proposed inverter and the quality of the line voltage waveforms are

evaluated in a wide range of carrier frequencies. Figs. 3.14(a) and 3.14(b) show the THD of the line voltage waveforms and inverter semiconductor efficiency for a set of carrier frequencies. While the quality of the line voltage waveforms is found better for higher carrier frequencies, semiconductor efficiency degrades with higher frequencies due to increased switching losses.

A wide range of SPWM switching frequency (1 kHz to 12 kHz) has been proposed in the literature for different multilevel inverters topologies [9, 10, 47, 66]. The optimum switching frequency is a trade-off between switching losses and the quality of the output voltage and hence the size of the system. According to Fig. 3.14(a), to maintain the efficiency of the proposed inverter at 97% or above, a carrier frequency of 4 kHz is considered. The efficiency will be reduced to 95.8% if a carrier frequency of 6 kHz is used. On the other hand, the line voltage THD corresponding to 4 kHz carrier frequency is 15.6% while it slightly reduced to 13.14% with a carrier frequency of 6 kHz (Fig. 3.14(b)). Hence, for the proposed topology a carrier frequency of 4 kHz provides a satisfactory performance in terms of inverter efficiency and quality of the output waveforms. At this frequency, the THD in the line current was found to be 1.37% as per the above case studies.

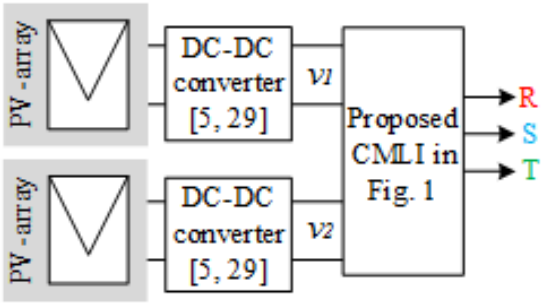


Figure 3. 15 Simplified block diagram for PV-application of the proposed CMLI

Table 3. 2 Inverter performance at different modulation index (based on simulation results)

Modulation index	0.6	0.7	0.8	0.9	1
Inverter efficiency (%)	76	80	94	95	97
Peak line voltage (V)	190	200	210	250	270
Peak line current (A)	3.3	3.54	3.8	4.6	5.2
$THD_{line\ voltage}$ (%)	38.11	36.92	34	23.3	15.6
$THD_{line\ current}$ (%)	3.62	2.51	2.14	1.53	1.37

3.4.4 Case study 4: Impact of Modulation index

Table 3.2 shows the inverter efficiency and the magnitudes of the inverter output line voltage and line current for different modulation indexes, M_i when the inverter is loaded by

20+j15.7Ω in each phase leg and operated at a carrier frequency of 4 kHz. As can be seen from Table 3.2, the inverter efficiency significantly reduced when M_i is less than 0.8. Table 2 also shows that while the magnitudes of the line voltage and line current increase with the increase of the modulation index, the THD in both waveforms is decreasing.

3.4.5 Case study 5: photovoltaic application

As mentioned in section II, the input DC supplies can be obtained from photovoltaic output terminals or other renewable energy source. In this case study, the feasibility of the proposed inverter with PV system is assessed. The performance of the proposed inverter is investigated by replacing the two input DC-power supplies in Fig. 3.1 by two PV-modules. A block diagram of PV-array connected to the proposed CMLI in this chapter is shown in Fig. 3.15. DC-DC converter is utilized to maintain the DC voltages v_1 and v_2 at constant levels as per the control approach proposed in [58, 67]. It is assumed that a constant voltage control algorithm as presented in [58, 67] is utilized to maintain the PV-modules output voltage at 80 volts as shown in Fig. 3.16(a). With a load of 20+j15.7Ω, the MLI output line voltage waveforms are as shown in Fig. 3.16(b). The number of levels and the THD of the output line voltage waveforms remain unchanged in comparison to the output waveforms depicted in Case study 1.

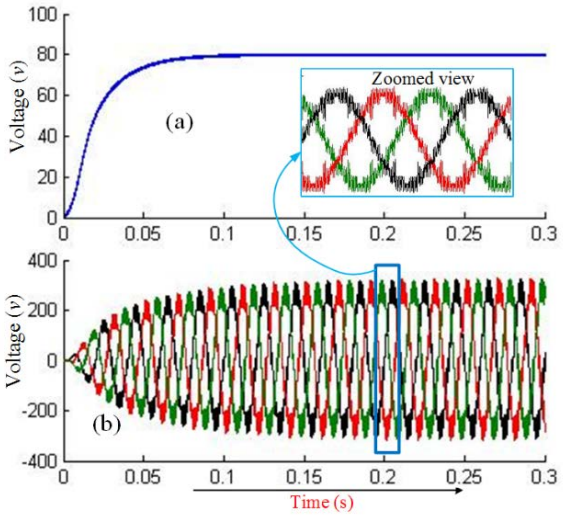


Figure 3. 16 PV application: (a) PV module output voltage, (b) proposed inverter output line voltage

In addition to their application in PV power conversion, half-bridge module based multilevel inverters have been also utilized for medium voltage and electric vehicle applications as reported in [65, 68]. It is expected that the topology proposed in this chapter can also be utilized for the aforementioned applications and provide additional advantages, e.g. galvanic isolation and reduced input DC-voltage supplies. According to manufacturers' data sheets [69], the utilized three-phase transformer is of high efficiency (up to 99%).

Hence, the overall efficiency of the proposed inverter will not be significantly affected in comparison with other existing half-bridge based CMLI. Moreover, as this topology requires less number of power electronic devices in comparison to other cascaded topologies, the overall losses are expected to be decreased.

3.5 Comparison with other MLI topologies

3.5.1 Comparison with conventional topologies

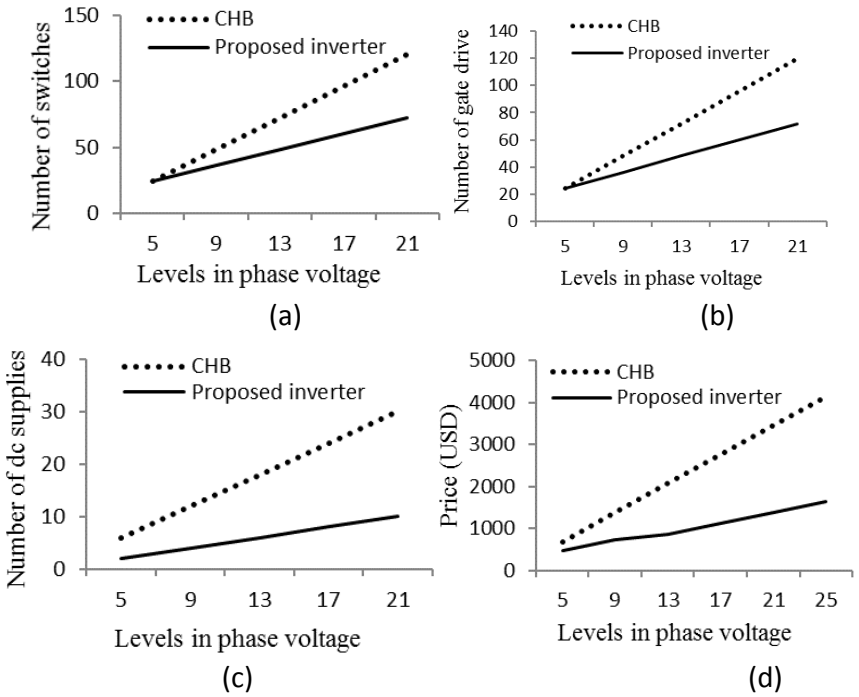


Figure 3. 17 Device counts and cost comparison with CHB: (a) number of switching devices, (b) number of gate drivers, (c) number of DC power supplies, (d) cost comparison per phase voltage level

Table 3.3 shows a general comparison between the proposed CMLI and conventional MLI i.e. diode clamped, flying capacitor and cascaded H-bridge (CHB) topologies with respect to the device count (as a function of the number of levels in the output voltage, m) and overall efficiency. In contrary with conventional MLI, Table 3.3 shows that the proposed CMLI does not require any diodes or capacitors, which is the main issue of conventional diode clamped and flying capacitor topologies [7]. The table also shows that the proposed topology requires 3(m+3) switching devices while other topologies require 6(m-1) switching devices. Hence, for any number of levels above 5, the proposed CMLI will require the least number of switching devices. Moreover, the proposed CMLI requires less number of DC-supplies than the CHB inverter.

Table 3. 3 Comparison between the proposed topology and conventional MLI

	Diode clamped	Flying Capacitor	CHB	Proposed CMLI
Number of clamping diodes [7]	3*(*m*-1)*(*m*-2)	0	0	0
Number of clamping capacitors [7]	0	3(*m*-1)*(*m*-2)/2	0	0
Number of voltage divider capacitors [7]	3*(*m*-1)	3*(*m*-1)	0	0
Number of switching devices [7]	6*(*m*-1)	6*(*m*-1)	6*(*m*-1)	3*(*m*+3)
Number of DC supplies [7]	1	1	3(*m*-1)/2	(*m*-1)/2
Output Transformer [16]	1	1	1	1
Inverter Efficiency [24] [25] [17]	Up to 96%	Up to 97%	Up to 95%	97%

Fig. 3.17 shows a comparison between the proposed inverter and conventional cascade H-bridge (CHB) inverter [5, 17] as a function of the number of levels *m* in the output voltage waveform. As shown in Fig. 3.17(a-c), the implementation of the proposed inverter calls for less number of power electronic switches, gate drive circuits and DC-supplies. Fig. 3.17(d) shows a cost comparison between the proposed CMLI and conventional CHB-based MLI to obtain 1.5kV (peak) in the line voltage. Cost estimation includes IGBT modules, gate drivers and full-bridge rectifiers and is based on 2017 market prices [70]. It is worth mentioning that a three phase transformer is an essential part in the conventional multilevel inverters for high-power grid integration to provide the required galvanic isolation [16]. Hence, the isolation transformer in the proposed topology in this chapter does not incur extra cost when the proposed cascaded inverter is utilized as a grid connected PV inverter. Fig. 3.17 shows that the proposed topology is a cost-effective choice when compared with the conventional CHB multilevel inverter topologies.

3.5.1 Comparison with conventional topologies

The main emphasis of the proposed inverter aimed at maximizing the number of output voltage levels with reduced number of DC-voltage supplies by utilizing the symmetry properties. Therefore, it is essential to compare the proposed topology with other equivalent half-bridge based topologies reported in the literatures [9, 10, 65] to confirm its superiority. As summarized from Table 3.4, different aspects are taken into account to draw a sensible comparison, this includes: the number of half-bridge cells, total number of power electronic switching devices, gate drive circuits, number of DC-power supplies or DC-link capacitors, number of the attainable output voltage levels in the line voltages.

Table 3. 4 Comparison of the proposed three-phase symmetric half-bridge topology with other half-bridge topologies proposed in the literatures

	Proposed topology in this chapter	Three phase topology proposed in [9]	Three phase topology proposed in [10]	Three phase topology proposed in [65]
No of half-bridge cells	6	6	15	9
No of total switching devices	24	24	42	18
No of gate driver	24	24	42	18
No of DC supplies or capacitors	2	6	15	9
No levels in the line voltage	13	9	11	7

As can be seen in Table 3.4, the proposed topology achieves higher number of output voltage levels by utilizing the same number of power electronic switching devices and gate drive circuits when compared with topologies proposed in [9, 10, 65].

Specifically, the topology proposed in [10], requires more than twice the number of total switching devices, gate drive circuits and DC-supplies for generating lower number of levels in the line voltage compared with the proposed topology in this chapter. On the other hand, although the topology proposed in [65], requires less number of symmetric half-bridge cells, it only generates seven-levels in the output line voltage. The topology proposed in [65] would require seven symmetric half-bridge modules in each phase leg to generate 13-level at the output line voltage, which is achieved in the proposed topology in this chapter by only using 3 symmetric half-bridge modules. This means, 42-switching device along with 19 DC-power supplies will be required, if the topology proposed in [65], is extended to generate 13-levels in the line voltage. Interestingly, the proposed cascaded multilevel inverter in this chapter requires the lowest number of DC-supplies than any other topology presented in Table 3.4.

3.6 Summary

This chapter presents a new symmetrical multilevel inverter topology with two different stages. The proposed inverter requires less power electronic devices and features modularity, hence simple structure, less cost, and high scalability. The number of input DC-supplies for the proposed topology is found to be nearly 67% less than the similar symmetric half-bridge topologies, which is a great achievement for industrial applications. This phenomenon will reduce the complexity of DC voltage management. As being a symmetric structure, all the switching devices experience same voltage stress, which is a very important factor for high voltage

applications. The feasibility of the proposed inverter is confirmed through simulation and experimental analysis for different operating conditions.

Chapter Four: Design and implementation of a novel three-phase cascaded half-bridge inverter

4.1 Introduction

In this chapter, a new circuit topology of a three phase half-bridge multilevel inverter (MLI) is proposed. While the three phase half-bridge topology presented in the former chapter able to reduce the number dc voltage supplies, this chapter introduces a device count reduction technique of half-bridge inverters which not only reduces the dc-voltage supplies, but also the power electronic devices. The proposed MLI that consists of a cascaded half-bridge structure along with a modified full-bridge structure requires less number of dc-power supplies and power semiconductor devices, e.g. insulated gate bipolar transistors and diodes when compared with the existing MLI topologies, which significantly reduces the size and cost of the inverter. Two different structures; isolated and non-isolated dc-power supply-based three-phase half-bridge MLIs are investigated. A number of generalized methods are proposed to determine the magnitude of the input dc-power supplies that has a great impact on the number of levels of the output voltage waveform. To verify the feasibility of the proposed MLI topology, a scaled down laboratory prototype three-phase half-bridge MLI is developed and the experimental results are analyzed and compared with the simulation results. Experimental and simulation results reveal the feasibility and excellent features of the proposed inverter system.

4.2 Proposed multilevel Inverter

The proposed inverter topology consists of half-bridge structure along with modified full-bridge structure, as depicted in Fig. 4. 1 which shows the proposed topology for the non-isolated (Fig. 4. 1a) and isolated (Fig. 4. 1b) dc-power supply-based half-bridge configuration. In each configuration, the half-bridge structure comprises n-number of series connected half-bridge modules. Each half-bridge module comprises two switches, G_{k1} and G_{k2} and a dc-power supply, E_k, where k can be any integer number. Each pair of switches, G_{k1} and G_{k2} in any half-bridge module are always working in complementary mode, i.e. if one switch is turned on, the other switch must be turned off. On the other hand, the modified full-bridge structure consists of three modified Full-bridge modules for the three-phase voltage generation. Each modified Full-bridge module has four switches, S_{x1}–S_{x4} and four power diodes, D_{x1}–D_{x4}, where x represents phase a, b or c. An input dc-power supply, $E_{(n+1)}$ is connected in parallel with all modified Full-bridge modules. The diodes (D_{x1}–D_{x2}) operate in conjugation to the switches (S_{x1}–S_{x2}) for providing proper blocking

between the modified Full-bridge modules and the Half-bridge structure while the diodes (D_{x3}–D_{x4}) take part during line voltage generation and prevent short circuit condition for the modified H-bridge modules when (S_{x1}–S_{x2}) is turned on. All utilized switches in the half-bridge and modified full-bridge structure are unidirectional. While the switches in the half-bridge structure contain internal anti-parallel diodes, switches in modified full-bridge structure do not utilize any diodes.

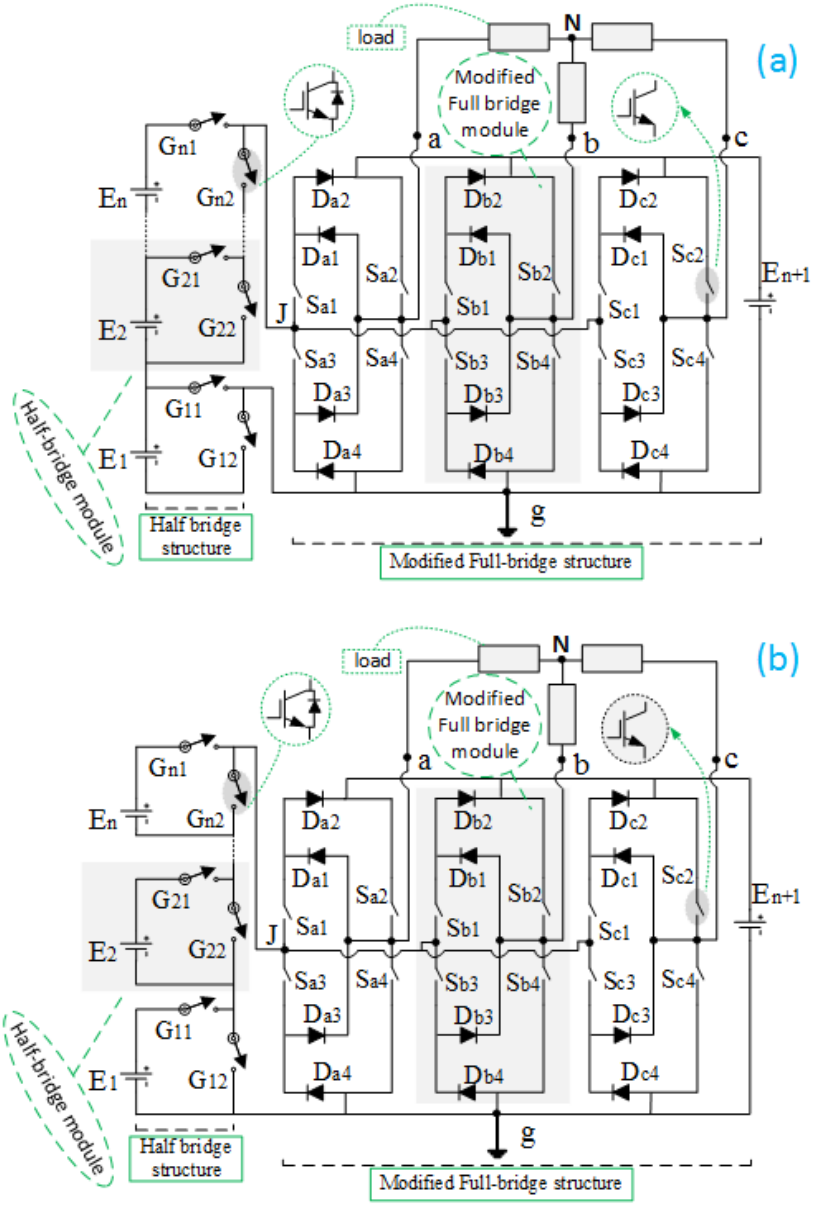


Figure 4. 1 Proposed generalized three phase half-bridge topology: (a) Non-isolated input dc-power supply-based half-bridge topology, (b) Isolated input dc-power supply-based half-bridge topology

The modified Full-bridge modules are connected with the half-bridge structure at a junction point 'J'. Only the modified Full-bridge modules are responsible to generate the maximum output voltage level (when S_{x2} is turned on) and zero voltage level (when S_{x4} is turned on) as shown in

Fig. 4.2a and 4.2b, respectively. The switches S_{x2} and S_{x4} are always operated in complementary mode on each phase arm a, b and c to avoid any short circuit fault. Both of the modified full-bridge and the half-bridge structures take part to generate the intermediate voltage levels between maximum, $E_{(n+1)}$ and zero voltage levels, as shown in Fig. 4. 2c.

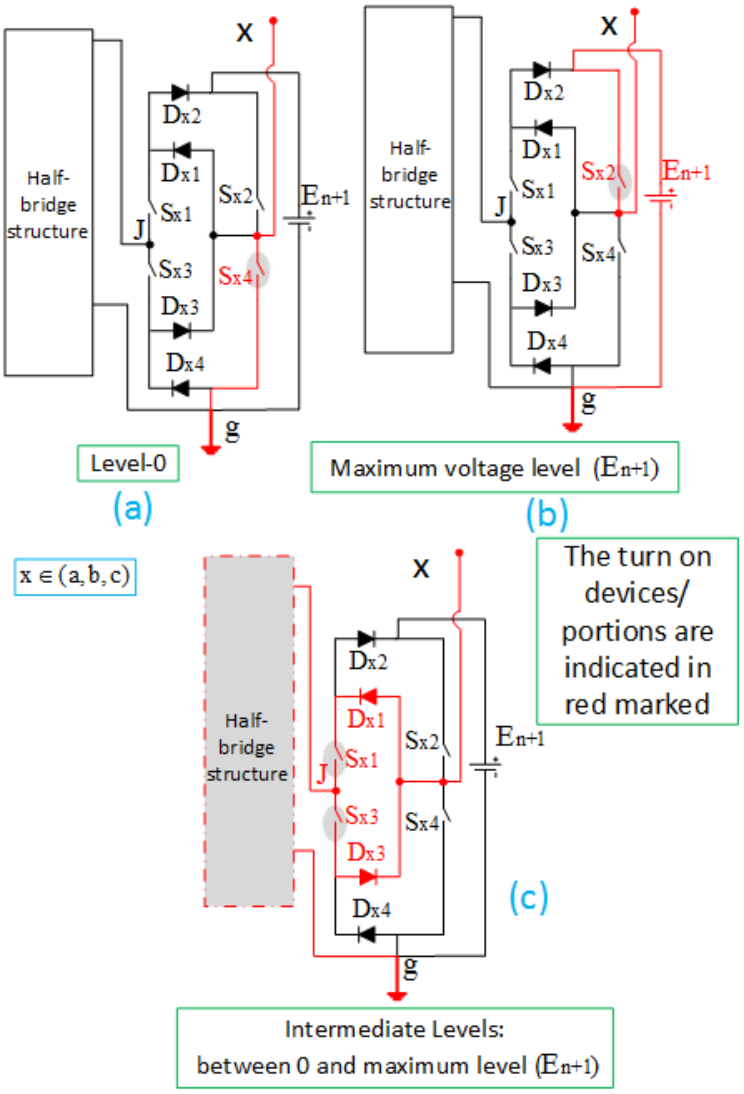


Figure 4. 2 Generalized overview of the output voltage level generation for: (a) Zero voltage level, (b) Maximum voltage level, (c) Intermediate voltage levels between zero and maximum level.

The switches S_{x1} and S_{x3} are always turned on at a time while operating with the half-bridge structure to generate the intermediate voltage levels for any particular phase arm. Table 4.1 and Table 4. 2 show the generalized switching mode of the non-isolated and isolated input supply-based half-bridge topologies shown in Fig. 4. 1a and Fig. 4. 2a, respectively.

Table 4. 1 Generalized switching states of the non-isolated dc-power supply-based proposed half-bridge MLI

Switches states										Pole voltage/ switching modes	Contributing inverter structure
G_{11}	G_{12}	G_{21}	G_{22}	…	G_{n1}	G_{n2}	S_{x1}, S_{x3}	S_{x2}	S_{x4}	V_{xg}	
**	**	**	**	**	**	**	0	0	1	0	Only modified full-bridges structure
**	**	**	**	**	**	**	0	1	1	E_{n+1}	
0	1	0	0	…	1	0	1	0	0	$\sum_{j=1}^{n} E_j$	Mutual contribution of half and modified full-bridge structures (V_{Jg})
0	1	0	0	…	0	1	1	0	0	$\sum_{j=1}^{n-1} E_j$	
…	…	…	…	…	…	…	…	…	…	…	
0	1	1	0	…	0	1	1	0	0	$\sum_{j=1}^{2} E_j$	
1	0	0	1	…	0	1	1	0	0	E_2	
0	1	0	1	…	0	1	1	0	0	E_1	

Table 4. 2 Generalized switching states of the isolated dc-power supply-based proposed half-bridge MLI

Switches states										Pole voltage/ switching modes	Contributing inverter structure
G_{11}	G_{12}	G_{21}	G_{22}	…	G_{n1}	G_{n2}	S_{x1}, S_{x3}	S_{x2}	S_{x4}	V_{xg}	
**	**	**	**	**	**	**	0	0	1	0	Only modified full-bridge structure
**	**	**	**	**	**	**	0	1	1	E_{n+1}	
1	0	1	0	…	1	0	1	0	0	$\sum_{j=1}^{n} E_j$	Mutual contribution of half and modified full-bridge structures (V_{Jg})
…	…	…	…	…	…	…	…	…	…	…	
1	0	1	0	…	0	1	1	0	0	$\sum_{j=1}^{2} E_j$	
0	1	1	0	…	0	1	1	0	0	E_2	
1	0	0	1	…	0	1	1	0	0	E_1	

In these tables, the switches G_{k1} and G_{k2} of the half-bridge modules are kept in “don not care” mode, as denoted by “**”, while generating maximum or zero voltage levels (Fig. 4. 2a and Fig. 4. 2b) as the two switches will have no impact on the generated voltage in these cases. The half-bridge structure contributes to the output voltage when S_{x1} and S_{x3} are turned on, as shown in Fig. 4. 2c.

The pole voltages, V_{xg} can be expressed by

$$V_{xg} = 0 + V_{Jg} + E_{n+1} \tag{4.1}$$

where V_{xg} ε (V_{ag}, V_{bg}, V_{cg})

The maximum amplitude of the pole voltage, $V_{xg,\,max}$ is

$$V_{xg,max} = E_{n+1} \tag{4.2}$$

The maximum number of levels, N_p in the pole voltage can be calculated from

$$N_p = V_{xg,max}/V_{dc} + 1 \tag{4.3}$$

where x ε (a, b, c)

The three phase line-line voltage can be obtained from

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} V_{ag} - V_{bg} \\ V_{bg} - V_{cg} \\ V_{cg} - V_{ag} \end{bmatrix} \tag{4.4}$$

The number of levels in the line voltages can be calculated from

$$N_{level} = 2N_p - 1 \tag{4.5}$$

On the other hand the phase voltage, V_{XN} as a function of the pole voltage, V_{xg} is given as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \tag{4.6}$$

The blocking voltage of the switches is an important parameter that identifies the total inverter semiconductor cost. The voltage rating of a semiconductor device is directly related to the value of the blocking voltage. Lower blocking voltage may reduce the switching losses significantly [17].

Table 4. 3 Different dc-power supply choosing methods and related parameters for non-isolated half-bridge based MLI

Proposed algorithm	Magnitude of dc-power supplies	$V_{xg,max} = E_{n+1}$	N_p	N_{level}	Total switches (N_{switch})	Total dc power supplies (N_{source})
Symmetric	$E_k = V_{dc}$; $E_{n+1} = (n+1)V_{dc}$ For k = 1, 2, 3, ..., n	$(n+1)\,V_{dc}$	n+2	2n+3	(2n+12)	(n+1)
Asymmetric	$E_1=E_3=\ldots=V_{dc}$ $E_2=E_4=\ldots=2V_{dc}$ $E_{n+1}=\sum_{k}^{n} E_k + E_1$ $=\begin{cases}\frac{(3n+2)}{2}V_{dc}; n = \text{even no}\\ \frac{(3n+1)}{2}V_{dc}; n = \text{odd no}\end{cases}$	$\begin{cases}\frac{(3n+2)}{2}\text{Vdc; n = even n}\\ \frac{(3n+1)}{2}\text{Vdc; n = odd n}\end{cases}$	$\begin{cases}\frac{(3n+4)}{2}\text{; even}\\ \frac{(3n+3)}{2}\text{; odd}\end{cases}$	$\begin{cases}(3n+3);\ \text{eve}\\ (3n+2);\ \text{odd}\end{cases}$		

Table 4. 4 Different dc-power supply choosing methods and related parameters for isolated Half-bridge based MLI

Proposed algorithm	Magnitude of dc-power supplies	$V_{xg,max} = E_{n+1}$	N_p	N_{level}	Total switches (N_{switch})	Total dc power supplies (N_{source})
Symmetric	$E_k = V_{dc}$; $E_{n+1} = (n+1)V_{dc}$ For k = 1, 2, 3, ..., n	$(n+1)\,V_{dc}$	n+2	2n+3	(2n+12)	(n+1)
Asymmetric -1	$E_1 = V_{dc}$; $E_k = 2V_{dc}$; $E_{n+1}=\sum_{k}^{n} E_k + 2E_1$ For k = 2, 3, ..., n	$2n\,V_{dc}$	2n+1	4n+1		
Asymmetric -2	$E_k = kV_{dc}$; $E_{n+1}=\sum_{k}^{n} E_k + E_1$ For k = 1, 2, 3, ..., n	$[\{n(n+1)\ /\ 2\}+1]\,V_{dc}$	$[n(n+1)\ /\ 2]+2$	n(n+1)+3		
Asymmetric -3	$E_k = 2^{(k-1)}\,V_{dc}$; $E_{n+1}=\sum_{k}^{n} E_k + E_1$ For k = 1, 2, 3, ..., n	$2^n\,V_{dc}$	$2^n + 1$	$(2^{n+1}+1)$		

Therefore, any reduction in the blocking voltage will not only reduce the semiconductors overall

cost but it will also improve the inverter efficiency. The voltage blocked by the switching devices of the proposed inverter is given by:

$$V_{Gk1} = V_{Gk2} = E_k; \quad V_{Sx1} = V_{Sx2} = V_{Sx3} = V_{Sx4} = E_{n+1} \tag{4.7}$$

Where the value of E_k and E_{n+1} can be obtained from Table 4.3 and 4.4.

In case of symmetric algorithm, the voltage rating or blocking voltage of the power electronic components in the half-bridge stage can be reduced by increasing the number of modules, but at the same time the blocking voltage of the power electronic components within the modified H-bridge stage increases.

If $V_{ll,(pk\text{-}pk)}$ and $V_{ll,rms}$ represent the peak-peak and RMS value in the desired line voltages (V_{ab}, V_{bc}, V_{ca}), then

$$V_{ll,(pk-pk)=N_{level}*V_{dc}} \tag{4.8}$$

$$V_{ll,rms} = V_{ll,(pk-pk)}/\sqrt{2} \tag{4.9}$$

Hence, $V_{dc} = V_{ll,(pk-pk)}/\sqrt{2} * N_{level}$ (4.10)

Equation (4.10) reveals that the magnitude of the input voltage supplies are inversely related with the number of levels that are increased with the increase of the half bridge modules number. However, for symmetric algorithm, the expression of the device blocking voltage in the modified H-bridge stage can be written as

$$E_{n+1} = V_{Jg} + E_1 = \sum_{k=1}^{n} E_k + V_{dc} = nV_{dc} + V_{dc} = (n+1)V_{dc} \tag{4.11}$$

Equation (4.11) indicates that the number of modules (n) in the half-bridge stage and the input voltage are controlling the value of E_{n+1}. Hence, it is essential to carefully choose the number of half-bridge modules in order to obtain an optimized E_{n+1} value. On the other hand, the device current rating depends on the load and since all modules are connected in series, hence device current rating is same for all the switches.

Table 4. 3 and Table 4. 4 list different input voltage combinations with related generalized parameters for the non-isolated and isolated half-bridge structure, respectively. According to (4.7), the symmetric method will show minimum blocking voltage on the switches, but the number of output voltage levels is less than that of asymmetric structures. On the other hand, the switching devices in asymmetric structures exhibit higher blocking voltage but it provides more voltage levels in the output voltage than the symmetric structure for any specific number of modules in the half-bridge stage. For example, for two modules (n=2) in the non-isolated dc-supply based half-bridge structure, three dc-power supplies and sixteen semiconductor switches are required for the symmetric (E_1=E_2=V_{dc}, E_3=3V_{dc}) and asymmetric (E_1= V_{dc}; E_2=2V_{dc}, E_3=4V_{dc})

structures as shown in Table 4. 3. Although the number of required components is the same for both structures, the switches in asymmetric structure exhibit more blocking voltage according to (4.7). On the other hand, seven levels will be shown in the line voltage when symmetric structure is implemented while the line voltage comprises nine levels for asymmetric configuration as shown in Table 4. 3. Though the inverter required components remain the same, but more switching action is required to generate nine levels than generating seven levels which leads to more switching loss. Hence though the number of voltage levels can be increased, asymmetric approach may increase switching losses.

4.3 Simulation method and experimental setup

In the proposed topology, staircase modulation is employed to achieve proper switching sequence (S_a, S_b, S_c) generations. The pole voltages, V_{xg} are considered as reference for switching signal generation to achieve three phase output voltages. The reference pole voltages ($V_{xg,ref}$) can be written as:

$$\left.\begin{aligned} V_{ag,ref} &= [(N_p-1)*V_{dc}/2]\{m_i*\cos 2\pi ft + [1 - m_i*\cos 6\pi ft/6]\} \\ V_{bg,ref} &= [(N_p-1)*V_{dc}/2]\{m_i*\cos(2\pi ft - 2\pi/3) + [1 - m_i*\cos 6\pi ft/6]\} \\ V_{cg,ref} &= [(N_p-1)*V_{dc}/2]\{m_i*\cos(2\pi ft + 2\pi/3) + [1 - m_i*\cos 6\pi ft/6]\} \end{aligned}\right\} \quad (4.12)$$

Where m_i is the modulation index; and f=line voltage frequency, t=instantaneous time.

It is worth to note that in the aforementioned reference pole voltage ($V_{xg,ref}$) equation a third harmonic component is added. The existence of the third harmonic component offers the inverter to perform with wide range of modulation index (m_i) and which may more than more than one ($m_i > 1$).

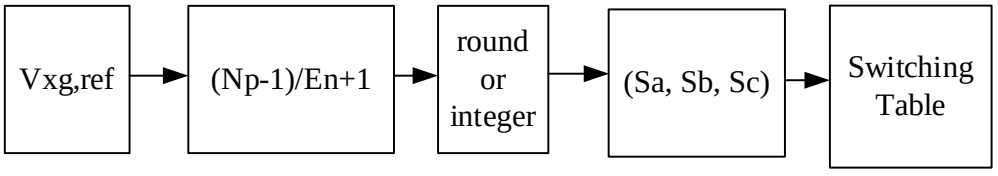


Figure 4. 3 Generalized modulation technique for switching sequence generation

Then the switching states (S_x) can be obtained by the following equation:

$$\left.\begin{aligned} S_a &= round[(N_p-1)*V_{ag,ref}/E_{n+1}] \\ S_b &= round[(N_p-1)*V_{bg,ref}/E_{n+1}] \\ S_c &= round[(N_p-1)*V_{cg,ref}/E_{n+1}] \end{aligned}\right\} \text{ Or } \left.\begin{aligned} S_a &= int\,[(N_p-1)*V_{ag,ref}/E_{n+1}] \\ S_b &= int\,[(N_p-1)*V_{bg,ref}/E_{n+1}] \\ S_c &= int\,[(N_p-1)*V_{cg,ref}/E_{n+1}] \end{aligned}\right\} \quad (4.13)$$

The modulation technique can be easily expressed by the block diagram shown in Fig. 4. 3.

The switching states (S_x) can be expressed by the space vector (V). The magnitude of the d and q voltage components (V_d, V_q) are responsible to locate the switching in the d-q space diagram and

can be represented by

$$V = V_q - jV_d \tag{4.14}$$

$$\left.\begin{aligned} V_d &= \frac{E_{n+1}}{\sqrt{3}(N_p-1)}(S_c - S_b) \\ V_q &= \frac{E_{n+1}}{3(N_p-1)}(2S_a - S_b - S_c) \end{aligned}\right\} \tag{4.15}$$

The number of switching states, S depends on the levels in the pole voltages, N_p and can be calculated as:

$$S = 6(N_p - 1) \tag{4.16}$$

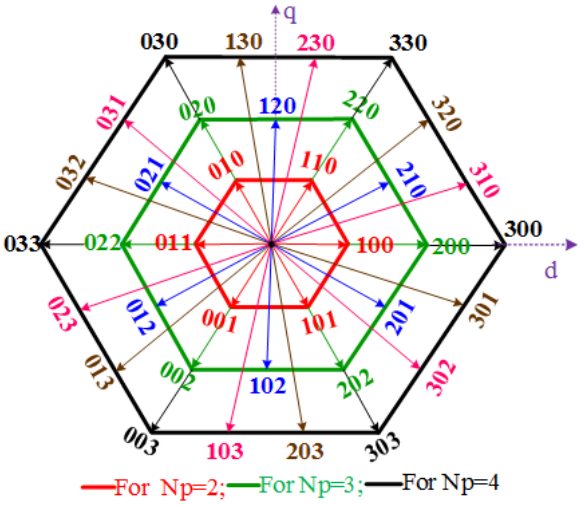


Figure 4. 4. The presentation of switching states in the space vector diagram

The generalized switching states can also be represented by the space vector diagram as shown in Fig. 4. 4. The diagonal points of the smallest hexagon represents the six switching states [(S_a, S_b, S_c) = (011, 010, 110, 100, 101, 001)] for achieving two levels in the pole voltage, N_p=2. However, the next hexagon represents twelve switching states, [(S_A, S_B, S_C) = (022, 021, 020, 120, 220, 210, 200, 201, 202, 102, 002, 012)] for achieving three levels in the output pole voltage, N_p=3. Similarly the next hexagons can be developed for getting any specific number of pole voltage levels, N_p= 4, 5……etc., according to (4.16).

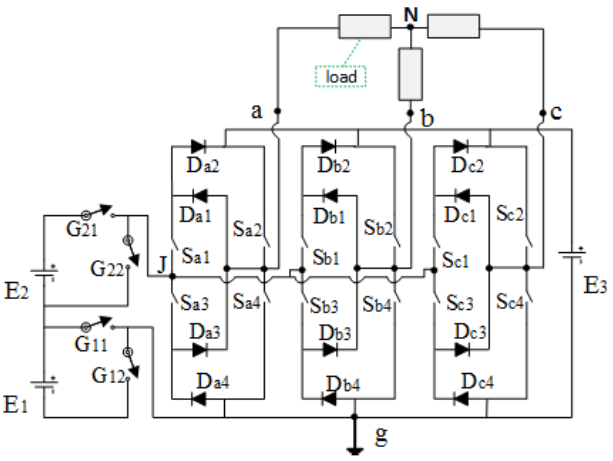


Figure 4. 5 Schematic of the implemented topology

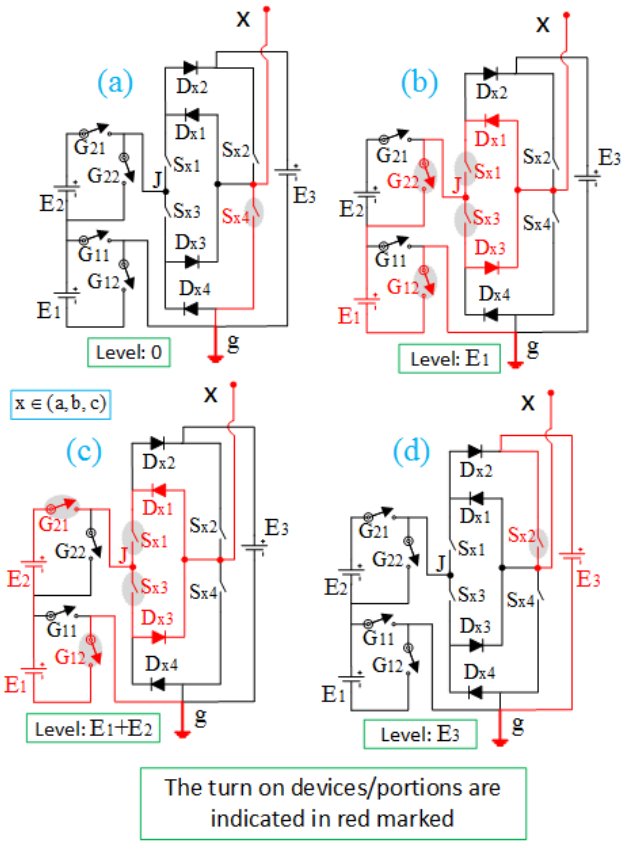


Figure 4. 6 Different switching mode to generate all the possible levels in the pole voltage: (a) Voltage level: zero; (b) Voltage level: E_1; (c) Voltage level: (E_1+E_2); (d) Voltage level: E_3

For simplicity, the symmetric input algorithm with two modules in the half-bridge structure (non-isolated source) is chosen for implantation as shown in Fig. 4. 5. As shown in Table 4.1, there are four switching modes for the chosen two modules (n=2) in the half-bridge structure. Hence four switching modes or switching combinations are required in achieving four levels (N_p=4), *[0, E_1, (E_1+E_2), E_3]* in the output pole voltages (V_{xg}). Since the symmetric input algorithm is considered, the input voltage sources can be expressed as E_1=E_2=V_{dc}; E_3=3V_{dc}. Fig. 4. 6 shows the switching

modes of the topology in Fig. 4. 5 where the turned on switches are marked by red color. The maximum and zero voltage level generation are explained in detail in Fig. 4.2. Fig.4. 6b and Fig.4.6c show the intermediate level generation for the considered inverter structure in which it could be seen that G_{12} is always turned on while G_{11} always turned off during two intermediate levels, [E_1, (E_1+E_2)] generation. According to Fig. 4.2, the switches of the half-bridge structure can stay at any valid switching mode during maximum and zero level generation. Hence during maximum and zero voltage generation, (G_{12}, G_{21}) can be kept in 0 or 1 mode which can lead to a reduction in the switching frequency of the two switches.

Table 4.5 Switching states sequence for a complete one cycle of three phase line voltage generation

Switching states			Period T[s]	G_{11}	G_{12}	G_{21}	G_{22}	S_{a1}, S_{a3}	S_{a2}	S_{a4}	S_{b1}, S_{b3}	S_{b2}	S_{b4}	S_{c1}, S_{c3}	S_{c2}	S_{c4}	V_{AB}	V_{BC}	V_{CA}
S_a	S_b	S_c																	
300			T_1	**0**	**1**	**0**	**1**	0	1	0	0	0	1	0	0	1	3	0	-3
				1	0	0	1												
				0	1	1	0												
310			T_2	0	1	0	1	0	1	0	1	0	0	0	0	1	2	1	-3
320			T_3	0	1	1	0	0	1	0	1	0	0	0	0	1	1	2	-3
330			T_4	0	1	0	1	0	1	0	0	1	0	0	0	1	0	3	-3
				1	0	0	1												
				0	**1**	**1**	**0**												
230			T_5	0	1	1	0	1	0	0	0	1	0	0	0	1	-1	3	-2
130			T_6	0	1	0	1	1	0	0	0	1	0	0	0	1	-2	3	-1
030			T_7	**0**	**1**	**0**	**1**	0	0	1	0	1	0	0	0	1	-3	3	0
				1	0	0	1												
				0	1	1	0												
031			T_8	0	1	0	1	0	0	1	0	1	0	1	0	0	-3	2	1
032			T_9	0	1	1	0	0	0	1	0	1	0	1	0	0	-3	1	2
033			T_{10}	0	1	0	1	0	0	1	0	1	0	0	1	0	-3	0	3
				1	0	0	1												
				0	**1**	**1**	**0**												
023			T_{11}	0	1	1	0	0	0	1	1	0	0	0	1	0	-2	-1	3
013			T_{12}	0	1	0	1	0	0	1	1	0	0	0	1	0	-1	-2	3
003			T_{13}	**0**	**1**	**0**	**1**	0	0	1	0	0	1	0	1	0	0	-3	3
				1	0	0	1												
				0	1	1	0												
103			T_{14}	0	1	0	1	1	0	0	0	0	1	0	1	0	1	-3	2
203			T_{15}	0	1	1	0	1	0	0	0	0	1	0	1	0	2	-3	1
303			T_{16}	0	1	0	1	0	1	0	0	0	1	0	1	0	3	-3	0
				1	0	0	1												
				0	**1**	**1**	**0**												
302			T_{17}	0	1	1	0	0	1	0	0	0	1	1	0	0	3	-2	-1
301			T_{18}	0	1	0	1	0	1	0	0	0	1	1	0	0	3	-1	-2

Since the maximum achievable number of pole voltage is (N_p=4), hence it is possible to operate the inverter at modulation index, m_i=1.15 according to equation (4.12). However, switching sequence will be updated if the modulation index is changed. The modulation index (m_i) can be expressed as three band limit according to the switching sequences: (a) $m_i \geq 1.01$; (b) $0.8 \leq m_i < 1.01$; (c) $M_i < 0.8$.

For $m_i \geq 1.01$, 18 switching states (300, 310, 320, 330, 230, 130, 030, 031, 032, 033, 023, 013, 003, 103, 203, 303, 302, 301) are available in the switching sequence. All the switching states are located on the edges of the black marked hexagon in Fig. 4. 4 and in Fig. 4.7a. The aforementioned 18-switching states (S_a, S_b, S_c) are listed in Table 4. 5 for a complete cycle of the three phase output line voltages. The time period T_1=T_2=T_3=…T_s of any switching state S_A–S_C can be expressed in generalized form by (4.17).

$$T_1 = T_2 = T_3 = \cdots = T_S = \frac{1/f_{line}}{S} = \frac{1/50Hz}{S} = 0.02/6(N_p - 1)\ second \quad (4.17)$$

Where f_{line} is the switching frequency of the line voltage.

Therefore, according to (4.17), the time period of each switching state in Table 4. 5 can be written as

$$T_1 = T_2 = T_3 = \cdots = T_{18} = 0.02/S = 0.02/18\ \ second \quad (4.18)$$

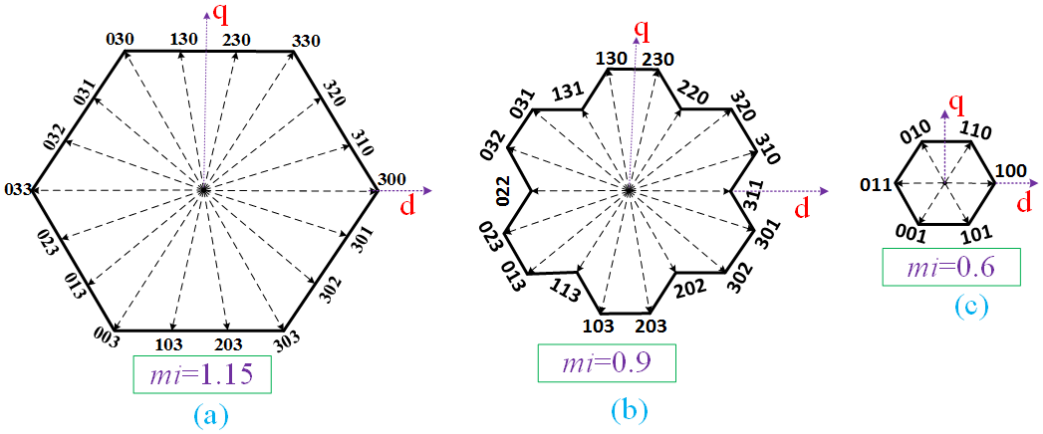


Figure 4. 7. Generalized switching states presentation by hexagon in d-q complex plane

This means that the switching logic combination of all switches will be changed every 1.11 ms to achieve the next switching state. The switching modes are chosen such that the switching frequency of the half-bridge structure is kept minimum. To achieve this goal, the red marked switching modes of G_{11}, G_{12}, G_{21}, and G_{22} are selected for switching signal generation during time period T_1, T_4, T_7, T_{11}, and T_{13}, as shown in Table 4. 5.

In case of $0.8 \leq m_i < 1.01$, the switching sequence also contains 18-switching states (311, 310, 320, 220, 230, 130, 131, 031, 032, 022, 023, 013, 113, 103, 203, 202, 302, 301) which are shown in Fig.

4. 7b. The inverter operates with six switching states (100, 110, 010, 011, 001, 101) if modulation index m_i < 0.8 is chosen as shown by the space diagram in Fig. 4.7c.

MATLAB/Simulink software is used to simulate the proposed MLI topology as shown in Fig. 4. 5. Furthermore, a laboratory prototype is developed to verify the simulation results. Digital signal processor (DSP), TMS320F2812 is used to achieve the real time switching signals. The insulated gate bipolar transistor (IGBT), IRG4BC40W, 600V/20 A and the diode, RHRP1540, 400V/15 A are used to build the prototype model for the modified Full-bridge modules. Four IGBTs, HGTG20N60B3D, 600V/40 A are used to implement the half-bridge structure. On the other hand, each modified Full-bridge module requires four diodes and four IGBTs. Fundamental frequency staircase modulation is applied as a control strategy. Modulation index m_i=1.15 is chosen to analyze the performance of the implemented topology. The calculated time period of each switching state for the 16-IGBT switches is equal to 1.11 ms.

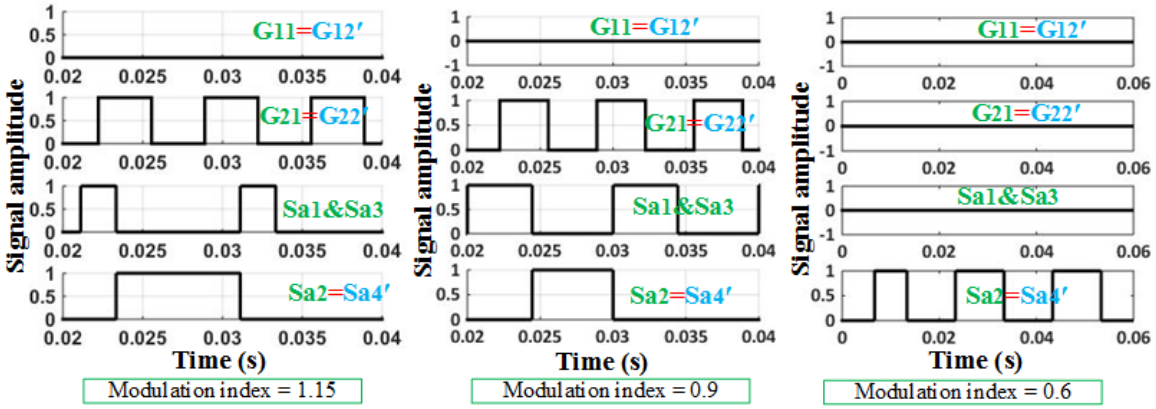


Figure 4. 8 The switching signals for a complete cycle of the switches (G_{11}, G_{22}, S_{a1}, S_{a2}, S_{a3})

According to the number of pulses per cycle, the operating switching frequencies, f_{swt} of all switches are not equal. Each pair of S_{x2} and S_{x4} in the modified H-bride modules are operated at switching frequency $f_{swt} = f_{line}$=50 Hz while the switching frequency for each pair of S_{x1} and S_{x3} is $f_{swt} = 2f_{line}$ = 100 Hz. For switches of the second (G_{21}, G_{22}) and first (G_{11}, G_{12}) half-bridge modules, the switching frequency is $f_{swt} = 3f_{line}$ = 150 Hz and f_{swt} = 0 Hz, respectively. Figs. 8a, 8b and 8c show the simulated switches gate signals of the cascaded half-bridge module and the modified Full-bridge module for phase-a for modulation index, m_i= 1.15, 0.9, and 0.6; respectively. The gate signal waveforms of G_{11}, G_{21}, S_{a1}, S_{a3}, and S_{a2} are shown in Fig. 4. 8. As can be seen, each pair of the switches (G_{11}, G_{12}), (G_{21}, G_{22}) and (S_{a2}, S_{a4}) operates in a toggle mode with each other.

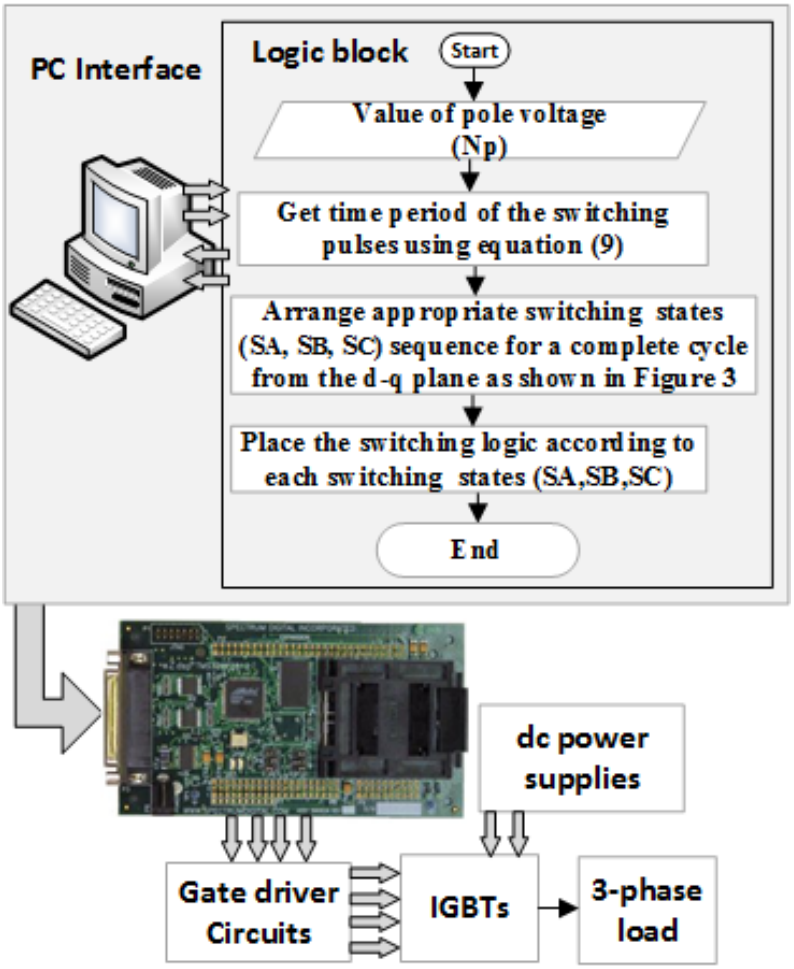


Figure 4. 9 The functional block diagram of the experimental setup

Fig. 4. 9 shows the functional block diagram of the developed hardware setup. The logic block is responsible to arrange the switching states sequence and manipulate the switching logics according to the switching states shown in Table 4. 5. The logic block in the PC transfers all the switching signals to the DSP, TMS320F2812 to generate the real time switching signals. As the DSP output signals are non-isolated of low amplitude, they cannot be directly connected to the IGBTs gate terminals.

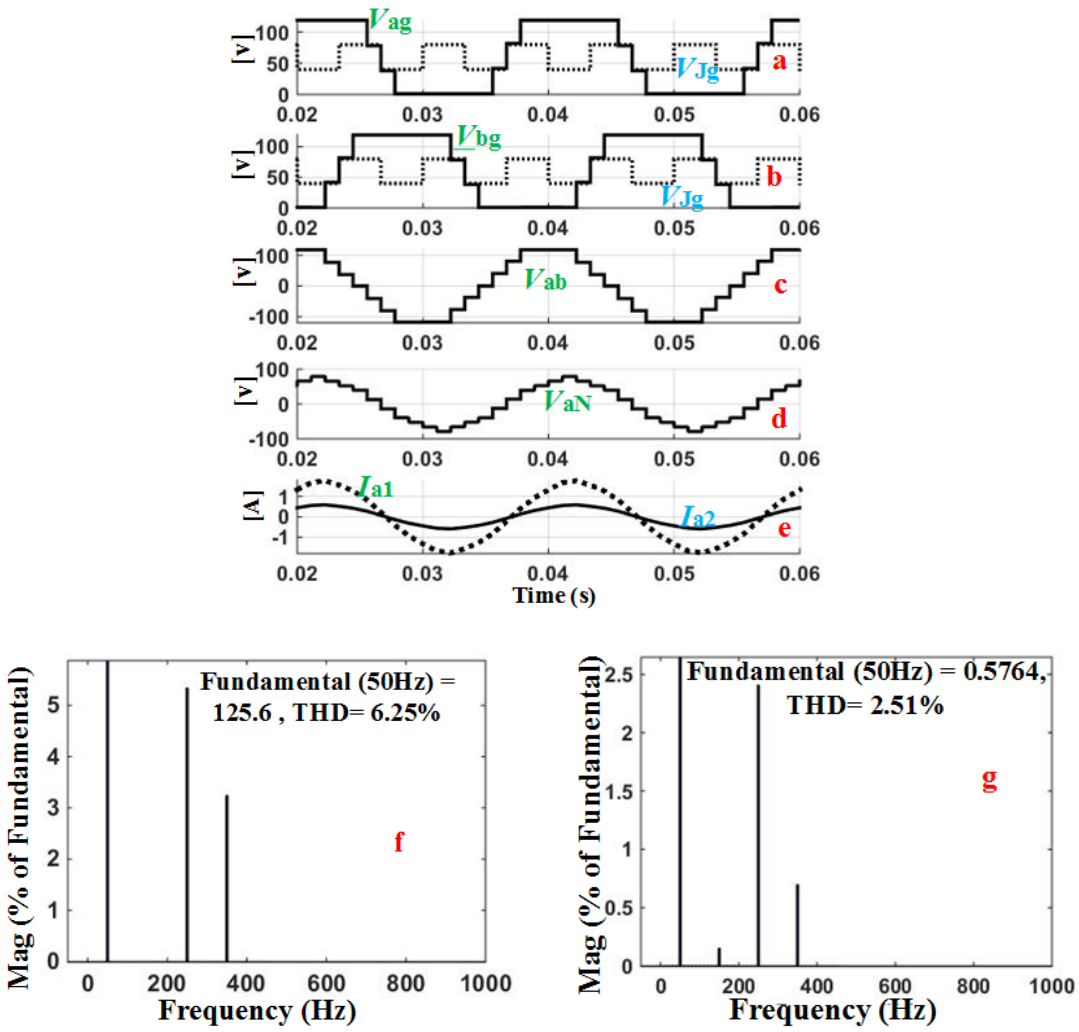


Figure 4. 10 Simulation results:(a) Intermediate voltage, V_{Jg} and pole voltage, V_{ag} , (b) Intermediate voltage, V_{Jg} and pole voltage, V_{Bg}, (c) Line voltage, V_{AB}, which is generated by utilizing, V_{ag} and V_{bg}, (d) Phase voltage, V_{aN}, (e) The line current, I_{a1} and I_{a2} for (R=40 Ω and L=15 mH in each phase) and (R=120 Ω and L=90 mH in each phase), respectively, (f) THD of the line voltage, (g) THD of the line current

Hence the DSP output signals are passed through different gate drive circuits for isolating the common ground of the gate signals and increasing its amplitude.

The input dc-power supplies are adjusted such as $E_1=E_2=V_{dc}=40$ V and $E_3=3V_{dc}=120$V. Three-phase R-L load is considered in the simulation and experimental results. Two different load values (R=40 Ω and L=15 mH in each phase), (R=120 Ω and L=90 mH in each phase) are investigated to observe the line current for different load condition.

4.4 Results and discussions

Fig. 4. 10 shows the simulation results for m_i=1.15 obtained using MATLAB/Simulink software. Fig. 4. 10a and 10b show the pole voltages, V_{ag}, V_{bg} and V_{Jg} for phase arms-a and b and

the junction point J, respectively. As shown in the Figure, the pole voltages comprises four levels [(0, V_{dc}, $2V_{dc}$, $3V_{dc}$)= (0, 40 V, 80 V, 120 V)] while V_{Jg} has two levels [(V_{dc}, $2V_{dc}$)= 40 V and 80 V]. The V_{Jg} plot verifies that the half-bridge structure has no contribution on the zero and maximum levels of the pole voltages, V_{xg}. The line voltage, V_{ab} is provided in Fig. 4. 10c which shows seven different voltage levels [(0, ± V_{dc}, *±2* V_{dc}, *±3* V_{dc}) = (0, ±40 V, ±80 V, ±120 V)] in the waveform. The phase voltage, V_{aN} for phase arm-a contains ten levels (±V_{dc}/3, ±3V_{dc}/3, ±4V_{dc}/3, ±5V_{dc}/3, ±6V_{dc}/3)= (*±13.33V, ±40V, ±53.33V, ±66.67V, ±80V*)] is shown in Fig. 4. 10d. The line current, I_{a1} and I_{a2} are depicted in Fig. 4. 10e for load values (R=40 Ω and L=15 mH in each phase) and (R=120 Ω and L=90 mH in each phase), respectively.

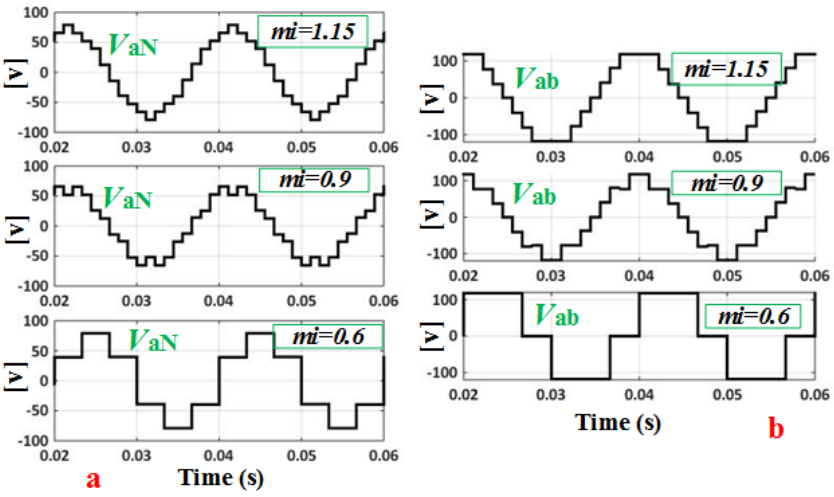


Figure 4. 11 Simulation results: (a) Phase voltage (V_{ag}) for different modulation index, (b) Line voltage (V_{ab}) for different modulation index

The total harmonic distortion (THD) in the generated voltage or current waveforms can be calculated as:

$$THD(\%) = \frac{100\%}{H_1}\sqrt{\sum_{k=2}^{\infty} H_k^2} \qquad (4.19)$$

where H_1 is the fundamental component of line current or voltage and k is harmonic order.

Fig. 4. 10(f) and (g) show the THD of the unfiltered line voltage and line current, respectively. To satisfy IEEE 1547-2003 standard, the THD value should be less than 5 % [36]. Although the current THD fulfils the IEEE standard, the voltage THD is slightly above 5% in the implemented 7-level topology. The amount of THD can be reduced by increasing the number of levels in the output voltage which could be achieved through adopting asymmetric input voltage supply or adding more half bridge modules.

Fig. 4.11 is provided to show the effect of change of the modulation index in the output voltage

wave forms. It is found the line voltages contain seven levels [(0, ±V_{dc}, ±2V_{dc}, ±3V_{dc}) = (0, 40 V, ±80 V, ±120 V)] for m_i= 1.15 and 0.9. But a significant change happens in the phase voltage, V_{xN}. Fig. 4.11a Shows ten levels (±V_{dc}/3, ±3V_{dc}/3, ±4V_{dc}/3, ±5V_{dc}/3, ±6V_{dc}/3)= (±13.33V, ±40V, ±53.33V, ±66.67V, ±80V)] and eight levels (±V_{dc}/3, ±2V_{dc}/3, ±4V_{dc}/3, ±5V_{dc}/3)= (±13.33, 26.67V, ±53.33V, ±66.67V) are found in the phase voltage V_{aN} for m_i=1.15 and 0.9; respectively. Again, the proposed inverter generates three levels (0, ±120V) in the line voltages and four levels [(±40V, ±80V)] in the phase voltages.

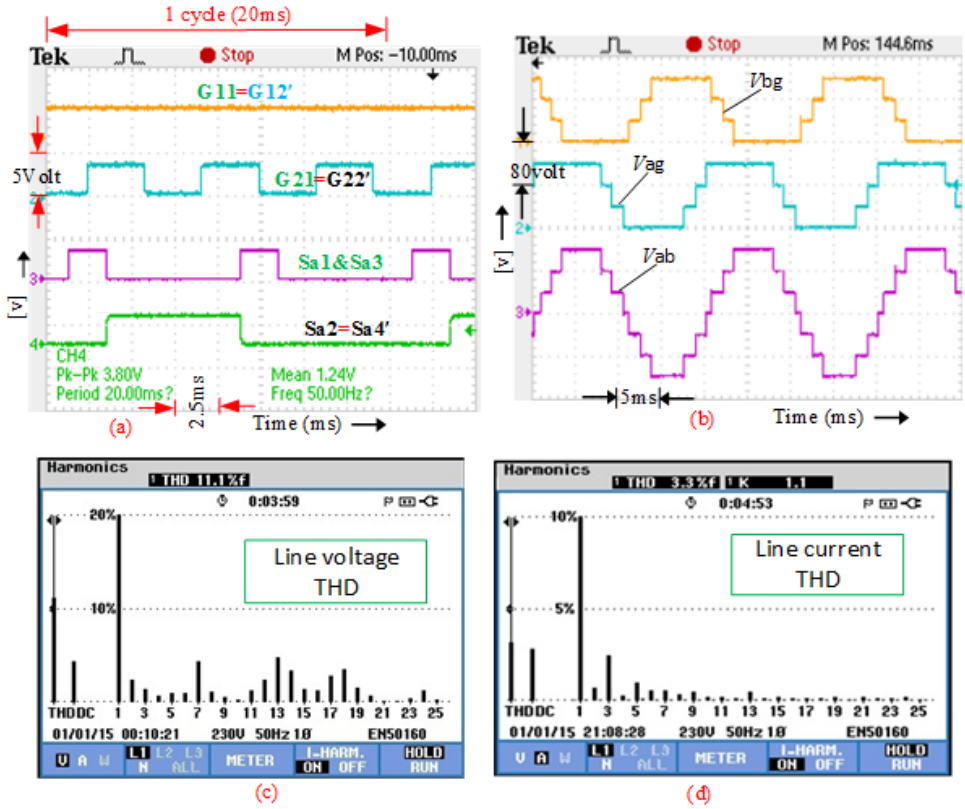


Figure 4. 12 Experimental results: (a) Gate signals of DSP output, (b) Pole voltage, V_{ag} and V_{bg} [80 V/div, 5 ms/div], and line voltage, V_{ab} [80 V/div, 5 ms/div], (c) THD of line voltage, (d) THD of line current

Fig. 4. 12 shows the experimental verification of the simulated three-phase MLI while each phase contains inductive load (R=120 Ω and L=90 mH). The figure shows the good agreement between simulation and practical results in terms of the switching gate signals in Fig. 4. 12(a), phase to ground voltages V_{ag}, V_{bg} and output line voltage V_{ab} in Fig. 4. 12(b). The experimental THD results shown in Figs. 12 (c) and (d) reveal a slight difference than the simulated values. The development of a new control algorithm for the proposed topology would be a probable solution in order to minimize the THD value. It is worth mentioning that the proposed half-bridge comprising non-isolated or isolated input dc-power supply based half-bridge structure can be extended to provide

any desired number of levels in the output voltage waveform.

In this proposed topology, IGBT with anti-parallel diode (HGTG20N60B3D) are utilized for the half-bridge structure and IGBT (IRG4BC40W) along with the diode (RHRP1540) are chosen for the modified H-bridge structure. The losses of a power electronic converter are mainly related with the semiconductor switching and conduction losses. The conduction losses take place as a result of semiconductor on-state resistance and forward device voltage drop, while the switching loss is associated with the device turn on-off frequency. The aforementioned device parameters and some other necessary parameters are provided in device datasheet by the manufacturer.

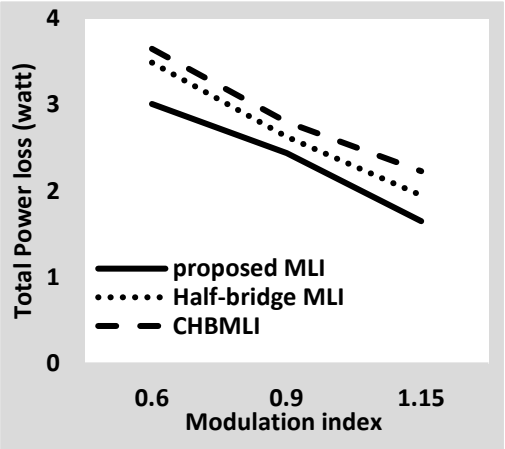


Figure 4. 13 Total loss for different modulation index [57, 71]

Although the parameters of semiconductor devices may vary for different MLI design and topologies, in sake of comparison, same parameters are used to calculate the losses of some MLI topologies published in the literatures to compare it with the losses of the MLI topology proposed in this chapter. Assumed parameters are: V_T = 1.8 V; R_T = 0.10; V_D = 1.2V; R_D = 0.10; β = 1 and t_{on}= t_{off} =1µs. By utilizing the equations (3.4)-(3.9), conduction, switching and total losses can be calculated. The comparison is performed among the conventional seven level three phase cascaded half bridge proposed in [22, 23] and cascaded H-bridge topologies (CHB) proposed in [37, 38]. Symmetric algorithm with load (R=120 Ω and L=90 mH in each phase) and each module input dc-supply voltage is 40 volt is considered. Fig. 4. 13 shows the total losses (P_{loss}) for different modulation index which reveals that the proposed topology in this chapter exhibits less power losses than the conventional three phase cascaded half bridge and CHBMLI.

4.5 Comparison with other MLI topologies

The main goal of the proposed 3-phase hybrid MLI topology in this chapter is to maximize the number of levels in the output voltage while minimizing the number of power electronic

components and input dc power supplies which will reduce the inverter cost, physical size and complexity of gate drive circuit. In order to highlight the superiority of the proposed topology over existing MLI topologies, a comprehensive comparison including the required number of semiconductor switches, gate driver circuits, diodes, input dc-power supplies and the generated voltage levels per switch of the proposed three-phase topology in this chapter and other three-phase symmetric half-bridge and full-bridge topologies published in the literatures is given in Table 4. 6. The voltage levels generated per switch (levels to switch ratio) is considered as an important parameter that reflects the contribution of each switch in producing the output voltage. As shown in Table 4. 6, the proposed topology exhibits the highest level to switch ratio.

Table 4. 6 Comparison of the implemented 7-level topology over other inverter topologies

	Proposed 3-phase half-bridge topology	DC linked three phase Half-bridge inverter [7]	Symmetrical Hybrid MLI [9]	3-Phase Cascaded MLI using Power Cells [10]	Half-bridge MLI topology proposed in Chapter-3	H-bridge cascade inverter [17]
No of levels in line voltage (N_{level})	7	13	9	9	7	7
No of switching devices for 3-phase	16	48	24	24	30	36
No of Diodes	16	48	24	24	30	36
Line voltage levels/ switch ratio	0.44	0.27	0.375	0.375	0.233	0.20
No of dc-power supplies or capacitor	3	18	6	12	3	9

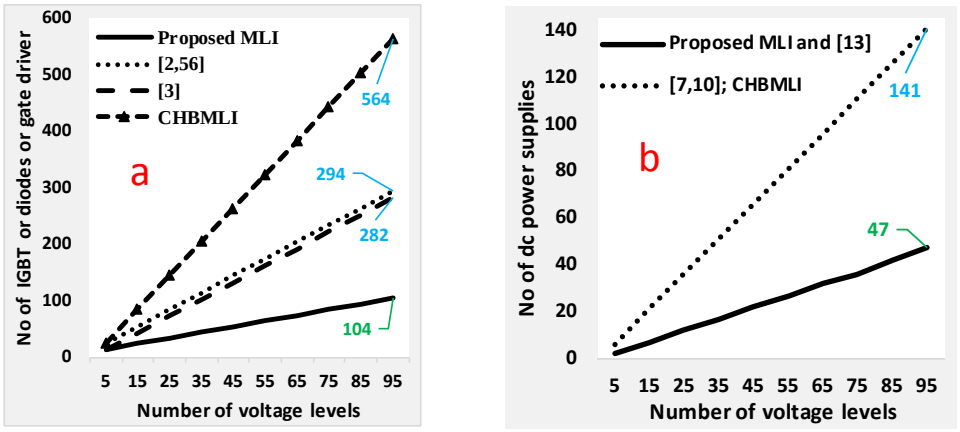


Figure 4. 14 Comparison study for the symmetric method in the half-bridge stage: (a) Number of semiconductor devices (IGBT or diode or gate drive circuit) versus number of levels in the line voltage (V_{level}), (b) Number of dc-power supplies versus number of levels in the line voltage (V_{level})

Figs. 14a and 14b show a generalized comparison for the number of power electronic components and input dc power supplies required by the proposed MLI topology in this chapter and some

conventional half-bridge topologies in the literatures. As shown in Fig. 4. 14, the proposed topology requires the least number of components for any desired number of levels in the output voltage. To generate 95 levels in the line voltages, Fig. 4. 14 shows about 65% reduction in the required number of power electronic components and number of dc-power supplies when the proposed topology is compared with other topologies.

4.6 Summary

This chapter presents a novel topology for a three phase half-bridge multilevel inverter that could be a better cost effective option than the existing conventional cascaded modular MLI inverter topologies as it comprises a reduced number of power switches, dc sources which significantly reduces the inverter cost, size and complexity. Results show that the number of power switches and dc-power supplies can be reduced by about 65% when the proposed topology is compared with other conventional half-bridge topologies. The proposed inverter is easy to implement and extend to generate any desired number of levels in the output voltage waveform. The THD of the output voltage waveform can be reduced by either increasing the number of half-bridge modules or by adopting asymmetric dc voltages among the half-bridge modules. The proposed topology can be facilitated for renewable energy applications by employing a common high-frequency magnetic-link. It is expected that the proposed new inverter topology will have great potential for renewable generation systems and smart grid applications.

Chapter Five: A New Cascaded Multilevel Inverter Topology with Galvanic Isolation

5.1 Introduction

This chapter presents a new compact three-phase cascaded multilevel inverter (CMLI) topology with reduced device count and high frequency magnetic link. While the device count reduction technique in chapter 4 is described for cascaded half-bridge inverter, this chapter introduces a generalized technique for the existing three phase cascaded MLI. Besides, this proposed topology overcomes the predominant limitation of separate dc voltage supplies, which CMLI always require. The high frequency magnetic link also provides a galvanic isolation between the input and output sides of the inverter, which is essential for various grid-connected applications. The proposed topology utilizes an asymmetric inverter configuration that consists of cascaded H-bridge cells and a conventional three-phase two-level inverter. A toroidal core is employed for the high frequency magnetic link to ensure compact size and high-power density. Compared with counterpart CMLI topologies available in the literatures, the proposed inverter has the advantage of utilizing the least number of power electronic components without compromising the overall performance, particularly when a high number of output voltage levels is required. The feasibility of the proposed inverter is confirmed through extensive simulation and experimentally validated studies.

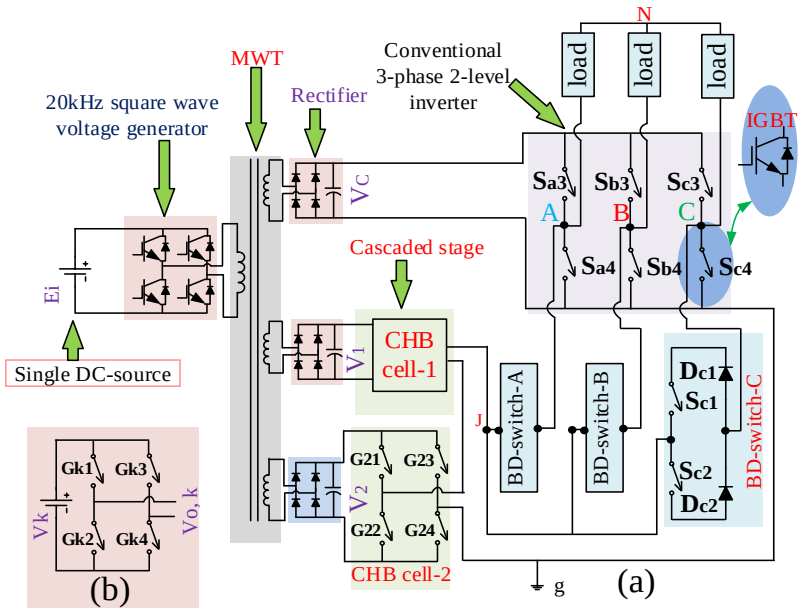


Figure 5. 1 Proposed cascaded multilevel inverter, (a) Proposed inverter when H-bridges are considered as cascaded cells, (b) A basic H-bridge

5.2 Proposed Cascaded Multilevel Inverter

The proposed CMLI consists of HFML, full-bridge rectifiers along with compact cascaded MLI as

shown in Fig. 5.1(a). The HFML comprises a single dc-source connected to a high frequency (20 kHz) square wave voltage generator that energizes the primary winding of a toroidal multi-winding transformer (MWT). The multiple windings on the secondary side of the MWT provide the isolated dc voltages required to create various levels in the output voltage. As can be seen from Fig. 5.1(a), the MLI has two main stages: cascaded stage and conventional three-phase, two-level inverter stage. The cascaded stage consists of two H-bridge (CHB) cells. While the three-phase two-level inverter is implemented using a conventional well-known structure[72] , the cascaded stage can be any cascaded inverter topology proposed in the literature. The voltages generated by the cascaded stage are transferred to the output terminals, A, B, C through Bi-directional (BD) switches. More cascaded cells can be added as required to increase the number of levels in the output voltage waveforms.

The input voltages to the H-bridge celles can be adjusted by controlling the MWT turns ratio. If '*n*' number of H-bridge cells are considered in the cascaded stage, then the equal magnitudes of the CHB input voltages can be expressed by

$$V_1=v;\ V_2=v;\ \ldots\ldots;\ V_n=v \tag{5.1}$$

Binary or trinary related input dc-supplies to the H-bridge cells can also be adopted, which is expressed by:

$$V_1=v;\ V_2=2^1v;\ \ldots\ldots;\ V_n=2^{n-1}v \tag{5.2}$$

$$V_1=v;\ V_2=3^1v;\ \ldots\ldots;\ V_n=3^{n-1}v \tag{5.3}$$

The conventional three-phase, two-level inverter is fed by a dc-supply of a magnitude of *Vc* that should be higher than the summation of all input dc voltages of the CHB cells. Hence V_C can be calculated from,

$$V_C = \sum_0^n V_x + V_1 = (V_1 + V_2 + \cdots + V_n) + v \tag{5.4}$$

A key feature of the proposed topology is that it allows for replacing the cascaded stage in Fig. 5. 1(a) by any existing cascaded MLI topology for developing a new three-phase cascaded MLI without tripling the number of device count required for MLI single-phase structure.

The conventional three-phase, two-level inverter has three-phase legs. Each leg comprises two switches, (S_{a3}, S_{a4}), (S_{b3}, S_{b4}), (S_{c3}, S_{c4}) operating in a toggle mode to generate two voltage levels (V_C and zero) in the pole voltages, V_{Ag}, V_{Bg}, V_{Cg}. Similar switching logic is applied for the three legs with a 120^0 phase shift.

The output points, *A, B, C* of each phase leg are connected to BD-switches as shown in Fig. 5. 1(a). Each BD-switch consists of two Insulated Gate Bipolar Transistors (IGBT) and two diodes. All voltage levels between V_C and zero are produced in the pole voltages by the cascaded stage when

the BD-switches are turned on (BD-switch is considered to be 'on' when both of the IGBTs are switched on). Fig. 5. 1(b) shows an H-bridge cell which comprises four switches (G_{K1}, G_{K2}, G_{K3}, G_{K4}) and a dc-input supply, V_K. Each H-bridge cell is able to generate three voltage levels, 0, $\pm V_K$ in the output voltage, $V_{O,K}$.

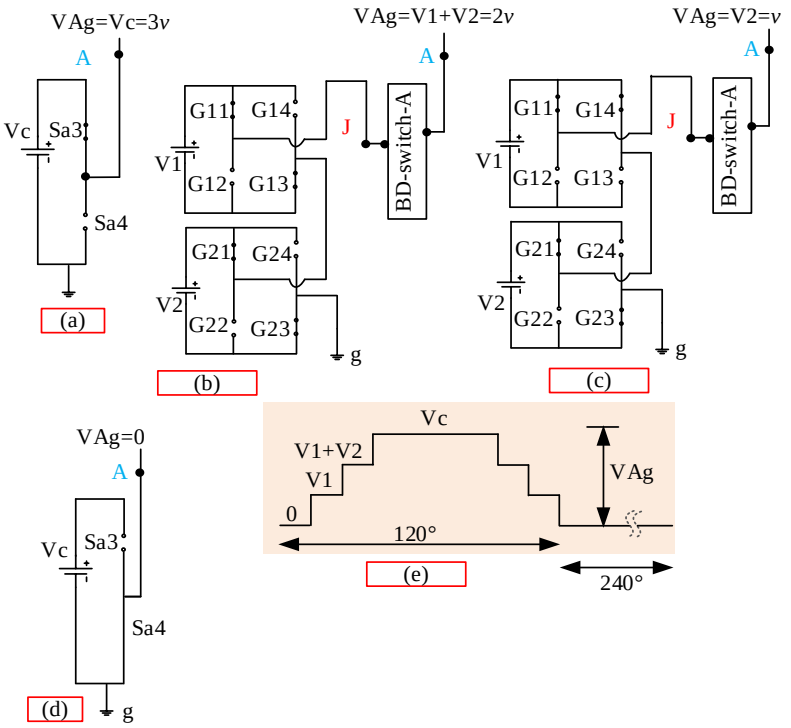


Figure 5. 2 Switching logics for generating four levels in the pole voltages: (a) level 3*v*; (b) Level 2*v*; (c) Level *v*; (d) Level 0; (e) Complete cycle of the pole voltage

It is worth noting that switches in the conventional three-phase, two-level inverter are completely turned off while generating voltage levels between V_C and zero. If same input voltages to the H-bridge cells are considered, then according to (5.1) and (5.4) the input voltages to the H-bridge cells and the conventional three-phase, two-level inverter can be expressed by,

$$V_1=V_2=v,\ V_C=3v \tag{5.5}$$

The switching logics for generating different levels as shown in Fig. 5. 2 reveal that the cascaded stage has no contribution in generating the V_C and 0-levels in the pole voltage V_{Ag} (Figs. 2(a), (d)). On the other hand, levels '2*v*' and '*v*' in the pole voltage are generated when the BD-switches in the conventional three-phase, two-level inverter are turned on and H-bridge cells contributes, as shown in Figs. 2(b) and (c), respectively. Both switches, *S*a3 and *S*a4 in phase leg-A of the conventional three-phase, two-level inverter are turned off while generating '2*v*' and '*v*' voltage levels. The switching logics are applied for 120^0 to create four voltage levels: 3*v*, 2*v*, *v*, 0 during ascending and descending modes of the pole voltage waveform, V_{Ag} as shown in Fig. 5. 2(e). The

cascaded stage utilizes the same switching logic to generate the three phase pole voltages V_{Ag}, V_{Bg} and V_{Cg} with a 120^0 phase shift between them.

The line voltages, V_{AB}, V_{BC}, V_{CA} are derived from the pole voltages as per the following equation,

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Ag} \\ V_{Bg} \\ V_{Cg} \end{bmatrix} \tag{5.6}$$

The proposed cascaded MLI topology is controlled by a low frequency staircase modulation technique [73, 74]. The designated switching states for generating four levels in the pole voltage waveform can be presented in a hexagonal form within the d-q plane as shown in Fig. 5. 3. If the number of levels in the pole voltages is N_p, then there will be $6(N_p\text{-}1)$ number of switching states [73, 74].

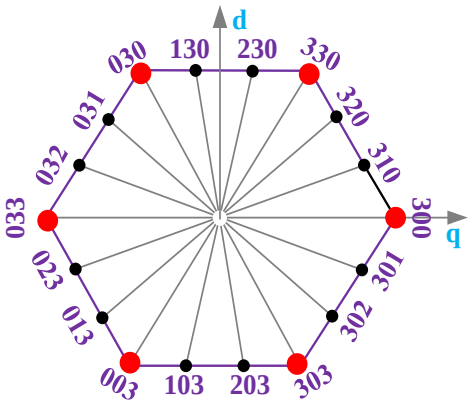
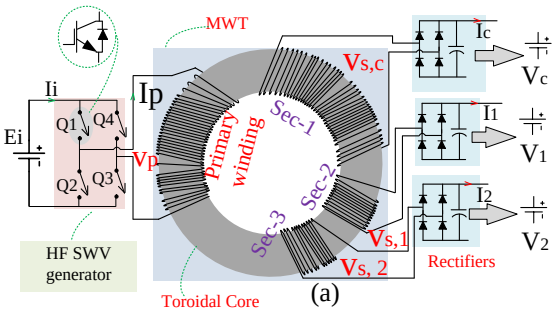


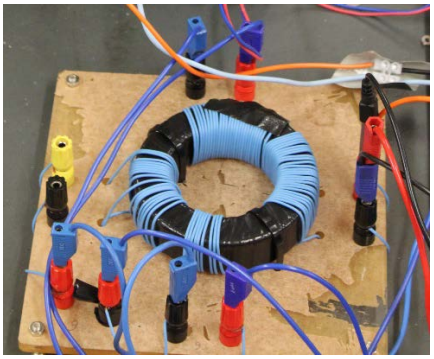
Figure 5. 3 Switching vectors in d-q complex plane of 18 switching states for generating four levels, N_p=4 in the pole voltage

Hence for generating 4 levels in the pole voltage, there will be 18 switching states as shown in Fig. 5. 3. Each of the switching state has three switching vectors, S_A, S_B, S_C for three phase voltage generation. The pole voltages are taken as reference to achieve the three switching vectors in each switching state at any instant of time [73]. In general, the switching angles for all switching states are equal and can be expressed as,

$$\text{Switching angle} = 360^0/6(N_P\text{-}1) \tag{5.7}$$

Thus the switching angle for each of the 18 switching states is 20^0 which means, a new switching state comes into operation every 20^0. In the switching sequence of the 18 switching states, the switching vectors 3, 2, 1, 0 are combined in an organised manner to generate three phase pole voltages.





(b)

Figure 5. 4 High frequency magnetic link: (a) multiple isolated dc supplies management from a single dc source, (b) Prototype of the laboratory MWT

5.3 HF-Magnetic link Design

The square wave voltage (SWV) generator is made of four insulated gate bipolar transistor, HGTG20N60B3D, 600V/40A, four IGBT gate driver circuits and a digital signal processor (DSP), TMS320F2812. The SWV generator converts the input 240-volt dc into a square wave high frequency voltage which is fed into the primary winding of the MWT as shown in Fig. 5. 4(a). The two pairs of switches, (Q1, Q3) and (Q2, Q4) in the SWV generator are operated in toggle mode to generate the 240 volt, 20 kHz square wave voltage. The number of secondary windings is identified based on the required number of the isolated dc-supplies. Three secondary windings are used in the developed inverter as shown in Fig. 5. 4(a). The magnitude of the conventional inverter input dc voltage, V_C would be '3v', if the input dc voltages to the cascaded cells are maintained at the same voltage level of v by adjusting the MWT turns ratio to be 3:3:1:1. Fig. 5. 4(b) shows the prototype of the MWT, which is made of a ferrite toroidal core.

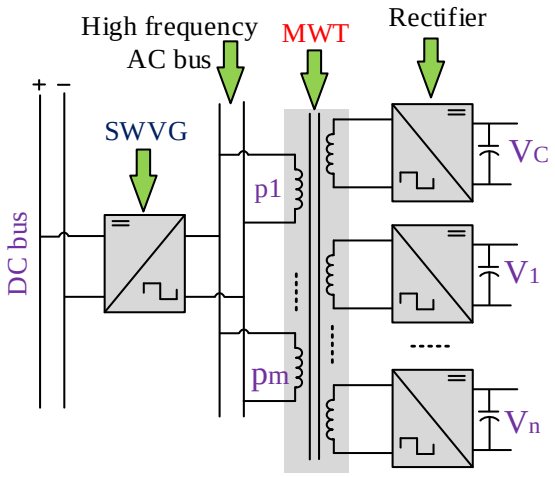


Figure 5. 5 Basic structure of MWT with multiple primary windings

5.3.1 Toroidal Transformer Winding Wire Selection

The ac resistance of the transformer windings is increased due to the skin and proximity effects, while operating with high frequency voltage and current. Multi-strained wire is utilized to reduce these effects. The diameter (*d*) of the conductor in the transformer primary and secondary windings depends on the load demand and can be calculated based on winding current (*I*), current density (*J*) and number of strains in the winding (S_n) as [25]:

$$d = \sqrt{\frac{4I/S_n}{\pi J}} \tag{5.8}$$

For simplicity, 100 copper strains of 0.5mm^2 cross-sectional area is chosen for the primary and secondary windings of the toroidal transformer. Multi-strain litz wire can be utilized in the transformer primary and secondary windings to maximize the current rating while minimizing the skin and proximity effects [5]. Moreover, the primary winding can also be split into multiple parallel windings to reduce the excitation current [75]. Fig. 5. 5 shows a schematic diagram for a possible MWT arrangement that has *m*-number of primary windings and (*n*+1) number of secondary windings. The square voltage wave generator (SWVG) in the primary side can be fed by any dc source that can be battery bank or photo voltaic (PV)-array [17].

The transformer leakage inductance is another key parameter that should be considered while designing the HFML. Analysis on the transformer leakage inductance for high and medium frequency operated MWT can be found in [75, 76]. According to [75], the excitation current and output power of a multi-winding transformer are inversely proportional with the leakage inductance. Hence optimum selection for the leakage inductance should be carefully made in

order to maintain the excitation current below the windings rated value while achieving a desired level of the output power. In the developed prototype, the maximum excitation current was 2A and the rated output power is 250VA.

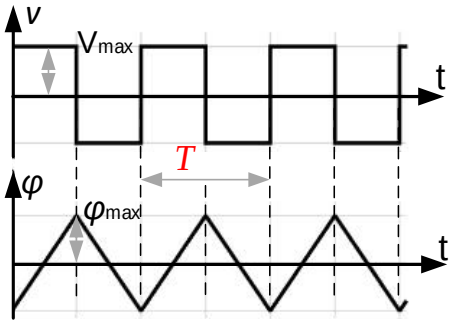


Figure 5. 6 Square wave voltage and flux in a toroidal transformer

5.3.2 Number of Turns and core selection

The HFML performs with a SWV, hence according to Faraday's law, the generated magnetic flux (φ) in the core would be a triangular waveform as depicted in Fig. 5. 6, where T, V_{max} and φ_{max} are the time-period, maximum voltage and magnetic flux, respectively.

For a complete cycle of the SWV, the triangular flux can be expressed as:

$$\varphi(t) = \begin{cases} \frac{\varphi_{max}}{\frac{T}{4}}\left(t - {}^{T}/_{4}\right), 0 \le t \le \frac{T}{2} \\ -\frac{\varphi_{max}}{{}^{T}/_{4}}\left(t - {}^{3T}/_{4}\right), \frac{T}{2} \le t \le T \end{cases} \tag{5.9}$$

According to Faraday's law, the correlation between the excitation voltage, *v(t)* and the magnetic flux within a transformer winding of *N*-turns can be derived as below:

$$\begin{aligned} v(t) &= N\frac{d\varphi}{dt} = N\frac{d}{dt}\left[\begin{cases} \frac{\varphi_{max}}{{}^{T}/_{4}}\left(t - {}^{T}/_{4}\right), 0 \le t \le \frac{T}{2} \\ -\frac{\varphi_{max}}{{}^{T}/_{4}}\left(t - {}^{3T}/_{4}\right), \frac{T}{2} \le t \le T \end{cases}\right] \\ &= \begin{cases} N\frac{\varphi_{max}}{{}^{T}/_{4}}, 0 \le t \le \frac{T}{2} \\ -N\frac{\varphi_{max}}{{}^{T}/_{4}}, \frac{T}{2} \le t \le T \end{cases} \\ &= \begin{cases} V_{max}, 0 \le t \le \frac{T}{2} \\ -V_{max}, \frac{T}{2} \le t \le T \end{cases} \end{aligned} \tag{5.10}$$

The rms voltage of the square wave can be written as:

$$\begin{aligned} V_{rms} &= V_{max} = N\frac{\varphi_{max}}{{}^{T}/_{4}} \\ &= 4f\varphi_{max} = 4fNA_eB_{max} \end{aligned} \tag{5.11}$$

where A_e and B_{max} represent the cross-sectional area of the toroidal core and the magnetic flux density, respectively.

According to (5.11), the core area of the toroidal core is inversely proportional with the SWV frequency (20 kHz). Toroidal core FERROXCUBE, T102/66/25-3C90, with A_e= 445.32mm², B_{max}= 200 mT is utilized for the HFML. According to (5.11), for V_{rms} =240V, the least number of turns in the primary winding of the implemented toroidal transformer is N= 34. The primary winding of the developed HFML in this chapter is designed with 36 turns to ease the calculation of the secondary winding turns. The two secondary windings connected to the CHB cells have the same turns' ratio with respect to the primary winding (3:1) while the winding connected to the conventional inverter via a full bridge rectifier comprises the same turns as the primary winding. The area occupied by the primary and the three secondary windings is 48 mm^2. The minimum hole-area (A_{min}) of the toroidal core is calculated by considering a clearance factor of 8 [54], which leads to a minimum hole-area, of 348mm^2. The chosen toroidal core is well suited for this design as it has 822.5mm^2 inner area with inner and outer diameters of 65.8 mm, 102mm and a thickness of 25mm. It is worth mentioning that although ferrite material has been widely utilized as toroidal core, some other magnetic materials such as Hitachi *Finmet*, and *Metglas* may provide better performance in terms of size, power capacity and efficiency [59].

Different parts of the laboratory scaled down prototype are shown in Fig. 5. 7. Table 5. 1 provides detailed specifications of various components of the developed proposed inverter topology. In the developed prototype, DSP TMS320F2812 control board is employed to generate the real-time gate pulses for the inverter switches. IGBT, HGTG20N60B3D, 600V/40A is utilized as the inverter switching device. Two IGBTs in each bidirectional switch require identical gate signals. Hence, DSP generates nine-gate signals for the conventional three-phase, two-level inverter (CTPTLI) and the three BD-switches.

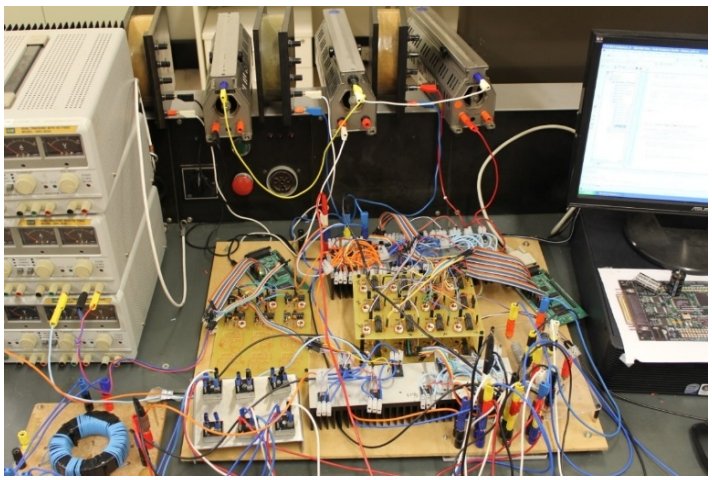


Figure 5. 7 Experimental prototype of the HF magnetic linked CMLI

Table 5. 1 Specifications of the developed scaled down test rig

Transformer	Toroidal core material	FERROXCUBE, T102/66/25-3C90
	Turns in primary winding	36
	Turns in secondary winding-1	36
	Turns in secondary winding-2 & 3	12
Rectifier unit	Full bridge rectifier module	KBPC5010, 1kV, 50A
IGBT rating	Switching devices in the CHB and CTPTLI	HGTG20N60B3D, 600V/40A
Bi-directional switches	Switching device	HGTG20N60B3D, 600V/40A
	Power Diode	RHRP1540, 400V/15A
Gate pulse generator		(DSP), TMS320F2812
Connected load		115+j94.2 Ω/phase
Line voltage		240V (peak)
Voltage levels in the line voltage		7
Apparent power of the test rig		250 VA

5.4 Performance of the proposed inverter

The performance of the proposed inverter under various loading and operating conditions is assessed as per the below case studies.

5.4.1 Case study 1: Performance of the proposed inverter with constant impedance load

Experimental analysis on the developed prototype is conducted while a balanced three phase load (Z=115+j94.2 Ω) is connected to each phase leg. Fig. 5. 8(a) presents the gate pulses of different switches within the cascaded stage; BD-switch-A and a switch in phase leg-A of the conventional three-phase two-level inverter. The waveforms of the pole voltages show four levels (0, 80v, 160v, 240v), while the voltage at the junction point J in Fig. 5. 1, V_{Jg} contains two levels (80v, 160v) as shown in Fig. 5. 8(b).

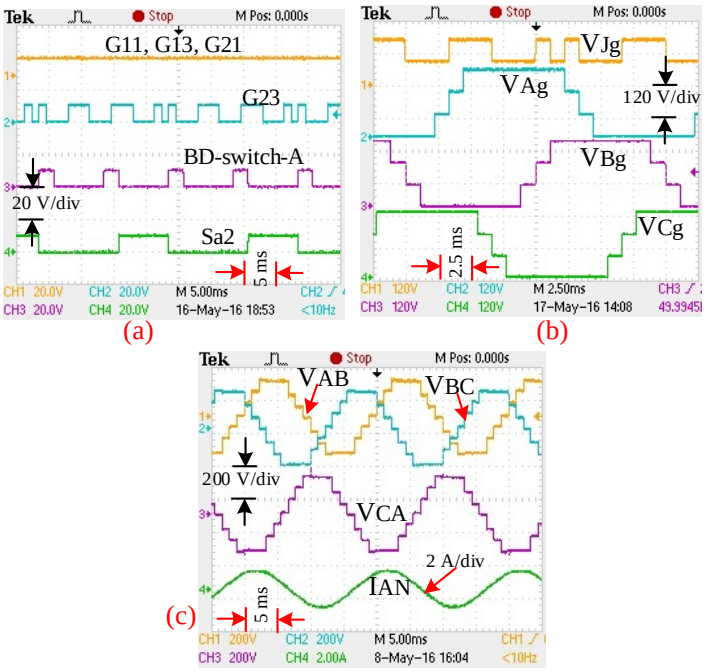


Figure 5. 8 Experimental waveforms of the proposed MLI with constant impedance load. (a) gate pulses for different switches in the H-bridge cells, BD-switch-A and a switch in conventional inverter within phase leg-A, (b) V_{Jg}, V_{Ag}, V_{Bg}, V_{Cg}, (c) line voltages (V_{AB}, V_{BC}, V_{CA}) and line current (I_{AN})

The line voltages comprise seven levels, (0, ±80v, ±160v, ±240v) in their waveforms as shown in Fig. 5. 8(c) which also shows the line current, I_{AN} waveform.

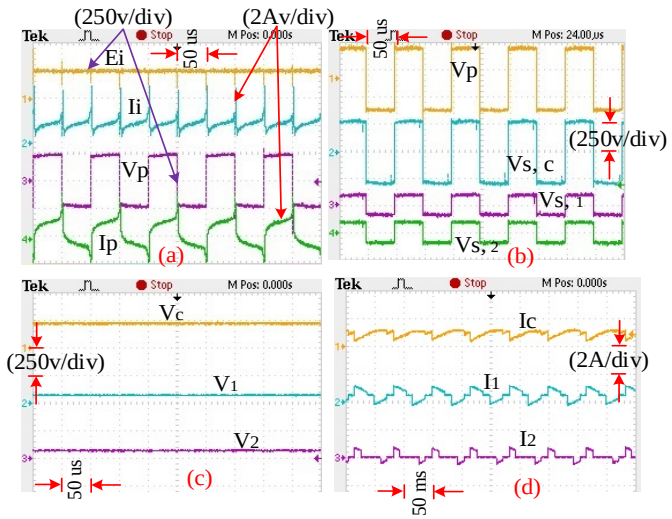


Figure 5. 9 Experimental performance with constant impedance load (a) input/output voltage/current *(E_i, I_i, V_p, I_p)* of the high frequency voltage generator, (b) primary, V_p and secondary voltages, *(V_{sc}; V_{s1}; V_{s2})* of the toroidal transformer, (c) rectifier output voltages *(V_C, V_1, V_2)* and (d) rectifier output current *(I_C, I_1, I_2)*

Fig. 5. 9(a) shows the experimental input and output waveforms of the SWV generator when the

input dc voltage, E_i is maintained at constant level. Fig. 5. 9(b) shows the high frequency voltage output from the primary and secondary sides of the MWT. The output voltages of the rectifier units are shown in Fig. 5. 9(c) while the inverter input currents at the cascaded cells and conventional three-phase two-level inverter stage are shown in Fig. 5. 9(d).

5.4.2 Case study 2: Performance of the proposed inverter with intermittent input dc source

In the experimental setup, a 'GW Laboratory dc power supply GPS-3030 is used as an input dc-power source for the SWV generator. For photo voltaic (PV) applications, a fluctuated input voltage to the MLI is expected due to the intermittent characteristics of the PV [77, 78]. To investigate the performance of the proposed inverter under such condition, voltage fluctuation is emulated using a programmable dc power supply while keeping the load similar to the previous case study.

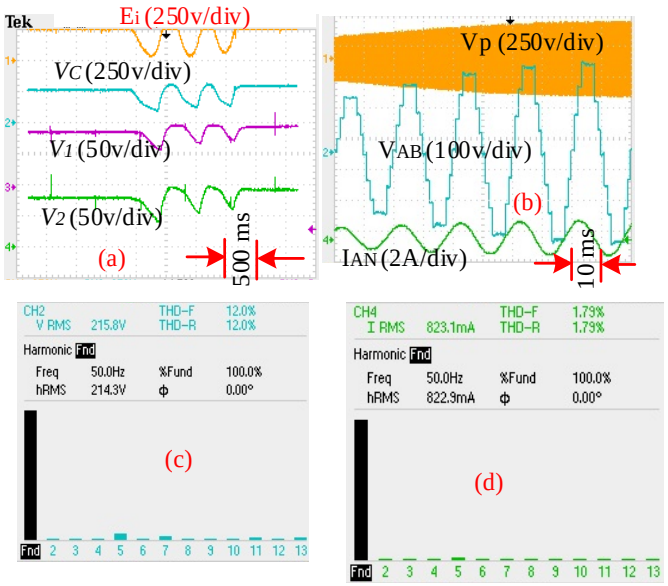


Figure 5. 10 Experimental performance with intermittent input dc source (a) input dc source voltage (E_i) and rectifier output voltages (V_C, V_1, V_2), (b) primary winding voltage of multi-winding transformer (V_p), line voltage (V_{AB}) and line current (I_{AN}), (c) line voltage THD and (d) line current THD

Fig. 5. 10 shows the impact of input source voltage, E_i fluctuation on the line voltage and line current of the proposed CMLI. The MWT always keeps the same voltage ratio between primary and secondary windings. Consequently, the rectifier produces similar voltage profiles to the cascaded inverter regardless the fluctuation of E_i as shown in Fig. 5. 10(a). While the magnitude of the cascaded inverter output line voltages and currents experience fluctuation, the number of levels in the inverter output voltage always remains unchanged as can be observed from Fig. 5. 10(b). This constant level-generating phenomenon ensures no increment in the total harmonic distortion (THD) in the inverter output voltage and current waveforms during fluctuation events

in the input dc voltage. As shown in Figs. 10(c) and (d), the line voltage waveforms exhibit 12% THD, while 1.79% THD is observed in the line current. The line voltage THD can be reduced to be less than 5% to comply with the IEEE standard [64] by increasing the number of levels. Nevertheless, the 12% THD in a 7-level inverter is quite low in comparison with other proposed cascaded MLI topologies producing the same number of levels in the output voltage waveform [10]. This key feature makes the proposed inverter topology a suitable candidate for voltage controlled motor drive applications in the machinery industry and electric vehicles.

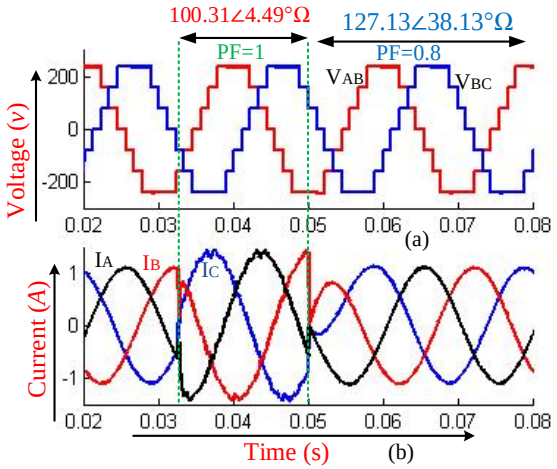


Figure 5. 11 Simulation results for a dynamic change in the load from nearly unity PF (100.31∠4.49°Ω) to 0.8 lagging PF (127.13∠38.13°Ω): (a) line voltage waveforms, (b) line current waveforms

5.4.3 Case study 3: Performance of the proposed inverter considering load dynamics

Inverter output voltage and current waveforms are observed during dynamic loading conditions. Fig. 5. 11 shows the simulation results when a load of nearly unity power factor (PF) (100.31∠4.49°Ω per phase leg) changed at t=0.0325s to 0.79 PF (127.13∠38.13°Ω per phase leg) that lasts for a duration of 0.0175s after which the original load is retained. Although a little distortion can be observed in the line current waveforms as shown in Fig. 5. 11(b) during the transition period, no significant effect can be seen in the line voltage waveforms shown in Figs. 11(a).

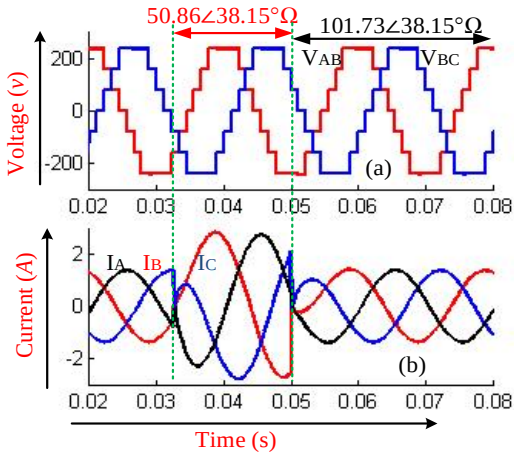


Figure 5. 12 Simulation results for a dynamic change in the load magnitude with the same PF: (a) line voltage waveforms, (c) line current waveforms

The performance of the proposed CMI is also observed for a change in the load magnitude with the same power factor. Fig. 5. 12 shows the inverter line voltage and current waveforms when the magnitude of a 0.79 PF lagging load (50.86∠38.15°Ω per phase leg) is doubled to 101.73∠38.15°Ω per phase leg at t=0.0325s for a duration of 0.0175s. Similar observations reported in the above case (Fig. 5.11) can be noticed here.

The above case studies reveal the feasible application of the proposed CMLI topology with renewable energy sources of intermittent characteristics and with loads of dynamic changes.

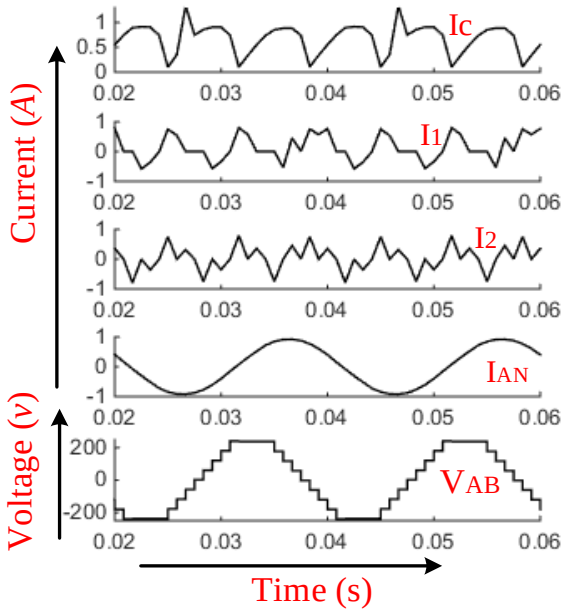


Figure 5. 13 Simulation results of rectifier output currents: I_C, I_1, I_2 and the MLI output voltage and current, V_{AB} and I_{AN} for asymmetric CHB input voltages

5.4.4 Case study 4: Performance of the proposed inverter under asymmetric dc voltages

This case study is carried out to investigate the performance of the proposed CMLI under asymmetric rectifier output voltages. The asymmetric rectifier voltages are implemented by changing the transformer turns ratio from 3:3:1:1 to 4:4:2:1 in order to get asymmetric voltage magnitudes for V_1 and V_2. According to this turns ratio, the rectifiers output voltages will be: V_C= 240V, V_1=60V and V_2=120V. Fig. 5.13 shows the rectifier output currents I_C, I_1, I_2 along with the MLI output voltage (V_{AB}) and current (I_{AN}) waveforms. As can be seen in the aforementioned figure, the number of levels in the MLI output voltage is increased to 9-levels since the H-bridge cascaded modules are now fed with binary-related input voltages (60V and 120V). This configuration achieves more levels in the output voltage waveform than symmetric CHB voltages as mentioned in the introduction section.

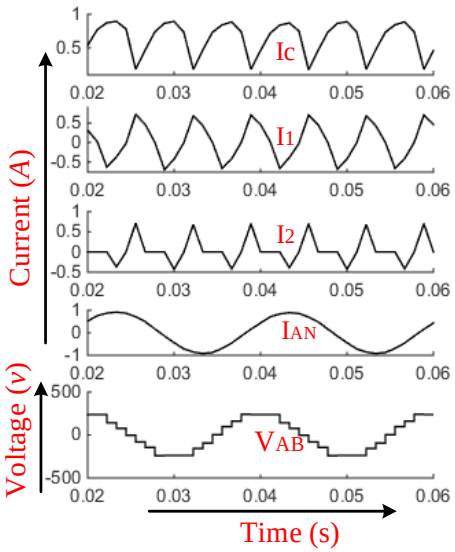


Figure 5. 14 Simulation results of rectifier output currents: I_C, I_1, I_2 and the MLI output voltage and current, V_{AB} and I_{AN} for unbalanced CHB input voltages

5.4.5 Case study 5: Effect of unbalanced CHB input voltages

The performance of the proposed inverter is also observed under unbalanced input voltages to the CHB cells. The imbalance may arise due to several factors including the ageing of the capacitors of the ripple filters connected to the rectifiers' terminals. In this case study, the voltage imbalance is created by adjusting the number of turns of the transformer two secondary windings connected to the CHB cells so that V_1=64V and V_2=96V. As can be seen in Fig. 5. 14, the line voltage which comprises 7-levels and current waveforms do not exhibit observable change due to the unbalanced input dc voltages to the CHB cells. Also, no abnormal change can be seen in the

rectifier output currents I_C, I_1 and I_2. This case study reveals the possible applications of the proposed CMLI topology in unbalanced dc voltage conversion systems.

It is worth noting that circulating current may arise within parallel-operation of voltage source inverters [79-81]. In the proposed topology, the inputs to the rectifier are magnetically isolated and they never operate in parallel at any switching state as shown in Fig. 5. 2 and hence, no circulating current is expected for this configuration.

5.5 Applications of the proposed inverter

With the revolution in power electronic technology, high rated semiconductor switches such as IGBT-module, FZ500R65KE3 with a voltage rating up to 6.5 kV, is readily available in the market [59]. Moreover, the voltage and current ratings of switching devices can be further extended by connecting multiple switches in a suitable series-parallel combination. This will facilitate the utilization of the proposed inverter in various grid-connected applications. For example, the proposed inverter can be utilized in hybrid renewable energy conversion systems in which different renewable energy sources such as solar photovoltaic, wind and battery storage are integrated via a common DC-link as shown in the block diagram of Fig. 5. 15 [82] in which the proposed topology facilitates the integration of such sources with the grid. Furthermore, as highlighted in case study 2 in section VI, the proposed inverter is a good candidate for motor drive and electric vehicles applications.

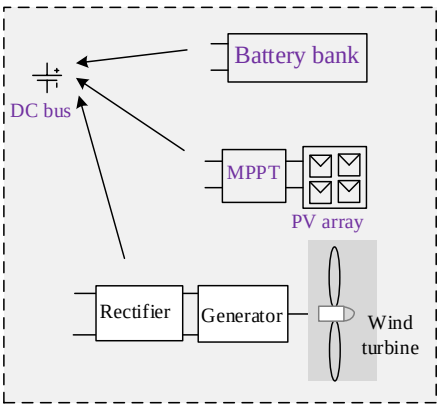


Figure 5. 15 Common DC-bus with hybrid renewable energy sources

5.6 Comparison with other three phase CMLI Topologies

In this section, the proposed CMLI concept proposed in this chapter is compared with some counterparts CMLI topologies proposed in the literatures. Several CMLI topologies are proposed

in the literature with the aim of reducing the device count and maximizing the number of levels in the output voltage [40, 43, 50].

Unfortunately, the majority of these topologies are only presented as a single-phase structure. To extend these inverters to three phase structures, the number of power electronic devices required is simply three times that of the single phase inverter structure [51, 55-57]. The proposed CMLI topology in this chapter allows the replacement of the cascaded stage in Fig. 5. 1(a) with any existing single phase topology to realize a three phase structure without tripling the device count as per the current practice.

Table 5. 2 Comparison of the proposed three phase inverter concept with conventional three phase structures

Three phase MLI		N_{level}	N_{Switch}	N_{Gate}	$N_{Rectifier}$
[56]	Conventional 3- phase structure	9	30	30	9
	This paper proposed structure	11	18	18	4
[50]	Conventional 3- phase structure	81	48	48	24
	This paper proposed structure	83	28	28	9
[43]	Conventional 3- phase structure	13	30	30	12
	This paper proposed structure	15	22	22	5
[40]	Conventional 3- phase structure	49	66	66	24
	This paper proposed structure	51	34	34	9

Table 5.2 shows a detailed device count comparison between the conventional three phase structure and the proposed three phase structure in this chapter for some recently developed CMLI topologies. As it can be seen from the table, the proposed topology in this chapter exhibits a significant reduction in the number of device count including number of switches N_{Switch}, number of gate driver circuits N_{Gate} and number of rectifiers $N_{Rectifier}$ while achieving higher levels N_{level} in the output voltage when compared with other conventional 3-phase CMLI structures.

On the other hand, various three-phase magnetic linked, asymmetric H-bridge modules-based CMLIs have been reported in the literature. In [54], an H-bridge module-based CMLI is implemented using high frequency magnetic link to generate 27-levels in the line voltages. An isolated dc-link H-bridge module- based CMLI could achieve 81-level in the output voltage as presented in [18]. In both cases, trinary relation is maintained among the input dc supplies to the H-bridge modules. Three H-bridge modules in the CMLI topology proposed in [54], are connected directly with the dc-power supply and hence, this arrangement does not ensure the essential galvanic isolation required for grid-connected applications. To facilitate a comparison with these two topologies, a trinary-relation has been maintained among the dc-supplies of the CHB cells in the CMLI proposed in this chapter. Also, the number of CHB cells has been increased to three to

achieve 29-levels in the output voltage waveform which is close to the 27-levels achieved in [54]. For comparison with the 81-level CMLI topology presented in [18], the number of CHB cells in the topology proposed in this chapter is increased to 4.

Table 5. 3 Comparison between the proposed CMLI and counterparts CMLI topologies proposed in [18] and [54]

Category	3-phase, 27-level CMLI proposed in [54]	Proposed CMLI with trinary-related three CHB cells	3-phase, 81-level CMLI proposed in [18]	Proposed CMLI with trinary-related four CHB cells
N_{level}	27	29	81	83
N_{Switch}	36	24	48	28
N_{Gate}	36	21	48	25
$N_{Rectifier}$	9	4	12	5
$THD_{line\ voltage}$	3%	2.97%	1%	1%

Table 5. 3 shows a detailed comparison between the proposed CMLI in this chapter and those proposed in [18] and [54], when generating close number of levels in the output voltage by adopting trinary related input dc voltages to the H-bridge modules in the cascaded stage.

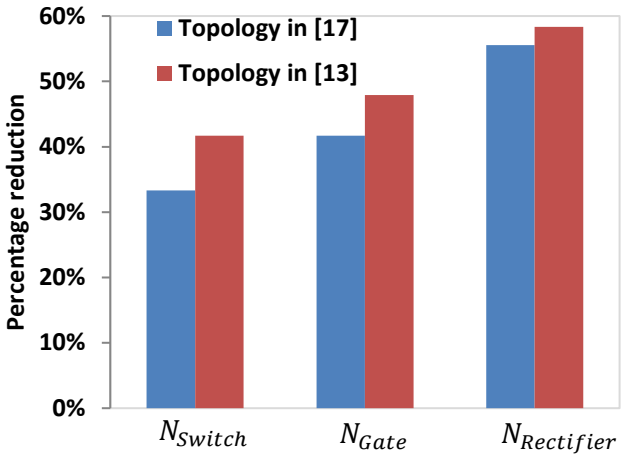


Figure 5. 16 Percentage reduction in device count with respect to CMLI topologies proposed in [18] and [54]

As can be seen in the table, a notable amount of device reduction is achieved while implementing the concept proposed in this chapter. The percentage reduction in the power electronic components employed to implement the proposed CMLI in this chapter when compared to the topologies in [13] and [17] is significant; in particular, when a higher number of levels in the output voltage waveform is required as can be seen in Fig. 5. 16. It should be noted that the device count reduction achieved in the proposed CMLI concept in this chapter does not compromise for the

quality of the output waveforms as can be seen from the number of voltage levels and THD in the voltage waveform.

5.7 Summary

A new high frequency magnetic linked-based cascaded multilevel inverter is presented in this chapter. The proposed concept exhibits several advantageous when compared with counterpart topologies proposed in the literatures. This includes the ability to extend the single-phase inverter to a three-phase structure without tripling the power electronic components as per the current practice in the literatures. Experimental and simulation analyses reveal the feasible applications of the proposed inverter with renewable energy sources of intermittent characteristics. Results also show the performance of the proposed inverter is not significantly impacted during load dynamic changes. The proposed concept is easy to implement as it can employ any cascaded inverter topology within a cascaded stage along with a simple conventional three-phase two-level inverter stage.

Chapter Six: Conclusions and Future work

6.1 Conclusions

This work presents a new design for a three phase cascaded MLI along with simulation and experimental results that validates the practical feasibility of the proposed three-phase MLI concept. Comparison with the published three phase MLI topologies shows the superiority of the proposed inverter concept over existing topologies in terms of reduced device count without compromising the quality of the output voltage.

The main contribution and key features of this research can be highlighted as follows:

- The ultimate goal of this research is to develop a generalized technique to reduce device count of three phase multilevel inverter; this goal is achieved in a systematic process.
- An extensive literature study has been done on different cascaded multilevel inverter topologies and their control strategies. Besides, the shortcomings of the existing multilevel inverter topologies are highlighted.
- A half-bridge cascade topology with non-isolated dc-voltage supplies is developed and proposed at the early stage of this research. The switching pulses of this topology is controlled by simple Sine Pulse Width Modulation (SPWM) strategy. The proposed topology reduces the number of dc-supplies up to 67% in comparison to the existing symmetric half-bridge multilevel inverter topologies. Besides, the proposed topology has been investigated under a number of case studies, different load power factor, dynamic load, variable carrier frequency and modulation index. Moreover, the performance of the topology is tested while a PV-array is connected as an input dc-voltage supply. The proposed half-bridge cascaded multilevel inverter is compared with a number of half-bridge inverter topologies in the literatures and it has been found that the proposed topology not only reduces the number of dc-supplies, but also optimizes the number of levels in the output voltage. The feasibility of the proposed inverter is confirmed through simulation and experimental analyses at different operating conditions.
- In spite of having the capability to reduce the number of dc-power supplies of the aforementioned three phase half-bridge inverter, it can't reduce the number of power electronic devices. In order to reduce the number of power electronic devices, an innovative technique has been adopted that allows the aforementioned non-isolated half-bridge inverter to be implemented with reduced number of power electronic devices. This

technique not only applicable for non-isolated cascaded half-bridge cells, but also is applicable for non-isolated half-bridge cells. A number of dc-voltage supply algorithms is developed to optimize the number of levels in the output voltage waveform. Furthermore, a stair case modulation technique is applied to generate different switching logics. Moreover, the proposed half-bridge cascaded multilevel inverter topology is compared with a number of cascaded inverter topologies. It has been found that the proposed technique reduces significant amount of power electronic components and dc-voltage supplies.

- While the aforementioned device count reduction technique is implemented only for half-bridge cascaded multilevel inverter, it is not extended as a generalized technique for other existing cascaded multilevel inverter topologies. The proposed device reduction concept can be adopted to extend any single phase MLI to 3-phase structure without tripling its components as per the current practice. Also, the new technique can be adopted by existing three phase topologies to reduce their device count without degrading the overall performance. Bothe symmetric and asymmetric three phase cascaded inverter topologies can adopt this device reduction technique. Furthermore, the dc-voltage supplies are managed by high frequency magnetic link from a single dc-source which makes the inverter a good candidate for renewable energy applications. Number of case studies have been conducted to verify the performance of the high frequency linked cascaded multilevel inverter including constant impedance load, intermittent input supply, dynamic load, asymmetric input dc-supplies and unbalanced input dc-supplies that revealed the superiority of the proposed inverter over existing ones.

- Since the number of inverter components is directly related with the cost, complexity and installation area, the new three phase concept offers a cost effective technique that is expected to have a great potential in renewable power generation systems and smart grid applications.

- The high frequency magnetic link provides galvanic isolation between input and output of the inverter that ensures more safety in grid connected inverter operation.

6.2 Future work

It expected that the proposed high frequency magnetic link cascaded MLI will play significant role in grid connected renewable energy conversion systems. Potential future research in this area could be:

- Recently, a number of magnetic materials such as Hitachi *Finmet*, and *Metglas* have been developed with the aim of reducing the size of the magnetic core of the multi-winding transformer. Hence, it is recommended to utilise the aforementioned magnetic materials to connect the proposed MLI system for high voltage and power applications.

- While this thesis investigated the proposed MLIs using open loop control algorithm, the inverter can be precisely controlled with closed loop algorithm which can extend its applications.

- While laboratory dc-voltage supply units are utilised as input source, real time PV and wind turbine generator can be connected as input source to investigate the performance of the inverter when connected to real systems.

- The high-frequency link inverter is tested under variable input voltage magnitudes and it shows a smooth linear change in the output voltage and current magnitudes. This phenomenon ensures a potential application of the high-frequency link inverter in voltage controlled variable speed motor drive design.

- While staircase space vector modulation technique is utilised as a control strategy in the proposed CMLI, it may raise abnormal situation when the inverter is designed for bi-directional power conversion and hence, standard pulse width modulation/Sine pulse width modulation can be developed and investigated.

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