

Real–Time Testing of Energy Storage Systems in Renewable Energy Applications

Cedric Caruana

(Corresponding Author)

Faculty of Engineering, The University of Malta, Msida MSD 2080, Malta.

Email: cedric.caruana@um.edu.mt

Phone: 0035623402438

Adnan Sattar

College of Engineering, The Petroleum Institute, P.O. Box 2533, Abu Dhabi, UAE.

Email: adnansattar54@gmail.com

Ahmed Al–Durra

College of Engineering, The Petroleum Institute, P.O. Box 2533, Abu Dhabi, UAE.

Email: aaldurra@pi.ac.ae

S.M. Muyeen

College of Engineering, The Petroleum Institute, P.O. Box 2533, Abu Dhabi, UAE.

Email: smmuyeen@pi.ac.ae

ABSTRACT

Energy storage systems provide a promising solution for the renewable energy sector to facilitate large–scale grid integration. It is thus very important to explore means to validate their control scheme and their behaviour in the intended application before actual commissioning. This paper presents a reduced–scale hardware–in–the–loop simulation for initial testing of the performance of energy storage systems in renewable energy applications. This relieves the need of selecting and tuning a detailed model of the energy storage element. A low–power test rig emulating the storage element and the power converter is interfaced with a real time digital simulator to allow dynamic experimental tests under realistic conditions. Battery energy storage for smoothing the output power of a variable speed wind turbine is considered in this paper; however the proposed test methodology can be easily adapted for other storage elements in renewable energy, distributed generation and smart grid applications. The proposed HIL simulation is detailed and the experimental performance is shown.

Keywords: DC-DC converters, Energy storage, HIL Simulation, Renewable Energy, Test Methodology

NOMENCLATURE

RTDS™	Real–time simulator from RTDS Technologies
BESS	Battery Energy Storage System
VRLA	Valve Regulated Lead Acid [battery]
AGM	Absorbed Glass Material
PMSG	Permanent magnet synchronous generator

IGBT	Insulated Gate Bipolar Transistor
PWM	Pulse Width Modulation
PI	Proportional Integral (controller)

1 INTRODUCTION

In the last decade, the global installed capacity and the generation of electricity from renewable energy sources have shown a substantial growth [1]. Wind energy, in particular, is a rapidly maturing technology with proven reliability and competitiveness. Despite the slowdown in 2013, more than 51GW of new wind power was brought online in 2014. This sets a new record at an increase of 44% in the annual market and raises the total installed capacity to above 369GW [2]. As opposed to the use of conventional sources, renewable energy generation is not able to follow a set reference as it depends on the availability of the natural resource. The negative effect of the variable output on the power system can be mitigated through the use of an energy storage system (ESS) that acts as a buffer between the renewable energy source and the grid [3].

Different technologies have been proposed in the literature for the implementation of ESS [4]. This paper focuses on electrochemical solutions, which includes several types of batteries and supercapacitors. Batteries are a well-established storage technology with the advantage of being modular and scalable [5]. Supercapacitors are also finding increasing applications due to their fast response. Battery-supercapacitor hybrid energy storage systems have also been proposed to increase both the technical and economic indexes of the ESS [6].

Battery energy storage systems (BESS) provide flexible energy management that allows renewable energy generation to achieve different objectives. These include smoothing of output power fluctuation [7]–[12], storage for dispatch at times with more favourable tariffs [13] and peak shaving [14]. Recently, BESS are also finding applications in grid frequency regulation, grid stabilization, provision of spinning reserve, load levelling and others [15]. To these effects, several BESS configurations and control strategies have been published [16]. It is essential however that such proposed configurations and control strategies be thoroughly tested to validate their performance.

Software simulation is an invaluable tool for the initial evaluation of control strategies and system configurations. Simulation studies are based on a model of the real system, making the

obtained results largely dependent on the accuracy of the used models [17]. BESS are generally comprised of a battery storage element and a bidirectional dc–dc converter. The difficulty generally arises in selecting the battery model. A wide selection of models is published in the literature, covering a wide range of applications. The models are pitched at representing different aspects of battery performance, which are relevant to particular applications; however the majority are not tuned for the operating conditions prevalent in BESS applications [12]. On top of this, the diverse BESS control algorithms impose different demands on the batteries. The model options range from simple voltage–sourced models to dynamic ones, which consider the influence of external parameters on the behaviour of the battery through variable parameters [18]–[20]. The simpler models are based on battery data that is generally available but they do not represent the behaviour with sufficient detail. The introduction of more parameters, which can also be dynamic to represent external variables, can reproduce sufficient detail however tuning the additional parameters is not a trivial task. Other approaches include impedance based models that rely directly on experimental test of the batteries under different operating conditions [21]. As an example, the lead–acid battery model proposed by [19], which applies for both discharging and charging operation, is shown in Fig. 1. The model includes a number of RC blocks, whose parameters are a function of the battery state–of–charge and electrolyte temperature. E_b and R_b are the battery electrochemical emf and the internal resistance respectively, both of which vary during operation. The parasitic branch models the non–ideal effects.

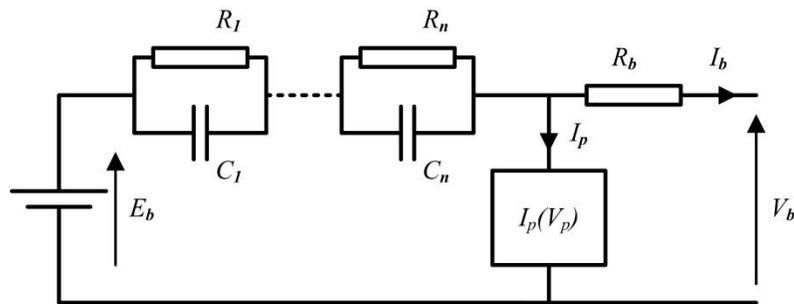


Fig. 1: Lead–acid battery model for both discharge and charge operation.

Increasing the number of RC blocks opens the potential of more accurate simulations, but at the cost of making the process of parameter identification increasingly complex. Accurate determination of the parameters generally requires a number of experimental tests [22]. Models that are tuned for the particular conditions encountered in the considered application are typically

used in the literature for the study of BESS in both wind and solar PV applications. The third order model proposed by [19] is used in [9][10], where the parameters are taken from [19] itself. The dynamic model described in [20] but with some modifications is used in [12].

Both the uncertainty and the complexity of the battery model can be overcome through the use of an experimental test rig. Experimental hardware, however, presents the challenges of development time and cost. Real-time hardware-in-the-loop (HIL) simulation combines software models with focused experimental hardware to provide a solution in between [23]. Different levels of HIL simulation are possible. These range from the implementation of control algorithms on actual microcontrollers [24] to the use of the simulator for the control of the full-scale hardware [25]. Reduced-scale HIL simulations control actual hardware but use focused, lower-power representative rigs, thus overcoming the challenges of full-scale hardware to provide a convenient intermediary step [26][27] before embarking on a full-scale prototype. A reduced-scale test bench for BESS in vehicular applications is proposed in [28]. A Li-ion battery is interfaced to a simulator through a high bandwidth amplifier, which sources or sinks the current demanded by the vehicle controller. The battery's terminal voltage is then used to assess the performance of software models. Lead-acid and Li-ion batteries are similarly interfaced to a simulator in [29]. The batteries emulate a storage element that is interfaced to an induction generator wind turbine. The battery terminal voltage is read and forced on the voltage source representing the battery in the simulated BESS to enhance the battery model. A 16kVA virtual synchronous generator (VSG) is interfaced through a power interface to a simulator in [30]. The voltage at a chosen bus in the simulation model is used as reference to set the voltage at the VSG terminals. The VSG current response is measured and injected onto the chosen bus through controlled current sources. In this way, the simulated power system is influenced by the external hardware.

This paper proposes a reduced-scale HIL simulation that can be used to test the performance of energy storage systems in renewable energy applications, without the need of specifying complex models for the energy storage elements. An experimental rig comprising of a low power ESS, including both the storage element and the power converter, and a loading unit is proposed. The test rig can be used to examine the behaviour of various battery technologies and supercapacitors. It is interfaced to a commercial real-time simulator for HIL simulation. This paper tests the effectiveness of the proposed HIL simulation by considering the case of a

BESS, interfaced through a dc–ac converter at the output of a variable–speed wind turbine, to smoothen the net power flow to the grid. The experimental rig, its control and the coupling to the modelled wind system are detailed. Experimental results detailing the performance of a VRLA AGM battery in wind output power smoothing application are shown.

2 WIND ENERGY SYSTEM MODEL

This section deals with modelling of the wind energy conversion system together with the BESS used for smoothing the net power transfer to the grid. The characteristics of the wind turbine are presented, followed by an introduction to the used real–time simulator, i.e. the RTDS™ platform. Finally the modeled wind energy conversion system, interfaced to the grid and with integrated BESS, is described and the chosen operating values are specified.

2.1 Wind Turbine

Variable–speed wind turbines allow for higher energy yield than fixed–speed wind turbines as the rotational speed can be varied for optimal aerodynamic energy conversion. The mechanical power extracted from the wind by a variable speed wind turbine P_w can be expressed mathematically by Eq. (1). ρ is the air density, A is the turbine swept area, C_p is the power coefficient and V is the wind speed. For wind turbines with blade pitch control, C_p is a function of the tip speed ratio λ and the blade pitch angle β . The tip speed ratio λ reflects the ratio between the turbine rotational speed ω_r and the wind speed V , as shown in Eq. (2) where R is the radius of the wind turbine rotor. For this work, C_p is approximated by Eq. (3) as a function of β and the λ_t parameter defined in Eq. (4) [31].

$$P_w = 0.5\rho AC_p(\lambda, \beta)V^3 \quad (1)$$

$$\lambda = \frac{\omega_r R}{V} \quad (2)$$

$$C_p(\lambda, \beta) = 0.73 \left[\frac{151}{\lambda_t} - 0.58\beta - 0.002\beta^{2.14} - 13.2 \right] e^{-18.4/\lambda_t} \quad (3)$$

$$\lambda_t = \frac{1}{\frac{1}{\lambda+0.02} \frac{0.003}{\beta^3+1}} \quad (4)$$

Variable speed wind turbines are controlled to track the optimal power that can be extracted from the wind. A common approach is to base the optimal power capture P_{w_opt} on the measured

rotational speed [32], as given by Eq. (5). C_{p_max} is the highest attainable C_p and λ_{opt} is the corresponding tip speed ratio. For the C_p characteristic used in this paper, the corresponding values are at 0.44 and 5.9 respectively. The angle β is set by the pitch controller such that the rotational speed of the turbine does not exceed its rated value. The control law can be simplified as shown in Eq. (5) where k is the constant of proportionality.

$$P_{w_opt} = 0.5\rho\pi R^5 \frac{C_{p_max}}{\lambda_{opt}^3} \omega_r^3 = k \cdot \omega_r^3 \quad (5)$$

2.2 RTDS™ Platform

The wind energy conversion system model is implemented on the RTDS™ platform [33][34]. RTDS™ is based on parallel processing hardware architecture which offers the capability of small time steps. For a typical renewable energy system including power electronic conversion, large time steps of 50µs and small time steps in the range of 1.4 to 2.5µs are possible.

RTDS™ facilitates interfacing through both analog and digital channels. Optical analog to digital converter (OADC) cards introduce optically isolated 16 bit analog to digital conversion. Giga Transceiver analog output (GTAO) cards provide 12 analog output channels that can output signals from both the large- and small- time steps. Digital Time Stamp (DITS) and Gigabit Transceiver Digital Input (GTDI) cards allow reading of pulse width modulated signals from an external controller.

2.3 Modeled System

A block diagram of the modeled system is shown in Fig. 2. A 5MW variable speed wind turbine, equipped with blade pitch mechanism, is directly coupled to a 5MW permanent magnet synchronous generator (PMSG) with magnet strength of 1.4pu. Permanent magnet synchronous generators relieve the need of the field supply required for wound rotor synchronous generators, whilst still allowing operation with a lower ratio gearbox or directly coupled to the wind turbine. The generator output is conditioned through fully rated back-to-back converters, which allow the conversion of the variable frequency, variable voltage output of the PMSG to a fixed frequency, fixed voltage suitable for grid interfacing. Transformer ($T1$) steps up the voltage to match that of the grid. The wind system is connected to the grid via a line at 6.6kV. The dc link

voltage of the back-to-back converters is set at 2.3kV. Transformer $T1$ is a 5MVA 1.25kV/6.6kV unit with an impedance of 0.1pu.

Different options for the integration of the ESS to renewable energy sources have been proposed in the literature [35]. For this work, a BESS interfaced to the grid via a dc-to-ac converter (interface converter) and step up transformer ($T2$), is introduced at the point of coupling (PoC), as shown in Fig. 2. The BESS dc link voltage is controlled at 1kV. Transformer $T2$ is a 2MVA 0.55kV/6.6kV unit with an impedance of 0.1pu. The battery bank is composed of a combination of VRLA AGM batteries, as described in Section 4.1. The bank is interfaced to the dc link through a dc-dc converter, which is controlled to regulate the power flow from the BESS. Standard vector control is used for the control of the wind turbine back-to-back converters and the BESS interface converter [36].

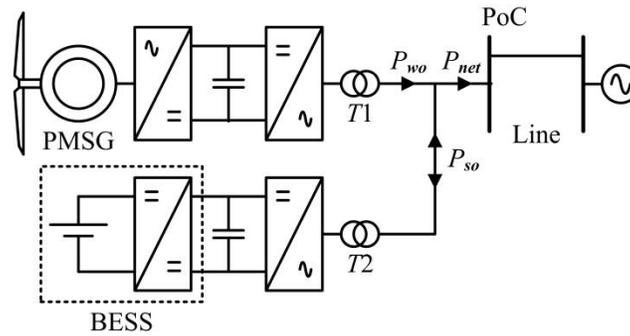


Fig. 2: Block diagram of the modeled variable speed wind turbine with integrated BESS via interface converter for output power smoothing.

3 ENERGY STORAGE SYSTEM TEST RIG

The focus of this paper is on the experimental test of the BESS under realistic conditions through reduced-scale HIL simulation. To this effect, a low power experimental hardware (test rig) is constructed. The test rig consists of an experimental energy storage system (eESS) and a similar unit for loading the eESS as required by the system simulation. The test rig is interfaced to the system model presented in Fig. 2, replacing the shown BESS for HIL simulation test. In such way, realistic power flows that are typical of wind output power smoothing scenarios are obtained from the eESS.

3.1 Test Rig Design and Concept

In the considered application, the BESS is required to drive the active power flow at the interface converter ac side (P_{STAT}) such that the net active power transfer to the grid follows a set reference P_{net}^* . The respective powers are indicated in Fig. 2, where P_{wo} is the wind output power. The BESS supplies/absorbs power to/from the interface converter's dc link. The BESS power is regulated through a suitable controller that generates the required duty cycle for the bidirectional buck converter that interfaces the battery bank to the dc link. Control of the interface converter dc link voltage then transfers the active power to/from the grid.

The same configuration is used for the test rig. The eESS consists of an energy storage device (primary element) interfaced to a dc link capacitor through a bidirectional buck converter. In order to load the eESS, a secondary storage element is interfaced to the dc link through a bidirectional boost converter. The configuration is shown in the upper part of Fig. 3. The boost converter is used to control the dc link voltage V_{dc} . In this way, power can be oscillated (less the losses) between the primary and secondary storage elements. Similar storage technology is used for both elements such that the performance of the eESS is not hindered by the characteristics of the secondary element. The buck- and boost- converters are switched independently as required by their respective controllers.

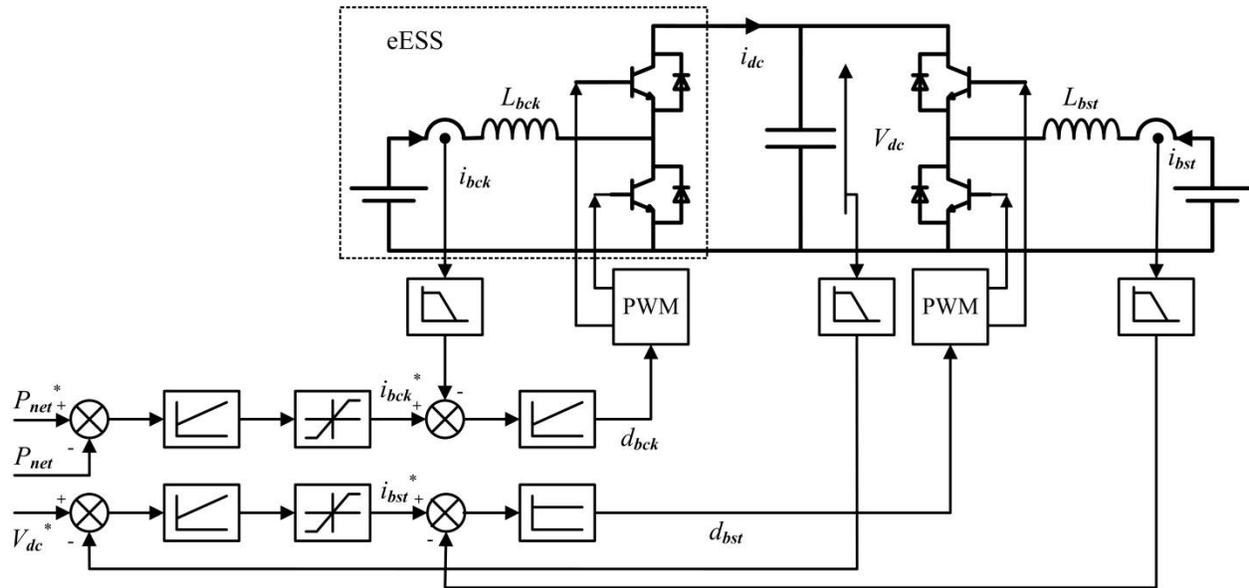


Fig. 3: Configuration of the experimental energy storage system (eESS) test rig and the proposed control structure.

3.2 Selection of the Components

The proposed test rig can be configured to test different energy storage technologies. This paper is focused on battery energy storage, specifically on valve regulated lead acid (VRLA) absorbed glass mat (AGM) batteries. Lead acid batteries offer low price, high unit-voltage, stable performance and a wide range of operating temperature [37]. In the actual BESS, the battery bank will consist of series- and parallel- combinations of a chosen battery. For the test rig, a 12V battery is used for each side. Further batteries can be added to the storage element, connected in series and in parallel to obtain higher voltage and Ampere-hour respectively. A Trojan Deep Cycle AGM 12V 33Ah battery was selected to allow a continuous charge current capability of up to 6A [38]. This facilitates the scaling of the currents between the modeled system and the eESS. The actual current flow in the test rig is simply up scaled from Amperes to kilo Amperes to get the equivalent current in the model. In order to limit the ripple in the current, the switching frequency was set to 10kHz and inductors of 0.8mH were used. High voltage rating IGBTs were used such that the conduction losses of the dc-dc converter can be scaled to approximate those of a full scale converter.

3.3 Control of the Test Rig

Standard cascaded control is used for both sides of the test rig. The control structures are shown in the lower part of Fig. 3. Inner current controllers are used as they allow maintaining the currents within set limits to protect the converters and the storage elements. For the eESS, an outer power controller driven by the reference P_{net}^* generates the reference for the required current flow from the storage element. The current reference i_{bck}^* is limited to reflect the rating of the buck converter and/or the storage element. An inner current controller then generates the duty cycle d_{bck} driving the buck converter. A PI controller is used for both stages. The dc link voltage V_{dc} is regulated to the set reference V_{dc}^* by an outer voltage controller. An inner current controller regulates the boost converter current to follow i_{bst}^* , hence generating the duty cycle d_{bst} driving the boost converter. A PI- and a P- controller are used for the outer and inner control stages respectively.

3.4 Control Design

Modeling of the dc–dc converters dynamic behavior facilitates the design of the controllers. The use of pulse width modulation makes the converters nonlinear and time variant [39]. State space averaging is a well–known technique to obtain a linear circuit representation. Small scale modeling techniques can then be applied to linearize the operation around a chosen steady state operating point. Canonical small signal models for the common dc–dc converters are given in [39][40]. As shown in Fig. 2, the bidirectional buck converter of the eESS is intended to vary the battery terminal voltage such that the desired current flow is attained. It is designed to operate in the continuous conduction mode. For the converter modeling, a simplified battery model consisting of a voltage source representing the primary battery open circuit voltage E_{bp} and a constant internal resistance is used. Both E_{bp} and the dc link voltage are assumed constant; any actual variations are considered as disturbances to the control loop. Considering only a one quadrant buck converter, the equivalent circuit is shown in Fig. 4(a). Setting the variation in the dc link– and battery open circuit– voltages to zero, the small signal control to battery current transfer function $G_{bck}(s)$ is then given by Eq. (6). $\tilde{i}_{bck}(s)$ and $\tilde{d}_{bck}(s)$ are small perturbations in the battery current and the duty cycle respectively. V_{dc} and D_{bck} are the assumed steady state operating points for the dc link voltage and the duty cycle respectively. R_{bp} is the primary battery internal resistance and L_{bck} is the buck converter inductance. The parameters used for the control design of the buck converter are shown in Table 1. A delay representing the combined effects of the pulse width modulation (PWM) and the sampling was considered for the control design.

$$G_{bck}(s) = \frac{\tilde{i}_{bck}(s)}{\tilde{d}_{bck}(s)} = \frac{V_{dc}}{D_{bck}} \frac{1/R_{bp}}{(L_{bck}/R_{bp})s+1} \quad (6)$$

Table 1: Buck and Boost Converters transfer function parameters

Buck Converter		Boost Converter	
Parameter	Value	Parameter	Value
V_{dc}	19.6 V	V_{dc}	19.6V
D_{bck}	0.612	D_{bst}	0.388
R_{bp}	50 mΩ	R_{bs}	50mΩ
L_{bck}	0.8 mH	L_{bst}	0.8mH
		C	680μF

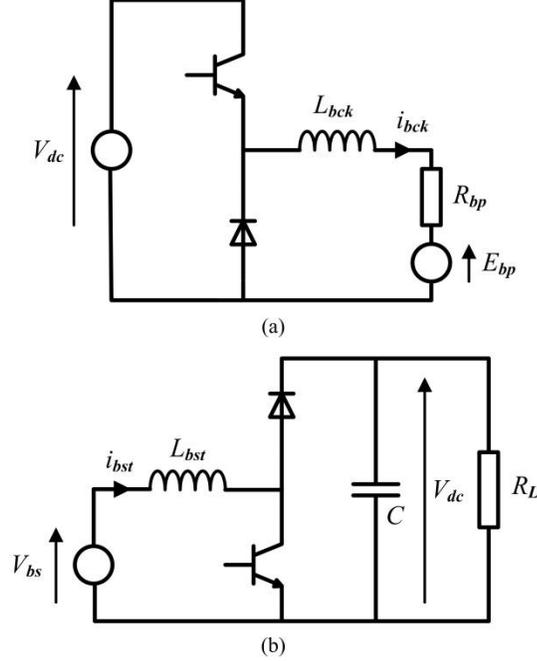


Fig. 4: Equivalent circuit of a 1–quadrant (a) buck converter and (b) boost converter.

The bidirectional boost converter is intended to control the dc link voltage. It is also designed to operate in the continuous conduction mode. For the converter modeling, the secondary battery terminal voltage V_{bs} is assumed constant. Considering only a one quadrant boost converter, the equivalent circuit is shown in Fig. 4(b). The power (or current) transfer to the eESS is considered through the introduction of the hypothetical load resistance R_L . As for the buck converter case, variations in the battery terminal voltage and the power flow to the eESS are considered as disturbances. Setting such disturbances to zero, the derived small signal control to dc link voltage transfer function $G_{bst}(s)$ is given by Eq. (7). $\tilde{v}_{dc}(s)$ and $\tilde{d}_{bst}(s)$ are small perturbations in the dc link voltage and the duty cycle respectively. V_{dc} and D_{bst} are the assumed steady state operating points for the dc link voltage and the duty cycle respectively. L_{bst} is the boost converter inductance. The parameters used for the control design of the boost converter are shown in Table 1.

$$G_{bst}(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{d}_{bst}(s)} = \frac{V_{dc}}{(1-D_{bst})} \frac{\left(1 - \frac{L_{bst}}{(1-D_{bst})^2 R_L} s\right)}{\frac{L_{bst} C}{(1-D_{bst})^2} s^2 + \frac{L_{bst}}{(1-D_{bst})^2 R_L} s + 1} \quad (7)$$

It can be seen from Eq. (7) that $G_{bst}(s)$ contains a right hand side (RHS) zero. It is desired to set the closed loop poles as far as possible from the RHS zero. However, if the control is designed such that there is a separation of more than one decade between the RHS zero and the poles, then the damping ratio will be considerably low [42]. The presence of the RHS zero and the possible low damping ratio severely restrict the attainable closed loop bandwidth. The restriction can be alleviated through the use of current mode control as it allows the introduction of substantial additional damping [39], hence allowing for higher closed loop bandwidths. The additional damping can be set to dominate the overall damping and is independent of R_L [42]. Alternative applicable control techniques include adaptive sliding mode control [43].

Current mode control consists of an inner current loop and an outer voltage loop as shown in Fig. 5. The delay block represents the combined effects of the PWM and the sampling, as for the buck converter control. The small signal transfer function of Eq. (7) can be split into two parts to show the inductor current i_{bst} . The small signal control to inductor current transfer function $G_{bst1}(s)$ and the small signal inductor current to dc link voltage transfer function $G_{bst2}(s)$ are given in [39][44] and are shown in Eqns. (8)–(9). Assuming a gain K_{pl} for the inner current loop P controller, the small signal control to dc link voltage is given by Eqn. (10). Considering the additional damping term as dominant, K_{pl} can be set to achieve the desired damping ratio. A value of 0.707 is suggested in [42]. If the current gain is small enough, the system resonant frequency only shows a small variation.

$$G_{bst1}(s) = \frac{\tilde{i}_{bst}}{\tilde{d}_{bst}(s)} = \frac{V_{dc}}{(1-D_{bst})^2 R_L} \frac{R_L C s + 2}{\frac{L_{bst} C}{(1-D_{bst})^2} s^2 + \frac{L_{bst}}{(1-D_{bst})^2 R_L} s + 1} \quad (8)$$

$$G_{bst2}(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{i}_{bst}(s)} = (1 - D_{bst}) R_L \frac{1 - \frac{L_{bst}}{(1-D_{bst})^2 R_L} s}{R_L C s + 2} \quad (9)$$

$$\frac{\tilde{v}_{dc}(s)}{\tilde{d}_{bst}(s)} = \frac{K_{pl} V_{dc}}{(1-D_{bst})} \frac{\left(1 - \frac{L_{bst}}{(1-D_{bst})^2 R_L} s\right)}{\frac{L_{bst} C}{(1-D_{bst})^2} s^2 + \left[\frac{L_{bst}}{(1-D_{bst})^2 R_L} s + \frac{K_{pl} V_{dc} C}{(1-D_{bst})^2}\right] + \left[1 + \frac{2K_{pl} V_{dc}}{(1-D_{bst})^2 R_L}\right]} \quad (10)$$

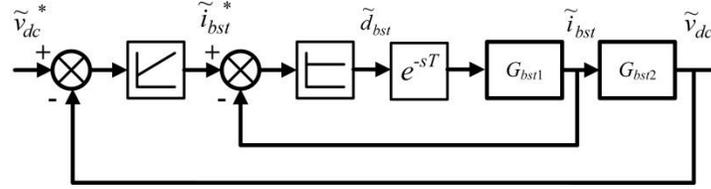


Fig. 5: Schematic of the current mode control scheme for the boost converter.

3.5 Implementation

The modelled system is implemented on the RTDSTM and is interfaced to the test rig via the GTA0 and OADC cards, as shown in Fig. 8. All the test rig controllers, shown in Fig. 3, are implemented on the RTDSTM. In order to mitigate possible time delays, it was opted to output a control signal for the duty cycles d_{bck} and d_{bst} from the RTDSTM and generate the PWM waveforms externally. Hall-effect sensors, with appropriate interface circuitry, were used to scale the current- and voltage- feedback signals to the input voltage range of the OADC cards. The signals were then scaled to actual currents and voltages in the software code. Both inductor currents (i_{bck} and i_{bst}) and the dc link voltage (V_{dc}) are filtered by a first order lag filter with a time constant of 0.16ms to attenuate the switching ripple.

The bandwidth of the buck converter current loop is set at around 300Hz with a phase margin of 74° , to be sufficiently fast to mitigate deadtime and current clamping effects [41]. Such bandwidth also provides a sufficient low frequency band where the output tracks the input frequency, as required for the smoothing operation. The resulting closed-loop bode plot is shown in Fig. 6. It can be observed that the buck converter will allow input tracking up to around 10Hz, which is sufficient for smoothing applications.

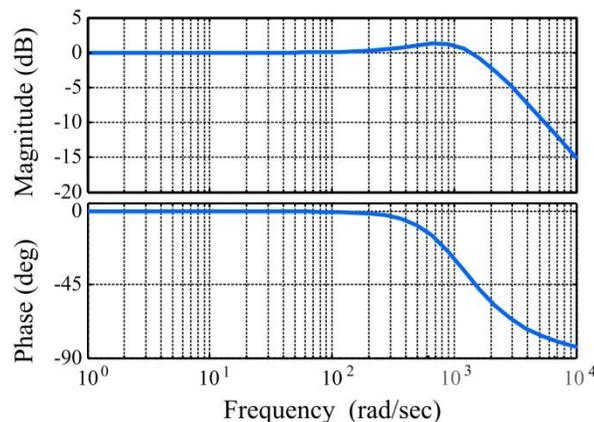


Fig. 6: Closed-loop bode plot for the current loop of the Buck converter.

The boost converter V_{dc} loop bandwidth was set at around 180Hz to provide sufficient disturbance rejection capability at the frequencies of interest. It can be seen from Fig. 7 that an attenuation of 40dB or higher is attained for frequencies up to around 1.6Hz, which is considered sufficient for renewable energy applications. A bandwidth of approximately 1Hz was set for the eESS power loop such that the boost converter can maintain the dc link voltage with low ripple.

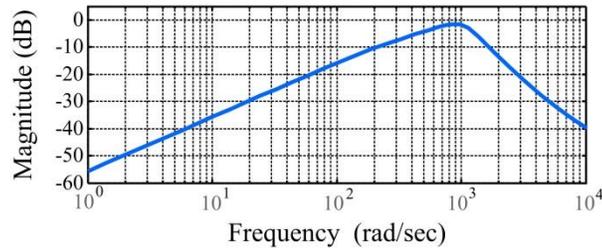


Fig. 7. Bode plot showing the disturbance rejection of the boost converter dc link voltage loop

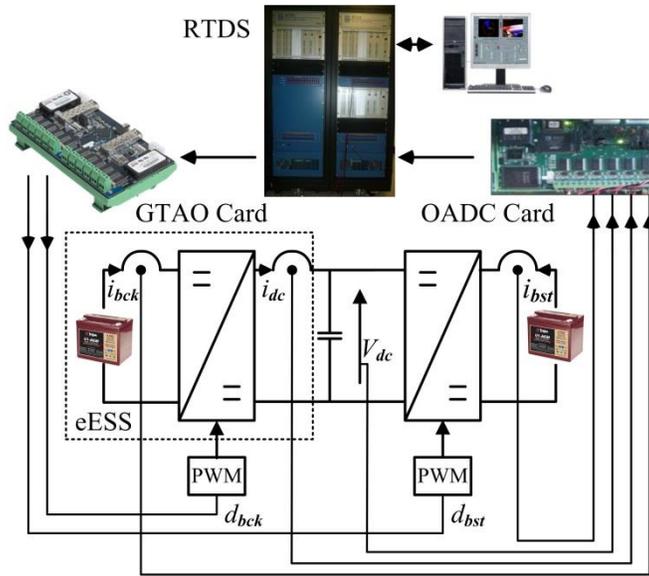


Fig. 8: Schematic diagram of the test system showing the RTDSTM, interface cards and the experimental rig.

The current fed by the eESS into the dc link i_{dc} is also measured, filtered and fed back to the RTDSTM. This signal is used to couple the eESS to the system model. In practice, i_{dc} will be a pulsed current at the PWM carrier frequency. Feeding back such a waveform is difficult and can

lead to significant distortion. As the aim of the system is to examine the response of the energy storage element, it is opted to filter the waveform to facilitate implementation and concentrate on the power transfer, as shown in Fig. 9. The same time constant as for the other filters is used. HIL operation is achieved by driving the eESS from the reference power transfer P_{net}^* at the model PoC and forcing the scaled version of the actual i_{dc} (i_{DC}^* in Fig. 9) into the model BESS interface converter dc link. A controlled voltage source in series with a resistance, connected across the interface converter dc link, is used to inject the current, as shown in the bold part of Fig. 9. A PI controller is used to generate the reference for the controlled voltage source such that the desired current i_{DC}^* flows into the interface converter dc link. The converter dc link voltage V_{DC} is fed forward to the reference of the controlled voltage source.

Both the simulated BESS interface converter– and the experimental rig– dc link voltages are considered to be well controlled by the respective controllers. The voltages are then assumed constant and are hence operated independently. For conditions where the BESS interface converter dc link voltage V_{DC} is expected to change, V_{dc}^* can be set to follow the (scaled) converter dc link voltage variation. This is not implemented for this work.

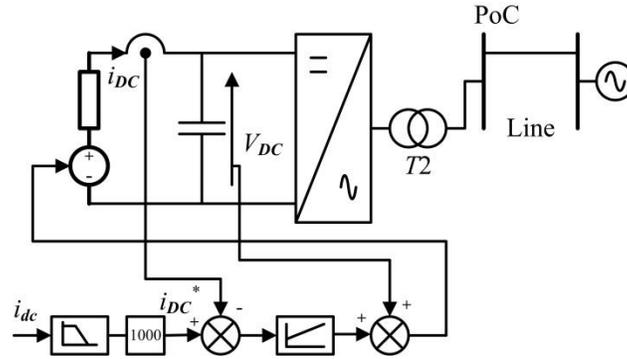


Fig. 9: Coupling of the eESS dc link current into the system model

3.6 Accuracy

An analysis of the accuracy of the proposed reduced scale HIL simulation methodology is now carried out in a similar way to [30]. The eESSs receive a duty cycle signal from the RTDS™ to drive the converters. The current response of the primary eESS is then fed back to influence the simulation. The main factors affecting the accuracy are the following: i) delay and

noise in the analog-to-digital and digital-to-analog converters; ii) filtering of the i_{dc} waveform; and iii) the dynamic performance of the secondary eESS.

The signals exchanged between the eESS and the RTDS™ are scaled to span most of the $\pm 10V$ input range such that the signal to noise ratio is kept high. The OADC and GTA0 have conversion times of $4\mu s$ and $1\mu s$ respectively. The respective delays are then very small and can be neglected. As explained previously, the captured i_{dc} current waveform is low pass filtered before being fed back to the RTDS™. The filter time constant of $0.16ms$ provides a sufficient separation from the spectrum of the wind variation resulting in a negligible effect. The main function of the secondary eESS is to absorb/supply power from/to the eESS as required. This is obtained by controlling the experimental rig dc link voltage. The dynamics of the outer voltage controller affects this power transfer. Using current mode control allowed the achievement of a suitable bandwidth. It can be concluded that it is the performance of the secondary eESS that has the major impact on the accuracy of the HIL simulation and it can be directly set through the controllers.

4 RESULTS

This section presents the performance of the proposed HIL simulation. Real wind speed data is used to drive the simulation runs, and the system is first simulated using a BESS model. The eESS is then coupled to the RTDS™ and the reduced-scale HIL simulation is conducted. The simulation is first verified against the software model and then the results are examined in detail for practical effects not visible in software models. For both cases a constant P_{net}^* reference of $0.6pu$ is set. This is chosen as an approximate average of the wind output power P_{wo} during the considered time period and is not intended to reflect an optimal setting.

4.1 Simulation Results

A hypothetical battery bank, consisting of a combination of the actual 12V battery in use, is considered. It is composed of 1000 strings of 51 batteries each, connected in parallel. This brings the nominal voltage to 612V and the bank resistance to 0.002Ω . It is noted that the considered 1000 strings are not intended as an optimal battery bank configuration but to facilitate upscaling between the test rig and the model currents as indicated in Section 3.2. Since it is not

the intention of this work to tune the battery model, but to replace the model with the actual battery in the simulation, a simpler model is used. This allows ideal behavior of the BESS, which is then used as a benchmark for the HIL simulation. The battery bank open circuit voltage is modeled as a linear function of the extracted charge, based on the open circuit voltage characteristics in [38], and the resistance is assumed constant.

The performance of the system in maintaining a constant net power transfer to the grid is shown in Fig. 10. The upper plot shows the wind speed while the second plot shows the wind output power P_{wo} , the reference grid power P_{net}^* and the net grid power P_{net} . The error between P_{net}^* and P_{net} is shown in the third plot. The chosen wind sample contains a number of steep variations that lead to fluctuations in P_{wo} from circa 0.4pu to circa 0.85pu. It can be observed that P_{net} follows the reference, with the error kept centred around zero and within ± 0.05 pu.

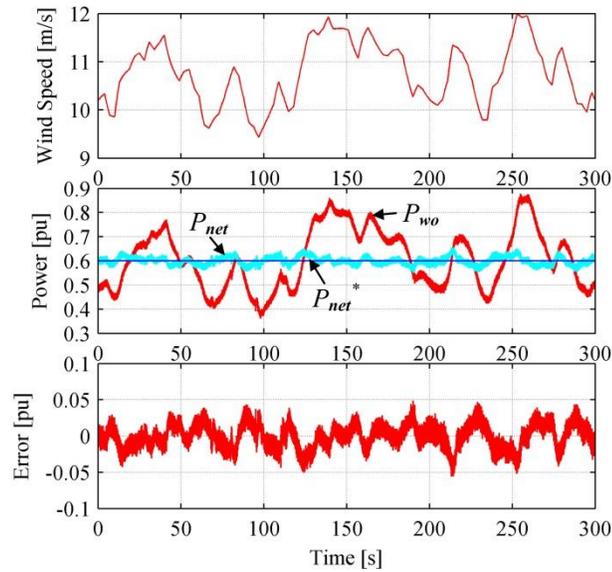


Fig. 10: Simulation test of wind output power smoothing using BESS: 1st plot – wind speed; 2nd plot – output powers P_{wo} , P_{net}^* and P_{net} and 3rd plot – error between P_{net}^* and P_{net} .

The performance of the modelled BESS and its interface converter is shown in Fig. 11. The interface converter power flow P_{so} at the PoC is shown in the upper plot. This basically follows the difference between P_{wo} and P_{net}^* . The corresponding battery bank current i_{bck} and the current at the output of the bidirectional buck converter i_{DC} are shown in the second plot. The interface converter dc link voltage is shown in the bottom plot. The i_{DC} and i_{bck} currents are seen to follow each other very closely, due to the ideal operation of the modeled dc-dc converter. The currents

follow the shape of P_{so} but with a positive offset. Such offset represents the losses in the modeled BESS interface converter. The voltage V_{DC} is seen to be well controlled at 1.0 pu by the respective controller.

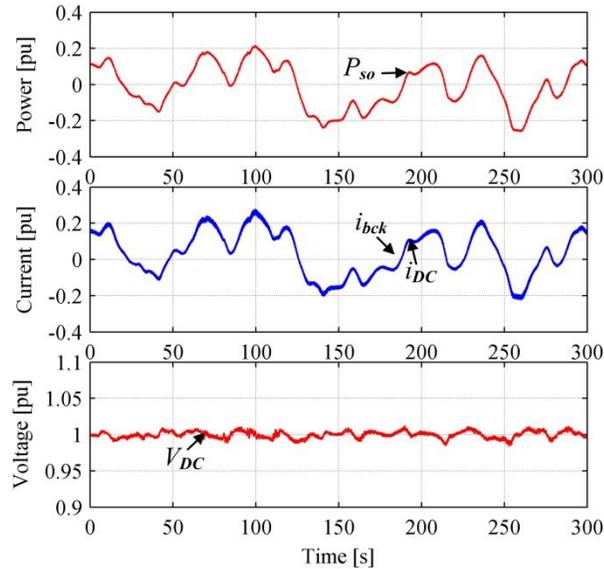


Fig. 11: Simulated performance of BESS and its interface converter in wind output power smoothing: 1st plot – interface converter output power P_{so} , 2nd plot – currents i_{bck} and i_{DC} and 3rd plot – modeled interface converter DC link voltage V_{DC} .

4.2 Experimental Results

The experimental rig is now interfaced to the system model and the measured dc link current (i_{dc}) is fed back, scaled and forced as i_{DC} into the model as shown in Fig. 9. The tuning of the eESS outer power controller is set identical to that of the simulation case. The experimental system performance is shown in Fig. 12, where the plots follow the same order as for Fig. 7. The same wind data as for the simulation test is used, however it is shifted in time as the 300s sample is continuously looped. It can be observed that the obtained performance is similar to that achieved in simulation with the error still centred around zero and within the ± 0.05 pu band. This means that the eBESS could provide the requested power with the required dynamics. Also, maintaining the error in the same band confirms that the proposed HIL methodology does not degrade the system performance hence making it effective.

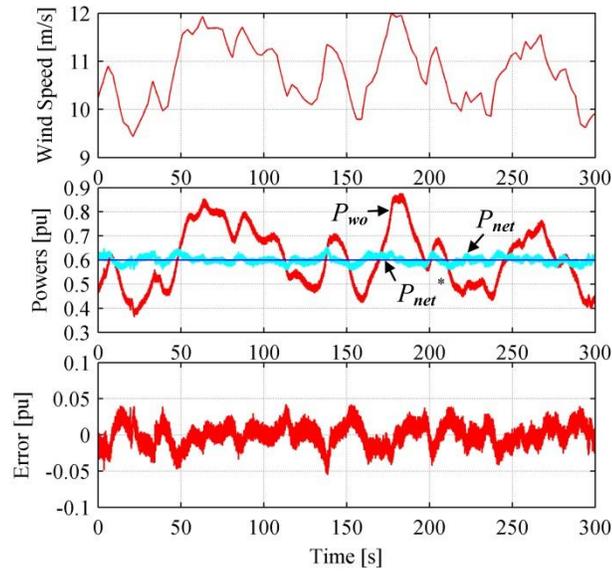


Fig. 12: HIL simulation of wind output power smoothing using AGM VRLA battery: 1st plot – wind speed; 2nd plot – output powers P_{wo} , P_{net}^* and P_{net} and 3rd plot – error between P_{net}^* and P_{net} .

The actual performance of the eBESS is shown in Fig. 13 and 14. Fig. 10 shows the performance of the battery, where the upper plot shows the terminal voltage and the lower plot shows the reference (i_{bck}^*) – and actual (i_{bck}) battery currents. The battery terminal voltage is seen to change with the variation in the current. As expected, the change is seen to be more involved than that predicted by the simpler battery model used for the simulation but it is not significantly high to influence the operation of the inner eBESS current controller. The current i_{bck} is seen to follow i_{bck}^* very closely. This reflects the set high bandwidth for the current controller.

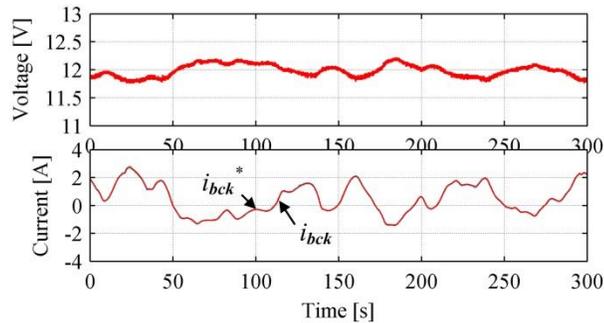


Fig. 13: Performance of the AGM VRLA battery in the HIL simulation: 1st plot –battery terminal voltage and 2nd plot – battery currents i_{bck}^* and i_{bck} .

Fig. 14 shows the performance of the eBESS bidirectional dc–dc converter. The first plot shows the BESS interface converter power flow at the PoC P_{so} . As for the simulation case, this reflects the difference between P_{wo} and P_{net}^* . The second plot shows the currents i_{bck} and i_{dc} expressed in pu. Contrary to the simulation case, the two currents do not overlap due to the non–ideal behavior of the experimental dc–dc converter. The control system effectively changes the duty cycle to overcome the effects of device voltage drops and the losses in the converter, which are mostly conduction losses in this case due to the low operating voltage of the converter. It can be observed that when the eBESS is supplying power, i_{bck} is higher than i_{dc} and vice versa when the eBESS absorbs power from the dc link due to the conduction losses in the converter. These are seen to depend on the magnitude of the current. The losses are pronounced here due to the use of a high voltage IGBTs. This is done intentionally such that these can be scaled to approximately the actual conduction losses of the full scale converter. As for the simulation case, the currents follow the shape of P_{STAT} but with a positive offset, reflecting the losses in the modeled interface converter. The third plot shows the dc link voltage V_{dc} of the eBESS. Similar to the simulated V_{DC} shown in Fig. 8, the experimental V_{dc} is tightly controlled at 1pu by the bidirectional boost converter. This confirms that it was not necessary for these tests to feedback the BESS interface converter dc link voltage to the experimental rig.

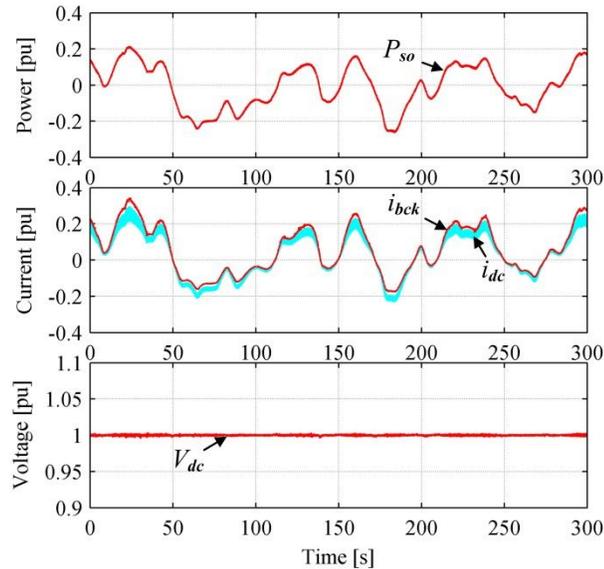


Fig. 14: Performance of the dc–dc converter in the HIL simulation: 1st plot –modeled BESS interface converter power P_{so} ; 2nd plot – currents i_{bck} and i_{dc} and 3rd plot – DC link voltage V_{dc} .

The measured i_{dc} is scaled and forced into the dc link of the modeled BESS interface converter. The reference i_{DC}^* and the actual i_{DC} currents are shown in . It can be observed that the coupling between the hardware and the model allows the injected current to follow the reference tightly, hence making the HIL experiment effective.

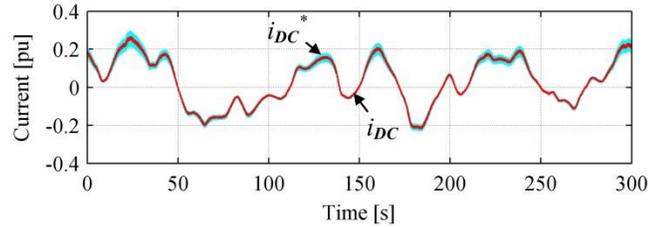


Fig. 15: The eESS dc link current coupled into the BESS interface converter model: reference current i_{DC}^* and interface converter model current i_{DC} .

5 CONCLUSION

This paper proposed a reduced-scale HIL simulation for evaluating the performance of batteries and supercapacitors in renewable energy applications. An experimental test rig consisting of an eESS, incorporating both the energy storage element and the dc-dc converter, and a secondary eESS for loading the primary eESS, was proposed. The experimental rig was controlled through the RTDS™ and the eESS current response was captured and fed back to the simulation model. The accuracy of the HIL simulation was seen to be dependent on the dynamics of the experimental rig dc voltage controller, which can be directly set. The selected control structure allowed the HIL simulation output power P_{net} to be maintained in the same band as for the ideal simulation case.

The proposed setup is intended to replace the use of more complex energy storage element models in ESS simulations. It allows close examination of the behavior of the storage element, the dc-dc converter and the ESS. The performance of different control structures can also be easily tested. The contributions of this paper can be summarized as follows:

- A scalable, reduced-scale HIL simulation was proposed for test of ESS under realistic conditions relieving the need of specifying complex models for the energy storage elements;
- A test rig capable of bidirectional power flow for emulating both the storage element and the power converter was proposed;

- The design, control and implementation of the reduced–scale HIL simulation were detailed; and
- Experimental results showing the effectiveness of the proposed HIL simulation were shown.

It is reiterated that the presented reduced–scale HIL simulation serves as an intermediary step before the implementation of the full hardware. Nonetheless, scale models allow more understanding of the system behavior and can be used to examine non–idealities of the real system. In this paper, the dc–dc converter conduction losses were considered through the use of high voltage IGBTs. The proposed test rig can be also be appropriately up scaled to allow emulation of different effects that might be expected in the full scale hardware, for example unbalance between the strings forming the storage element. In this way, extensive knowledge of the system can be gained through the proposed HIL simulation.

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