Modelling, Simulation and Real time Implementation of A Three Phase AC to AC Matrix Converter

Narayanaswamy P.R. Iyer, B.Sc(Engg); M.Sc(Engg); M.E.(UTS)

This thesis is presented for the Degree of Doctor of Philosophy of Curtin University

February 2012
Dedicated to the
Loving Memory of my Parents
Late Prof. P.K. Ramanatha Iyer
and
Late Smt. P.N. Kavery Ammal
Declaration

To the best of my knowledge and belief this thesis contains no material previously published by any other person except where due acknowledgment has been made.

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university.

Signature: P.R. Narayana Swamy

Date: October 2011
ACKNOWLEDGEMENT

This research work started when I enrolled as a full time doctoral research candidate at the School of Electrical and Information Engineering, University of Sydney, NSW, Australia in July 2008. Dr. Vassilios Agelidis, the then Energy Australia chair in Electrical Power Engineering, School of Electrical and I.E., University of Sydney, NSW was my supervisor. Although initially things were moving alright, at a later stage he expressed inability to supervise my research work, went on leave from around February 2010 and later resigned and left the University of Sydney, NSW around July 2010. Since then I had been advised by the Head of School and also by the Postgraduate coordinator at the School of Electrical and I.E., University of Sydney, NSW to find another supervisor within the same school or if that was not possible, to find a supervisor in an University elsewhere within Australia and transfer my research work and fellowship to that University where I am given permission to. In the School of Electrical and I.E., University of Sydney, NSW, no other faculty members were interested to supervise my research work.

Finally I was able to get financial support and supervision at Curtin University of Technology, Perth, WA and permission to transfer my research work and fellowship from the University of Sydney, NSW and continue here further on the same research topic for the remaining period of my research degree candidature. I am grateful to Dr. Chem V. Nayar, Professor, Department of Electrical and Computer Engineering, Curtin University of Technology, Perth, WA for expressing support and supervision to continue my research work here in which I was formerly working at the University of Sydney, NSW. I am also sincerely thankful to Dr. Sumedha Rajakaruna, Senior Lecturer, Department of Electrical and Computer Engineering, Curtin University of Technology, Perth, WA and cosupervisor, for his support during the period of my research degree candidature here. Many sincere thanks to Dr. Kevin Fynn, Head of the School of Electrical Engineering and Computing, Curtin University of Technology, Perth, WA for his support and cooperation and chairing my research candidacy session.

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ABSTRACT

Matrix converters (MCs) are essentially forced commutated cycloconverters with inherent four quadrant operation consisting of a matrix of bidirectional switches such that there is a switch for each possible connection between the input and output lines. Matrix converter directly converts the AC input voltage at any given frequency to AC output voltage with arbitrary amplitude at any unrestricted frequency without the need for a dc link capacitor storage element at the input side.

The introduction of bidirectional switches using power transistors and IGBTs made easy realization of the matrix converter. The real development of the matrix converter starts with the work of Venturini and Alesina who proposed a mathematical analysis and introduced the Low-Frequency Modulation Matrix concept to describe the low frequency behavior of the matrix converter [1-3]. In this, the output voltages are obtained by multiplication of the modulation matrix or transfer matrix with the input voltages. One of the essential requirements for switching three phase AC to three phase AC MC is that two or more bidirectional switches connected to any one output phase should NOT be closed simultaneously, as this will cause dangerously high short circuice current. Similarly any one bidirectional switch connected to each output phase should remain closed to provide a current path with inductive load.

This thesis mainly provides an account of the three phase AC to three phase AC MC modelling concept with SIMULINK software using fundamental Venturini and Optimum Venturini modulation algorithm [1-8], advanced modulation algorithm such as that proposed by Sunter-Clare [11-12] and by Ned Mohan [13-14, 16-17], application of these algorithms for the Vector control of three phase Induction Motor (IM) drive [15], real time hardware in the loop simulation [51,54-55] for a three phase AC to single phase AC MC, three phase AC to three phase AC Multilevel MC (MMC) with three [18-19] and six flying capacitors per output phase using PSCAD software (as SIMULINK started shooting trouble), Indirect (ISVM) [25-30] and Direct (DASVM, DSSVM, CZASVM) [31-38] Space Vector Modulation, newly discovered dual programmable AC to DC rectifier concept using three phase AC to three phase AC MC [43-45], Delta-Sigma Modulated MC [46-49] and single phase AC to three phase AC MC [50]. In addition a novel concept of a single phase / three phase AC to single phase / three phase AC converter using a DC link, complementary N and P MOSFETs and IGBTs is presented. A chapter on model verification is also presented where selected SIMULINK models from various chapters have been verified by using either PSCAD or PSIM software. An appendix on PIC microcontroller PIC16F84A application to saw-tooth carrier waveform generation and switching three phase AC to three phase AC converters using a DC link is added. Another appendix on speed control and brake by plugging of three phase induction motor fed by matrix converter is presented. List of publications from this thesis is presented on third appendix.
LIST OF ABBREVIATIONS

Symbols:

A,B,C Input phase
a,b,c Output phase
C Capacitor
Cl Filter capacitor
D damping constant
f Frequency
fc Carrier frequency
fo Output frequency
fsw Switching Frequency
i Instantaneous Current
io Instantaneous Output Current
J Moment of Inertia
k Modulation index
kp, ki Proportional and Integral constant
L Inductor
Lf Filter inductor
M Modulation Function
P Number of Poles
q Modulation Index
R Resistance
RL Load resistance
S Switch position or Switch Function
SI, S1 Input Current Sector
SV, SV Output Voltage Sector
T Period
Tc Carrier period
Tem Electromagnetic torque
Ts Sample time
Tsw Switching period
v Instantaneous voltage
Vdc DC Link Voltage
vi Instantaneous input voltage
Vim Maximum line to neutral input Voltage
vo Instantaneous output voltage
Vsaw Saw-tooth carrier Voltage
Vtri Triangle Carrier Voltage
\( \delta, d \) Duty-cycle or Duty-ratio
\( \lambda \) Flux linkage
\( \sigma \) Leakage factor
\( \phi_i \) Input power factor angle
\( \phi_o \) Output power factor angle
\( \omega_i \) Input angular frequency
\( \omega_o \) Output angular frequency

**Suffix:**

\( a,b,c \) Output phase quantities
\( A,B,C \) Input phase quantities
\( d,q \) \( d \)-axis and \( q \)-axis quantities
\( i \) Input
\( l \) Leakage
\( m \) Mutual
\( o \) Output
\( r \) Rotor quantities
\( s \) Stator quantities
\( c \) Carrier
\( \text{sw} \) Switching

**Superfix:**

\( 0 \) Zero switching configuration
\( \text{I, II, III, IV} \) Four Switching configurations

**Acronym:**

AC Alternating current
ASVM Asymmetrical Space Vector Modulation
CMC Conventional Matrix Converter
CZASVM Centre Zero Asymmetrical Space Vector Modulation
DASVM Direct Asymmetrical Space Vector Modulation
DC Direct current
DSVM Direct Space Vector Modulation
FC Flying Capacitor
HEV Hybrid Electric Vehicle
HIL Hardware in the Loop
IGBT Insulated Gate Bipolar Transistor
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<td>IM</td>
<td>Induction Motor</td>
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<tr>
<td>ISVM</td>
<td>Indirect Space Vector Modulation</td>
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<tr>
<td>KVL</td>
<td>Kirchhoff's Voltage Law</td>
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<td>MC</td>
<td>Matrix Converter</td>
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<tr>
<td>MMC</td>
<td>Multilevel Matrix Converter</td>
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<tr>
<td>PH1</td>
<td>Single phase</td>
</tr>
<tr>
<td>PH3</td>
<td>Three phase</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
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<tr>
<td>ssf, SSF</td>
<td>Sector Switch Function</td>
</tr>
<tr>
<td>SSVM</td>
<td>Symmetrical Space Vector Modulation</td>
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<tr>
<td>SVM</td>
<td>Space Vector Modulation</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
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<tr>
<td>ZCC</td>
<td>Zero Crossing Comparator</td>
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Chapter I

Introduction

1.1 BACKGROUND: The most desirable features of the power electronic frequency converters are:

a) Simple and Compact Power Circuit.  
b) Variable output voltage magnitude and frequency.  
c) Sinusoidal input and output currents.  
d) Unity Power Factor operation for any type of load.  
e) Regeneration capability.  

Matrix converter (MC) fulfills all these requirements and is the most sought after converter for industrial drives application. Matrix converters are essentially forced commutated cycloconverters with inherent four quadrant operation consisting of a matrix of bidirectional switches such that there is a switch for each possible connection between the input and output lines. Matrix converter directly converts the AC input voltage at any given frequency to AC output voltage with arbitrary amplitude at any unrestricted frequency without the need for a DC link capacitor storage element at the input side.

The early work, prior to the development of Matrix Converter using bidirectional semiconductor switches, was the cycloconverters using thyristors with forced commutation circuits which act as bidirectional switches.  But the power circuit of these thyristor cycloconverters were too bulky and the performance was poor.  The introduction of bidirectional switch using power transistors and IGBTs made easy realization of the matrix converter.  
The real development of the matrix converter starts with the work of Venturini and Alesina who proposed a mathematical analysis and introduced the Low-Frequency Modulation Matrix concept to describe the low frequency behavior of the matrix converter [1-3].  In this, the output voltages are obtained by multiplication of the modulation matrix or transfer matrix with the input voltages.

One limitation of the matrix converter is that the maximum output voltage available is limited to 86.6 % of the input voltage in the linear modulation range.  

As mentioned, it is the development of the bidirectional switches using semiconductor components that makes matrix converter really attractive.  Although number of topologies for bidirectional switches are available, the common emitter IGBT topology is used here in this thesis work.  Some of the IGBT topologies used as bidirectional switches are shown in Fig. 1.1.  These topologies are respectively a) Diode-Embedded  
b) Common-Emitter  
c) Common-Collector  
d) Antiparallel in series with Diodes and e) Reverse Blocking or R-B IGBT.

The correct method of applying gate pulse to a common-emitter IGBT bidirectional switch is shown in Fig. 1.2(A).  The sinusoidal voltage input, the pulse width modulated output voltage across the load and the gate switching pulses are shown in Fig. 1.2(B), (C) and (D) respectively.  

A three phase AC to three phase AC MC consists of nine bidirectional switches (eighteen IGBTs each with a diode in parallel as in Fig. 1.1(b)).  The topology of the three phase AC to three phase AC MC is shown in Fig. 1.3.  The three phase input voltage terminals are marked A, B and C and the corresponding three phase AC output voltage terminals are marked a, b and c respectively.  The bidirectional switches are
Chapter I: Introduction

\[ \text{(a) DIODE EMBEDDED} \]

\[ \text{(b) COMMON EMITTER} \]

\[ \text{(c) COMMON COLLECTOR} \]

\[ \text{(d) TWO ANTIPARALLEL IGBTs IN SERIES WITH DIODES} \]

\[ \text{(e) REVERSE BLOCKING IGBTs OR RB-IGBTs} \]

FIG. 1.1: BIDIRECTIONAL SWITCH TOPOLOGY

FIG. 1.2: CORRECT METHOD OF APPLYING GATE PULSE TO A BIDIRECTIONAL SWITCH

represented as $S_k$ where $K \in \{A, B, C\}$ and $j \in \{a, b, c\}$ respectively. Thus a three phase AC to three phase AC MC can be represented as $3 \times 3$ MC. A $3 \times 3$ MC has twenty seven switching combinations as shown in Table 1.1 below.

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<th>II-b</th>
<th>II-c</th>
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<td>I A A C B C vAB vBC vCA L a b k 1 0 0 1 0 0 1</td>
<td>1 0 0 0 1 0 0</td>
<td>0 0 0 1 0 0 1</td>
<td>0 0 0 1 0 0 1</td>
</tr>
<tr>
<td>II A A C B C vAB vBC vCA L a b k 1 0 1 0 0 0 1</td>
<td>1 0 0 0 1 0 0</td>
<td>0 0 0 1 0 0 1</td>
<td>0 0 0 1 0 0 1</td>
</tr>
<tr>
<td>III A A C B C vAB vBC vCA L a b k 1 0 1 0 0 0 1</td>
<td>1 0 0 0 1 0 0</td>
<td>0 0 0 1 0 0 1</td>
<td>0 0 0 1 0 0 1</td>
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</tbody>
</table>

In Table 1.1, corresponding to Group II-c, C C A means that the input phase C is connected to output phase a and b and input phase A is connected to output phase c. Referring to Fig.1.3, output phase to phase voltage $v_{AB}$, $v_{BC}$ and $v_{CA}$ are respectively zero (VCC), $V_{CA}$ and $V_{AC}$ or $V_{CA}$. Also input current $i_A$, $i_B$ and $i_C$ are the load currents $ic$, 0 and $-ic$ respectively. This is illustrated diagrammatically for Group II-a of Table 1.1 below:
The position of the nine bidirectional switches corresponding to Group II-a in Table 1.1 is shown in Fig. 1.4. The switches SAa, SCb and SCc are closed and all others are open. Applying Kirchoff’s law to Fig. 1.4, the following set of equations will result:

\[
\begin{align*}
    v_{ab} &= v_{AC} = -v_{CA} \\
    v_{bc} &= 0 \\
    v_{ca} &= v_{CA} \\
    i_A &= i_a \\
    i_B &= 0 \\
    i_C &= -i_a
\end{align*}
\]  

Also in Fig. 1.4, assigning closed switch as logic 1 and open switch as logic 0, switches SAa to SCc in order can be assigned the position: 1 0 0 0 0 1 0 0 1.

Referring to Fig. 1.3, in terms of the switch position the output voltage corresponding to phase a and the input current corresponding to phase A can be expressed as follows:

\[
\begin{align*}
    v_a &= S_{Aa} \cdot v_A + S_{Ba} \cdot v_B + S_{Ca} \cdot v_C \\
    i_A &= S_{Aa} \cdot i_a + S_{Ab} \cdot i_b + S_{Ac} \cdot i_c
\end{align*}
\]  

One of the essential requirements for switching three phase AC to three phase AC MC is that two or more bidirectional switches connected to any one output phase should NOT be closed simultaneously, as this will cause dangerously high short circuit current. Similarly any one bidirectional switch connected to each output phase should remain closed to provide a current path with inductive load. This necessitates saw-tooth carrier signal to be compared with modulation functions for each of the bidirectional switches in a comparator and the resulting output is given to logic gates in such a manner that the gate pulses to the three bidirectional switches connected to any one output phase occur in sequence or one after the other.

1.2 OBJECTIVE: The following are the objective of this thesis:

- Develop models for MC
  - To develop models for three phase AC to three phase AC Conventional MC topology connected to R-L load and Vector Controlled Induction Motor drive, using Venturini, Optimum Venturini and other Advanced Modulation algorithms.
  - To develop models for three phase AC to three phase AC Multilevel MC topology with three and six Flying capacitors per output phase, using Venturini algorithm.
  - To develop models for Direct and Indirect Space Vector Modulated three phase AC to three phase AC MC topology.
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-To develop model for the newly discovered Dual Programmable AC to DC Rectifier using Three Phase AC to Three Phase AC MC topology.
-To develop models for three phase AC to three phase AC MC when switching is carried out by sample time based modulation technique also known as Delta-Sigma Modulation.
-To develop model for single phase AC to three phase AC MC topology.
-To develop models for a single phase/three phase AC to single phase/three phase AC converter topology using a DC link voltage.

Hardware implementation
-To implement in real time, a three phase AC to single phase AC MC using dSPACE DS1104 Hardware Controller Board.

Explore applications
-Applications of three phase AC to three phase AC MC for Industrial AC Drives [6-7, 14, 40-41, 56], Wind Energy Conversion [57-59], Aircraft Control Applications [60-61] and Railway Electric Traction Power Supply [62] are already reported in the literature. In this thesis additional applications for the speed control and brake by plugging of two separately excited DC motors fed by the newly discovered Dual Programmable AC to DC Rectifier suitable for Hybrid Electric Vehicle and Electric traction is presented. In addition another application of three phase AC to three phase AC MC for the speed control and brake by plugging or by reversing the phase sequence of three phase Induction Motor is presented.

1.3 RESEARCH METHODOLOGY: The following are the research methods used:

- Develop Models for MC
  - Software approach
    - SIMULINK [51]
    - PSIM [52]
    - PSCAD [53]
  - Hardware implementation
    - Real time Hardware using dSPACE [54]

1.4 THESIS OUTLINE AND NOVELTY: This thesis mainly provides an account of the three phase AC to three phase AC MC modelling using the software SIMULINK. Unless specified otherwise the term model in this thesis refers to SIMULINK model. The outline and novelty of each chapter in this thesis is discussed below:

Many literature references have been referred for developing the model presented in this thesis. The literature review in Chapter II provides the brief account of the work and the literatures referred relevant to the particular chapter.

The three phase AC to three phase AC matrix converter low frequency modulation matrix concept was first developed by Alesina and Venturini [1-3]. Chapter III presents an overview of this Venturini
Chapter I: Introduction

and Optimum Venturini modulation algorithm and models of three phase AC to three phase AC MC based on these algorithms. An appendix is provided in this chapter to prove that Venturini algorithm works well with both three phase sine wave and cosine wave input voltages.

Advanced Modulation algorithm for three phase AC to three phase AC MC such as that proposed by Sunter-Clare [11-12] and that by Ned Mohan [13-14, 16-17] is presented in Chapter IV along with model simulation results. An appendix is provided in this chapter to prove the validity of Advanced Modulation algorithm proposed by Ned Mohan for both three phase sine wave and cosine wave input voltages.

Vector controlled three phase Induction Motor (IM) drive is reported in the literature [15]. Based on this reference, model for three phase AC to three phase AC MC driving a vector controlled IM drive presented in Chapter V using all of the above mentioned algorithms with simulation results. An appendix is provided to determine the PI controller parameters required for vector control using MATLAB source code.

Real time Hardware-in-the-Loop (HIL) simulation using SIMULINK model in conjunction with dSPACE modules and interfacing through a dSPACE ds1104 hardware controller board [51, 53-55] to the real three phase AC to single phase AC MC assembled using hardware IGBT components in the laboratory is presented in Chapter VI. Here a three phase square wave input voltage from a three phase inverter is used as the input and a single phase square wave output voltage is obtained from the above MC. The model uses Venturini algorithm for generating modulation functions to generate gate pulses for the bidirectional switches. A Hewlett-Packard saw-tooth carrier generator interfaced to the ADC input of the ds1104 hardware controller board is used to compare the modulation functions and generate gate pulses using logic circuit blocks in SIMULINK. This gate pulses from SIMULINK logic circuit block is interfaced to DAC outputs of ds1104 hardware controller board which is used for applying gate pulses to the MC. Real time simulation results are compared with model simulation results.

Based on three phase AC to three phase AC Multilevel Matrix Converter (MMC) with two and three Flying capacitors (FCs) [18-19], models have been developed using PSCAD [53] for three phase AC to three phase AC MMC with three and six FC per output phase. These are presented in Chapter VII. In this case SIMULINK models couldn’t be developed as the model started shooting trouble. The model representation of three phase MMC with three FC using logic sates of the bidirectional switches is a novel feature. The model for three phase MMC with six FC is newly proposed. Simulation results using PSCAD are also presented. An appendix is provided to derive the operation of the three phase MMC with six FC for selected bidirectional switch combinations.

Models for Direct Asymmetrical (ASVM) and Direct Symmetrical (SSVM) Space Vector Modulation [31-38] of three phase AC to three phase AC MC is presented in Chapter VIII. A new Direct
Asymmetrical Centre Zero Space Vector Modulation (CZSVM) is proposed in this chapter. Simulation results are presented. Two appendices, one for calculating output voltage and input current from the state of the bidirectional switches and another for calculating the duty-cycle along the x-y axis are presented.

Indirect Space Vector Modulation (ISVM) [25-30] of three phase AC to three phase AC MC considers that the above MC is equivalent to a three phase AC to DC rectifier and a DC to three phase AC Inverter. Based on this technique model has been developed for three phase AC to three phase AC ISVM MC and are presented with simulation results in Chapter IX. Appendices are provided to derive the various equations and tables presented in this chapter.

Dual fixed AC to DC rectifier using three phase AC to three phase AC MC topology [43-45] is reported in the literature based on which Dual Programmable AC to DC rectifier using the above MC topology is presented in Chapter X. This Dual Programmable AC to DC rectifier is an outcome as a result of "Newtonian thought" by the author of this thesis to the first sentence in the first paragraph under the subheading "Using a Matrix Converter as an AC/DC Rectifier" in page 356 of reference 43 which reads thus: "To operate a matrix converter as an ac-dc rectifier, the output frequency is set to zero, and the output voltage phase angle is set to $30^\circ$. The "Newtonian thought" made by the author of this thesis is "Why 30 degree phase angle for output phase voltage; why NOT some other value"? This is considered by the author of this thesis as a fantastic breakthrough discovery and a greatest achievement in this research thesis having enormous industrial applications. Models have been developed for the dual programmable AC to DC rectifier using the above MC topology and simulation results are presented. Derivations for the dual DC output voltage magnitude have been presented using phasor diagrams which is an original contribution in this thesis. The application of this Dual Programmable AC to DC rectifier driving separately excited DC motor and Permanent Magnet DC motor suitable for Hybrid Electric Vehicle (HEVs) and Electric Traction is highlighted. At this stage, the author of this thesis is only able to dream future generation of at least one model of HEV and Bullet electric train/normal electric train running on the roadways and railways based on the method developed in Chapter X of this research thesis. An appendix is provided to derive suitability of the dual programmable AC to DC rectifier using three phase cosine wave input voltages.

Models based on sample time or discrete time based modulation technique also known as Delta-Sigma modulation technique [46-49] is reported in Chapter XI. This models use Z transform approach. Models have been presented for three phase AC to three phase AC MC with Delta-Sigma modulation using both Venturini algorithm and Advanced Modulation algorithm proposed by Ned Mohan for both R-L load and three phase IM load. The Delta-Sigma modulated MC using Advanced modulation algorithm is newly proposed in this thesis. Simulation results are presented.

Single phase AC to three phase AC MC topology, without the need for rectification and inversion, is reported in the literature [50] based on which model has been developed for single phase AC to three
Chapter I: Introduction

A novel AC to AC converter using a DC link is a new idea or a new method developed by the author of this thesis. Here models and simulation results for both single phase/three phase AC voltages at supply frequency to single phase/three phase AC output voltages with a variable frequency and magnitude is presented using the software PSIM [51]. The model essentially consists of N-P MOSFET pairs driven by op.amplifier zero crossing comparator to produce single phase / three phase square wave AC output voltage at supply frequency which are given as input to IGBT bidirectional switches driven by counter and Multiplexer to produce variable frequency output voltage. Pulse Width Modulation is achieved by conventional technique. The model and simulation results are presented in Chapter XIII. An appendix is provided with simulation results to explain the operation of supply frequency N-P MOSFET inverter and that of the variable output frequency inverter using IGBT bidirectional switches.

Finally the selected SIMULINK models presented in various chapters of this thesis have been verified for performance, by simulation using either PSIM or PSCAD software. This verification report is presented in Chapter XIV of this thesis. This model verification may be considered as a written thesis defence.

Chapter XV presents the summary of contributions and conclusions derived from this research thesis work.

Appendix I presents the PIC microcontroller PIC16F84A approach for generating a 2 kHz saw-tooth carrier generator to replace the one discussed using IC NE555 in Chapter X and another gate drive for IGBT bidirectional switches in the three phase AC to three phase AC converter using a DC link presented in Chapter XIII, to replace the one presented using modulo six counter and multiplexer.

Appendix II presents the speed control and brake by plugging of three phase IM fed by matrix converter. This novel method of speed control and braking using the model implemented in real time using dSAPCE makes it suitable for Hybrid Electric Vehicles and Electric traction.

Appendix III presents the list of publications from this thesis work.
Chapter II

Literature Review

2.1 INTRODUCTION: This chapter provides the review of literature relating to modelling, simulation and experimental verification of Three Phase AC to AC Matrix Converter. The literature referred for this research work is given under References. Detailed chapter by chapter reference made is given below:

2.2 VENTURINI AND OPTIMUM VENTURINI MODULATION ALGORITHM: Chapter III deals with the modelling of MC using Venturini and Optimum Venturini Modulation algorithm [1-5]. The low frequency modulation matrix m(t) is defined and the matrix converter behaviour is modelled as 
\[ v_o(t) = m(t) * v_i(t) \] 
and 
\[ i_i(t) = m^T(t) * i_o(t) \]
where \( v_o(t), v_i(t), i_i(t) \) and \( i_o(t) \) are the output voltage, input voltage, input current and output current respectively. The solution of m(t) gives the nine modulation functions for the MC, given the angular frequency \( \omega_i \) and \( \omega_o \) of the three phase cosine wave input, output voltages and modulation index q [1-5]. The general solution is termed Venturini First method and the solution assuming Unity Input Phase Displacement Factor is termed Venturini second method in this thesis. In optimum Venturini method, the nine modulation functions are presented assuming that the three phase output voltage \( v_o(t) \) contains the normal cosine wave component of voltages at frequency \( \omega_o \) added with third harmonic component of input voltage and from which subtracting third harmonic component of output voltage corresponding to their respective frequencies in appropriate proportions [4-5]. In Chapter III, the models are developed for MC using the Venturini First, Second and Optimum Venturini method, in SIMULINK and the simulation results are presented for R-L load [9-10, 51].

2.3 ADVANCED MODULATION ALGORITHMS: In Chapter IV, modelling of MC in SIMULINK using Advanced modulation algorithms such as proposed by Sunter-Clare [11-12] and that by Ned Mohan is presented [13-14, 16-17]. The Venturini modulation algorithm is suitable for synchronous operation of the input with the output [11]. This approach is unsuitable for closed loop applications where it is required to calculate the duty cycle every sampling period to achieve voltage control in which output frequency is continuously varying with time [11]. To overcome this problem the approach taken is to measure the input voltage at every sampling period and to determine voltage vector magnitude and ratio and position directly [11]. A simplified version of Venturini algorithm is defined in terms of the three phase input and output voltage at each sampling instant [11-12]. This allows the demand voltage ratio, output voltage magnitude and angle to be updated at every sampling period which is a requirement for closed loop control [11-12]. The simplified Venturini algorithm is used to develop the model of the three phase Matrix converter in SIMULINK [11-12, 51].
Chapter II: Literature Review

A novel carrier based modulation technique is used for modelling the three phase AC to three phase AC matrix converter [13-14, 16-17]. This method avoids the use of sector information and look-up table. In this method the output line to neutral voltage $v_a$ of the matrix converter is expressed either in the form $v_a = (3/2).k.Vim\cos(\phi_i)\cos(\omega_o t)$ or in the form $v_a = (3/2).k.Vim\cos(\phi_i)\sin(\omega_o t)$, where $k$ is the modulation index, $Vim$ is the maximum line to neutral input voltage, $\phi_i$ is the input power factor angle and $\omega_o$ is the output angular frequency. Further mathematical manipulations are done so that the duty ratios of the matrix converter switches lie in the range 0 to 1. The control duty ratio signals thus obtained are compared with a triangular carrier signal to obtain the gate pulse for the nine bidirectional switches of the matrix converter. Simulation results using SIMULINK are presented assuming unity input power factor [51].

2.4 VECTOR CONTROLLED THREE PHASE INDUCTION MOTOR DRIVE FED BY MATRIX CONVERTER: In chapter V, vector controlled three phase Induction Motor drive fed by Matrix converter is studied in detail by model simulation [13-15]. SIMULINK software is used for Model development [51]. The proposed scheme uses the carrier-based PWM scheme of MC for generation of PWM gate pulses based on various algorithms such as by Venturini, Sunter-Clare and Ned Mohan [1-8, 11-12, 13-15]. Carrier based Vector control scheme uses two PI controllers, one for the speed control loop and the other for the current control loop. The dq axis model of the three phase induction motor in synchronously rotating reference frame is used. Simulation results are presented.

2.5 HARDWARE IN THE LOOP SIMULATION OF A THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER: In chapter VI, Hardware-in-the-Loop simulation of a three phase AC to single phase AC matrix converter is presented. The dSPACE DS1104 hardware controller board is used for this experiment [54]. The input used is a three phase 50 Hz square wave AC voltage, having a line to neutral RMS voltage of 123 Volts. The single phase AC output voltage has a frequency of 50 Hz. The model is developed in SIMULINK [51]. Venturini algorithm assuming unity input phase displacement factor is used to generate gate pulse for the three bidirectional switches. Both simulation and hardware experimental results are presented.

2.6 MULTILEVEL MATRIX CONVERTER: The modelling and simulation of Three phase AC to three phase AC Multilevel Matrix Converter with three flying capacitors per output phase is presented in Chapter VII [18-19]. Three phase multilevel matrix converters are proposed for reducing the harmonic components of the line to neutral, line to line output voltages and the input current [18-19]. The model equations showing the relation between three phase input and output voltages as well as for input and output currents are presented. Venturini modulation algorithm for bidirectional switches is implemented using two saw-tooth carrier signals out of phase by 180 degrees or $T_{sw}/2$ seconds where $T_{sw}$ is the period of the saw-tooth carrier signal. The model is extended for three phase AC to three phase AC multilevel matrix converter with six flying capacitors per output phase. Simulation results using PSCAD are presented.
2.7 DIRECT SPACE VECTOR MODULATION OF MATRIX CONVERTER: The direct Asymmetrical Space Vector Modulation and Symmetrical Space Vector Modulation (SSVM) for three phase AC to three phase AC Matrix Converter are presented in Chapter VIII [31-35]. The model of the three phase MC using ASVM and SSVM technique is developed in SIMULINK [36-38, 51]. In addition a new Centre Zero ASVM technique is also proposed in this chapter. The space-vector modulation technique, owing to the two degrees of freedom, represents the general solution of the modulation problem of matrix converters. This technique can be considered the best solution for the possibility to achieve the highest voltage transfer ratio and to optimize the switching pattern through a suitable use of the zero voltage vector configurations. This solution has been obtained using the duty-cycle space-vector approach, which consists of a representation of the switch state by space vectors [31-35]. In space vector approach, the input currents and output voltages are represented as space vectors in the complex plane. From 27 switching states, only 21 switching states are used for space vector approach. The eighteen active voltage states are assigned numbers from ±1 to ±9 and the three zero voltage vectors are assigned 01, 02 and 03 [31-35]. These switch states for output voltage and input currents are represented as hexagons in complex plane. With the sector number of output voltage and that for input current, the switch states common to both are noted and tabulated in four switching configurations. The duty cycles for the four switching configurations are derived for a given modulation index and that for zero voltage vector is calculated using the relation that the sum of the duty cycles for the four switching configurations and that for zero voltage vector state is unity [31-35]. Two sets of rules are proposed for these techniques in order to simplify the model implementation. Rules for assigning the zero voltage vector for ASVM, SSVM and CZASVM are proposed. SIMULINK model is developed and the simulation results are presented [36-37].

2.8 INDIRECT SPACE VECTOR MODULATION OF MATRIX CONVERTER: The indirect Space Vector Modulation (ISVM) for three phase AC to three phase AC Matrix Converter is presented in Chapter IX. In the proposed voltage Space Vector PWM control of MCs, the Indirect Transfer Function approach is used where the input AC voltage is first rectified to create a fictitious DC voltage which is then inverted at the required output frequency [25-30]. For low harmonic distortion, the inverter operation is achieved by Space Vector Modulation (SVM) simultaneously with input current SVM for rectification [25-30]. The simultaneous output voltage-input current SVM algorithm is reviewed here and the model of the 3 X 3 MC is derived based on this algorithm using SIMULINK. The simulation results are presented.

2.9 DUAL PROGRAMMABLE AC TO DC RECTIFIER USING THREE PHASE MATRIX CONVERTER: Three Phase AC to Three Phase AC Matrix Converter based dual AC to DC rectifier is reported in the literature [43-45]. But these reports only indicate that dual DC output voltages with fixed value is possible by setting the desired AC output voltage phase angle leading by 30 degrees and the frequency of output voltage zero in the model [43-44]. Detailed modelling studies using SIMULINK reveals that with the frequency of desired AC output voltage set to zero, as the AC output voltage phase angle is varied from 0 to +π and 0 to –π, dual DC output voltages in multitude of
combinations are possible such as a) Both voltages positive and unequal, b) Both voltages positive and equal, c) Any one voltage zero and the other positive, d) Any one Voltage positive and the other negative with unequal modulus value, e) Any one voltage positive and the other negative with equal modulus value, f) Any one Voltage zero and the other negative, g) Both voltages negative and unequal, h) Both voltages negative and equal. In this chapter, a detailed insight into this discovery is made with a mathematical derivation for the dual DC output voltage magnitude. Theoretical finding is confirmed by SIMULINK model simulation. The model is extended to verify the speed control, acceleration and braking of separately excited DC motors. Applications of this separately excited DC motor and Permanent Magnet DC motor for Hybrid Electric Vehicles and Electric Traction are highlighted.

2.10 DELTA-SIGMA MODULATION OF MATRIX CONVERTER: The chapter XI examines the recently proposed delta-sigma modulation technique for matrix converter [46-49]. A model of the three phase AC to three phase AC matrix converter using delta-sigma modulation technique is developed in SIMULINK [51]. Both Venturini [1-5] as well as advanced modulation algorithm [13-14, 16-17] are used for generating the modulation voltage signals. Simulation is carried out for a given sampling frequency. It is seen from simulation results that voltage harmonic peaks are reduced at integral multiples of sampling frequency [46-48]. The delta-sigma modulation technique can reduce noise peaks in the output voltage as compared to conventional PWM technique and has the advantage of maintaining noise regulation. Also performance of three phase induction motor drive fed by delta-sigma modulated MC using the above two algorithms are presented.

2.11 SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER: For single phase AC to three phase AC power conversion, three phase indirect method is used where the single phase AC is first rectified to DC and this DC link voltage is inverted to AC using three phase inverter. A control and designing method of the capacitance of the compensation capacitor for a direct single phase AC to three phase AC matrix converters with application to a variable speed induction motor is reported in the literature [50]. The amplitude of the compensation capacitor voltage is controlled to absorb the single phase power fluctuation along with the load power. A method is proposed to decide the input side parameters such as the capacitance of the compensation capacitor, considering the input voltage and the power of the IM [50]. A circuit configuration with a compensation capacitor in the input side is introduced which absorbs the fluctuating power due to the single phase AC power. Here the single phase AC source is connected to an LC filter and compensating capacitor [50]. The two nodes of the LC filter and the compensating capacitor end terminals are connected to nine bidirectional switches [50]. Indirect virtual rectifier-inverter analysis is used. Derivations for modulation ratio and output power flow are presented [50]. A method of designing and selecting the compensating capacitor is given in terms of the output phase voltage, output power flow and input frequency [50]. In this chapter a detailed analysis of the single phase AC to three phase AC MC is presented. A model of this single phase AC to three phase AC MC is developed in SIMULINK [51].
Simulation results of the single phase AC to three phase AC MC is presented for both R-L load and three phase IM load.

2.12 A NOVEL AC TO AC CONVERTER USING A DC LINK: A novel method of generating a Pulse Width Modulated Single Phase and Three Phase variable frequency, variable voltage AC from the normal 220 Volts/440 Volts, Single Phase/Three phase 50 Hz AC supply mains using a step down transformer and an intermediate DC link is presented here.

2.13 MODEL VERIFICATION: This chapter provides the verification of models of selected three phase AC to three phase AC Matrix Converter topologies discussed in the previous chapters using either PSIM or PSCAD software [52-53].

2.14 CONCLUSIONS: This chapter provides the summary of contributions and conclusions drawn from the simulation results or performance of the three phase Matrix Converter models discussed in the previous chapters and suggestion for further research work.

2.15 APPENDIX: The first appendix provides the gate drive using PIC microcontroller PIC16F84A to generate 2kHz saw-tooth carrier waveform and also the gate drive for the bidirectional switches in the novel three phase AC to three phase AC converter using a DC link. The second appendix provides the speed control and braking of three phase IM fed by MC, highlighting applications for HEVs. The third appendix provides the list of publications from this thesis.
Chapter III
Modelling of Three Phase Matrix Converters Using Venturini and Optimum Venturini Modulation Algorithms

3.1 INTRODUCTION: Recently considerable interest is shown in the development of AC to AC converters also known as “Matrix Converters” for Adjustable Speed Drive applications [1-8]. Although several topologies for IGBT bidirectional switches have been proposed, the common emitter bidirectional switch topology is used here. The switching of the bidirectional switches in an MC is really complicated. Several algorithms have been proposed for switching the MC bidirectional switches. This chapter presents the model of the three phase AC to three phase AC MC using Venturini and Optimum Venturini modulation algorithms. The model is developed using the software SIMULINK [51]. Simulation results are presented.

3.2 MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER: A three phase AC to three phase AC matrix converter is shown in Fig. 3.1. While operating the Matrix Converter, two essential points must be remembered. The three or any two combination of the bidirectional switches in any one output phase should NOT be closed at the same instant of time [4-5]. Referring to Fig. 3.1, if any two or all of switches SAa, SBa and SCa are closed simultaneously, the input lines are short circuited causing dangerous short circuit currents through the bidirectional switches. Similarly with inductive loads all the three bidirectional switches connected to an output phase should NOT be open simultaneously [4-5]. One switch at least in any output phase must remain closed. Matrix converter directly converts the AC input voltage at any given frequency to AC output voltage with arbitrary amplitude at any unrestricted frequency without the need for a dc link capacitor storage element at the input side. Sinusoidal input and output currents can be obtained with unity

![Diagram of Three Phase Matrix Converter](image-url)
power factor for any load. It has regeneration capability [1-5]. One limitation of the matrix converter is that the maximum output voltage available is limited to 86.6 % of the input voltage in the linear modulation range [4-5].

The introduction of bidirectional switch using power transistors made easy realization of the matrix converter. The real development of the matrix converter starts with the work of Venturini and Alesina who proposed a mathematical analysis and introduced the Low-Frequency Modulation Matrix concept to describe the low frequency behaviour of the matrix converter [1-3]. In this, the output voltages are obtained by multiplication of the modulation matrix or transfer matrix with the input voltages. Models for three phase ac to three phase ac matrix converters using Venturini modulation algorithm is reported [9-10]. These models are developed in SIMULINK [51].

The 3 X 3 matrix converter shown in Fig.3.1 connects the three phase AC source to the three phase load. The switching Function for a 3 X 3 matrix converter can be defined as follows [4-5]:

\[
S_{K_j} = \begin{cases} 
1 & \text{when } S_{K_j} \text{ is closed} \\
0 & \text{when } S_{K_j} \text{ is open} 
\end{cases} \quad (3.1)
\]

\[K \in \{A, B, C\} \text{ and } j \in \{a, b, c\}\]

The above constraint can be expressed in the following form:

\[S_{A_j} + S_{B_j} + S_{C_j} = 1 \quad \text{for } j \in \{a, b, c\} \quad (3.2)\]

With the above restrictions a 3 X 3 matrix converter has 27 possible switching states which are given in Table 1.1 of chapter I [25-30].

The mathematical expression that represents the operation of a three phase AC to three phase AC Matrix Converter (MC) can be expressed as follows [4-5]:

\[
\begin{bmatrix}
    v_a(t) \\
v_b(t) \\
v_c(t)
\end{bmatrix} =
\begin{bmatrix}
    S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\
    S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\
    S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t)
\end{bmatrix} *
\begin{bmatrix}
    v_A(t) \\
v_B(t) \\
v_C(t)
\end{bmatrix} \quad (3.3)
\]

\[
\begin{bmatrix}
    i_A(t) \\
i_B(t) \\
i_C(t)
\end{bmatrix} =
\begin{bmatrix}
    S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\
    S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\
    S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t)
\end{bmatrix}^T *
\begin{bmatrix}
    i_a(t) \\
i_b(t) \\
i_c(t)
\end{bmatrix} \quad (3.4)
\]

where \(v_a, v_b\) and \(v_c\) and \(i_A, i_B\) and \(i_C\) are the output voltages and input currents respectively. To determine the behaviour of the MC at output frequencies well below the switching frequency, a modulation duty cycle can be defined for each switch. The modulation duty cycle \(M_{K_j}\) for the switch \(S_{K_j}\) in Fig.3.1 is defined as in equation 3.5 below.

\[
M_{K_j} = \frac{t_{K_j}}{T_s} \quad (3.5)
\]

\[K \in \{A, B, C\} \text{ and } j \in \{a, b, c\}\]
where \( t_{kj} \) is the on time for the switch \( S_{kj} \) between input phase \( K \in \{ A, B, C \} \) and \( j \in \{ a, b, c \} \) and \( T_s \) is the period of the PWM switching signal or sampling period. In terms of the modulation duty cycle, equations 3.2, 3.3 and 3.4 can be rewritten as given below.

\[
\begin{bmatrix}
    v_A(t) \\
    v_B(t) \\
    v_C(t)
\end{bmatrix} =
\begin{bmatrix}
    M_{AA}(t) & M_{BA}(t) & M_{CA}(t) \\
    M_{AB}(t) & M_{BB}(t) & M_{CB}(t) \\
    M_{AC}(t) & M_{BC}(t) & M_{CC}(t)
\end{bmatrix} \ast
\begin{bmatrix}
    v_A(t) \\
    v_B(t) \\
    v_C(t)
\end{bmatrix}
\]

(3.6)

\[
\begin{bmatrix}
    i_A(t) \\
    i_B(t) \\
    i_C(t)
\end{bmatrix} =
\begin{bmatrix}
    M_{AA}(t) & M_{BA}(t) & M_{CA}(t) \\
    M_{AB}(t) & M_{BB}(t) & M_{CB}(t) \\
    M_{AC}(t) & M_{BC}(t) & M_{CC}(t)
\end{bmatrix} \ast
\begin{bmatrix}
    i_A(t) \\
    i_B(t) \\
    i_C(t)
\end{bmatrix}
\]

\( M_{kj} + M_{kj} + M_{cj} = 1 \) \( j \in \{ a, b, c \} \)

**3.3 VENTURINI AND OPTIMUM VENTURINI MODULATION ALGORITHM:** The modulation problem normally encountered in matrix Converter can be stated as follows:

The input voltages and output currents are given as defined in equation 3.9 and 3.10 below [1-5]:

\[
v_i = \begin{bmatrix}
    v_A \\
    v_B \\
    v_C
\end{bmatrix} = V_{im} \ast \begin{bmatrix}
    \cos(\omega_i t) \\
    \cos(\omega_i t - \frac{2\pi}{3}) \\
    \cos(\omega_i t - \frac{4\pi}{3})
\end{bmatrix}
\]

(3.9)

\[
i_o = \begin{bmatrix}
    i_A \\
    i_B \\
    i_C
\end{bmatrix} = I_{om} \ast \begin{bmatrix}
    \cos(\omega_o t + \varphi_o) \\
    \cos(\omega_o t + \varphi_o - \frac{2\pi}{3}) \\
    \cos(\omega_o t + \varphi_o - \frac{4\pi}{3})
\end{bmatrix}
\]

(3.10)

Where \( \omega_i, \omega_o, \) and \( \varphi_o \) are the input and output angular frequency and output phase displacement angle.

The problem is to find a modulation matrix \( M(t) \) such that equations 3.11 and 3.12 below and the constraint in equation 3.8 are satisfied.

\[
v_o = M(t) \ast v_i = \begin{bmatrix}
    v_A \\
    v_B \\
    v_C
\end{bmatrix} = q \ast V_{im} \ast \begin{bmatrix}
    \cos(\omega_o t + \varphi_o) \\
    \cos(\omega_o t + \varphi_o - \frac{2\pi}{3}) \\
    \cos(\omega_o t + \varphi_o - \frac{4\pi}{3})
\end{bmatrix}
\]

(3.11)

where \( q \ast V_{im} = V_{om} \)

\[
i_i = [M(t)]^T \ast i_o = \begin{bmatrix}
    i_A \\
    i_B \\
    i_C
\end{bmatrix} = \frac{q \ast \cos(\varphi_o)}{\cos(\varphi_i)} \ast I_{om} \ast \begin{bmatrix}
    \cos(\omega_i t + \varphi_i) \\
    \cos(\omega_i t + \varphi_i - \frac{2\pi}{3}) \\
    \cos(\omega_i t + \varphi_i - \frac{4\pi}{3})
\end{bmatrix}
\]

(3.12)

where \( q \) is the voltage transfer ratio, \( \varphi_i \) is the input phase displacement angle. The solution of equations 3.9 to 3.12 can be expressed as in equations 3.13 and 3.14 below for \( \varphi_i = \varphi_o \) and for \( \varphi_i = -\varphi_o \) respectively.
3.17 is modified to equation 3.19 shown below:

\[ M_{1} = \frac{1}{3} \begin{bmatrix} 1 + 2q \cos(\omega_m t) & 1 + 2q \cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q \cos\left(\omega_m t - \frac{4\pi}{3}\right) \\ 1 + 2q \cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q \cos(\omega_m t) & 1 + 2q \cos\left(\omega_m t - \frac{4\pi}{3}\right) \\ 1 + 2q \cos\left(\omega_m t - \frac{4\pi}{3}\right) & 1 + 2q \cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q \cos(\omega_m t) \end{bmatrix} \] (3.13)

where \( \omega_m = (\omega_o - \omega_i) \)

\[ M_{2} = \frac{1}{3} \begin{bmatrix} 1 + 2q \cos(\omega_m t) & 1 + 2q \cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q \cos\left(\omega_m t - \frac{4\pi}{3}\right) \\ 1 + 2q \cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q \cos(\omega_m t) & 1 + 2q \cos\left(\omega_m t - \frac{4\pi}{3}\right) \\ 1 + 2q \cos\left(\omega_m t - \frac{4\pi}{3}\right) & 1 + 2q \cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q \cos(\omega_m t) \end{bmatrix} \] (3.14)

where \( \omega_m = -(\omega_o - \omega_i) \)

This basic solution gives the direct transfer function approach. During each switching sequence \( T_s \), the average output voltage must fit into the input voltage envelope for any output frequency. Also combining the two solutions in equation 3.13 and 3.14 gives a method for input displacement factor control. This can be expressed as in equation 3.15 and 3.16 below:

\[ M(t) = \alpha_1 \cdot M_1(t) + \alpha_2 \cdot M_2(t) \] (3.15)

\[ (\alpha_1 + \alpha_2) = 1 \] (3.16)

For unity input phase displacement factor \( \alpha_1 = \alpha_2 = 0.5 \). For unity input displacement factor, the modulation function can be expressed as in equation 3.17 below:

\[ M_{Kj} = \frac{t_{Kj}}{T_s} = \left[ \frac{1}{3} + \frac{2v_K v_j}{3V_{im}} \right] \] (3.17)

\[ f or K = A, B, C and j = a, b, c \]

This method has little practical significance because of the 50% voltage ratio limitation. Venturini’s optimum method employs a common mode addition technique defined in equation 3.18 below:

\[ v_o = q \cdot V_{im} \ast \begin{bmatrix} \cos(\omega_o t) - \frac{1}{6} \cdot \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} \cdot \cos(3\omega_i t) \\ \cos(\omega_o t + \frac{4\pi}{3}) - \frac{1}{6} \cdot \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} \cdot \cos(3\omega_i t) \\ \cos(\omega_o t + \frac{2\pi}{3}) - \frac{1}{6} \cdot \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} \cdot \cos(3\omega_i t) \end{bmatrix} \] (3.18)

The target output voltage using equation 3.18 is 86.6% of the input voltage. In this case equation 3.17 is modified to equation 3.19 shown below:

\[ M_{Kj} = \frac{t_{Kj}}{T_s} = \left[ \frac{1}{3} + \frac{2v_K v_j}{3V_{im}} + \frac{4q}{9\sqrt{3}} \cdot \sin(\omega_i t + \beta_K) \cdot \sin(3\omega_i t) \right] \] (3.19)

\[ f or K = A, B, C and j = a, b, c and \beta_K = 0, \frac{2\pi}{3}, \frac{4\pi}{3} f or K = A, B, C respectively. \]

In equation 3.19, \( v_j \) include the common mode addition defined in equation 3.18.

3.4 MODEL DEVELOPMENT: To study the behaviour of the three phase AC to three phase AC MC using Venturini and Optimum Venturini Modulation algorithm, a model of this matrix converter
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is developed in SIMULINK [51]. The data shown in TABLE 3.1 are used to develop the model for all the above algorithms. The MC switching is developed based on equations 3.13, 3.17, 3.18 and 3.19.

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Modulation Index q</th>
<th>RMS Line to Neutral Input Voltage (Volts)</th>
<th>Input Frequency Hz</th>
<th>Output Frequency Hz</th>
<th>Carrier Frequency kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.4</td>
<td>220</td>
<td>50</td>
<td>50</td>
<td>2</td>
</tr>
</tbody>
</table>

### 3.4.1 MODEL OF A MATRIX CONVERTER USING VENTURINI FIRST METHOD:

The model of the three phase MC is developed using equation 3.13 for the data shown in Table 3.1. Equation 3.13 is proved in A3.2 Appendix in this chapter. The input and the output voltage are defined in equations 3.9 and 3.11. The nine modulation functions defined in equation 3.13 is developed using Embedded MATLAB Function in SIMULINK. These modulation functions are compared with a 2 kHz saw-tooth carrier generator and the gate pulses for the nine bidirectional switches are developed satisfying the constraint in equation 3.8 using another Embedded MATLAB Function. The source code used to generate the nine gate pulses is given below:

```matlab
function [tAa, tBa, tCa, tAb, tBb, tCb, tAc, tBc, tCc] = fcn(MAa, MBa, MCa, MAb, MBb, MCb, MAC, MBc, MCc, vsaw)
    if(vsaw < MAa)
        tAa = 1;
    else
        tAa = 0;
    end
    if(vsaw < (MAa+MBa))
        tABab = 1;
    else
        tABab = 0;
    end
    tBa = (~tAa & tABab);
    tCa = ~(tABab);
    if (vsaw < MAb)
        tAb = 1;
    else
        tAb = 0;
    end
    if (vsaw < (MAb + MBb))
        tBAba = 1;
    else
        tBAba = 0;
    end
    tBb = (tBAba & ~tAb);
    tCb = ~(tBAba);
    if (vsaw < (MAb + MBb))
        tABa = 1;
    else
        tABa = 0;
    end
    if (vsaw < (MAb + MBb))
        tBAb = 1;
    else
        tBAb = 0;
    end
    tBb = (tBAb & ~tAb);
    tCb = ~(tBAb);
    if (vsaw < (MAb + MBc))
        tBAc = 1;
    else
        tBAc = 0;
    end
    tBc = (tBAc & ~tAc);
    tCc = ~(tBAc);
```

TABLE 3.1: Model Parameters
In the source code above, the less than (<) and the plus (+) sign can be generated using op. amp. comparator and summer and the logic operation AND (\&) and NOT (~) can be developed using integrated circuits AND and NOT gates respectively.

The nine bidirectional switches are the IGBT/diode model in the power electronics library and the Three Phase AC source used as input voltage is from the Electrical Sources library in the SimPowersystems blockset.

The three phase cosine input voltage as defined in equation 3.9 with data as in Table 3.2 can be generated by entering 90 in the box corresponding to Phase angle of phase A (degrees)”, 50 in the box for frequency and 381.04 in the box for phase-to-phase rms voltage (V) in the three phase AC Source model.

The model of the three phase MC using Venturini First method developed in SIMULINK is shown in Fig. 3.2. A balanced three phase R-L load of 50 Ohms and 0.5 H is used. This R-L load is from the Elements library in the SimPowersystems blockset. The Three phase V-I measurement and Single phase Voltage measurement blocks are from the Measurements library in the SimPowersystems blockset.

3.4.2 SIMULATION RESULTS: The simulation of the MC using the Venturini First Method using the data in Table 3.1 is carried out using SIMULINK. The Fixed step ode3 (Bogacki-Shampine) solver is used. Harmonic spectrum of the line to neutral output voltage, phase A input current and line to line output voltage are shown in Fig. 3.3. to Fig. 3.5 respectively. The simulation results for the three phase line to neutral output voltage, phase A input current, three phase line to line output voltage and three phase load current are shown in Fig. 3.6 to Fig. 3.9 respectively. The simulation results from the harmonic spectrum are tabulated in Table 3.2 below. The 2 kHz saw-tooth carrier waveform and the gate pulse for the nine bidirectional switches are shown in Fig. 3.10 and Fig. 3.11 respectively.

3.4.3 MODEL OF A MATRIX CONVERTER USING VENTURINI SECOND METHOD: The model of the three phase MC is developed using equation 3.17 for the data shown in Table 3.1. Unity input phase displacement factor is assumed. The input voltage is defined in equation 3.9 and the output voltage in 3.11. The nine modulation functions defined in equation 3.17 is developed using Embedded MATLAB Function in SIMULINK. These modulation functions are compared with a 2 kHz saw-tooth carrier generator and the gate pulses for the nine bidirectional switches are developed satisfying the constraint in equation 3.8 using another Embedded MATLAB Function. The source code used to generate the nine gate pulses and the method of development of the model are already explained in section 3.4.1 in this chapter.
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FIG. 3.2: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING VENTURINI FIRST METHOD

- Discrete, 
- Ts = 1e-006 s.
- powergui
- RMS 1
- node 0
- V-I Measurement
- signalrms
- node 0
- g
- C
- E
- g
- C
- E
- g
- C
- E
- g
- C
- E
- MAa
- MBa
- MCa
- MAb
- MBb
- MCb
- MAc
- MBc
- MCc
- fcn
- Venturini Duty Cycle Algorithm
- 0.3405
- Display1
- 240.8
- Display
- 2000 Hz
- 50
- 50
- 0.4
### TABLE 3.2: Model Simulation Results 1

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Algorithm</th>
<th>THD of Line to Neutral Output Voltage (p.u.)</th>
<th>THD of Line to Line Output Voltage (p.u.)</th>
<th>THD of Input Current (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Venturini First Method</td>
<td>2.27</td>
<td>1.22</td>
<td>1.329</td>
</tr>
</tbody>
</table>
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FIG. 3.6

FIG. 3.7

FIG. 3.8
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FIG. 3.9

FIG. 3.10

FIG. 3.11
At this stage it is worth noting that the three phase AC voltage generated by the grid is a sine wave of the form given below:

\[ V_K = V_{in} \cdot \sin(\omega t \cdot t - \gamma) \quad (3.20) \]

where \( K = \text{Input Phase} A, B, C \) for \( \gamma = 0, \frac{2\pi}{3}, \frac{4\pi}{3} \) respectively.

The equation 3.17 is proved valid in Appendix A3.3 in this chapter both for three phase cosine wave and sine wave input and output voltages respectively. Hence although input and output voltages are defined in equations 3.9 and 3.11, a phase lag of \( \pi / 2 \) radians is intentionally applied to these three phase input and output voltages so that this MC model by Venturini second method gains practical significance. The model of the three phase MC using Venturini second method developed in SIMULINK is shown in Fig. 3.12. In this model, the three phase cosine wave input and output voltages defined in equation 3.9 and 3.11 each made to phase lag by \( \pi / 2 \) radians is used.

**3.4.4 SIMULATION RESULTS:** The simulation of the MC using the Venturini second Method using the data in Table 3.1 is carried out using SIMULINK. The variable step ode15s (Stiff/NDF) solver is used. Harmonic Spectrum of the Line to neutral output voltage, Phase A Input Current and Line to Line output voltage are shown in Fig. 3.13. to Fig. 3.15 respectively. The simulation results for the three phase Line to neutral output voltage, Phase A input current, three phase Line to Line output voltage and three phase load current are shown in Fig. 3.16 to Fig. 3.19 respectively. The simulation results from the Harmonic Spectrum are tabulated in Table 3.3. The 2 kHz saw-tooth carrier signal and the gate pulse pattern are already shown for the Venturini First method and are not repeated here.

**3.4.5 MODEL OF A MATRIX CONVERTER USING OPTIMUM VENTURINI MODULATION ALGORITHM:** The model of the three phase MC is developed using equation 3.19 with the input and output voltages as defined in equation 3.9 and 3.18 respectively for the data given in Table 3.1. The nine modulation functions defined in equation 3.19 is developed using Embedded MATLAB Function in SIMULINK. These modulation functions are compared with a 2 kHz saw-tooth carrier generator and the gate pulses for the nine bidirectional switches are developed satisfying the constraint in equation 3.8 using another Embedded MATLAB Function. The source code used to generate the nine gate pulses and the method of development of the model are already explained in section 3.4.1 in this chapter. The SIMULINK model is shown in Fig. 3.20.

**3.4.6 SIMULATION RESULTS:** The simulation of the MC using the Optimum Venturini method using the data in Table 3.1 is carried out using SIMULINK. The variable step ode15s (Stiff/NDF) solver is used. Harmonic spectrum of the Line to neutral output voltage, Phase A input current and line to line output voltage are shown in Fig. 3.21. to Fig. 3.23 respectively. The simulation results for the three phase line to neutral output voltage, Phase A input current, three phase line to line output voltage and three phase load current are shown in Fig. 3.24 to Fig. 3.27 respectively. The simulation results from the harmonic spectrum are tabulated in Table 3.4. The 2 kHz saw-tooth carrier signal
Chapter III: Modelling of Three Phase Matrix Converters Using Venturini and Optimum Venturini Modulation Algorithms

FIG. 3.12: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING VENTURINI SECOND METHOD
TABLE 3.3: Model Simulation Results 2

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Algorithm</th>
<th>THD of Line to Neutral Output Voltage (p.u.)</th>
<th>THD Line to Line Output Voltage (p.u.)</th>
<th>THD of Input Current (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Venturini Second Method</td>
<td>2.28</td>
<td>1.34</td>
<td>2.8</td>
</tr>
</tbody>
</table>
Chapter III: Modelling of Three Phase Matrix Converters Using Venturini and Optimum Venturini Modulation Algorithms
Chapter III: Modelling of Three Phase Matrix Converters Using Venturini and Optimum Venturini Modulation Algorithms

FIG. 3.20: OPTIMUM VENTURINI MODULATION ALGORITHM FOR THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER

NOTE: THIS IS AN ACCURATE MODEL

Discrete, Ts = 1e-006 s.

powergui

NARAYANASWAMY. P.R.IYER
FACULTY OF E.I.E.
THE UNIV. OF SYDNEY
REDFERN, SYDNEY, NSW-2006.
TABLE 3.4: Model Simulation Results 3

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Algorithm</th>
<th>THD of Line to Neutral Output Voltage (p.u.)</th>
<th>THD Line to Line Output Voltage (p.u.)</th>
<th>THD of Input Current (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Optimum Venturini</td>
<td>1.86</td>
<td>1.328</td>
<td>1.70</td>
</tr>
</tbody>
</table>
and the gate pulse pattern are already shown for the Venturini First method and are not repeated here.

### 3.5 DISCUSSION OF RESULTS:
Comparing the total harmonic distortion (THD) of line to neutral output voltage by the three methods, this value is minimum for optimum Venturini and maximum for Venturini second method. The THD for line to line output voltage and input current are minimum Venturini First method and maximum for Venturini second method in both cases. The linear modulation range for Venturini first and second method is 0 to 0.5 and for Optimum Venturini method is 0 to 0.866.

The application of Venturini algorithm second method for the speed control and brake by plugging of three phase induction motor fed by MC is presented in Appendix II.

### 3.6 CONCLUSIONS:
This chapter examines the detailed development of the SIMULINK model by Venturini first, second and Optimum Venturini method. The modulation index used is within the linear modulation range for all the three methods. The predicted performance is valid for values of modulation index lying within this linear modulation range.

### A3.1 APPENDIX: Case A:
Consider the three phase input and output voltages as defined in equations 3.9 and 3.11. The nine modulation functions are defined in equation 3.13, using which the output voltage $v_a$ across phase a can be expressed as follows:

$$v_a = q^* V_{im}^* \cos\left[\omega_m t\right] = \frac{1}{3} \left[ (1+2q.\cos(a))V_{im}\cos(\beta)+\left(1+2q.\cos\left(a-\frac{2\pi}{3}\right)\right)V_{im}\cos\left(\beta-\frac{2\pi}{3}\right) \right]$$

(A3.1.1)

where $a=\omega_m t$, $\beta=\omega_p t$ and $\omega_m = \left(\omega_p - \omega_o\right)$

Using the relation $\cos(A)\cos(B) = 0.5 \cos(A+B) + 0.5 \cos(A-B)$ in equation A3.1.1 and simplifying, we have the following equation:

$$v_a = \frac{V_{im}}{3} \left[ \cos(\beta) \cos\left(\beta-\frac{2\pi}{3}\right) + \cos\left(\beta-\frac{4\pi}{3}\right) + q^* \left( \cos(a+\beta) + \cos\left(a+\beta-\frac{4\pi}{3}\right) + \cos(a+\beta-\frac{8\pi}{3}) \right) \right]$$

(A3.1.2)

Equation A3.1.2 simplifies to the following:

$$v_a = q^* V_{im}^* \cos(a-\beta)$$

$$= q^* V_{im}^* \cos\left(\omega_m t\right)$$

(A3.1.3)
Equation A3.1.3 well agree with the expression for output voltage $v_a$ in the LHS of equation A3.1.1. This proves Venturini algorithm first method for three phase cosine wave input and output voltages.

Case B: Now consider the three phase input and output voltages defined in equation 3.9 and 3.11 all made to phase lag by 90 degrees so that they are now three phase sine wave input and output voltages at the respective frequencies. The nine modulation functions are defined in equation 3.13, using which the output voltage $v_a$ across phase a can be expressed as follows:

$$v_a = q^* V_{im}^* \sin (\omega_O t) = \frac{1}{3} \left[ \left( 1 + 2 q \cos \left( \frac{2\pi}{3} \right) \right) V_{im}^* \sin \left( \beta - \frac{2\pi}{3} \right) \right] + \left( 1 + 2 q \cos \left( \frac{4\pi}{3} \right) \right) V_{im}^* \sin \left( \beta - \frac{4\pi}{3} \right)$$

(A3.1.4)

where $\omega = \frac{\omega_i + \omega_o}{2}$ and $\omega = \omega_o - \omega_i$

Using the relation $\sin(A) \cos(B) = 0.5 \sin(A+B) + 0.5 \sin(A-B)$ in equation A3.1.4 and simplifying, we have the following equation:

$$v_a = \frac{V_{im}^*}{3} \left[ \sin \left( \beta \right) + \sin \left( \beta - \frac{2\pi}{3} \right) + \sin \left( \beta - \frac{4\pi}{3} \right) + q^* \left[ \sin \left( \alpha + \beta \right) + \sin \left( \alpha - \frac{8\pi}{3} \right) \right] \right]$$

(A3.1.5)

Equation A3.1.5 simplifies to the following:

$$v_a = q^* V_{im}^* \sin \left( \beta - \alpha \right)$$

(A3.1.6)

Equation A3.1.6 well agree with the expression for output voltage $v_a$ in the LHS of equation 3.1.4. This proves Venturini algorithm first method for three phase sine wave input and output voltages.

A3.2 APPENDIX: Case A: Consider the three phase input and output voltages as defined in equations 3.9 and 3.11. The nine modulation functions are defined in equation 3.17, using which the modulation functions for the three bidirectional switches between input phase A and output phase a can be expressed as follows:

$$M_{Aa} = \frac{1}{3} + \frac{2}{3} V_{im}^2 \left[ q^* V_{im}^* \cos (\omega_i t) \right]$$

(A3.2.1)

Similarly modulation functions $M_{Ba}$ and $M_{Ca}$ can be expressed as follows:
\[ M_{Ba} = \frac{1}{3} + \frac{2}{3} \left[ q \ast \cos\left(\omega_i \cdot t - \frac{2\pi}{3}\right) \ast \cos(\omega_o \cdot t) \right] \quad (A3.2.2) \]

\[ M_{Ca} = \frac{1}{3} + \frac{2}{3} \left[ q \ast \cos\left(\omega_i \cdot t - \frac{4\pi}{3}\right) \ast \cos(\omega_o \cdot t) \right] \quad (A3.2.3) \]

Output voltage for phase a can be expressed as follows:

\[ v_a = q \ast V_{im} \ast \cos(\omega_o \cdot t) = M_{Aa} \ast v_A + M_{Ba} \ast v_B + M_{Ca} \ast v_C \quad (A3.2.4) \]

Using equations 3.9 and A3.2.1 to A3.2.3 in equation A3.2.4 and letting \( \omega_i \cdot t = \theta \), the RHS of equation A3.2.4 reduces to the following:

\[ v_a = \frac{V_{im}}{3} \left[ \cos(\theta) + \cos\left(\theta - \frac{2\pi}{3}\right) + \cos\left(\theta - \frac{4\pi}{3}\right) \right] + \frac{2}{3} V_{im} \ast q \ast \cos(\omega_o \cdot t) \ast \left[ \cos^2(\theta) + \cos^2\left(\theta - \frac{2\pi}{3}\right) + \cos^2\left(\theta - \frac{4\pi}{3}\right) \right] \quad (A3.2.5) \]

The term 1 in equation A3.2.5 reduces to zero. Noting that \( \cos^2(\theta) = \frac{1}{2} + \frac{1}{2} \cos(2\theta) \) and using this in term 2 of equation A3.2.5, we have the following:

\[ v_a = \frac{2}{3} V_{im} \ast q \ast \cos(\omega_o \cdot t) \ast \left[ \frac{3}{2} + \cos(2\theta) + \cos\left(2\theta - \frac{4\pi}{3}\right) + \cos\left(2\theta - \frac{8\pi}{3}\right) \right] \]

\[ = q \ast V_{im} \ast \cos(\omega_o \cdot t) \quad (A3.2.6) \]

Equation A3.2.6 well agree with the LHS of equation A3.2.4. This proves Venturini algorithm with three phase cosine wave input and output voltages and with unity input phase displacement factor.

**Case B:** Now consider the three phase input and output voltages defined in equation 3.9 and 3.11 all made to phase lag by 90 degrees so that they are now three phase sine wave input and output voltages at the respective frequencies. The nine modulation functions are defined in equation 3.17, using which the modulation functions for the three bidirectional switches between input phase A and output phase a can be expressed as follows:

\[ M_{Aa} = \frac{1}{3} + \frac{2}{3} \left[ V_{im} \ast \sin(\omega_i \cdot t) \ast q \ast V_{im} \ast \sin(\omega_o \cdot t) \right] \]

\[ = \frac{1}{3} + \frac{2}{3} \left[ q \ast \sin(\omega_i \cdot t) \ast \sin(\omega_o \cdot t) \right] \quad (A3.2.7) \]

Similarly modulation functions \( M_{Ba} \) and \( M_{Ca} \) can be expressed as follows:
\[ M_{Ba} = \frac{1}{3} + \frac{2}{3} \left[ q^* \sin \left( \omega_i t - \frac{2\pi}{3} \right) \right] \sin (\omega_o t) \]  
\[ M_{Ca} = \frac{1}{3} + \frac{2}{3} \left[ q^* \sin \left( \omega_i t - \frac{4\pi}{3} \right) \right] \sin (\omega_o t) \]  

Output voltage for phase a can be expressed as follows:

\[ v_a = q^* V_{im} \sin (\omega_o t) = M_{Aa} \cdot v_A + M_{Ba} \cdot v_B + M_{Ca} \cdot v_C \]  

Using equations A3.2.7 to A3.2.9 and the newly defined three phase sine wave input voltages in equation A3.2.10, and letting \( \omega_i t = \theta \), the RHS of equation A3.2.10 reduces to the following:

\[ v_a = \frac{V_{im}}{3} \left[ \sin(\theta) + \sin \left( \theta - \frac{2\pi}{3} \right) + \sin \left( \theta - \frac{4\pi}{3} \right) \right] + \frac{2}{3} V_{im} \cdot q^* \sin (\omega_o t) \cdot \left[ \sin^2(\theta) + \sin^2 \left( \theta - \frac{2\pi}{3} \right) + \sin^2 \left( \theta - \frac{4\pi}{3} \right) \right] \]  

The term 1 in equation A3.2.11 reduces to zero. Noting that \( \sin^2(\theta) \) is \([ 0.5 - 0.5 \cos(2\theta) ]\) and using this in term 2 of equation A3.2.11, we have the following:

\[ v_a = \frac{2}{3} V_{im} \cdot q^* \sin (\omega_o t) \cdot \left[ \frac{3}{2} \cos(2\theta) - \cos \left( 2\theta - \frac{4\pi}{3} \right) - \cos \left( 2\theta - \frac{8\pi}{3} \right) \right] \]

\[ = q^* V_{im} \cdot \sin (\omega_o t) \]  

Equation A3.2.12 well agree with the LHS of equation A3.2.10. This proves Venturini algorithm with three phase sine wave input and output voltages and with unity input phase displacement factor.
Chapter IV

Modelling of Three Phase Matrix Converters Using Advanced Modulation Algorithms

4.1 INTRODUCTION: Although Venturini and Optimum Venturini algorithm form the fundamental method used for switching three phase Matrix Converters (MC), recently new algorithms have been proposed for switching MC. These include the algorithm proposed by Sunter-Clare [11-12] and the one proposed by Ned Mohan [13-14, 16-17]. This chapter examines the performance of MC in detail when switching is carried out using these two new algorithms.

4.2 SUNTER-CLARE MODULATION ALGORITHM: The Venturini modulation algorithm is suitable for synchronous operation of the input with the output [11-12]. This approach is unsuitable for closed loop applications where it is required to calculate the duty cycle every sampling period to achieve voltage control in which output frequency is continuously varying with time [11-12]. To overcome this problem the approach taken is to measure the input voltage at every sampling period and to determine voltage vector magnitude and ratio and position directly [11-12]. A simplified version of Venturini algorithm is defined in terms of the three phase input and output voltages at each sampling instant [11-12]. This allows the demand voltage ratio, output voltage magnitude and angle to be updated at every sampling period which is a requirement for closed loop control [11-12].

For the real time implementation of the proposed modulation algorithm, it is required to measure any two of three line to line input voltages. Then \( V_{im} \) and \( \omega_{i, t} \) are calculated as give below [11-12].

\[
V_{im}^2 = \frac{4}{3} \left[ v_{AB}^2 + v_{BC}^2 + v_{AB} \cdot v_{BC} \right] \quad (4.1)
\]

\[
\omega_{i, t} = \arctan \left( \frac{v_{BC}}{\sqrt{3} \left( \frac{2v_{AB}}{3} + v_{BC} \cdot v_{BC} \right)} \right) \quad (4.2)
\]

where \( v_{AB}, v_{BC} \) are the input line voltages.

The target output peak voltage and position are calculated as follows:

\[
V_{om}^2 = \frac{2}{3} \left[ v_a^2 + v_b^2 + v_c^2 \right] \quad (4.3)
\]

\[
\omega_{o, t} = \arctan \left( \frac{v_b - v_c}{\sqrt{3} \cdot v_a} \right) \quad (4.4)
\]

where \( v_a, v_b \) and \( v_c \) are the target phase output voltages. In a closed loop system such as a field oriented or a vector controlled drive system, the voltage magnitude and angle may be direct outputs of the control loop. Then the voltage ratio is calculated as follows:

\[
q = \sqrt{\frac{V_{om}^2}{V_{im}^2}} \quad (4.5)
\]
where \( q \) is the desired voltage ratio and \( V_{im} \) is the peak input voltage. The triple harmonic terms are found using the following equations.

\[
K_{31} = \frac{2q}{9q_m} \sin \left( \omega_i t \right) \sin \left( 3 \omega_i t \right) \\
K_{32} = \frac{2q}{9q_m} \sin \left( \omega_i t - \frac{2\pi}{3} \right) \sin \left( 3 \omega_i t \right) \\
K_{33} = -\frac{q^2}{6} \sin \left( 3 \omega_o t \right) - \frac{1}{4q_m} \cos \left( 3 \omega_o t \right)
\]

where \( q_m \) is the maximum voltage transfer ratio which is 0.866. Then the three modulation functions for output phase a are given as follows:

\[
M_{Aa} = \frac{1}{3} + k_{31} + \frac{2}{3V_{im}} \left( v_a + k_{33} \right) \left( \frac{V_{BC}}{3} + \frac{V_{AB}}{3} \right) + v_{sa} \\
M_{Ba} = \frac{1}{3} + k_{32} + \frac{2}{3V_{im}} \left( v_b + k_{33} \right) \left( \frac{V_{BC}}{3} - \frac{V_{AB}}{3} \right) \\
M_{Ca} = 1 - \left( M_{Aa} + M_{Ba} \right) \\
M_{Ab} = \frac{1}{3} + k_{31} + \frac{2}{3V_{im}} \left( v_a + k_{33} \right) \left( \frac{V_{BC}}{3} + \frac{V_{AB}}{3} \right) \\
M_{Bb} = \frac{1}{3} + k_{32} + \frac{2}{3V_{im}} \left( v_b + k_{33} \right) \left( \frac{V_{BC}}{3} - \frac{V_{AB}}{3} \right) \\
M_{Cb} = 1 - \left( M_{Ab} + M_{Bb} \right) \\
M_{Ac} = \frac{1}{3} + k_{31} + \frac{2}{3V_{im}} \left( v_a + k_{33} \right) \left( \frac{V_{BC}}{3} + \frac{V_{AB}}{3} \right) \\
M_{Bc} = \frac{1}{3} + k_{32} + \frac{2}{3V_{im}} \left( v_b + k_{33} \right) \left( \frac{V_{BC}}{3} - \frac{V_{AB}}{3} \right) \\
M_{Cc} = 1 - \left( M_{Ac} + M_{Bc} \right)
\]

The modulation functions have third harmonic components at the input and output frequencies added to them to produce output voltage \( V_o \). This is a requirement for getting maximum possible voltage ratio. The three phase output voltages and input currents can be defined in terms of modulation functions as in equation 3.6 and 3.7 with constraint as in equation 3.8 given in Chapter III.

### 4.2.1 MODEL DEVELOPMENT:
To study the behaviour of the three phase AC to three phase AC Matrix converter using Sunter-Clare Modulation algorithm, a model of this MC is developed in SIMULINK [51]. The data shown in Table 3.1 in Chapter III are used to develop the model.

### 4.2.2 MODEL OF A MATRIX CONVERTER USING SUNTER-CLARE ALGORITHM:
A model of the Three Phase AC to three phase AC Matrix converter using the above Sunter-Clare algorithm developed in SIMULINK is shown in Fig. 4.1. In this case three phase sine wave input and output phase voltages with peak values \( V_{im} \) and \( q^*V_{im} \) having frequency \( \omega_i \) and \( \omega_o \) rad/sec respectively are used. The three phase sine wave input and output voltages along with equations 4.1 to 4.17 are calculated using an Embedded MATLAB Function. The nine modulation functions derived from equations 4.9 to 4.17 are compared with a saw-tooth carrier generator \( v_{sa} \) and the nine gate pulse are derived in Embedded MATLAB Function using the following source code:

```matlab
if (MAa >= vsaw)
    tAa = 1;
else
    tAa = 0;
end
if ((MAa + MBA) >= vsaw)
```


\begin{verbatim}
   tABa = 1;
   else
   tABa = 0;
   end
   tBa = (tAa & ~(tABa) | tABa & ~tAa);
   tCa = ~(tABa);
   if (MAb >= vsaw)
      tAb = 1;
   else
      tAb = 0;
   end
   if ((MAb + MBb) >= vsaw)
      tBAb = 1;
   else
      tBAb = 0;
   end
   tBb = (tAb & ~(tBAb) | tBAb & ~tAb);
   tCb = ~(tBAb);
   if (MAc >= vsaw)
      tAc = 1;
   else
      tAc = 0;
   end
   if ((MAc + MBc) >= vsaw)
      tBAc = 1;
   else
      tBAc = 0;
   end
   tBc = (tAc & ~(tBAc) | tBAc & ~tAc);
   tCc = ~(tBAc);
\end{verbatim}

In the above source code, the symbols (>=), (&), (|) and (~) represent greater than or equal to, logic AND, OR and NOT operation respectively. The above source code can also be realized using integrated circuit Op.Amp. comparators, EXCUSIVE OR and NOT gates. The above source code is an alternative method and performs the same function as that give in section 3.3.1 of Chapter III. The three phase AC Voltage source, nine IGBT switches of the MC, R-L load etc. are the same as that given in Fig. 3.2 of Chapter III.

### 4.2.3 SIMULATION RESULTS:

The simulation of the model shown in Fig. 4.1 was carried out using SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current and line to line output voltage are shown in Fig. 4.1 to 4.3 respectively. Simulation results for the line to neutral output voltage, input current, line to line output voltage, load current are shown in Fig. 4.5 to 4.8. The 2 kHz saw-tooth carrier and gate pulse pattern are the same as in Section 3.3.2 of Chapter III. Simulation results are tabulated in Table 4.1 below:

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|}
\hline
Sl.No. & Algorithm & THD of Line to Neutral Output Voltage (p.u.) & THD of Line to Line Output Voltage (p.u.) & THD of Input Current (p.u.) \\
\hline
1 & Sunter-Clare & 1.715 & 1.303 & 2.46 \\
\hline
\end{tabular}
\caption{Model Simulation Results 1}
\end{table}
FIG. 4.1: THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING SUNTER-CLARE ALGORITHM
Chapter IV: Modelling of Three Phase Matrix Converters Using Advanced Modulation Algorithms

FIG. 4.2: LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM - SUNITER-CLARE ALGORITHM

FIG. 4.3: PHASE A INPUT CURRENT AND HARMONIC SPECTRUM - SUNITER-CLARE ALGORITHM

FIG. 4.4: LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM - SUNITER-CLARE ALGORITHM
4.3 NED MOHAN MODULATION ALGORITHM USING THREE PHASE COSINE WAVE INPUT VOLTAGES: A novel carrier-based modulation scheme is proposed by Ned Mohan et.al. which requires no sector information and look-up table to calculate duty ratios, with output voltage amplitude 0.866 times that of the input voltage and the input power factor controllable [13-14, 16-17]. This algorithm is briefly explained below:

Let the three phase input voltages, \( v_i = [v_A \ v_B \ v_C]^T \) be defined as in equation 3.9 and the corresponding output phase voltages be defined as in equation 3.6 given in Chapter III. The duty ratios be chosen such that the output voltages are independent of the input frequency. This is possible by considering the input voltages in stationary reference frame and the output voltages in synchronous reference frame. Hence \( M_{Aa}, M_{Ba} \) and \( M_{Ca} \) are chosen as given in equation 4.18 below:

\[
\begin{bmatrix}
M_{Aa} \\
M_{Ba} \\
M_{Ca}
\end{bmatrix} = \begin{bmatrix}
k_a \cdot \cos(\omega_i t - \varphi_i) \\
 k_b \cdot \cos\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\
 k_c \cdot \cos\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right)
\end{bmatrix}
\] (4.18)

Using equation 3.6, 3.9 and 4.18 and simplifying, the output voltage equation \( v_a \) for phase \( a \) reduces to the following:

\[
v_a = \frac{3}{2} \cdot k_a \cdot V_{im} \cdot \cos(\varphi_i) \quad (4.19)
\]

Equation 4.19 shows that the output phase voltage \( v_a \) is independent of the input frequency but dependent only on the amplitude of the input voltage. Equation 4.19 is proved in A4.1 Appendix.

The modulation index \( k_i \) is a function of the output frequency \( \omega_o \) as defined below:

\[
\begin{bmatrix}
k_a \\
k_b \\
k_c
\end{bmatrix} = \begin{bmatrix}
k \cdot \cos(\omega_o t) \\
k \cdot \cos\left(\omega_o t - \frac{2\pi}{3}\right) \\
k \cdot \cos\left(\omega_o t - \frac{4\pi}{3}\right)
\end{bmatrix}
\] (4.20)

Where \( k_a, k_b \) and \( k_c \) are the modulation indices for phase \( a, b \) and \( c \) respectively.

Using equations 4.19 and 4.20, the output phase voltage \( v_a \) simplifies to the following:

\[
v_a = \frac{3}{2} \cdot k \cdot V_{im} \cdot \cos(\varphi_i) \cdot \cos(\omega_o t) \quad (4.21)
\]

From equation 4.18 and 4.20, it is clear that the duty-ratios of the switches takes negative values. But the requirement is that the duty ratios of the switches must lie in the range 0 to 1. This is made possible by adding offset duty ratios to the existing duty ratios. Thus absolute values of duty ratios are added. The offset duty ratio is defined by equation 4.22 below:

\[
\begin{bmatrix}
D_A(t) \\
D_B(t) \\
D_C(t)
\end{bmatrix} = \begin{bmatrix}
|k_a \cdot \cos(\omega_i t - \varphi_i)| \\
|k_b \cdot \cos\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right)| \\
|k_c \cdot \cos\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right)|
\end{bmatrix}
\] (4.22)

Thus the new duty ratios are defined below:
To calculate input power factor, the input current is represented as a function of duty ratios and output
expressed as follows:

\[
\begin{bmatrix}
M_{Aa} \\
M_{Ba} \\
M_{Ca}
\end{bmatrix} = \begin{bmatrix}
D_A(t) + k_a \cos(\omega_i t - \phi_i) \\
D_B(t) + k_a \cos(\omega_i t - \phi_i - \frac{2\pi}{3}) \\
D_C(t) + k_a \cos(\omega_i t - \phi_i - \frac{4\pi}{3})
\end{bmatrix}
\] (4.23)

Using equation 4.22 in 4.23, in order that the new duty ratio in 4.23 lies in the range 0 to 1, the
following inequality should be satisfied:

\[0 < 2 |k_a| = 2k < 1\] (4.24)

Thus the maximum value of \(k_a\) and \(k\) can be 0.5. Using this value, the offset duty ratios are chosen as
given below:

\[
\begin{bmatrix}
D_A(t) \\
D_B(t) \\
D_C(t)
\end{bmatrix} = \begin{bmatrix}
|0.5 \cos(\omega_i t - \phi_i)| \\
0.5 \cos\left(\omega_i t - \phi_i - \frac{2\pi}{3}\right) \\
0.5 \cos\left(\omega_i t - \phi_i - \frac{4\pi}{3}\right)
\end{bmatrix}
\] (4.25)

To utilize the input voltage capability to the full extend, additional common mode voltage term is
added which gives the new modulation index as given below:

\[
\begin{bmatrix}
M_{Aa} \\
M_{Ba} \\
M_{Ca}
\end{bmatrix} = \begin{bmatrix}
D_A(t) + \left[k_a - \left\{\max(k_a, k_b, k_c) + \min(k_a, k_b, k_c) \right\}/2\right] \cos(\omega_i t - \phi_i) \\
D_B(t) + \left[k_a - \left\{\max(k_a, k_b, k_c) + \min(k_a, k_b, k_c) \right\}/2\right] \cos\left(\omega_i t - \phi_i - \frac{2\pi}{3}\right) \\
D_C(t) + \left[k_a - \left\{\max(k_a, k_b, k_c) + \min(k_a, k_b, k_c) \right\}/2\right] \cos\left(\omega_i t - \phi_i - \frac{4\pi}{3}\right)
\end{bmatrix}
\] (4.26)

Similar calculations apply to the other two output phases b and c.

To calculate input power factor, the input current is represented as a function of duty ratios and output
currents, as defined in equation 3.7 in Chapter III. Hence the input current in phase A can be
expressed as follows:

\[i_A = (k_a \cdot i_a + k_b \cdot i_b + k_c \cdot i_c) \cos(\omega_i t - \phi_i)\] (4.27)

In equation 4.27, the modulation index and output currents are at output frequency. Equation 4.27
simplifies to the following:

\[i_A = \left(\frac{3}{2} \cdot k \cdot I_o \cdot \cos(\phi_o)\right) \cos(\omega_i t - \phi_i)\] (4.28)

Where \(I_o\) is the amplitude of the output current and \(\phi_o\) is the output power factor angle.

Comparing equation 4.28 with the input phase voltage \(v_A\), it is seen that the input current lags the
input phase voltage by an angle of \(\phi_i\). Thus \(\phi_i\) is chosen to be zero for unity power factor operation.
Also from equation 4.21, we have

\[q = \frac{3}{2} \cdot k \cdot \cos(\phi_i)\] (4.29)

The switching signals corresponding to output phase a are obtained by comparing \(M_{Aa}\) and \(M_{Ba} +
M_{Ca}\) with a triangular carrier signal whose peak value is one and minimum value is zero. The
resulting PWM signals are given to logic gates to obtain the switching pulses for the matrix converter.
4.3.1 MODEL DEVELOPMENT: A model of the three phase matrix converter using the above Ned Mohan algorithm was developed in SIMULINK [51]. The input power factor is unity. The value of modulation index $k$ used is 0.26667 for a q value of 0.4 using equation 4.29. The triangle carrier has a peak value of one and a minimum value of zero. The values for the input voltage, input frequency, output frequency and triangle carrier frequency are the same as shown in Table 3.1 in Chapter III.

4.3.2 MODEL OF A MATRIX CONVERTER USING NED MOHAN ALGORITHM: The SIMULINK model of the MC using Ned Mohan algorithm for three phase cosine wave input voltages is shown in Fig. 4.9. The modulation index $k$, input frequency $f_i$, output frequency $f_o$, time $t$ and input p.f. angle $\phi_i$ are given as inputs to calculate $k_a$, $k_b$, $k_c$ and $D_A(t)$, $D_B(t)$ and $D_C(t)$ according to equations 4.20 and 4.25 using Embedded MATLAB function. The minimum and maximum values of the outputs $k_a$, $k_b$ and $k_c$ are calculated using two MinMax block in the Simulink block set. The two resulting outputs $\text{min}_k_{abc}$ and $\text{max}_k_{abc}$ together with the above calculated values for $D_A(t)$, $D_B(t)$ and $D_C(t)$ and the input $\phi_i$ are used to calculate the duty ratios of the switches according to equation 4.26 using the same Embedded MATLAB function.

A 2 kHz triangle carrier with a peak value and minimum value of one and zerovolt is generated using a 2 kHz square pulse generator with 50 % duty cycle, a subtractor and an integrator with multiplication constant. The nine calculated values of the duty ratios for the switches and the 2 kHz triangle carrier are given as inputs to another Embedded MATLAB function to generate the gate switching pulses for the nine bidirectional switches. A method of generating the gate switching pulses using adders, comparators and logic gates is also shown in Fig. 4.9. The source code for generating the gate switching pulses is the same as given in section 4.2.2 above, except that the nine gate pulses $tAa$ to $tCc$, $tABAa$, $tBAb$ and $tBAc$ in this source code are replaced by $qAa$ to $qCc$, $qABAa$, $qABBb$ and $qABc$ respectively. The three phase cosine wave generator, the nine IGBT bidirectional switch matrix, R-L load etc. are the same as explained in Section 3.3.1 of Chapter III.

4.3.3 SIMULATION RESULTS: The simulation of the model shown in Fig. 4.9 was carried out using SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current and line to line output voltage are shown in Fig. 4.10 to 4.12 respectively. Simulation results for the line to neutral output voltage, input current, line to line output voltage, load current are shown in Fig. 4.13 to 4.16. The 2 kHz triangle carrier and gate pulse pattern are shown in Fig. 4.17 and 4.18 respectively. Simulation results for a modulation index $k$ of 0.26667 and three phase cosine wave input voltage are tabulated in Table 4.2 below:

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Algorithm</th>
<th>THD of Line to Neutral Output Voltage (p.u.)</th>
<th>THD Line to Line Output Voltage (p.u.)</th>
<th>THD of Input Current (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ned Mohan</td>
<td>2.80</td>
<td>1.398</td>
<td>2.829</td>
</tr>
</tbody>
</table>

TABLE 4.2: Model Simulation Results 2
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FIG. 4.9: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING NED MOHAN ALGORITHM


NOTE: (\(3/2\) * \(k\) * \(\cos(\phi_i)\) = \(q\) IN VENTURINI ALGORITHM)

### Diagram Description

- **Continuous powergui**
- **Transfer Fcn**
- **Scope**
- **Scope5**
- **Scope6**
- **Scope7**
- **Scope8**
- **Scope9**
- **Scope10**
- **Scope11**
- **Scope12**
- **Scope13**
- **Scope14**
- **Scope15**
- **Scope16**

**Nodes and Connectors**
- **MAa**, **MAb**, **MAC**, **Mbc**, **MBb**, **MBc**, **MCa**, **MCb**, **MCc**
- **qAc**, **qAb**, **qAa**, **qBc**, **qBb**, **qBa**, **qCa**, **qCb**, **qAa**
- **vtri**

**Mathematical Expressions**
- \(k\)
- \(\phi_i\)
- \(\text{fofitmin}_k_{\text{abc}}\)
- \(\text{max}_k_{\text{abc}}\)

**Display Values**
- \(251.1\)
- \(249.3\)
- \(118.1\)
- \(2.806\)

**Additional Elements**
- **Signal THD**
- **RMS1**
- **RMS2**
- **Pulse Generator1**
- **MinMax1**, **MinMax2**
- **XOR**
- **Add1**

**Diagram Legend**
- **Vin**
- **Vout**
- **Iin**
- **Iout**

**Diagram Title**

FIG. 4.9: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING NED MOHAN ALGORITHM
Chapter IV: Modelling of Three Phase Matrix Converters Using Advanced Modulation Algorithms

- **Fig. 4.10:** Line to Neutral Output Voltage and Harmonic Spectrum - NED Mohan Algorithm

- **Fig. 4.11:** Phase A Input Current and Harmonic Spectrum - NED Mohan Algorithm

- **Fig. 4.12:** Line to Line Output Voltage and Harmonic Spectrum - NED Mohan Algorithm
4.4 NED MOHAN MODULATION ALGORITHM USING THREE PHASE SINE WAVE INPUT VOLTAGES: Let the three phase input voltages, \( v_i = [v_A \ v_B \ v_C]^T \) be defined as in equation 4.30 and the corresponding output phase voltages \( v_o = [v_a \ v_b \ v_c]^T \) be defined as in equation 4.31 given below:

\[
\begin{align*}
\dot{v}_i &= V_{im} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t - \frac{4\pi}{3}) \end{bmatrix} \quad (4.30) \\
\dot{v}_o &= q \ast V_{im} \begin{bmatrix} \sin(\omega_o t + \phi_o) \\ \sin(\omega_o t + \phi_o - \frac{2\pi}{3}) \\ \sin(\omega_o t + \phi_o - \frac{4\pi}{3}) \end{bmatrix} \quad (4.31)
\end{align*}
\]

The duty ratios be chosen such that the output voltages are independent of the input frequency. This is possible by considering the input voltages in stationary reference frame and the output voltages in synchronous reference frame. Hence \( M_{Aa}, M_{Ba} \) and \( M_{Ca} \) are chosen as given in equation 4.32 below:
\[
\begin{bmatrix}
M_{Aa} \\
M_{Ba} \\
M_{Ca}
\end{bmatrix} = \begin{bmatrix}
k_a \sin(\omega_a t - \varphi_i) \\
k_a \sin(\omega_a t - \frac{2\pi}{3}) \\
k_a \sin(\omega_a t - \frac{4\pi}{3})
\end{bmatrix}
\] (4.32)

Using equation 4.30, 4.31 and 4.32 and simplifying, the output voltage equation \(v_a\) for phase a reduces to the following:

\[
v_a = \frac{3}{2} k_a V_{\text{im}} \cos(\varphi_i) \quad (4.33)
\]

Equation 4.33 shows that the output phase voltage \(v_a\) is independent of the input frequency but dependent only on the amplitude of the input voltage. Equation 4.33 is proved in A4.1 Appendix.

The modulation index \(k_a\) is a function of the output frequency \(\omega_a\) as defined below:

\[
\begin{bmatrix}
k_a \\
k_b \\
k_c
\end{bmatrix} = \begin{bmatrix}
k \sin(\omega_a t) \\
k \sin(\omega_a t - \frac{2\pi}{3}) \\
k \sin(\omega_a t - \frac{4\pi}{3})
\end{bmatrix}
\] (4.34)

Where \(k_a\), \(k_b\) and \(k_c\) are the modulation indices for phase a, b and c respectively.

Using equations 4.33 and 4.34, the output phase voltage \(v_a\) simplifies to the following:

\[
v_a = \left[\frac{3}{2} k_a V_{\text{im}} \cos(\varphi_i) \sin(\omega_a t)\right] \quad (4.35)
\]

From equation 4.32 and 4.34, it is clear that the duty-ratios of the switches takes negative values. But the requirement is that the duty ratios of the switches must lie in the range 0 to 1. This is made possible by adding offset duty ratios to the existing duty ratios. Thus absolute values of duty ratios are added. The offset duty ratio is defined by equation 4.36 below:

\[
\begin{bmatrix}
D_a(t) \\
D_b(t) \\
D_c(t)
\end{bmatrix} = \begin{bmatrix}
|k_a \sin(\omega_a t - \varphi_i)| \\
|k_a \sin(\omega_a t - \frac{2\pi}{3})| \\
|k_a \sin(\omega_a t - \frac{4\pi}{3})|
\end{bmatrix}
\] (4.36)

Thus the new duty ratios are defined below:

\[
\begin{bmatrix}
M_{Aa} \\
M_{Ba} \\
M_{Ca}
\end{bmatrix} = \begin{bmatrix}
D_a(t) + k_a \sin(\omega_a t - \varphi_i) \\
D_b(t) + k_a \sin(\omega_a t - \frac{2\pi}{3}) \\
D_c(t) + k_a \sin(\omega_a t - \frac{4\pi}{3})
\end{bmatrix}
\] (4.37)

Using equation 4.36 in 4.37, in order that the new duty ratio in 4.37 lies in the range 0 to 1, the following inequality should be satisfied:

\[
0 < 2 |k_a| = 2 k < 1 \quad (4.38)
\]

Thus the maximum value of \(k_a\) and \(k\) can be 0.5. Using this value, the offset duty ratios are chosen as given below:
To calculate input power factor, the input current is represented as a function of duty ratios and output currents, as defined in equation 3.7 in Chapter III. Hence the input current in phase A can be expressed as follows:

\[
\begin{bmatrix}
D_A(t) \\
D_B(t) \\
D_C(t)
\end{bmatrix} =
\begin{bmatrix}
0.5 \cdot \sin(\omega t - \varphi_i) \\
0.5 \cdot \sin\left(\omega t - \varphi_i - \frac{2\pi}{3}\right) \\
0.5 \cdot \sin\left(\omega t - \varphi_i - \frac{4\pi}{3}\right)
\end{bmatrix}
\]

(4.39)

To utilize the input voltage capability to the full extend, additional common mode voltage term is added which gives the new modulation index as given below:

\[
\begin{bmatrix}
M_{Aa} \\
M_{Ba} \\
M_{Ca}
\end{bmatrix} =
\begin{bmatrix}
D_A(t) + [k_a - \{\max(k_{a_r}, k_{b_r}, k_{c_r}) + \min(k_{a_r}, k_{b_r}, k_{c_r})\}/2] \cdot \sin(\omega t - \varphi_i) \\
D_B(t) + [k_a - \{\max(k_{a_r}, k_{b_r}, k_{c_r}) + \min(k_{a_r}, k_{b_r}, k_{c_r})\}/2] \cdot \sin(\omega t - \varphi_i - \frac{2\pi}{3}) \\
D_C(t) + [k_a - \{\max(k_{a_r}, k_{b_r}, k_{c_r}) + \min(k_{a_r}, k_{b_r}, k_{c_r})\}/2] \cdot \sin(\omega t - \varphi_i - \frac{4\pi}{3})
\end{bmatrix}
\]

(4.40)

Similar calculations apply to the other two output phases b and c.

To calculate input power factor, the input current is represented as a function of duty ratios and output currents, as defined in equation 3.7 in Chapter III. Hence the input current in phase A can be expressed as follows:

\[i_A = (k_{a_r} \cdot i_a + k_{b_r} \cdot i_b + k_{c_r} \cdot i_c) \cdot \sin(\omega t - \varphi_i) \]  

(4.41)

In equation 4.27, the modulation index and output currents are at output frequency. Equation 4.27 simplifies to the following:

\[i_A = \left(\frac{3}{2} \cdot k \cdot I_o \cdot \cos(\varphi_0)\right) \cdot \sin(\omega t - \varphi_i) \]  

(4.42)

Where \(I_o\) is the amplitude of the output current and \(\varphi_0\) is the output power factor angle.

Comparing equation 4.42 with the input phase voltage \(v_{a_r}\), it is seen that the input current lags the input phase voltage by an angle of \(\varphi_i\). Thus \(\varphi_i\) is chosen to be zero for unity power factor operation. Also from equation 4.35, we have

\[q = \frac{3}{2} \cdot k \cdot \cos(\varphi_i) \]  

(4.43)

The switching signals corresponding to output phase a are obtained by comparing \(M_{Aa}\) and \((M_{Aa} + M_{Ba})\) with a triangular carrier signal whose peak value is one and minimum value is zero. The resulting PWM signals are given to logic gates to obtain the switching pulses for the matrix converter.

**4.4.1 MODEL DEVELOPMENT:** A model of the three phase matrix converter using the above Ned Mohan algorithm for three phase sine wave input is developed in SIMULINK [51]. The input power factor is unity. The value of modulation index \(k\) used is 0.26667 for a \(q\) value of 0.4 using equation 4.43. The triangle carrier has a peak value of one and a minimum value of zero. The values for the input voltage, input frequency, output frequency and triangle carrier frequency are the same as shown in Table 3.1 in Chapter III.
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FIG. 4.19: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER WITH THREE PHASE SINE WAVE VOLTAGE INPUT USING NED MOHAN ALGORITHM

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**Fig. 4.9:** Line to Neutral Output Voltage and Harmonic Spectrum - NED Mohan Algorithm with Three Phase Sine Wave Input Voltage

**Fig. 4.10:** Phase A Output Current and Harmonic Spectrum - NED Mohan Algorithm with Three Phase Sine Wave Input Voltage

**Fig. 4.11:** Three Phase 50 Hz AC to Three Phase 50 Hz AC MC NED Mohan Algorithm with Three Phase Sine Wave Input Voltage for k = 0.26667 and f = 2 kHz

**Fig. 4.12:** Line to Line Output Voltage and Harmonic Spectrum - NED Mohan Algorithm with Three Phase Sine Wave Input Voltage
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FIG. 4.23

FIG. 4.24

FIG. 4.25

FIG. 4.26
4.4.2 MODEL OF A MATRIX CONVERTER USING NED MOHAN ALGORITHM: The SIMULINK model of the MC using Ned Mohan algorithm for three phase sine wave input voltages is shown in Fig. 4.19. The modulation index \( k \), input frequency \( f_i \), output frequency \( f_o \), time \( t \) and input p.f. angle \( \phi_i \) are given as inputs to calculate \( k_a \), \( k_b \), \( k_c \) and \( D_A(t), D_B(t) \) and \( D_C(t) \) according to equations 4.34 and 4.39 using Embedded MATLAB function. The minimum and maximum values of the outputs \( k_a \), \( k_b \), and \( k_c \) are calculated using two MinMax block in the Simulink block set. The two resulting outputs \( \text{min}_k_{abc} \) and \( \text{max}_k_{abc} \) together with the above calculated values for \( D_A(t) \), \( D_B(t) \) and \( D_C(t) \) and the input \( \phi_i \) are used to calculate the duty ratios of the switches according to equation 4.40 using the same Embedded MATLAB function.

A 2 kHz triangle carrier with a peak value and minimum value of one and zero volt is generated using a 2 kHz square pulse generator with 50% duty cycle, a subtractor and an integrator with multiplication constant. The nine calculated values of the duty ratios for the switches and the 2 kHz triangle carrier are given as inputs to another Embedded MATLAB function to generate the gate switching pulses for the nine bidirectional switches. A method of generating the gate switching pulses using adders, comparators and logic gates is also shown in Fig. 4.19. The source code for generating the gate switching pulses is the same as given in section 4.2.2 above, except that the nine gate pulses \( tAa \) to \( tCc \), \( tABa \), \( tBAb \) and \( tBAc \) in this source code are replaced by \( qAa \) to \( qCc \), \( qABa \), \( qABb \) and \( qABc \) respectively. The three phase sine wave generator, the nine IGBT bidirectional switch matrix, R-L load etc. are the same as explained in Section 3.3.1 of Chapter III, except that in the three phase AC source model, in the box corresponding to Phase Angle of Phase A (in degrees), a value of zero is entered.

4.4.3 SIMULATION RESULTS: The simulation of the model shown in Fig. 4.19 was carried out using SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current and line to line output voltage are shown in Fig. 4.20 to 4.22 respectively. Simulation results for the line to neutral output voltage, input current, line to line output voltage, load current are shown in Fig. 4.23 to 4.26. The 2 kHZ triangle carrier and gate pulse pattern are same as shown in Fig. 4.17 and 4.18 respectively. Simulation results for a modulation index \( k \) of 0.26667 and three phase sine wave input voltage are tabulated in Table 4.3 below:

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Algorithm</th>
<th>THD Line to Neutral Output Voltage (p.u.)</th>
<th>THD Line to Line Output Voltage (p.u.)</th>
<th>THD of Input Current (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ned Mohan</td>
<td>2.567</td>
<td>1.377</td>
<td>2.622</td>
</tr>
</tbody>
</table>

4.5 DISCUSSION OF RESULTS: Comparing the results in Table 4.2 with Table 4.3, it is seen that with three phase sine wave input voltages the value of THD for the line to neutral, line to line and input current are lower compared to three phase cosine wave input voltages for the Ned Mohan algorithm. Comparing Table 4.1 with Table 4.2 and 4.3, it is seen that the THD of line to neutral, line to line voltages and the input current are much lower for Sunter-Clare algorithm as compared to Ned
Mohan algorithm. Considering practical implementation issues discussed in Section 3.3.3 of Chapter III, Ned Mohan algorithm with three phase sine wave input voltages is preferable to that with three phase cosine wave input voltages. The linear range for modulation index is 0.866 for Sunter-Clare algorithm and 0.577 for Ned Mohan algorithm.

4.6 CONCLUSIONS: Considering factors like THD of line to neutral, line to line output voltages and input current, it is seen that Sunter-Clare algorithm is superior to Ned Mohan algorithm. The two algorithms discussed in this chapter are recently proposed. Also for both the algorithms the modulation index is well within the linear modulation range.

A4.1 APPENDIX: The Sunter-Clare algorithm is empirical based on assumptions and hence a direct mathematical proof can’t be given. Ned Mohan algorithm for three phase cosine wave and sine wave input voltages is proved below:

Case A: The phase a output voltage $v_a$ using equation 4.18 for three phase cosine wave input voltages can be be defined as follows:

$$v_a = k_a \cdot V_{im} \cdot \left[ \cos(\omega_i t) \cdot \cos(\omega_i t - \phi_i) + \cos(\omega_i t - 2\pi/3) \cdot \cos(\omega_i t - 2\pi/3 - \phi_i) + \cos(\omega_i t - 4\pi/3) \cdot \cos(\omega_i t - 4\pi/3 - \phi_i) \right]$$  \hspace{1cm} (A4.1.1)

$\cos(A)\cdot\cos(B) = (1/2) \cdot \cos(A+B) + (1/2) \cdot \cos(A-B)$ \hspace{1cm} (A4.1.2)

Using equation A4.1.2 in equation A4.1.1 and simplifying,

$$v_a = k_a \cdot V_{im} \cdot \left[ (1/2) \cdot \cos(2\omega_i t - \phi_i) + (-1/2) \cdot \cos(2\omega_i t - \phi_i) + (3/2) \cdot \cos(\phi_i) \right]$$  \hspace{1cm} (A4.1.3)

i.e. $v_a = (3/2) \cdot k_a \cdot V_{im} \cdot \cos(\phi_i)$ \hspace{1cm} (A4.1.4)

Equation A4.1.4 well agrees with equation 4.19.

Case B: The phase a output voltage $v_a$ using equation 4.32 for three phase sine wave input voltages can be be defined as follows:

$$v_a = k_a \cdot V_{im} \cdot \left[ \sin(\omega_i t) \cdot \sin(\omega_i t - \phi_i) + \sin(\omega_i t - 2\pi/3) \cdot \sin(\omega_i t - 2\pi/3 - \phi_i) + \sin(\omega_i t - 4\pi/3) \cdot \sin(\omega_i t - 4\pi/3 - \phi_i) \right]$$  \hspace{1cm} (A4.1.5)

$\sin(A)\cdot\sin(B) = (1/2) \cdot \cos(A-B) - (1/2) \cdot \cos(A+B)$ \hspace{1cm} (A4.1.6)

Using equation A4.1.6 in equation A4.1.5 and simplifying,

$$v_a = \left[ \frac{1}{2} \cdot k_a \cdot V_{im} \cdot \left[ \cos(\phi_i) - \cos(\theta) + \cos(\phi_i) - \cos(\theta - \frac{4\pi}{3}) + \cos(\phi_i) - \cos(\theta - \frac{8\pi}{3}) \right] \right]$$  \hspace{1cm} (A4.1.7)

where $\theta = (2\omega_i t - \phi_i)$

$$v_a = \frac{3}{2} \cdot k_a \cdot V_{im} \cdot \cos(\phi_i)$$  \hspace{1cm} (A4.1.8)

Equation A4.1.8 well agrees with equation 4.33.

This proves Ned Mohan algorithm for three phase cosine wave and sine wave input voltages.
Chapter V
Matrix Converter Fed Vector Controlled Three Phase Induction Motor Drive

5.1 INTRODUCTION: The three phase AC to three phase AC Matrix Converter (MC) finds applications in three phase Induction Motor (IM) drives [6-8, 12, 14]. This chapter examines the modelling aspects of vector controlled three phase IM drive fed by MC. The performance of the Vector controlled three phase IM drive is obtained by simulation using SIMULINK when the MC is switched by various carrier based modulation techniques such as by using Venturini and the recently proposed Sunter-Clare and Ned Mohan algorithms.

5.2 VECTOR CONTROL OF THREE PHASE INDUCTION MOTOR DRIVE: This section on Vector control of three phase IM drive is completely based on reference 15. Referring to Fig.5.1, at time $t$, the d-axis is shown at an angle $\theta_{da}$ with respect to the stator a-axis. The relation connecting d-q axis stator current with the abc-axis stator current can be expressed as in equation 5.1 below.

$$
\begin{bmatrix}
    i_{sd} \\
    i_{sq}
\end{bmatrix}
= \sqrt{\frac{2}{3}} \begin{bmatrix}
    \cos(\theta_{da}) & \cos(\theta_{da}-\frac{2\pi}{3}) & \cos(\theta_{da}-\frac{4\pi}{3}) \\
    -\sin(\theta_{da}) & -\sin(\theta_{da}-\frac{2\pi}{3}) & -\sin(\theta_{da}-\frac{4\pi}{3})
\end{bmatrix} \begin{bmatrix}
    i_a \\
    i_b \\
    i_c
\end{bmatrix}
$$

(5.1)

In equation 5.2, $\theta_{dA}$ is the angle made by the rotor A-axis with the d-axis.

The inverse relation connecting the abc-axis stator current with dq-axis stator current can be expressed as follows:

$$
\begin{bmatrix}
    i_a \\
    i_b \\
    i_c
\end{bmatrix}
= \sqrt{\frac{2}{3}} \begin{bmatrix}
    \cos(\theta_{da}) & -\sin(\theta_{da}) \\
    \cos(\theta_{da}-\frac{2\pi}{3}) & -\sin(\theta_{da}-\frac{2\pi}{3}) \\
    \cos(\theta_{da}-\frac{4\pi}{3}) & -\sin(\theta_{da}-\frac{4\pi}{3})
\end{bmatrix} \begin{bmatrix}
    i_{sd} \\
    i_{sq}
\end{bmatrix}
$$

(5.3)

Similar transformation applies to abc-axis voltages and flux linkages in the stator.
The transformation of rotor currents in the dq-axis to abc-axis can be obtained by replacing $\theta_{da}$ to $\theta_{dA}$ in equation 5.3. This is given below:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta_{dA}) & -\sin(\theta_{dA}) \\ \cos(\theta_{dA} - \frac{2\pi}{3}) & -\sin(\theta_{dA} - \frac{2\pi}{3}) \\ \cos(\theta_{dA} - \frac{4\pi}{3}) & -\sin(\theta_{dA} - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} i_{rd} \\ i_{rq} \end{bmatrix}$$  (5.4)

The same transformation matrix given in equation 5.4 applies to voltages and flux linkages in the rotor.

**5.2.1 FLUX LINKAGES OF STATOR AND ROTOR WINDINGS:** The flux linkages in the stator d and q axis windings can be expressed as follows [15]:

$$\lambda_{sd} = L_s i_{sd} + L_m i_{rd}$$  (5.5)
$$\lambda_{sq} = L_s i_{sq} + L_m i_{rq}$$  (5.6)
$$L_s = L_{ls} + L_m$$  (5.7)

Similarly for the rotor, the flux linkage expression in the d-q axis windings can be expressed as follows:

$$\lambda_{rd} = L_r i_{rd} + L_m i_{sd}$$  (5.8)
$$\lambda_{rq} = L_r i_{rq} + L_m i_{sq}$$  (5.9)
$$L_r = L_{lr} + L_m$$  (5.10)

**5.2.2 VOLTAGE EQUATIONS FOR STATOR AND ROTOR DQ-AXIS WINDINGS:** The dq-axis voltage equation for the stator can be expressed as follows [15]:

$$v_{sd} = R_s i_{sd} + \frac{d}{dt}(\lambda_{sd}) - \omega_d \lambda_{sq}$$  (5.11)
$$v_{sq} = R_s i_{sq} + \frac{d}{dt}(\lambda_{sq}) + \omega_d \lambda_{sd}$$  (5.12)

In equations 5.11 and 5.12, $\omega_d$ is the speed of the dq-axis reference frame relative to the stator winding.

The rotor dq-axis voltage expression is given below [15]:

$$v_{rd} = R_r i_{rd} + \frac{d}{dt}(\lambda_{rd}) - \omega_d \lambda_{rq}$$  (5.13)
$$v_{rq} = R_r i_{rq} + \frac{d}{dt}(\lambda_{rq}) + \omega_d \lambda_{rd}$$  (5.14)

$$\omega_d = \left( \frac{\omega_m}{\text{No. of Poles}} \right) * \omega_{\text{mech}}$$  (5.15)
$$\omega_m = \frac{\text{No. of Poles}}{2} \cdot \omega_{\text{mech}}$$  (5.16)
In equations 5.13 and 5.14 $\omega_{dA}$ is the speed of the dq-axis reference frame relative to the rotor winding speed.

The value of $\omega_d$ can be an arbitrary choice. The three common reference frames are classified as follows:

$\omega_d = \omega_{syn} = \text{synchronous reference frame}$

$\omega_d = 0 = \text{stationary reference frame}$

$\omega_d = \omega_m = \text{rotor reference frame}$

PI controllers can be easily designed in synchronous reference frame and hence this reference frame is chosen here.

5.2.3 ELECTROMAGNETIC TORQUE: The torque is produced in the rotor d-axis due to flux density in the q-axis windings and in the rotor q-axis due to flux density in the d-axis windings. These two torque acts in opposite direction. The net electromagnetic torque can be expressed as follows [15]:

$$T_{em} = \frac{P}{2}(\lambda_{rq}i_{rd} - \lambda_{rd}i_{rq}) \quad (5.17)$$

Equation 5.17 can also be expressed in the following form:

$$T_{em} = \frac{PL}{2}(i_{sq}i_{rd} - i_{sd}i_{rq}) \quad (5.18)$$

5.2.4 ELECTRODYNAMICS: The acceleration is determined by the difference of the electromagnetic torque and the load torque acting on $J_{eq}$, the combined inertia of the motor and the load. In terms of the rotor speed $\omega_{mech}$ in mechanical radians per second, the following equation is valid [15]:

$$J_{eq} \frac{d(\omega_{mech})}{dt} = (T_{em} - T_L) \quad (5.19)$$

In equation 5.19, $T_L$ is the load torque.

Substituting equations 5.5 to 5.7 in equations 5.11 to 5.12, the stator voltage equations can be expressed as follows:

$$v_{sd} = R_s i_{sd} - a_{sd}\lambda_{sq} + \frac{L_{sh} di_{sd}}{dt} + \frac{L_{sh} di_{sq}}{dt} + \frac{L_{sh} di_{sq} + i_{sd}}{dt} \quad (5.20)$$

$$v_{sq} = R_s i_{sq} + a_{sd}\lambda_{sd} + \frac{L_{sh} di_{sq}}{dt} + \frac{L_{sh} di_{sq} + i_{q}}{dt} \quad (5.21)$$

Similarly, using equations 5.8 to 5.10 in equations 5.13 and 5.14, the rotor voltage equations can be expressed as follows:
\[ v_{rd} = 0 = R_r \cdot i_{rd} - \omega dA \cdot \lambda_{rd} + \frac{L_{tr}}{dt} \left( i_{rd} \right) + \frac{L_m}{dt} \left( i_{rd} + i_{rd} \right) \] (5.22)

\[ v_{rq} = 0 = R_r \cdot i_{rq} + \omega dA \cdot \lambda_{rq} + \frac{L_{tr}}{dt} \left( i_{rq} \right) + \frac{L_m}{dt} \left( i_{rq} + i_{rq} \right) \] (5.23)

### 5.2.5 PRINCIPLE OF COMPUTER SIMULATION OF THREE PHASE INDUCTION MOTOR DRIVE:

The \(dq\) winding currents can be calculated from flux linkage equations. Combining equations 5.5, 5.6 and 5.8, 5.9, we have the following:

\[
\begin{bmatrix}
\lambda_{sd} \\
\lambda_{sq} \\
\lambda_{rd} \\
\lambda_{rq}
\end{bmatrix} =
\begin{bmatrix}
L_s & 0 & L_m & 0 \\
0 & L_f & 0 & L_m \\
L_m & 0 & L_r & 0 \\
0 & L_m & 0 & L_r
\end{bmatrix}
\begin{bmatrix}
i_{sd} \\
i_{sq} \\
i_{rd} \\
i_{rq}
\end{bmatrix} +
\begin{bmatrix}
\dot{i}_{sd} \\
\dot{i}_{sq} \\
\dot{i}_{rd} \\
\dot{i}_{rq}
\end{bmatrix}
\] (5.24)

\[
\begin{bmatrix}
i_{sd} \\
i_{sq} \\
i_{rd} \\
i_{rq}
\end{bmatrix} =
\begin{bmatrix}
L_s & 0 & L_m & 0 \\
0 & L_f & 0 & L_m \\
L_m & 0 & L_r & 0 \\
0 & L_m & 0 & L_r
\end{bmatrix}
^{-1}
\begin{bmatrix}
\lambda_{sd} \\
\lambda_{sq} \\
\lambda_{rd} \\
\lambda_{rq}
\end{bmatrix} +
\begin{bmatrix}
\dot{i}_{sd} \\
\dot{i}_{sq} \\
\dot{i}_{rd} \\
\dot{i}_{rq}
\end{bmatrix}
\] (5.25)

For computer simulation, initial values of \(dq\)-axis stator and rotor currents must be known and so also the flux linkages. These are given below:

\[ i_{sd}(0) = \sqrt{2/3} \cdot (3 \cdot (Is/2) \cdot \cos(\theta_i)) \] (5.26)

\[ i_{sq}(0) = \sqrt{2/3} \cdot (3 \cdot (Is/2) \cdot \sin(\theta_i)) \] (5.27)

Similarly we can calculate \(v_{sd}(0), v_{sq}(0)\) and the \(dq\)-axis stator and rotor flux linkages.

### 5.2.6 PRINCIPLE OF VECTOR CONTROL:

Accurate speed control of three phase IM can be achieved by vector control [15]. In speed and position control, the ability to produce a step change in torque on command represents total control over the drives. In vector control of three phase IM drives, the \(d\)-axis is aligned with the rotor flux linkage space vector such that the rotor flux linkage in the \(q\)-axis is zero. Thus we have the following equations:

\[ \lambda_{rq}(t) = 0 \] (5.28)

Using equation 5.28 in equation 5.9 and simplifying,

\[ i_{rq} = - \frac{L_m \cdot i_{sq}}{L_r} \] (5.29)

The condition \(d\)-axis is always aligned with \(\lambda_{r}\), such that \(\lambda_{r} = 0\) also results in \(d\lambda_{rq}/dt = 0\). Using this value of \(\lambda_{r}\) and \(d\lambda_{rq}/dt\) in the \(dq\)-axis equivalent circuit, the new simplified equivalent circuit for vector control of three phase IM is shown in Fig. 5.2 and 5.3.

In vector control, as long as the \(d\)-axis is aligned with rotor flux linkage, the \(q\)-axis rotor flux linkage and its first derivative are zero. Also in a squirrel cage rotor, \(v_{rq} = 0\) and equation 5.14 gives the following equation:
Using equation 5.29 and 5.31 in equation 5.30, the rotor slip speed can be expressed as follows:

\[
\omega_d \frac{\tau}{L} = \frac{L_m \cdot i_{sq}}{\tau_r \cdot \lambda_{rd}} \tag{5.32}
\]

Since flux linkage in the rotor q-axis is zero, the e.m. torque is produced by rotor d-axis flux linkage acting on rotor q-axis current. The e.m. torque Tem is given below:

\[
T_{em} = - \frac{P \cdot \lambda_{rd} \cdot i_{sq}}{2} \tag{5.33}
\]

Using equation 5.29 in equation 5.33, we have the following:

\[
T_{em} = \frac{P \cdot \lambda_{rd} \cdot i_{sq}}{2} \cdot \left( \frac{L_m \cdot i_{sq}}{L_r} \right) \tag{5.34}
\]

### 5.2.7 D-AXIS ROTOR FLUX LINKAGE DYNAMICS:

Referring to Fig.5.2 and using Laplace Transform, we have the following equations [15]:

\[
i_{rd} (s) = \frac{-sL_m \cdot i_{sd} (s)}{R_r + sL_r} \tag{5.35}
\]

Using equation 5.8 and equation 5.31 in equation 5.35 and simplifying,

\[
\lambda_{rd} (s) = \frac{L_m \cdot i_{sd} (s)}{(1 + s \tau_r)} \tag{5.36}
\]

In time domain, equation 5.36 can be expressed as follows:

\[
\frac{d \lambda_{rd}}{dt} + \frac{\lambda_{rd}}{\tau_r} = \frac{L_m \cdot i_{sd}}{\tau_r} \tag{5.37}
\]

The detailed model of the three phase vector controlled IM using Current Regulated PWM inverter is shown in Fig. 5.3 and 5.4. The d-axis winding reference stator current \( i'_{sd} \) controls the rotor flux linkage \( \lambda_{rd} \) and the q-axis winding reference stator current \( i'_{sq} \) controls the rotor e.m. torque Tem. The reference dq-axis stator currents are converted into abc-axis reference stator phase current \( i^*_{a}(t), i^*_{b}(t) \) and \( i^*_{c}(t) \).
A current regulated PWM inverter supplies the current to the three phase IM.

The current references \( i_{sd}^* \) and \( i_{sq}^* \) are generated by cascaded torque, speed and position control loops shown in the block diagram of Fig. 5.4, where \( \theta_{\text{mech}}^* \) is the position reference input. The actual position \( \theta_{\text{mech}} \) and the rotor speed \( \omega_{\text{mech}} \) are measured and the rotor flux linkage \( \lambda_{rd} \) is calculated as shown in Fig. 5.4. For extended speed range operation beyond rated speed flux weakening is implemented.

To design speed loop without torque loop, the torque expression is derived at the rated value of \( i_{sd}^* \).

In steady state under vector control, \( i_{rd} = 0 \) in Fig. 5.2. Using equation 5.8, under vector control in steady state, we have the following equation:

\[
\lambda_{rd} = L_m i_{sd} \quad (5.38)
\]

Substituting equation 5.38 and equation 5.29 into the torque expression of equation 33, we have the following:

\[
T_{em} = \frac{p}{2} \left[ \frac{L_m^2}{L_r} i_{sd}^* i_{sq} \right] = k i_{sq} \quad (5.39)
\]

where \( k \) is a constant. The speed loop diagram is shown in Fig. 5.5, where PI controller constants are calculated on the basis that the cross over frequency of the open loop is 25 rad/sec and the phase margin is 60 degrees.
The stator voltages to be applied can be calculated as follows:

The switching frequency of the PWM converter is maintained constant. The voltage to be applied to the PWM converter in order to get the stator current equal to the reference value is derived below:

The leakage factor \( \sigma \) is defined as follows:

\[
\sigma = 1 - \frac{L_m}{L_s L_r} \quad (5.40)
\]

Using equation 5.8 in equation 5.5, simplifying and using equation 5.40, we have the following:

\[
\lambda_{sd} = \sigma L_s i_{sd} + \frac{L_m \lambda_{rd}}{L_r} \quad (5.41)
\]

Using equation 5.6 and 5.29, we have the following:

\[
\lambda_{sq} = \sigma L_s i_{sq} \quad (5.42)
\]

Using equations 5.41 and 5.42 in equations 5.11 and 5.12 and simplifying, we have the following:

\[
v_{sd} = -R \frac{d}{dt} i_{sd} + \sigma L_s \frac{d}{dt} i_{sd} + \frac{L_m}{L_r} \frac{d}{dt} \lambda_{rd} - \sigma \omega_d L_s i_{sq} \quad \text{(5.43)}
\]

and

\[
v_{sq} = -R \frac{d}{dt} i_{sq} + \sigma L_s \frac{d}{dt} i_{sq} + \frac{\omega_d L_m \lambda_{rd}}{L_r} + \sigma \omega_d L_s i_{sd} \quad \text{(5.44)}
\]

5.2.8 DESIGNING THE PI CONTROLLERS: In equations 5.43 and 5.44, the term \( v_{sd}' \) and \( v_{sq}' \) are due to d and q-axis stator currents. The \( v_{sd\_comp} \) and \( v_{sq\_comp} \) are disturbance terms. These equations are re-written as follows [15]:

\[
v_{sd} = -R \frac{d}{dt} i_{sd} + \sigma L_s \frac{d}{dt} i_{sd} \quad (5.45)
\]

and

\[
v_{sq} = -R \frac{d}{dt} i_{sq} + \sigma L_s \frac{d}{dt} i_{sq} \quad (5.46)
\]

The compensation terms are given below:

\[
v_{sd\_comp} = \frac{L_m}{L_r} \frac{d}{dt} \lambda_{rd} - \sigma \omega_d L_s i_{sq} \quad (5.47)
\]

\[
v_{sq\_comp} = \omega_d L_m \lambda_{rd} + \sigma \omega_d L_s i_{sd} \quad (5.48)
\]

The block diagram is shown in Fig. 5.6. As shown in Fig. 5.6, reference voltages for the stator d and q-axis are generated from stator d and q-axis stator currents \( i_{sd} \) and \( i_{sq} \). Using the calculated value of 0da, the reference phase voltages \( v^*_{a}, v^*_{b}, \) and \( v^*_{c} \) are calculated. The actual phase voltages \( v_{a}, v_{b}, \) and \( v_{c} \) are supplied by the three phase PWM inverter. The voltages \( v'_{sd} \) and \( v'_{sq} \) in Fig. 5.6 are generated by PI controllers in the current loop. Assuming perfect compensation, each channel results in the block diagram shown in Fig. 5.7(A) & (B). The transfer Function \( \text{isd}(s)/v'_{sd}(s) \) and \( \text{isq}(s)/v'_{sq}(s) \) are derived from equation 5.45 and 5.46 respectively. The PI controller for current loop is designed assuming that the bandwidth of the current loop controller is 10 times the bandwidth of the speed loop controller (250 rad/sec) and the phase margin is 60 degrees.
5.3 MODEL OF VECTOR CONTROLLED THREE PHASE IM. DRIVE: In this section the model of the vector controlled three phase IM drive is developed using SIMULINK [51]. The performance of the above IM drive is studied in detail by simulation. The three phase IM drive used here has the parameters given in Table 5.1.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Parameters</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RMS Line to Line Input Supply Voltage</td>
<td>400</td>
<td>Volts</td>
</tr>
<tr>
<td>2</td>
<td>Input Frequency</td>
<td>50</td>
<td>Hz</td>
</tr>
<tr>
<td>3</td>
<td>Power Output</td>
<td>4</td>
<td>kW</td>
</tr>
<tr>
<td>4</td>
<td>RMS Line to Line Machine Voltage</td>
<td>400</td>
<td>Volts</td>
</tr>
<tr>
<td>5</td>
<td>Machine Frequency</td>
<td>50</td>
<td>Hz</td>
</tr>
<tr>
<td>6</td>
<td>No. of Phase</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>No. of Poles</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Stator Resistance Rs</td>
<td>1.405</td>
<td>Ohms</td>
</tr>
<tr>
<td>9</td>
<td>Stator Leakage Inductance Ls</td>
<td>0.005839</td>
<td>Henries</td>
</tr>
</tbody>
</table>
5.3.1 DEVELOPMENT OF THE MODEL: The model of Vector Controlled three phase IM drive developed in SIMULINK using parameters shown in Table 5.1 is shown in Fig. 5.8. The model is developed based on the equations and requirements set forth in Section 5.2. The MATLAB program to calculate the PI controller parameters for the speed control and current control loop, for the IM parameters in Table 5.1, is given in A5.1 Appendix in this chapter together with the simulation results. From the simulation results, the values are tabulated in Table 5.2.

<table>
<thead>
<tr>
<th>SL NO</th>
<th>Rotor Resistance $R_{r'}$</th>
<th>1.395</th>
<th>Ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Rotor Leakage Inductance $L_{lr'}$</td>
<td>0.005839</td>
<td>Henries</td>
</tr>
<tr>
<td>12</td>
<td>Mutual Inductance $L_m$</td>
<td>0.1722</td>
<td>Henries</td>
</tr>
<tr>
<td>13</td>
<td>Moment of Inertia $J$</td>
<td>0.0131</td>
<td>Kg-m^2</td>
</tr>
<tr>
<td>14</td>
<td>Damping Constant $B$</td>
<td>0.002985</td>
<td>Nw-m-sec</td>
</tr>
</tbody>
</table>

### TABLE 5.2: PI Controller Parameters

<table>
<thead>
<tr>
<th>SL NO</th>
<th>SPEED CONTROL LOOP</th>
<th>CURRENT CONTROL LOOP</th>
<th>ROTOR SPEED</th>
<th>INITIAL D-AXIS STATOR CURRENT AMPS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Kp</td>
<td>Ki</td>
<td>Kpi</td>
<td>Kii</td>
</tr>
<tr>
<td>1</td>
<td>0.1257</td>
<td>1.8139</td>
<td>1.7831</td>
<td>662.9626</td>
</tr>
</tbody>
</table>

The model shown in Fig. 5.8 uses the values shown in Table 5.2 for the PI controller parameters for the speed control and current control loop, initial d-axis stator current and the rotor speed set point. The initial d-axis stator current $I_{sd_0}$ is subtracted from the estimated/actual d-axis stator current from the IM model and the difference which gives the d-axis stator reference current $I_{sd*}$ is given to PI controller in the current control loop to generate d-axis stator reference voltage $v_{sd*}$. Similarly the rotor speed set point is subtracted from the actual/estimated rotor speed from the IM model and the difference speed is given to PI controller in the speed control loop to generate q-axis stator current reference $I_{sq*}$. This $I_{sq*}$ is subtracted from the actual/estimated q-axis stator current from the IM model and the difference is given to PI controller in the current control loop to generate q-axis stator reference voltage $v_{sq*}$. The actual/estimated angular position of the stator a-axis reference with respect to the d-axis $\theta_{da_{est}}$, $v_{sd*}$, $v_{sq*}$ are given to three Function blocks in Simulink block set to generate the three phase abc-axis equivalent of stator voltages $v_a$, $v_b$ and $v_c$ [15]. These values of $v_a$, $v_b$ and $v_c$ together with the rotor position $\theta_{da}$ from the IM model are given to two Function blocks to generate the dq-axis equivalent of the stator voltages $v_{sd}$ and $v_{sq}$ [15]. Using $v_{sd}$, $v_{sq}$, rotor speed $\omega$ from the IM model, stator resistance and the stator dq-axis flux linkages as input, Embedded MATLAB Function1 block together with integrators in Fig. 5.8 generate the stator dq-axis flux linkages using equations 5.11 and 5.12. In vector control of three phase IM drive, rotor q-axis flux linkage $\lambda_{rq}$ is set to zero. The equations 5.25 and 5.37 are combined together to generate stator cur -
FIG. 5.8: MODEL OF A THREE PHASE VECTOR CONTROLLED INDUCTION MOTOR DRIVE
rents and the rotor d-axis flux linkage $\lambda_{rd}$ as shown in Fig. 5.8, where the DSP constant1 block together with the LU Inverse1 block calculates the inverse of the stator and rotor inductance matrix defined in equation 5.25. The dq-axis stator and rotor flux linkages given as input to the MUX block is multiplied by the inverse of the stator and rotor inductance matrix using Matrix multiply1 block to generate the dq-axis stator and rotor currents. Using d-axis stator current as input, the two gain blocks, the subtractor and the integrator block calculates rotor d-axis flux linkage $\lambda_{rd}$ using equation 5.37 given above. Using the given IM parameters, computed isq and $\lambda_{rd}$, Embedded MATLAB Function2 block calculates the rotor slip speed $\omega_{dA}$ and the electromagnetic torque $T_{em}$ using equations 5.32 and 5.34 respectively. The load torque $T_L$ is generated using step block which is assumed to vary from 30 Nw-m to 15 Nw-m in 0.1 second. The E.M. torque $T_{em}$ and load torque $T_L$ are used to compute the rotor speed $\omega_{mech}$ according to equation 5.19 using a subtractor block, gain block and integrator as shown in Fig. 5.8. This value of $\omega_{mech}$ is multiplied by the number of pair of poles to get the rotor speed in electrical radians per second which is then added with computed rotor slip speed $\omega_{dA}$ to calculate the synchronous speed $\omega_d$ according to equation 5.15. This value of $\omega_d$ is integrated to get stator angular position with respect to the d-axis $\theta_{da}$, as shown in Fig. 5.8.

These computed values of isd, isq and $\theta_{da}$ are transformed to abc-axis stator currents using three function blocks using the dq-axis to abc-axis transformation [15]. Using this computed values of stator and rotor currents in the abc-axis, Embedded MATLAB Function3 block along with summing and integrating blocks re-estimates slip speed $\omega_{dA\_est}$ and e.m. torque $T_{em\_est}$, $\theta_{da\_est}$ and $\lambda_{rd\_est}$ using equations 5.32, 5.34, 5.37 and 5.15 for comparison and feedback to the actual model of vector controlled three phase IM drive.

5.3.2 SIMULATION RESULTS: The simulation of the vector controlled three phase IM drive was carried out using SIMULINK [51]. The ode15s (stiff/NDF) solver is used. Simulation results for the rotor speed, E.M. Torque, stator currents and the load torque are shown in Fig. 5.9 to 5.12 respectively.

5.3.3 DISCUSSION OF RESULTS: From the simulation results it is seen that as the load torque is varied from 30 Nw-m to 15 Nw-m, the rotor speed from the set point of 149.2257 mech.rad per sec shoots up and finally settles to the set point value. Rotor E.M. torque $T_{em}$ falls from the initial value of 30 Nw-m falls to 15 Nw-m in 0.1 second corresponding to load torque. Stator current initially shoots up and finally settles to a constant value. This shows the accuracy of vector control of three phase IM drive.

5.4 VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC: The vector controlled three phase IM drive whose parameters are given in table 5.1 and 5.2 when fed by a three phase AC to three phase AC MC is studied here using model simulation. SIMULINK is used for model development [51]. The MC is switched by various carrier based modulation algorithms such as by Venturini, Sunter-Clare and Ned Mohan [1-8, 11-17]. The performance of the above IM drive when
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fed by MC using all the above modulation algorithms is presented.

5.4.1: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING VENTURINI MODULATION ALGORITHM: The model of the vector controlled three phase IM drive fed by MC using Venturini modulation algorithm is shown in Fig. 5.13. Here unity input phase displacement factor is assumed. The model of the MC is already explained under section 3.3.3 of chapter III. The vector controlled three phase IM model is the one explained in Section 5.3 above. This vector controlled three phase IM model is used twice one to generate the gate pulses for the MC and the other to replace the hardware component of three Phase IM. The changes in the MC model is explained below:

Here modulation index q is calculated from the vector controlled three phase IM model. The reference value of dq-axis stator voltages vsd*, vsq* and theta_da_est are used to transform dq-axis stator voltage to abc-axis stator voltage as explained in Section 5.3 above. The stator voltage Va thus obtained is multiplied by 1.414 to obtain maximum output voltage per phase Vom. This value of Vom is then divided by maximum input voltage per phase Vim (400*√2/√3 Volts from Table 5.1) to obtain the value of q. This q value is used in the Embedded MATLAB Function to generate the nine modulation functions for the MC switches. These nine modulation functions are compared with a
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FIG. 5.13: VECTOR CONTROLLED THREE PHASE INDUCTION MOTOR DRIVE FED BY MATRIX CONVERTER USING VENTURINI ALGORITHM
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2 kHz saw-tooth carrier and the gate pulses are generated using a second Embedded MATLAB Function as explained in Section 3.3.1 of Chapter III.

5.4.2 SIMULATION RESULTS: The simulation results using SIMULINK are shown in Fig. 5.14. The ode 23tb (Stiff/TR-BDF2) solver is used. From the simulation results it is seen that as the load torque varies from 30 to 15 Nw-M in 0.1 second, the Rotor E.M. torque after the initial transient settles to 15 Nw-M and the rotor speed reaches the set point of 149.2257 mech.radians per second. Rotor torque-speed curve also confirms this value.

5.4.3: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING SUNTER-CLARE MODULATION ALGORITHM: The model of the vector controlled three phase IM drive fed by MC using Sunter-Clare modulation algorithm is shown in Fig. 5.15. The model of the MC is already explained under section 4.2 of Chapter IV. The vector controlled three phase IM model is the one explained in Section 5.3 above. This vector controlled three phase IM model is used twice one to generate the gate pulses for the MC and the other to replace the hardware component of the three Phase IM. The changes in the MC model is explained below:

Here maximum output voltage per phase is calculated from the vector controlled three phase IM model. The reference values of dq-axis stator voltages vsd*, vsq* and theta_da_est are used to transform dq-axis stator voltage to abc-axis stator voltage as explained in Section 5.3 above. The stator voltage Va thus obtained is multiplied by 1.414 to obtain maximum output voltage per phase Vom. This Vom value is used in the Embedded MATLAB Function to generate the nine modulation functions for the MC switches. These nine modulation functions are compared with a 2 kHz saw-tooth carrier and the gate pulses are generated using the same Embedded MATLAB Function as explained in section 4.2.2 of Chapter IV.
5.4.4 SIMULATION RESULTS: The simulation results using SIMULINK are shown in Fig. 5.16 [51]. The ode 15s (Stiff/NDF) solver is used. From the simulation results it is seen that as the load torque varies from 30 to 15 Nw-M in 0.1 second, the Rotor E.M. torque after the initial transient settles to 15 Nw-M and the rotor speed reaches the set point of 149.2257 mech.radians per second. Rotor torque-speed curve also confirms this value.

5.4.5: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING NED MOHAN MODULATION ALGORITHM: The model of the vector controlled three phase IM drive fed by MC using Ned Mohan modulation algorithm is shown in Fig. 5.17. The model of the MC is already explained under section 4.4 of chapter IV. The vector controlled three phase IM model is the one explained in Section 5.3 above. This vector controlled three phase IM model is used twice one to generate the gate pulses for the MC and the other to replace the hardware component of the three Phase IM. The changes in the MC model is explained below:

Here output voltage per phase is calculated from the vector controlled three phase IM model. The reference values of dq-axis stator voltages vsd*, vsq* and theta_da_est are used to transform dq-axis stator voltages to abc-axis stator voltages as explained in Section 5.3 above. The stator voltage Va thus obtained is multiplied by 2/3 (0.6667) and then divided by maximum value of input voltage per phase Vim which is 326.56 from Table 5.1. This gives $k_a = k\sin(\omega \cdot t)$ as per equation 4.33 of Chapter IV. This value of $k_a$ is made to phase lag by 6.667 milliseconds and 13.333 milliseconds, for a 50 Hz output voltage, using two transport delay modules to obtain $k_b$ and $k_c$. These values of $k_a$, $k_b$ and $k_c$ are given to two min-max units to find the minimum and maximum of these three values which are termed min_k_abc and max_k_abc respectively. The input power factor angle $\phi_i$ is zero. The input and output frequency from Table 5.1 along with $k_a$, $k_b$, $k_c$, min_k_abc, max_k_abc, $\phi_i$ and time modules are given as input to the Embedded MATLAB Function to generate the nine modulation functions for the MC switches. These nine modulation functions are then compared with a 2 kHz
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Fig. 5.17: Vector Controlled Three Phase Induction Motor Drive Fed by Matrix Converter Using Ned Mohan Algorithm
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triangle carrier and the gate pulses are generated using another Embedded MATLAB Function as explained in section 4.4.2 of Chapter IV.

5.4.6 SIMULATION RESULTS: The simulation results using SIMULINK are shown in Fig. 5.18 [51]. The ode 15s (Stiff/NDF) solver is used. From the simulation results it is seen that as the load torque varies from 30 to 15 Nw-M in 0.1 second, the Rotor E.M. torque after the initial transient settles to 15 Nw-M and the rotor speed, after the initial overshoot reaches the set point of 149.2257 mech.radians per second. Rotor torque-speed curve also confirms this value.

5.5 DISCUSSION OF RESULTS: The performance of the vector controlled IM drive when fed by MC which are switched by three carrier based modulation techniques such as by Venturini, Sunter-Clare and Ned Mohan algorithm is studied by model simulation. Although all these algorithms causes the rotor speed to reach their set point, it is seen that Sunter-Clare algorithm reaches set point of rotor speed without overshoot, Venturini algorithm with a small overshoot and Ned Mohan algorithm causing large initial overshoot.

5.6 CONCLUSIONS: It is seen by model simulation that the vector controlled three phase IM drive when fed by MC, reaches set point of rotor speed irrespective of the algorithms used for switching the MC bidirectional switches. Accurate control of speed irrespective of load variation is achieved.

A5.1 APPENDIX: The MATLAB m file for calculating the initial conditions and PI controller parameters for the speed control and current control loop of the three phase IM whose parameters are given in Table 5.1 is given below:

```matlab
%%Calculation of Initial Conditions
%%Induction Motor Parameters
%%Narayanaswamy P.R. Iyer
%%Reference: Ned Mohan: "Advanced Electric Drives - Analysis, Control and
```
Rs=1.405;  % IM parameters in Table 5.1
Rr=1.395;
Xls=1.833446;
Xlr=1.833446;
Xm=54.07;
Jeq=0.0131;  % Damping constant neglected being small.
p=4;  % Number of Poles.
% Power output Pout = 4 kVA.
% Steady State Operating Conditions
f=50; VLLrms= 400; s=0.05;                            % phase-a voltage is at its positive peak at t=0
Wsyn=2*pi*f;                                           % synchronous speed in electrical rad/s
Wm=(1-s)*Wsyn;                                         % rotor speed in electrical rad/s
% Phasor Calculations
Va = VLLrms * sqrt(2)/ sqrt(3);                         % Va phasor
% Space Vectors at time t=0 with stator a-axis as the reference
Vs_0 = (3/2) * Va;                                      % Vs(0) space vector
Theta_Vs_0 = angle(Vs_0);                               % angle of Vs(0) space vector
% We will assume that at t=0, d-axis is aligned to the stator a-axis. Therefore, Theta_da_0=0
Theta_da_0 = 0;
Vsd_0 = sqrt(2/3) * abs(Vs_0) * cos(Theta_Vs_0 - Theta_da_0);  %%Similar to Eq.5-26.
Vsq_0 = sqrt(2/3) * abs(Vs_0) * sin(Theta_Vs_0 - Theta_da_0);  %%Similar to Eq.5-27.
% Calculation of machine inductances
Ls = (Xls + Xm) / (2*pi*f);
Lm = Xm / (2*pi*f);
Lr = (Xlr + Xm) / (2*pi*f);
tau_r=Lr/Rr;
% Calculations of dq-winding currents
A = [Rs        -Wsyn*Ls       0         -Wsyn*Lm  ;
     Wsyn*Ls    Rs            Wsyn*Lm    0        ;
     0         -s*Wsyn*Lm     Rr        -s*Wsyn*Lr;...
     s*Wsyn*Lm  0             s*Wsyn*Lr  Rr];  %%Eq. 5-5 to 5-15.
Ainv = inv(A);
V_dq_0=[Vsd_0; Vsq_0; 0; 0];
I_dq_0=Ainv*V_dq_0;
Isd_0=I_dq_0(1)
Isq_0=I_dq_0(2)
Ird_0=I_dq_0(3)
Irq_0=I_dq_0(4)
% Electromagnetic Torque, which equals Load Torque in Initial Steady State
Tem_0 = (p/2) * Lm * (Isq_0 * Ird_0 - Isd_0 * Irq_0)
TL_0 = Tem_0
% Wmech = rotor speed in actual rad/s
Wmech_0=(2/p)*Wm
% Inductance matrix M in Eq. 5-24
M = [Ls 0 Lm 0 ;
     0 Ls 0 Lm;...
     Lm 0 Lr 0;...
     0 Lm 0 Lr];
% dq winding Flux Linkages with the d-axis aligned with the stator a-axis
fl_dq_0 = M * [Isd_0; Isq_0; Ird_0; Irq_0];
\[fl\_sd\_0 = fl\_dq\_0(1)\]
\[fl\_sq\_0 = fl\_dq\_0(2)\]
\[fl\_rd\_0 = fl\_dq\_0(3)\]
\[fl\_rq\_0 = fl\_dq\_0(4)\]

\[[\text{thetar}, fl\_r\_dq\_0]=\text{cart2pol}(fl\_rd\_0, fl\_rq\_0)\]
\[[\text{thetas}, fl\_s\_dq\_0]=\text{cart2pol}(fl\_sd\_0, fl\_sq\_0)\]
\[[\text{theta}Is\_dq, Is\_dq\_0]=\text{cart2pol}(Isd\_0, Isq\_0)\]
\[[\text{theta}Vs\_dq, Vs\_dq\_0]=\text{cart2pol}(Vsd\_0, Vsq\_0)\]

% d-axis is now aligned with the rotor flux which results in the following new values:
\[fl\_rd\_0=fl\_r\_dq\_0 \quad \%\text{fl}_rq\_0\text{ equals zero}\]
\[[fl\_sd\_0, fl\_sq\_0]=\text{pol2cart}(\text{thetas}-\text{thetar}, fl\_s\_dq\_0)\]
\[[Isd\_0, Isq\_0]=\text{pol2cart}(\text{theta}Is\_dq-\text{thetar}, Is\_dq\_0)\]
\[[Vsd\_0, Vsq\_0]=\text{pol2cart}(\text{theta}Vs\_dq-\text{thetar}, Vs\_dq\_0)\]

% Calculations for the controller
\[Wc=25; \quad \%\text{crossover freq in rad/s}\]
\[k=(p/2)*(Lm*Lm/Lr)*Isd\_0;\]
\[\text{PM}=60*pi/180; \quad \%\text{phase margin in rad/s}\]
\[Wc\_kp\_by\_ki=\tan(\text{PM}); \quad \%\text{kp and ki are shown in Fig. 5-8}\]
\[k=\text{Wc}*\text{Wc}^\ast\ast*\text{Ki}/(\text{Wc}^\ast\ast*\text{Kp}+\text{Ki}/\text{Wc})\]

% check to show that at Wc, \ GOLmag=1 and GOLang= (-180 degrees + phase margin of 60 degrees)
\[\text{GOL}=(\text{Kp}+\text{Ki}/(\text{Wc}^\ast\ast))*k/(\text{Jeq}^\ast\ast*\text{Wc})\quad \%\text{open-loop transfer function}\]
\[\text{GOLmag}=\text{abs}(\text{GOL})\]
\[\text{GOLang}=\text{angle}(\text{GOL})\ast180/\pi\]

% PI in current loop
\[\sigma=1-Lm*Lm/(Ls*Lr) \quad \%\text{Eq. 5-40}\]
\[\text{Wei}=10*\text{Wc} \quad \%\text{Current-loop bandwidth is ten times that of the speed loop}\]
\[\text{PMi}=\text{PM}\]
\[\text{Wei}_kpi\_by\_kii=\tan(\text{PMi}-\text{Pi}/2+\text{Atan}(\text{Wei}^\ast\text{Ls}^\ast\sigma^\ast\text{Rs}))\]
\[\text{ki}=\text{Wei}^\ast\text{sqrt}(\text{Rs}^\ast\text{Rs}+((\text{Wei}^\ast\text{Ls}^\ast\sigma)^2)/\text{sqrt}(\text{Wei}_kpi\_by\_kii^2+1))\]
\[\text{kp}=\text{Wei}^\ast\text{sqrt}(\text{Rs}^\ast\text{Rs}+((\text{Wei}^\ast\text{Ls}^\ast\sigma)^2)/\text{sqrt}(\text{Wei}_kpi\_by\_kii^2+1))\]

% check to show that at Wci, \ GOLimag=1 and GOLiang= (-180 degrees + phase margin of 60 degrees)
\[\text{GOLi}=(\text{Kpi}+\text{Kii}/(\text{Wci}^\ast\ast))/(\text{Rs}^\ast\ast\text{Wci}^\ast\ast\text{Ls}^\ast\sigma)\]
\[\text{GOLimag}=\text{abs}(\text{GOLi})\]
\[\text{GOLiang}=\text{angle}(\text{GOLi})\ast180/\pi\]

---------------------------------------
The simulation results of the above MATLAB m file are given below:
\[\text{Isd}_0 = \]
\[12.8478\]
\[\text{Isq}_0 = \]
\[-8.0860\]
\[\text{Ird}_0 = \]
\[-13.0734\]
\[\text{Irq}_0 = \]
\[1.2962\]
\[\text{Tem}_0 = \]
\[30.6555\]
\[\text{TL}_0 = \]
\[30.6555\]
\[ W_{\text{mech}}_0 = 149.2257 \]
\[ f_{l_{sd}}_0 = 0.0362 \]
\[ f_{l_{sq}}_0 = -1.2158 \]
\[ f_{l_{rd}}_0 = -0.1151 \]
\[ f_{l_{rq}}_0 = -1.1610 \]
\[ \text{thetar} = -1.6696 \]
\[ f_{l_{r_{dq}}}_0 = 1.1667 \]
\[ \text{thetas} = -1.5411 \]
\[ f_{l_{s_{dq}}}_0 = 1.2163 \]
\[ \text{theta}_\text{Is}_{dq} = -0.5617 \]
\[ I_{s_{dq}}_0 = 15.1806 \]
\[ \text{theta}_\text{Vs}_{dq} = 0 \]
\[ V_{s_{dq}}_0 = 400.0000 \]
\[ f_{l_{rd}}_0 = 1.1667 \]
\[ f_{l_{sd}}_0 = 1.2063 \]
\[ f_{l_{sq}}_0 = 0.1559 \]
\[ I_{sd}_0 = 6.7789 \]
\[ I_{sq}_0 = 13.5829 \]
\[ V_{sd}_0 = -39.4661 \]
\[ V_{sq}_0 = 398.0483 \]
ki = 1.8139
kp = 0.1257
GOL = -0.5000 - 0.8660i
GOLmag = 1
GOLang = -120.0000
sigma = 0.0645
Wci = 250
PMi = 1.0472
Wci_kpi_by_kii = 0.6724
kii = 662.9626
kpi = 1.7831
GOLi = -0.5000 - 0.8660i
GOLimag = 1.0000
GOLiang = -120.0000
Chapter VI
Real Time Hardware-in-the-Loop Simulation of A Three Phase AC to Single Phase AC Matrix Converter

6.1 INTRODUCTION: Hardware in the Loop (HIL) is a technique used in the development and testing of complex real time Embedded Systems. HIL simulation provides an effective platform by adding the complexity of the plant under control to the test platform. The complexity of the plant under control is included in test and development by adding a mathematical representation or model of all related system under consideration [55]. These mathematical representations are referred to as the “plant simulation”. The embedded system to be tested interacts with this plant simulation [55]. The ability to design and automatically test power electronics systems with HIL simulations will reduce development cycle, increase efficiency, improve reliability and safety of these systems for large number of applications [55]. There are at least three strong reasons for using hardware-in-the-loop simulation for power electronics, namely: 1) reduction of development cycle, 2) demand to extensively test control hardware and software in order to meet safety and quality requirements, and 3) need to prevent costly and dangerous failures [55].

6.2 MODEL OF THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER: The model of the three phase AC to Single phase AC Matrix converter (MC) is developed using Venturini modulation algorithm assuming unity input phase displacement factor [1-4]. A schematic of the three phase AC to single phase AC MC is shown in Fig. 6.1. Here there are three bidirectional switches connected to each input phase A, B, C and all these switches are connected to one output phase a in series with a resistive load. The 3 X 1 matrix converter shown in Fig.6.1 connects the three phase ac source to the single phase load. The switching Function for a 3 X 1 matrix converter can be defined as follows [4-5]:

![Diagram of Three Phase AC to Single Phase AC Matrix Converter](image-url)
\[ S_{kj} = \begin{cases} 
1 & \text{when } S_{kj} \text{ is closed} \\
0 & \text{when } S_{kj} \text{ is open} 
\end{cases} \quad (6.1) \]

The above constraint can be expressed in the following form:
\[ S_{kJ} + S_{Bj} + S_{Cj} = 1 \quad (6.2) \]

Here the input-output voltage relation simplifies to the equation 6.3 below:
\[ \begin{bmatrix} v_a \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \end{bmatrix} \begin{bmatrix} v_a \\ v_B \\ v_C \end{bmatrix} \quad (6.3) \]

Similarly the input-output current relation can be expressed as in equation 6.4 below:
\[ \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (6.4) \]

where \( v_a \) and \( i_A, i_B, i_C \) are the output voltage and input currents respectively.

To determine the behaviour of the MC at output frequencies well below the switching frequency, a modulation duty cycle can be defined for each switch. The modulation duty cycle \( M_{kj} \) for the switch \( S_{kj} \) in Fig.6.1 is defined as in equation 6.5 below.
\[ M_{kj} = \frac{t_{kj}}{T_s} \quad (6.5) \]

where \( t_{kj} \) is the on time for the switch \( S_{kj} \) between input phase \( K \in \{A,B,C\} \) and \( j \in \{a\} \) and \( T_s \) is the period of the PWM switching signal or sampling period. In terms of the modulation duty cycle, equations 6.2, 6.3 and 6.4 can be rewritten as given below:
\[ \begin{bmatrix} v_a \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} M_{Aa} & M_{Ba} & M_{Ca} \end{bmatrix} \begin{bmatrix} v_a \\ v_B \\ v_C \end{bmatrix} \quad (6.6) \]

\[ \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} M_{Aa} & M_{Ba} & M_{Ca} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (6.7) \]

\[ M_{Aa} + M_{Ba} + M_{Cj} = 1 \quad (6.8) \]

The Venturini modulation algorithm for a three phase AC to three phase AC MC is already presented in Section 3.2 of Chapter III. For unity input phase displacement factor, the modulation function can be expressed as in equation 6.9 below:
\[ M_{kj} = \frac{t_{kj}}{T_s} = \frac{1}{3} + \frac{2v_k.v_j}{3v_m^2} \quad (6.9) \]

where \( k = A, B, C \) and \( j = a \)

In terms of the modulation duty cycle, equations 6.2, 6.3 and 6.4 can be rewritten as given below:
\[ \begin{bmatrix} v_a \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} M_{Aa} & M_{Ba} & M_{Ca} \end{bmatrix} \begin{bmatrix} v_a \\ v_B \\ v_C \end{bmatrix} \quad (6.6) \]

\[ \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} M_{Aa} & M_{Ba} & M_{Ca} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (6.7) \]

\[ M_{Aa} + M_{Ba} + M_{Cj} = 1 \quad (6.8) \]

The Venturini modulation algorithm for a three phase AC to three phase AC MC is already presented in Section 3.2 of Chapter III. For unity input phase displacement factor, the modulation function can be expressed as in equation 6.9 below:
\[ M_{kj} = \frac{t_{kj}}{T_s} = \frac{1}{3} + \frac{2v_k.v_j}{3v_m^2} \quad (6.9) \]

where \( k = A, B, C \) and \( j = a \)
6.3 MODEL DEVELOPMENT: To study the behaviour of the three phase AC to single phase AC MC using Venturini Modulation algorithm assuming unity input phase displacement factor, a model of this matrix converter is developed in SIMULINK [51]. The data shown in Table 6.1 are used to develop the model. The MC switching is developed based on equations 6.9. A resistive load of 4700 Ohms is used.

6.3.1 MODEL OF THREE PHASE AC TO SINGLE PHASE AC MC USING VENTURINI ALGORITHM: The model of the three phase AC to single phase AC MC is developed using Venturini second method discussed in Section 3.3.3 of Chapter III. Unity input Phase Displacement factor is assumed. The model is developed using SIMULINK [51]. The data shown in Table 6.1 is used to develop the model. The model simulation is carried out for both three phase sine wave input voltages as well as for three phase square wave input voltages, for the parameters in Table 6.1. The model is shown in Fig. 6.2. The bidirectional switches are shown for both three phase sine wave and square wave inputs. The gate pulse for the three bidirectional switches are developed using Embedded MATLAB function, saw-tooth carrier and logic gates. Embedded MATLAB function is used to realize equations 3.9, 3.11 of Chapter III and the three modulation functions for output phase a, defined in equation 6.9. Using these three modulation functions and a 5 kHz saw-tooth carrier as inputs, gate timing pulses are generated using comparators and logic gates for the three bidirectional switches, as shown in Fig. 6.2. The three phase sine wave input has a RMS value of 123 Volts between line and neutral and frequency 50 Hz. In addition, model is shown to generate three phase 123 Volts (RMS), 50 Hz square wave input, using three threshold switches. When the second input to each of the threshold switches which are three phase 50 Hz sine wave voltages crosses zero and goes positive and negative, the output of the threshold switch goes +123 Volts and -123 Volts respectively. The modulation index and output frequency are set to 0.5 and 50 Hz respectively.

6.3.2 SIMULATION RESULTS: The simulation of the above model was carried out in SIMULINK [51]. The ode15S(Stiff/NDF) solver is used in both cases. Simulation results for three phase 50 Hz square wave input voltage and three phase sine wave input voltage are discussed below:

(a) Response to Three Phase Square Wave Input Voltage: The simulation result of the output voltage for the three phase 123 Volts(RMS), 50 Hz square wave input is shown in Fig. 6.3. The output voltage across the load resistor is found to be 123 Volts(RMS) which is shown in Fig. 6.5. The three Phase 50 Hz square wave input voltage is shown in Fig. 6.4 and its RMS value is shown in Fig. 6.6.

(b) Response to Three Phase Sine Wave Input Voltage: The response to the three phase 50 Hz sine wave input voltage is shown in Fig. 6.7 which shows the three phase sine wave input voltage, the output voltage across the resistive load and load current.
Chapter VI: Real Time Hardware-in-the-Loop Simulation of A Three Phase AC to Single Phase AC Matrix Converter

FIG. 6.2: SIMULINK MODEL FOR THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER
(A): Three Phase Sine Wave Input; (B): Three Phase Square Wave Input
Chapter VI: Real Time Hardware-in-the-Loop Simulation of A Three Phase AC to Single Phase AC Matrix Converter
Simulation results for the three phase 50 Hz square wave input voltage are tabulated in Table 6.2.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Input Voltage</th>
<th>Output Voltage</th>
<th>Modulation Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Three Phase Square Wave</td>
<td>Single Phase Square Wave</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>50 Hz</td>
<td>50 Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>123 V (L to N)</td>
<td>123 V (L to G)</td>
<td></td>
</tr>
</tbody>
</table>

### 6.4 EXPERIMENTAL VERIFICATION USING dSPACE HARDWARE CONTROLLER BOARD:

The first experiment is developed using dSPACE DS1104 hardware controller board to study the gate drive waveforms for three phase 50 Hz AC to single phase 50 Hz AC MC [54]. The experimental set up is shown in the photograph in Fig. 6.8. The method of interfacing the

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**dSPACE Experimental set up for the Gte Drive of a 3 X 1 Matrix Converter**

The dSPACE hardware controller board to the SIMULINK model of three phase AC to single phase AC MC is shown in Fig. 6.9. The DS1104 has a main processor MPC8240 and a slave DSP TMS320F240 [54]. In Fig. 6.9, the Embedded MATLAB Function generates the three modulation functions MAa, MBa and MCa. The comparator block, A<=B provides output HIGH when saw-tooth carrier VSAW input given to node A is less than or equal to the input given to node B. The comparator connected to VSAW and MAa produces output tAa and that connected to VSAW and
FIG. 6.9: DSPACE DS1104 HARDWARE CONTROLLER BOARD INTERFACE TO THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER SIMULINK MODEL
(MAa+MBa) produces output tABa. The outputs tAa and tABa are connected to EXCLUSIVE-OR gate to obtain tBa and the output tABa is inverted using a NOT gate to obtain tCa. tAa, tBa and tCa form the gate pulses for the bidirectional switches connected between phases Aa, Ba and Ca respectively in Fig. 6.1. The photograph of the waveform of the gate drive obtained for the above experiment is shown in Fig. 6.10 and that using control desk is shown in Fig. 6.11.

The second experiment is developed to observe the performance of an actual Three phase 50 Hz AC to Single Phase AC MC when switching of bidirectional switches is done using the above gate pulse drive. The hardware set up for this experiment is shown in Fig. 6.12. Fig.6.9(B) which is a high input impedance op.amp. shows the method of connecting the output of DAC 1 of DS1104 hardware controller board to the bidirectional switch. Similar connections apply to DAC 2 and DAC 3 of DS1104 hardware controller board. All IGBTs used in the experiment were STGP14NC60KD with a voltage and current rating of 600 V, 25 A. This MC board is shown in Fig. 6.13. The Texas Instruments quad TL084 op.amp is used for isolation as this has a high input impedance of the order of $10^{12}$ Ohms and slew rate of the order of 13 V/μsec. Although Venturini algorithm is developed for three phase sine wave AC input voltage only, in this experiment, a three phase 50 Hz square wave AC input voltage is used. The magnitude of the input voltage used is 123 Volts (RMS) line to neutral.
The waveform of this input voltage for the reference phase is shown in Fig. 6.14 in both the channels. The gate drive pattern obtained is already shown in Fig. 6.10 and 6.11. The output voltage observed across the load resistor is found to be 86 Volts(RMS) and this waveform is shown in Fig. 6.15. In this experiment a modulation index of 0.5 is used. The dSPACE hardware controller board experimental result is tabulated in Table 6.3.

6.5 DISCUSSION OF RESULTS: The Real time Hardware in the Loop simulation of the above Three Phase AC to Single Phase AC MC is carried out using dSPACE [54]. The real time platform is
### TABLE 6.3: dSPACE Experimental Results

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Input Voltage</th>
<th>Output Voltage</th>
<th>Modulation Index</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Nature</td>
<td>Frequency</td>
<td>RMS Value</td>
</tr>
<tr>
<td>1)</td>
<td>Three Phase Square Wave</td>
<td>50 Hz (L to N)</td>
<td>123 V</td>
</tr>
</tbody>
</table>
developed using dSPACE DS 1104 hardware controller board. In this dSPACE experiment, a three phase 50 Hz square wave AC from a three phase inverter is used as the input. A resistive load is used for this experiment. The experimental results obtained are shown. The experimental results are verified by simulation. Venturini modulation algorithm assuming unity input phase displacement factor is used for the real time experiment on the above MC and also for the verification by simulation.

6.6 CONCLUSIONS: The waveform observed using oscilloscope almost well agree with the one obtained by simulation of the model. However the RMS value of the output voltage by experiment has a variation of 30% compared to the one obtained by simulation of the model. The bidirectional IGBT switch models use RC snubber for convergence of simulation, whereas no such snubber is present in the IGBTs used for the experiment.
Chapter VII

Three Phase AC to Three Phase AC Capacitor Clamped Multilevel Matrix Converter

7.1 INTRODUCTION: Multilevel technology is a good solution for medium and high voltage power conversion [18-22]. There are three kinds of multilevel converters namely diode clamped [20], capacitor clamped [21-22] and cascade [23]. Among them, capacitor clamped multilevel converter is the most suitable topology for direct AC to AC conversion [21-22]. This chapter describes the multilevel matrix converter with a capacitor clamped or flying capacitor or multicell topology [18-19]. Venturini algorithm is used for generating gate pulses for multilevel matrix converter, the application of which is different from the conventional single cell matrix converter. Simulation results using the software SIMULINK are provided. The simulation results by SIMULINK are reviewed or re-examined and additional supplementary simulation results are provided using the software PSCAD.

7.2 MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE: The three phase capacitor clamped multilevel matrix converter (MMC) with three flying capacitors (FC) per output phase is shown in Fig. 7.1 [18-19]. The IGBT switches in Fig. 7.1 are bidirectional. The analysis is given below:

Consider switches SAa1, SAa2, SBa1 and SBa2 and capacitor C1. Let all the four switches be identical with off resistance Roff. With all four switches off, applying Kirchoff's law to the above four switches with C1 connected to supply \( V_{AB} \), we can express the voltage \( V_{c1} \) across C1 as follows:

\[
V_{c1} = \frac{V_{AB}}{4 \times R_{off}} \times 2 \times R_{off} = \frac{(V_A - V_B)}{2}
\]  

(7.1)

where \( V_{c1} \) has the polarity positive at the top and negative at the bottom plate. The same analysis holds good for other flying capacitors C2 to C9. Thus \( V_{c1} = V_{c4} = V_{c7}, V_{c2} = V_{c5} = V_{c8} \) and \( V_{c3} = V_{c6} = V_{c9} \).

In Fig. 7.1, for the above switch combinations, Table 7.1 is valid. A detailed table for output
phase a is shown in Table 7.2 [18-19]. Capacitance of the flying capacitor is selected using equation 2 below:

\[ C = \frac{I_o}{\Delta V_c \cdot p \cdot f_{sw}} \]  

(7.2)

where \( I_o \) is the peak value of load current, \( p \) is the number of cells per output phase and \( f_{sw} \) is the switching frequency and \( \Delta V_c \) is the flying capacitor percentage voltage ripple [18-19]. The switching function for the bidirectional switches in Fig. 7.1 can be expressed as in equation 7.3 below:

\[
S_{ijk} = \begin{cases} 
0 & \text{when switch open} \\
1 & \text{when switch closed} 
\end{cases} 
\]

(7.3)

\[
S_{Ajk} + S_{Bjk} + S_{Cjk} = 1 
\]

\[ i \in \text{Input Phase} \quad A,B,C; \quad j \in \text{Output Phase} \quad a,b,c \quad \text{and} \quad k = \text{Switch Column Count} \quad 1, 2 \]

The modelling equation referring to Table 7.2 for the output voltage can be expressed as in equation 7.4 and referring to Fig. 7.1, the modelling equation for the three phase input currents can be expressed as in equation 7.5 below:

7.3 CONTROL OF MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE BY VENTURINI METHOD: Let the input and output voltages be expressed as in equation 3.9 and 3.11 in Chapter III. For unity input phase displacement factor, the nine modulation functions for a three phase AC to three phase AC conventional matrix converter is given in equation 3.17 and its validity for three phase cosine wave and sine wave input and output voltages is proved in A3.3 Appendix in Chapter III. Here the modified modulation function assuming unity input phase displacement factor for the three phase MMC with eighteen bidirectional switches shown in Fig. 7.1, is given in equation 7.6 below:
Chapter VII: Three Phase AC to Three Phase AC Capacitor Clamped Multilevel Matrix Converter

\[\begin{bmatrix}
v_a \\
v_b \\
v_c
\end{bmatrix} = \begin{bmatrix}
S_Aa & S_Ab & S_Ac \\
S_Ba & S_Bb & S_Bc \\
S_Ca & S_Cb & S_Cc
\end{bmatrix} \begin{bmatrix}
v_A \\
v_B \\
v_C
\end{bmatrix} + \begin{bmatrix}
w_A/2 \\
w_B/2 \\
w_C/2
\end{bmatrix}
\]

where
\[S_{Aa} = S_{Aa1} \cap S_{Aa2}, S_{Ba} = S_{Ba1} \cap S_{Ba2}, S_{Ca} = S_{Ca1} \cap S_{Ca2}, S_{C1} = S_{C10} \cup S_{C11} \cup S_{C12} \cup S_{C13}, S_{Ab} = S_{Ab1} \cap S_{Ab2}, S_{Cb} = S_{Cb1} \cap S_{Cb2}, S_{Cd} = S_{Cd1} \cap S_{Cd2}, S_{Ac} = S_{Ac1} \cup S_{Ac2} \cup S_{Ac3} \cup S_{Ac4}, S_{Cc} = S_{Cc1} \cup S_{Cc2} \cup S_{Cc3} \cup S_{Cc4}
\]

\[i_A = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix}, \quad i_A = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
S_{Aa} \cup S_{Ab} \cup S_{Ac} \\
S_{Ba} \cup S_{Bb} \cup S_{Bc} \\
S_{Ca} \cup S_{Cb} \cup S_{Cc}
\end{bmatrix}, \quad i_A = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix}
\]

where
\[S_{Aa} = S_{Aa1} \cap S_{Aa2}, S_{Ab} = S_{Ab1} \cap S_{Ab2}, S_{Ba} = S_{Ba1} \cap S_{Ba2}, S_{Ca} = S_{Ca1} \cap S_{Ca2}, S_{Cb} = S_{Cb1} \cap S_{Cb2}, S_{Ac} = S_{Ac1} \cap S_{Ac2}, S_{Cc} = S_{Cc1} \cap S_{Cc2}
\]

\[M_{ijk} = \frac{i_{jk}}{T_s} = \frac{1}{3} \left[ 1 + \frac{2v_i v_j}{3V_{m}^2} \right] \quad (7.6)
\]

for \(i \in A, B, C\) and \(j \in a, b, c\) and \(k \in 1, 2\).

Signals controlling switches in individual cells of the converter should be shifted with respect to each other by an angle of \(2\pi/p\), where \(p\) is the number of switching cells which in this case is two. Displacement of carrier signals involved in the control of switches \(S_{ij}\) and \(S_{ij2}\) is \(T_{sw}/2\), where \(T_{sw} = 1/f_{sw}\) is the carrier switching period. Duty cycles for switch group \(S_{ij}\) are by comparison of modulation function with the saw-tooth carrier starting from the origin and that for switch group \(S_{ij2}\) are by comparison of the modulation functions with the saw-tooth carrier phase shifted by \(T_{sw}/2\) or \(\pi\) radians [19].
7.4 OUTPUT FILTER: The output filter circuit shown in Fig. 7.1 is a RLC circuit, with \( R_f, L_f \) and \( C_f \) connected in series whose resonant frequency matches with the carrier switching frequency \( f_{sw} \) [19], as given below:

\[
f_{SW} = \frac{1}{2\pi \sqrt{L_f C_f}}
\]  

(7.7)

7.5 MODEL DEVELOPMENT: The model of the three phase AC to three Phase AC MMC with three flying capacitors per output phase using SIMULINK [51] is shown in Fig. 7.2. The model parameters are shown in Table 7.3. The modulation function shown in equation 7.6 is used to calculate the duty-cycle for the bidirectional switches. In Fig. 7.2, the Embedded MATLAB Function with the inputs \( q, V_{im}, f_i, f_o \) and time module calculates the nine modulation for the three phase input and output voltages defined in equation 3.9 and 3.11 of Chapter III, each phase voltage corresponding to input and output duty phase shifted by \( \pi/2 \) radians. The switching pulses for the nine switches starting from SAa1 to SCc1 in the first column of Fig. 7.1 are obtained by comparison of the respective modulation functions with a 5 kHz saw-tooth waveform VSAW1 and applying logic operation using a second Embedded MATLAB Function. The same for the other group of bidirectional switches SAa2 to SCCc2 in the second column of Fig. 7.1 are obtained by comparing the respective modulation functions with another 5kHz saw-tooth waveform VSAW2 which is phase shifted by \( \pi \) radians or \( T_{sw}/2 \) seconds \( (1/(2*f_{sw})) \) from the first saw-tooth waveform VSAW1 and applying logic operation using a third Embedded MATLAB Function. The source code for the logic operation to generate the gate pulses for the two groups of nine bidirectional switches is the same as in section 3.3.1 of Chapter III. The only difference is that the second Embedded MATLAB Function compares the nine modulation functions with saw-tooth carrier VSAW1 and performs logic operation to generate gate pulses tAa1 to tCc1 for the nine switches in the first column of Fig. 7.1 and the third Embedded MATLAB Function compares the nine modulation functions with saw-tooth carrier VSAW2 and performs logic operation to generate gate pulses tAa2 to tCc2 for the nine switches in the second column of Fig. 7.1. The output filter parameter is chosen by assuming a 10 Ohms resistance, 2 milli Henry inductance and the output filter capacitor using equation 7.7 for the carrier switching frequency \( f_{sw} \) in Table 7.3. The flying capacitor C1 to C9 in Fig. 7.1 is selected by assuming a peak value of
FIG. 7.2: MODEL OF THREE PHASE AC TO THREE PHASE AC MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE
load current of 2 Amps, a voltage ripple of ΔVc of 20% for the carrier switching frequency fsw in Table 7.3.

7.5.1 SIMULATION RESULTS: The simulation of the three phase MMC with three FC per output phase for the data in Table 7.3 is carried out using SIMULINK [51]. The Fixed step ode5 (Dormand-Prince) solver is used. Harmonic Spectrum of the Line to neutral output voltage, Phase A Input Current and Line to Line output voltage are shown in Fig. 7.3. to Fig. 7.5 respectively. The simulation results for the three phase Line to neutral output voltage, Phase A input current, three phase Line to Line output voltage and three phase load current are shown in Fig. 7.6 to Fig. 7.9 respectively. The two 5 kHz saw-tooth carrier and the gate pulse for the nine group of bidirectional switches in the first and second column of Fig. 7.1 are shown in Fig. 7.10 and 7.11(A) and (B) respectively. The simulation results from the Harmonic Spectrum are tabulated in Table 7.4.

7.5.2 DISCUSSION OF RESULTS: The simulation results for the line to neutral and line to line output voltage indicate severe voltage unbalance for output phase b for the former case and the phase b-c for the later. This in turn has caused load current unbalance. Therefore the model for the above MMC with three FC per output phase has been reviewed or re-examined using the software PSCAD.

7.6 SIMULATION OF THREE PHASE MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE USING PSCAD: The simulation of the three phase MMC with three FC has been re-examined here using the software PSCAD [53] for reasons mentioned in section 7.5.2. The parameters given in Table 7.3 is used. The complete model of the above mentioned MMC is shown in Fig. 7.12 using PSCAD [53]. The three phase sine wave input and output voltages to develop nine modulation functions are developed using the AM/FM/PM modulator in the Continuous System Model Functions (CSMF) library. The nine modulation functions for the bidirectional switches are also developed using adders, multipliers and dividers in the CSMF library. The two saw-tooth carrier signals VSAW1 and VSAW2 having switching frequency fsw of 5 kHz with a phase difference of π radians (1/(2*fsw) seconds) are developed using two X-Y Transfer Function block also in the CSMF library. The voltmeter, ammeter, FFT and THD measurement blocks are from the Meters library. The three phase AC source for the MMC is from the sources library, the elements resistor, inductor, capacitor are from Passive Elements library and the bidirectional IGBT switches are from the HVDC, FACTS and Power Electronics library.

The gate pulse for the group of switches in the first column of Fig. 7.1 is by comparison with saw-tooth carrier VSAW1 and that for the second column is by comparison with VSAW2. To generate gate pulse for switch SAA1 in Fig. 7.1, the modulation function MAA is compared with VSAW1. The comparator output tAA1 is HIGH if VSAW1 is less than or equal to MAA, else its output is LOW. Similarly the sum of the modulation functions (MAA + MBA) is compared with VSAW1 in a second comparator whose output tABA1 is HIGH if VSAW1 is less than or equal to (MAA + MBA), else its
### TABLE 7.4: PH3 MMC with Three FC – SIMULINK Simulation Results

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Topology</th>
<th>Parameters</th>
<th>Line to Neutral Output Voltage</th>
<th>Line to Line Output Voltage</th>
<th>Phase A Input Current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Peak Fundamental (Volts)</td>
<td>T.H.D. (p.u.)</td>
<td>Peak Fundamental (Volts)</td>
</tr>
<tr>
<td>1)</td>
<td>Three phase MMC With THREE FC</td>
<td>Table 7.3</td>
<td>156.1</td>
<td>0.9837</td>
<td>323.9</td>
</tr>
</tbody>
</table>

**Figure 7.2**: Three Phase MMC with three FC per output phase - Line to neutral output voltage and harmonic spectrum.

**Figure 7.4**: Three Phase MMC with three FC per output phase - Phase A input current and harmonic spectrum.

**Figure 7.6**: Three Phase MMC with three FC per output phase - Line to line output voltage and harmonic spectrum.
Chapter VII: Three Phase AC to Three Phase AC Capacitor Clamped Multilevel Matrix Converter
output is LOW. The pulse outputs tAa1 and tABa1 are given to EXCLUSIVE-OR gate to obtain gate pulse tBa1. Gate pulse tCa1 is obtained by inverting tABa1 using a NOT gate. Similar method is adopted with VSAW2 for the group of bidirectional switches in the second column of Fig. 7.1.

7.6.1 SIMULATION RESULTS: The simulation results for the three phase line to neutral and line output voltages, Phase A input current, Load current, Harmonic spectrum and THD of line to neutral, line to line output voltages and input current, and the gate pulses to the three groups of switches in the first and second column of Fig. 7.1 corresponding to output phase a are shown in Fig. 7.13. The simulation results are tabulated in Table 7.5.

<table>
<thead>
<tr>
<th>SL.No.</th>
<th>Topology</th>
<th>Parameters</th>
<th>Line to Neutral Output Voltage</th>
<th>Line to Line Output Voltage</th>
<th>Phase A Input Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Three Phase MMC With THREE FC</td>
<td>Table 7.3</td>
<td>155.17</td>
<td>1.0278</td>
<td>266.7</td>
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</table>

7.7 DISCUSSION OF RESULTS: Examination of the waveforms for all the three phases relating to line to neutral output voltage, line to line output voltage, input current, load current and the peak fundamental magnitude and THD of the first three quantities above obtained by simulation of the model using SIMULINK and PSCAD reveals that there is a serious error with regard to the simulation results using SIMULINK. The simulation results using PSCAD indicate a closely well balanced line to neutral, line to line voltages and load current.

7.8 MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE: This section on capacitor clamped three phase AC to three phase AC Multilevel Matrix Converter (MMC) with SIX flying capacitors (FC) per output phase is a development based on the method of analysis for three phase AC to three phase AC MMC with three FC presented in section 7.2 above. The above mentioned MMC with six FC is shown in Fig. 7.14. This topology has a total of nine bidirectional switches in each output phase. Three bidirectional switches are in series between each input phase and the output phase. A total of six flying capacitors per output phase, three in series in two groups are connected as in Fig. 7.14. The analysis is carried out below:

Referring to Fig. 7.15, assume that all the nine bidirectional switches connected to each output phase are identical having an off resistance of Roff. Then a total resistance of 6*Roff is coming in series across the input line to line voltage VAB, a resistance of 2*Roff and 4*Roff are coming in series across the voltage of flying capacitors C11 and C12 in the output phase a of Fig. 7.14, where VAB is (VA – VB). Then by potential divider action the voltage across flying capacitor C11 and C12 are
(VAB/3) and (2*VAB/3) respectively, with polarity positive at the top and negative at the bottom plate. This voltage levels are shown in Fig. 7.15. Then applying KVL to the groups of switches connected between input phase A, B and the output phase a, the truth table shown in Table 7.6 is valid. Table 7.6 is derived in Appendix A7.1.

The complete truth table for all the bidirectional switches connected between input phase A, B and C and the output phase a is shown in Table 7.7. From Table 7.7, it is clear that the output phase to neutral voltage has ten voltage levels. The flying capacitor is selected according to equation 7.2 [19].

![Diagram showing the three-phase AC to three-phase AC capacitor clamped multilevel matrix converter](image)

**TABLE 7.6: Truth Table for PH3 MMC with Six FC**

<table>
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<tr>
<th>Sl.No.</th>
<th>SAa1</th>
<th>SAa2</th>
<th>SAa3</th>
<th>SBa1</th>
<th>SBa2</th>
<th>SBa3</th>
<th>Output Voltage Van (Volts)</th>
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<td>1</td>
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<td>VB</td>
</tr>
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<td>SBa2</td>
<td>SBa3</td>
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</tr>
</tbody>
</table>

### 7.8.1 CONTROL OF MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE BY VENTURINI METHOD:

Let the input and output voltages be expressed as in equation 3.9 and 3.11 in Chapter III. For Unity input phase displacement factor, the nine modulation functions for a three phase AC to three phase AC conventional matrix converter is given in equation 3.17 and its validity for three phase cosine wave and sine wave input and output voltages is proved in A3.3 Appendix in Chapter III. Here the modified modulation function assuming unity input phase displacement factor for the twenty seven bidirectional switches of the three phase MMC shown in Fig. 7.14 is given below:

$$M_{ijk} = \frac{t_{ijk}}{T_s} = \left[ \frac{1}{3} + \frac{2v_i v_j}{3V_{cm}^2} \right]$$  \hspace{1cm} (7.8)

for \( i \in A, B, C \) and \( j \in a, b, c \) and \( k \in 1, 2, 3 \).

Signals controlling switches in individual cells of the converter should be shifted with respect to each other by an angle of \( 2\pi/p \), where \( p \) is the number of switching cells which in this case is three. Displacement of carrier signals involved in the control of switches \( S_{ij1}, S_{ij2} \) and \( S_{ij3} \) is \( T_{sw}/3 \) and \( 2T_{sw}/3 \) respectively where \( T_{sw} = 1/f_{sw} \) is the carrier switching period. Duty cycles for switch group \( S_{ij1} \) are by comparison of modulation function with the saw-tooth carrier starting from the origin, that for switch group \( S_{ij2} \) and \( S_{ij3} \) are by comparison of the modulation functions with the saw-tooth carrier phase shifted by \( T_{sw}/3 \) or \( 2\pi/3 \) radians and \( 2T_{sw}/3 \) or \( 4\pi/3 \) radians respectively [19].

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The output filter is a R-L-C series circuit which is set to resonate at the carrier switching frequency and whose values are selected according to equation 7.7 [19].

7.8.2 SIMULATION OF THREE PHASE MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE USING PSCAD: The simulation of the three phase MMC with six FC has been carried out here using the software PSCAD [53] for reasons mentioned in section 7.5.2. The parameters given in Table 7.3 is used. The complete model of the above mentioned MMC is shown in Fig. 7.16 using PSCAD [53]. The three phase sine wave input and output voltage modules for generating the modulation functions and the method of generation of the nine modulation functions for the bidirectional switches are already explained in section 7.6 above. The three saw-tooth carrier signals VSAW1, VSAW2 and VSAW3 having switching frequency fs of 5 kHz with a phase difference of 2π/3 and 4π/3 radians (1/(3*fs) seconds and 2/(3*fs) seconds) are developed using three X-Y Transfer Function block also in the CSMF library. The gate pulse for the group of switches in the first column of Fig. 7.14 is by comparison of the modulation functions MAa and (MAa+MBa) with saw-tooth carrier VSAW1 using two comparators and giving the output of these two comparators to logic gates which is already explained in section 7.6 above. For the group of switches in the second and third column of Fig. 7.14, the above modulation functions are compared with saw-tooth carrier VSAW2 and VSAW3 respectively using two comparators and the method of generating the gate pulse using logic gates is the same as explained in section 7.6 above.

7.8.3 SIMULATION RESULTS: The simulation results for the three phase line to neutral and line output voltages, Phase A input current, Load current, Harmonic spectrum and THD of line to neutral, line to line output voltages and input current, the three saw-tooth carrier waveforms and the gate pulses to the three groups of switches in the first, second and third column of Fig. 7.14 corresponding to output phase a are shown in Fig. 7.17. The simulation results are tabulated in Table 7.8.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Topology</th>
<th>Parameters</th>
<th>Line to Neutral Output Voltage</th>
<th>Line to Line Output Voltage</th>
<th>Phase A Input Current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Peak Fundamental (Volts)</td>
<td>T.H.D. (p.u.)</td>
<td>Peak Fundamental (Volts)</td>
</tr>
<tr>
<td>1)</td>
<td>Three Phase MMC With SIX FC</td>
<td>Table 7.3</td>
<td>152.74</td>
<td>0.879</td>
<td>270.336</td>
</tr>
</tbody>
</table>

7.9 DISCUSSION OF RESULTS: Comparison of the simulation results using PSCAD shown in Table 7.5 with that of Table 7.8 shows that the three phase MMC with six FC per output phase has a lower value of THD for the line to neutral output voltage, line to line output voltage and phase A input current compared to the three phase MMC with three FC per output phase. The percentage decrease in THD for the former topology compared to the later one is 14.47%, 16.24% and 24.5% respectively for the line to neutral output voltage, line to line output voltage and phase A input current.
Chapter VII: Three Phase AC to Three Phase AC Capacitor Clamped Multilevel Matrix Converter
Chapter VII: Three Phase AC to Three Phase AC Capacitor Clamped Multilevel Matrix Converter

THREE PHASE MMC WITH SIX FC PER OUTPUT PHASE

FIG. 7.17
7.10 CONCLUSIONS: The modelling and simulation aspects of the three phase AC to three phase AC MMC with three FC and that with six FC per output phase have been explored in this chapter using two software packages SIMULINK and PSCAD for the former topology and with PSCAD for the later topology. Obviously the SIMULINK model gives erroneous performance compared to that with PSCAD for the former topology. Comparison of the values in Table 7.5 and 7.8 indicate that as the number of flying capacitors per output phase increases from three to six, the T.H.D. of line to neutral, line to line output voltages and input current decreases, which highlights the advantage of using more number of flying capacitors per output phase for the three phase matrix converter.

A7.1 APPENDIX: The entries in Table 7.6 are derived below. Referring to Fig. 7.15, the following analysis using KVL holds good:

1) $S_{Aa1} = 1; S_{Aa2} = 1; S_{Aa3} = 1$. All other switches 0.
   The output $v_a$ is directly connected to the input phase voltage $V_A$. $v_a = V_A$. (A7.1)

2) $S_{Aa1} = 1; S_{Aa2} = 1; S_{Ba3} = 1$. All other switches 0.
   $v_a = V_A - (V_A - V_B)/3 = (2V_A + V_B)/3$ (A7.2)

3) $S_{Aa1} = 1; S_{Ba2} = 1; S_{Ba3} = 1$. All other switches 0.
   $v_a = V_A - 2 * (V_A - V_B)/3 = (V_A + 2V_B)/3$ (A7.3)

4) $S_{Aa1} = 1; S_{Ba2} = 1; S_{Aa3} = 1$. All other switches 0.
   $v_a = V_A - 2 * (V_A - V_B)/3 + (V_A - V_B)/3 = (2V_A + V_B)/3$ (A7.4)

5) $S_{Ba1} = 1; S_{Ba2} = 1; S_{Ba3} = 1$. All other switches 0.
   The output $v_a$ is directly connected to the input phase voltage $V_B$. $v_a = V_B$. (A7.5)
Chapter VIII
Direct Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

8.1 INTRODUCTION: The most used modulation strategy for Matrix Converter is the Space Vector Modulation since it is well suitable for digital implementation [31-35]. It provides full exploitation of the input voltage and good load current quality [31-35]. The Space vector modulation approach has advantages with respect to the traditional carrier based modulation technique such as a) Immediate comprehension of the required commutation process. b) Simplified control algorithm. c) Maximum voltage transfer without adding third harmonic components and avoiding a fictitious DC link and d) No synchronisation requirements with input voltage waveform. Moreover, the proposed switching algorithm allows to reduce the number of switching devices involved in a commutation process with respect to conventional switching strategies. As the modulation strategy is defined in terms of the output waveform amplitude and phase angle, it is readily adapted to high-performance motor drive applications such as field-oriented control [31-35]. The algorithm is based on the instantaneous space vector representation of input and output voltages and currents. It analyses all the possible switching configurations available in three-phase MCs and does not need the concept of a virtual dc link. This modulation technique is also known as Direct Space Vector Modulation (DSVM). In this chapter the models of the three phase AC to three phase AC MC using Direct Asymmetrical and Direct Symmetrical Space Vector modulation algorithm have been developed using SIMULINK and the results obtained by simulation are presented.

8.2 DIRECT SPACE VECTOR MODULATION ALGORITHM: The three phase AC to three phase AC MC and the twenty seven switching states are shown in Fig. 3.1 and Table 3.1 respectively in Chapter III. Direct Space Vector Modulation (DSVM) algorithm uses 21 of 27 possible states that can be generated by the matrix of bidirectional switches and can fully control both the output voltage vector and input current displacement angle [25-38]. These states are presented in Table 8.1. The meaning of Table 8.1 is given in A8.1 Appendix. The Space Vector Modulation (SVM) technique is explained below [31].

The output voltage and input current space vector hexagon are shown in Fig. 8.1(A) and (B). At any sampling instant, the output voltage vector \( v_o \) and the input current displacement angle \( \phi_i \) are known as reference quantities [Fig. 8.2(a) and (b)]. The input line-to-neutral voltage vector \( v_i \) is imposed by the source voltages and is known by measurements. Then, the control of \( \phi_i \) can be achieved controlling the phase angle \( \beta \) of the input current vector. In principle, the SVM algorithm is based on the selection of four active switching configurations that are applied for suitable time intervals within each sampling period \( T_s \). The zero configurations are applied to complete \( T_s \) [31].
| SL.NO. | STATES a b c | SWITCHES ON | OUTPUT PHASE VOLTAGE | INPUT CURRENT | |
|-------|-------------|-------------|----------------------|---------------|
|       |             |             | |                  | /Ia | /Ib | /Ic | |
| 1     | ABB +1      | S_{Aa} S_{Bb} S_{Bc} | $\frac{2 \cdot v_{AB}}{3}$, 0 | $\frac{2 \cdot i_a}{\sqrt{3}}$, $-\frac{\pi}{6}$ | |
| 2     | BAA -1      | S_{Bb} S_{Ab} S_{Ac} | $\frac{-2 \cdot v_{AB}}{3}$, 0 | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $-\frac{\pi}{6}$ | |
| 3     | BCC +2      | S_{Bb} S_{Cb} S_{Cc} | $\frac{2 \cdot v_{BC}}{3}$, 0 | $\frac{2 \cdot i_a}{\sqrt{3}}$, $\frac{\pi}{2}$ | |
| 4     | CBB -2      | S_{Cb} S_{Bb} S_{Bc} | $\frac{-2 \cdot v_{BC}}{3}$, 0 | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $\frac{\pi}{2}$ | |
| 5     | CAA +3      | S_{Ca} S_{Ab} S_{Ac} | $\frac{2 \cdot v_{CA}}{3}$, 0 | $\frac{2 \cdot i_a}{\sqrt{3}}$, $\frac{7 \pi}{6}$ | |
| 6     | ACC -3      | S_{Aa} S_{Cc} S_{Cc} | $\frac{-2 \cdot v_{CA}}{3}$, 0 | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $\frac{7 \pi}{6}$ | |
| 7     | BAB +4      | S_{Bb} S_{Ab} S_{Bc} | $\frac{2 \cdot v_{AB}}{3}$, $\frac{2 \pi}{3}$ | $\frac{2 \cdot i_a}{\sqrt{3}}$, $-\frac{\pi}{6}$ | |
| 8     | ABA -4      | S_{Ab} S_{Bb} S_{Ac} | $\frac{-2 \cdot v_{AB}}{3}$, $\frac{2 \pi}{3}$ | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $-\frac{\pi}{6}$ | |
| 9     | CBC +5      | S_{Ca} S_{Bb} S_{Cc} | $\frac{2 \cdot v_{BC}}{3}$, $\frac{2 \pi}{3}$ | $\frac{2 \cdot i_a}{\sqrt{3}}$, $\frac{\pi}{2}$ | |
| 10    | BCB -5      | S_{Bb} S_{Cc} S_{Bc} | $\frac{-2 \cdot v_{BC}}{3}$, $\frac{2 \pi}{3}$ | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $\frac{\pi}{2}$ | |
| 11    | ACA +6      | S_{Aa} S_{Cc} S_{Ac} | $\frac{2 \cdot v_{CA}}{3}$, $\frac{2 \pi}{3}$ | $\frac{2 \cdot i_a}{\sqrt{3}}$, $\frac{7 \pi}{6}$ | |
| 12    | CAC -6      | S_{Ca} S_{Ab} S_{Cc} | $\frac{-2 \cdot v_{CA}}{3}$, $\frac{2 \pi}{3}$ | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $\frac{7 \pi}{6}$ | |
| 13    | BBA +7      | S_{Bb} S_{Bc} S_{Ac} | $\frac{2 \cdot v_{AB}}{3}$, $\frac{4 \pi}{3}$ | $\frac{2 \cdot i_a}{\sqrt{3}}$, $-\frac{\pi}{6}$ | |
| 14    | AAB -7      | S_{Ab} S_{Bb} S_{Bc} | $\frac{-2 \cdot v_{AB}}{3}$, $\frac{4 \pi}{3}$ | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $-\frac{\pi}{6}$ | |
| 15    | CCB +8      | S_{Ca} S_{Cc} S_{Bc} | $\frac{2 \cdot v_{BC}}{3}$, $\frac{4 \pi}{3}$ | $\frac{2 \cdot i_a}{\sqrt{3}}$, $\frac{\pi}{2}$ | |
| 16    | BBC -8      | S_{Bb} S_{Cc} S_{Cb} | $\frac{-2 \cdot v_{BC}}{3}$, $\frac{4 \pi}{3}$ | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $\frac{\pi}{2}$ | |
| 17    | AAC +9      | S_{Aa} S_{Cc} S_{Cc} | $\frac{2 \cdot v_{CA}}{3}$, $\frac{4 \pi}{3}$ | $\frac{2 \cdot i_a}{\sqrt{3}}$, $\frac{7 \pi}{6}$ | |
| 18    | CCA -9      | S_{Ca} S_{Cc} S_{Cc} | $\frac{-2 \cdot v_{CA}}{3}$, $\frac{4 \pi}{3}$ | $\frac{-2 \cdot i_a}{\sqrt{3}}$, $\frac{7 \pi}{6}$ | |
| 19    | AAA 0       | S_{Aa} S_{Ab} S_{Ac} | 0, 0 | 0 | 0 | 0 | |
| 20    | BBB 0       | S_{Bb} S_{Bb} S_{Bc} | 0, 0 | 0 | 0 | 0 | |
| 21    | CCC 0       | S_{Cc} S_{Cc} S_{Cc} | 0, 0 | 0 | 0 | 0 | |
To explain the SVM algorithm, referring to Fig. 8.2(A) and (B), both output voltage vector \( v_o \) and input current vector \( i_i \) are assumed to be in sector I. The reference voltage vector \( v_o \) is resolved into the components \( v_{oα} \) and \( v_{oβ} \) along the two adjacent vector directions. The component \( v_{oβ} \) can be synthesized using two voltage vectors having the same direction of \( v_{oβ} \). Among the six possible switching configurations, \( ±7, ±8, ±9 \) shown in Fig. 2(A), the ones that allow also the modulation of the input current direction must be selected. It is seen that this constraint allows the elimination of two switching configurations, +8 and -8 in this case. Among the remaining four switching configurations for sector I, the application of the positive switching configurations +7 and +9 are assumed which are common to both output voltage and input current sectors. With similar considerations, the switching configurations required to synthesize the component \( v_{oα} \) which are common to both output voltage and input current sectors can be found as +1 and +3 respectively [31].

Using the same procedure, it is possible to determine the four switching configurations related to any possible combination of output voltage and input current sectors, leading to the results summarized in Table 8.2. Four symbols (I, II, III, IV) are also introduced in the last row of Table 8.2 to identify the four general switching configurations, valid for any combination of input current and output voltage sectors [31-38].

Now it is possible to write in a general form, the four basic equations of the SVM algorithm, which satisfy simultaneously the requirements of the reference output voltage vector and input current displacement angle. With reference to the output voltage vector, the following two equations can be written:

\[
\vec{v}_{oα} = \vec{v}_o * \delta^i + \vec{v}_o * \delta^{II} = \frac{2}{\sqrt{3}} \cdot v_o \cdot \cos \left( \alpha - \frac{\pi}{3} \right) \cdot e^{i\left(S_{oβ-1} \frac{\pi}{3} \pm \frac{\pi}{3}\right)} \ldots \text{(8.1)}
\]

\[
\vec{v}_{oβ} = \vec{v}_o * \delta^{III} + \vec{v}_o * \delta^{IV} = \frac{2}{\sqrt{3}} \cdot v_o \cdot \cos \left( \alpha + \frac{\pi}{3} \right) \cdot e^{i\left(S_{oβ-1} \frac{\pi}{3}\right)} \ldots \text{(8.2)}
\]

With reference to the input current displacement angle, two equations are obtained by imposing on the vectors \((\vec{i}_i^I * \delta^i + \vec{i}_i^II * \delta^{II}) \) and \((\vec{i}_i^III * \delta^{III} + \vec{i}_i^IV * \delta^{IV}) \) the direction defined by \( β \). This can be achieved by imposing a null value on the two-vector component along the direction perpendicular to \( e^{jβ} \) (i.e., \( j e^{jβ} \)), leading to the following equations:

\[
(\vec{i}_i^I * \delta^i + \vec{i}_i^II * \delta^{II}) * j e^{jβ} * e^{j(S_{i-1}) \frac{\pi}{3}} = 0 \ldots \text{(8.3)}
\]

\[
(\vec{i}_i^III + \vec{i}_i^IV) * j e^{jβ} * e^{j(S_{i-1}) \frac{\pi}{3}} = 0 \ldots \text{(8.4)}
\]

\( \delta^i, \delta^{II}, \delta^{III} \) and \( \delta^{IV} \) are the duty cycles (i.e., \( \delta^i = t^i/Ts \) ) of the four switching configurations, \( S_o = 1, 2 \ldots 6 \) represents the output voltage sector, and \( S_i = 1, 2 \ldots 6 \) represents the input current sector. \( v_o, v_{oα}, v_{oβ}, v_i, v_{iα}, v_{iβ} \) are the output voltage vectors associated respectively with the switching configurations I, II, III, IV given in Table II. The same convention hold good for the input current vectors.
Solving equations 8.1 to 8.4 leads to the following equations for the duty cycles:
\[ \delta' = (-1)^{(S_v + S_i)} \frac{2q}{\sqrt{3}} \cos\left(\alpha - \frac{\pi}{3}\right) \cos\left(\beta - \frac{\pi}{3}\right) \cos(\varphi_i) \quad ... (8.5) \]

\[ \delta'' = (-1)^{(S_v + S_i + 1)} \frac{2q}{\sqrt{3}} \cos\left(\alpha - \frac{\pi}{3}\right) \cos\left(\beta + \frac{\pi}{3}\right) \cos(\varphi_i) \quad ... (8.6) \]

\[ \delta''' = (-1)^{(S_v + S_i + 1)} \frac{2q}{\sqrt{3}} \cos\left(\alpha + \frac{\pi}{3}\right) \cos\left(\beta - \frac{\pi}{3}\right) \cos(\varphi_i) \quad ... (8.7) \]

\[ \delta'''' = (-1)^{(S_v + S_i)} \frac{2q}{\sqrt{3}} \cos\left(\alpha + \frac{\pi}{3}\right) \cos\left(\beta + \frac{\pi}{3}\right) \cos(\varphi_i) \quad ... (8.8) \]

A proof of equations 8.1, 8.2, 8.5 and 8.6 are given in A8.2 Appendix. Furthermore, for the feasibility of the control strategy, the sum of the absolute values of the four duty-cycles must be lower than unity.

\[ i.e., |\delta'| + |\delta''| + |\delta'''| + |\delta''''| \leq 1 ... (8.9) \]

The zero configurations are applied to complete the sampling period \( T_s \), as shown below:

\[ \delta^0 = 1 - \delta' - \delta'' - \delta''' - \delta'''' ... (8.10) \]

In equations 8.5 to 8.8, negative value appears which corresponds to the corresponding negative switching state given in Table 8.1.

Switching strategies deal with the switching configuration sequence, that is, the order in which the active and zero vectors are applied along the commutation period. Here both the Asymmetrical SVM (ASVM) and Symmetrical SVM (SSVM) are analyzed in detail and a simulation models are developed.

The ASVM uses only one of the three zero configurations in the middle of the sequence so that minimum switch commutations are achieved between one switching state and the next one. Using this technique the switching commutations are up to eight for each commutation period. This way switching losses are minimized.

Two simple rules are proposed for both ASVM and SSVM which are given below [31-38]:

**Rule 1:** If \((SV + SI)\) is even, then the order of the switching sequence is : \(\delta''', \delta', \delta'', \delta''''\).

**Rule 2:** If \((SV + SI)\) is odd, then the order of the switching sequence is : \(\delta'', \delta''', \delta''''\).

Also referring to equations 8.5 to 8.8, if \((SV + SI)\) is even, \(\delta''''\) and \(\delta'''\) have a negative sign and if \((SV + SI)\) is odd, \(\delta''\) and \(\delta''''\) have a negative sign. This negative sign corresponds to the negative switching state in Table 8.1.

With regard to zero configuration for ASVM, Table 8.3 shown below can be used. For example, considering output voltage vector in sector 1 and input current vector in sector 4 (i.e., \(SV = 1; SI = 4\)) within their respective hexagons, it can be seen that \((SV + SI)\) is odd, rule 2 applies with \(\delta''\) and \(\delta''''\).
having negative sign. Also using Table 8.3, the following is the only possible double-sided sequences that can be generated for ASVM technique:

-9, +3, -1, +7 which from table 8.1 is given below:


![Gate pulse pattern for ASVM using Tables 8.1 to 8.3, rules 1 and 2 is shown in Table 8.4.](image)

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>SV, SI</th>
<th>(SV+SI)</th>
<th>SSF-X HIGH</th>
<th>BIDIRECTIONAL SWITCH GATE PULSE PATTERN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1, 1 or 4, 4</td>
<td>Even</td>
<td>ssf1</td>
<td>ACC AAB ABB ABA BAB</td>
</tr>
<tr>
<td>2</td>
<td>1, 4 or 4, 1</td>
<td>Odd</td>
<td>ssf2</td>
<td>CCA AAA CAA BAA BBA</td>
</tr>
<tr>
<td>3</td>
<td>1, 5 or 4, 2</td>
<td>Even</td>
<td>ssf3</td>
<td>CBB CCA CCC CCA CAA</td>
</tr>
<tr>
<td>4</td>
<td>1, 2 or 4, 5</td>
<td>Odd</td>
<td>ssf4</td>
<td>BBC CCC ACC AAC AAB</td>
</tr>
<tr>
<td>5</td>
<td>1, 3 or 4, 6</td>
<td>Even</td>
<td>ssf5</td>
<td>BAA BBB BBC BCC CCB</td>
</tr>
<tr>
<td>6</td>
<td>1, 6 or 4, 3</td>
<td>Odd</td>
<td>ssf6</td>
<td>AAB ABA BBB CBB CCB</td>
</tr>
<tr>
<td>7</td>
<td>2, 4 or 5, 1</td>
<td>Even</td>
<td>ssf7</td>
<td>CCA ACA AAA ABA BBA</td>
</tr>
<tr>
<td>8</td>
<td>2, 1 or 5, 4</td>
<td>Odd</td>
<td>ssf8</td>
<td>CAC AAA AAB BAB BBA</td>
</tr>
<tr>
<td>9</td>
<td>2, 2 or 5, 5</td>
<td>Even</td>
<td>ssf9</td>
<td>BBC CBC CCC CAC AAC</td>
</tr>
<tr>
<td>10</td>
<td>2, 5 or 5, 2</td>
<td>Odd</td>
<td>ssf10</td>
<td>BCB CCC CCA ACA</td>
</tr>
<tr>
<td>11</td>
<td>2, 6 or 5, 3</td>
<td>Even</td>
<td>ssf11</td>
<td>AAB BAB BBB BCB CBC</td>
</tr>
<tr>
<td>12</td>
<td>2, 3 or 5, 6</td>
<td>Odd</td>
<td>ssf12</td>
<td>ABA BBA BBB BCB CBC</td>
</tr>
<tr>
<td>13</td>
<td>3, 1 or 6, 4</td>
<td>Even</td>
<td>ssf13</td>
<td>CAC AAA ABA BAB BABB</td>
</tr>
<tr>
<td>14</td>
<td>3, 4 or 6, 1</td>
<td>Odd</td>
<td>ssf14</td>
<td>ACC ACA AAA ABA ABB</td>
</tr>
<tr>
<td>15</td>
<td>3, 5 or 6, 2</td>
<td>Even</td>
<td>ssf15</td>
<td>BCB CCC ACC ACA</td>
</tr>
<tr>
<td>16</td>
<td>3, 2 or 6, 5</td>
<td>Odd</td>
<td>ssf16</td>
<td>CBB CBC CCC CAC CAA</td>
</tr>
<tr>
<td>17</td>
<td>3, 3 or 6, 6</td>
<td>Even</td>
<td>ssf17</td>
<td>ABA ABB BBB CBB CBC</td>
</tr>
<tr>
<td>18</td>
<td>3, 6 or 6, 3</td>
<td>Odd</td>
<td>ssf18</td>
<td>BAA BAB BBB BCB CBC</td>
</tr>
</tbody>
</table>

With regard to zero configuration for SSVM, Table 8.5 shown below can be used.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>SV, SI</th>
<th>(SV+SI)</th>
<th>SSF-X HIGH</th>
<th>BIDIRECTIONAL SWITCH GATE PULSE PATTERN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1, 1 or 4, 4</td>
<td>Even</td>
<td>ssf1</td>
<td>ACC AAB ABB ABA BAB</td>
</tr>
<tr>
<td>2</td>
<td>1, 4 or 4, 1</td>
<td>Odd</td>
<td>ssf2</td>
<td>CCA AAA CAA BAA BBA</td>
</tr>
<tr>
<td>3</td>
<td>1, 5 or 4, 2</td>
<td>Even</td>
<td>ssf3</td>
<td>CBB CCA CCC CCA CAA</td>
</tr>
<tr>
<td>4</td>
<td>1, 2 or 4, 5</td>
<td>Odd</td>
<td>ssf4</td>
<td>BBC CCC ACC AAC AAB</td>
</tr>
<tr>
<td>5</td>
<td>1, 3 or 4, 6</td>
<td>Even</td>
<td>ssf5</td>
<td>BAA BBB BBC BCC CCB</td>
</tr>
<tr>
<td>6</td>
<td>1, 6 or 4, 3</td>
<td>Odd</td>
<td>ssf6</td>
<td>AAB ABA BBB CBB CCB</td>
</tr>
<tr>
<td>7</td>
<td>2, 4 or 5, 1</td>
<td>Even</td>
<td>ssf7</td>
<td>CCA ACA AAA ABA BBA</td>
</tr>
<tr>
<td>8</td>
<td>2, 1 or 5, 4</td>
<td>Odd</td>
<td>ssf8</td>
<td>CAC AAA AAB BAB BBA</td>
</tr>
<tr>
<td>9</td>
<td>2, 2 or 5, 5</td>
<td>Even</td>
<td>ssf9</td>
<td>BBC CBC CCC CAC AAC</td>
</tr>
<tr>
<td>10</td>
<td>2, 5 or 5, 2</td>
<td>Odd</td>
<td>ssf10</td>
<td>BCB CCC CCA ACA</td>
</tr>
<tr>
<td>11</td>
<td>2, 6 or 5, 3</td>
<td>Even</td>
<td>ssf11</td>
<td>AAB BAB BBB BCB CBC</td>
</tr>
<tr>
<td>12</td>
<td>2, 3 or 5, 6</td>
<td>Odd</td>
<td>ssf12</td>
<td>ABA BBA BBB BCB CBC</td>
</tr>
<tr>
<td>13</td>
<td>3, 1 or 6, 4</td>
<td>Even</td>
<td>ssf13</td>
<td>CAC AAA ABA BAB BABB</td>
</tr>
<tr>
<td>14</td>
<td>3, 4 or 6, 1</td>
<td>Odd</td>
<td>ssf14</td>
<td>ACC ACA AAA ABA ABB</td>
</tr>
<tr>
<td>15</td>
<td>3, 5 or 6, 2</td>
<td>Even</td>
<td>ssf15</td>
<td>BCB CCC ACC ACA</td>
</tr>
<tr>
<td>16</td>
<td>3, 2 or 6, 5</td>
<td>Odd</td>
<td>ssf16</td>
<td>CBB CBC CCC CAC CAA</td>
</tr>
<tr>
<td>17</td>
<td>3, 3 or 6, 6</td>
<td>Even</td>
<td>ssf17</td>
<td>ABA ABB BBB CBB CBC</td>
</tr>
<tr>
<td>18</td>
<td>3, 6 or 6, 3</td>
<td>Odd</td>
<td>ssf18</td>
<td>BAA BAB BBB BCB CBC</td>
</tr>
</tbody>
</table>

For example, considering output voltage vector in sector 1 and input current vector in sector 4 (i.e., SV = 1; SI = 4) within their respective hexagons, it can be seen that (SV + SI) is odd, rule 2 applies
with $\delta^I$ and $\delta^{IV}$ having negative sign. Also using Table 8.5, the following is the only possible double-sided sequences that can be generated for SSVM technique.

-9, +3, -1, +7 which from table 1 is given below:

\[
\text{CCC-CCA--AAA--BBA--BBB-BBB-BBB-BBA--BAA--AAA--CAA--CCA--CCC}
\]

The gate pulse pattern for SSVM using Tables 8.1 to 8.3, rules 1 and 2 is shown in Table 8.6 below:

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>SV, SI</th>
<th>SSF_ X HIGH</th>
<th>BIDIRECTIONAL SWITCH GATE PULSE PATTERN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1, 1 or 4, 4</td>
<td>Even</td>
<td>ssf1</td>
</tr>
<tr>
<td>2</td>
<td>1, 4 or 4, 1</td>
<td>Odd</td>
<td>ssf2</td>
</tr>
<tr>
<td>3</td>
<td>1, 5 or 4, 2</td>
<td>Even</td>
<td>ssf3</td>
</tr>
<tr>
<td>4</td>
<td>1, 2 or 4, 5</td>
<td>Odd</td>
<td>ssf4</td>
</tr>
<tr>
<td>5</td>
<td>1, 3 or 4, 6</td>
<td>Even</td>
<td>ssf5</td>
</tr>
<tr>
<td>6</td>
<td>1, 6 or 4, 3</td>
<td>Odd</td>
<td>ssf6</td>
</tr>
<tr>
<td>7</td>
<td>2, 4 or 5, 1</td>
<td>Even</td>
<td>ssf7</td>
</tr>
<tr>
<td>8</td>
<td>2, 1 or 5, 4</td>
<td>Odd</td>
<td>ssf8</td>
</tr>
<tr>
<td>9</td>
<td>2, 2 or 5, 5</td>
<td>Even</td>
<td>ssf9</td>
</tr>
<tr>
<td>10</td>
<td>2, 5 or 5, 2</td>
<td>Odd</td>
<td>ssf10</td>
</tr>
<tr>
<td>11</td>
<td>2, 6 or 5, 3</td>
<td>Even</td>
<td>ssf11</td>
</tr>
<tr>
<td>12</td>
<td>2, 3 or 5, 6</td>
<td>Odd</td>
<td>ssf12</td>
</tr>
<tr>
<td>13</td>
<td>3, 1 or 6, 4</td>
<td>Even</td>
<td>ssf13</td>
</tr>
<tr>
<td>14</td>
<td>3, 4 or 6, 1</td>
<td>Odd</td>
<td>ssf14</td>
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<tr>
<td>15</td>
<td>3, 5 or 6, 2</td>
<td>Even</td>
<td>ssf15</td>
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<tr>
<td>17</td>
<td>3, 3 or 6, 6</td>
<td>Even</td>
<td>ssf17</td>
</tr>
<tr>
<td>18</td>
<td>3, 6 or 6, 3</td>
<td>Odd</td>
<td>ssf18</td>
</tr>
</tbody>
</table>

### 8.3 MODEL OF DIRECT ASYMMETRICAL SPACE VECTOR MODULATED THREE PHASE MATRIX CONVERTER:

The SIMULINK model of the Direct Asymmetrical Space Vector Modulated (DASVM) three phase AC to three phase AC MC is shown in Fig. 8.3. The power circuit of the model is developed using the SimPowerSystems blockset in SIMULINK [51]. This mainly consists of three phase AC voltage source, bidirectional switch matrix, output filter and R-L load. The arrangement of the bidirectional switch matrix using IGBTs is the same as shown in Fig. 3.2 of Chapter III.

The modulation algorithm is developed in several sub units using Embedded MATLAB Function, MATLAB Function, Math Function, Logical and Bit Operator and using Sources block set in SIMULINK [51]. The various sub units are explained below:
8.3.1 DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR: This is developed using Embedded MATLAB Function block in SIMULINK, as shown in Fig. 8.3. With peak line to neutral input voltage, desired peak output phase voltage, input frequency, output frequency, time, angular frequency of reference frame $\omega_c$ as input parameters, the three phase output voltage can be resolved into dq-axis component voltages [42] and the absolute value of the angle of the output phase voltage, $v_{out\_angle}$ can be calculated using the function $\text{atan2}(voq,vod)$. Using input voltage and input phase displacement angle, a similar procedure is used to calculate the absolute value of the input current angle, $i_{in\_angle}$. The value of reference frame frequency $\omega_c$ is zero. This is illustrated in Program segment I below:

```matlab
PROGRAM SEGMENT I
function [voa,vob,voc,ViA,ViB,ViC,q,voq,vod,Viq,Vid,vout_angle,i_in_angle,...] = fcn(vom,fo,t,vim,fi,wc,phi_i,...)
voa = vom*sin(2*pi*fo*t);
vob = vom*sin(2*pi*fo*t - 2*pi/(3));
voc = vom*sin(2*pi*fo*t + 2*pi/(3));
ViA = vim*sin(2*pi*fi*t);
ViB = vim*sin(2*pi*fi*t - 2*pi/(3));
ViC = vim*sin(2*pi*fi*t + 2*pi/(3));
q = vom/vim;
voq = (2/(3))*(voa*cos(wc*t)+ vob*cos(wc*t - (2*pi/(3))) + voc*cos(wc*t + (2*pi/(3))));
vod = (2/(3))*(voa*sin(wc*t)+ vob*sin(wc*t - (2*pi/(3))) + voc*sin(wc*t + (2*pi/(3))));
Viq = (2/(3))*(ViA*cos(wc*t)+ ViB*cos(wc*t - (2*pi/(3))) + ViC*cos(wc*t + (2*pi/(3))));
Vid = (2/(3))*(ViA*sin(wc*t)+ ViB*sin(wc*t - (2*pi/(3))) + ViC*sin(wc*t + (2*pi/(3))));
vout_angle = atan2(voq,vod);
i_in_angle = atan2(Viq,Vid);
```

These two values of $v_{out\_angle}$ and $i_{in\_angle}$ are used to calculate the output voltage sector $sv$, input current sector $si$, $\alpha$ and $\beta$ values for output voltage and input current using MATLAB function, REM functions and SUBTRACT modules.

Program segment II illustrates the MATLAB code for duty cycle sequencing and sector switch function generation. Duty-cycle $dI$, $dII$, $dIII$, $dIV$ and $d0$ are calculated using equations 8.5 to 8.8 and 8.10 assuming unity input power factor. With (sv+si) even and odd, rule 1 and 2 for duty cycle are followed with zero vector duty cycle $d0$ introduced at the middle of the four duty cycles, $dI$, $dII$, $dIII$, $dIV$. This is used to calculate the timing $A$, $B$, $C$, $D$ and $E$, by comparison of the cumulative sector timing with a triangle carrier $Vtri$ as shown in Program Segment II. This triangle carrier $Vtri$ has a period $Ts$, peak value $Ts/2$ Volts and minimum value zero, as shown in Fig. 8.4. Cumulative sector timing is obtained by appropriately adding the value of duty-ratio and multiplying by $Ts/2$, as per rules 1 and 2 given above. Sector switch functions ssf1 to ssf18 are determined using if-then-else statement. For example sector switch function ssf1 is HIGH only when $sv = si = 1$ or $sv = si = 4$ and is LOW otherwise.
FIG. 8.3: SIMULINK MODEL OF THREE PHASE AC TO THREE PHASE AC DIRECT ASVM MATRIX CONVERTER
Chapter VIII: Direct Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

PROGRAM SEGMENT III

function [y] = fcn(u)
%%Narayanaswamy. P.R. Iyer
vout_angle = u(1);
i_in_angle = u(2);
if (vout_angle > -pi && vout_angle <= -2*pi/(3))
y(1) = 4;
else if (vout_angle > -2*pi/(3) && vout_angle <= -pi/(3))
y(1) = 5;
else if (vout_angle > -pi/(3) && vout_angle <= 0)
y(1) = 6;
else if (vout_angle > 0 && vout_angle <= pi/(3))
y(1) = 1;
else if (vout_angle > pi/(3) && vout_angle <= 2*pi/(3))
y(1) = 2;
else if (vout_angle > 2*pi/(3) && vout_angle <= pi)
y(1) = 3;
end
end
end
end
if (i_in_angle > -pi && i_in_angle <= -2*pi/(3))
y(2) = 4;
else if (i_in_angle > -2*pi/(3) && i_in_angle <= -pi/(3))
y(2) = 5;
else if (i_in_angle > -pi/(3) && i_in_angle <= 0)
y(2) = 6;
else if (i_in_angle > 0 && i_in_angle <= pi/(3))
y(2) = 1;
else if (i_in_angle > pi/(3) && i_in_angle <= 2*pi/(3))
y(2) = 2;
else if (i_in_angle > 2*pi/(3) && i_in_angle <= pi)
y(2) = 3;
end
end
end
end

sv = y(1);
si = y(2);

PROGRAM SEGMENT II

%%Narayanaswamy. P.R. Iyer
function(q,dI,dII,dIII,dIV,d0,A,B,C,D,E,ssf1,ssf2,ssf3,…ssf18) =
fcn(Vom,fo,Tim,wc,phi_i,alfa,beta,sv,si,Ts,vtri)
q = Vom/Vim  %%Duty cycle calculations
dI = (2*q*cos(alfa - pi/(3))*cos(beta - pi/(3)))/(sqrt(3)*cos(phi_i));
dII = (2*q*cos(alfa - pi/(3))*cos(beta + pi/(3)))/(sqrt(3)*cos(phi_i));
dIII = (2*q*cos(alfa+pi/(3))*cos(beta + pi/(3)))/(sqrt(3)*cos(phi_i));
dIV = (2*q*cos(alfa+pi/(3))*cos(beta - pi/(3)))/(sqrt(3)*cos(phi_i));
d0 = (1 - dI - dII - dIII - dIV);
if (rem((sv+si),2) == 0) %%even sequence
  A = 1; else
  A = 0;
end
if ( vtri <= (dIII + dI)*Ts/(2))
  B = 1; else
  B = 0;
end
if ( vtri <= (dIII + dI + d0)*Ts/(2))
  C = 1; else
  C = 0;
end
if ( vtri <= (dIII + dI + d0 + dII)*Ts/(2))
  D = 1; else
  D = 0;
end
if ( vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
  E = 1; else
  E = 0;
end
else
  if ( vtri <= (dIII + dI)*Ts/(2))  %%odd sequence
    A = 1; else
    A = 0;
end
if ( vtri <= (dIII + dI + d0)*Ts/(2))
  B = 1; else
  B = 0;
end
if ( vtri <= (dIII + dI + d0 + dII)*Ts/(2))
  C = 1; else
  C = 0;
end
if ( vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
  D = 1; else
  D = 0;
end
if ( vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
  E = 1; else
  E = 0;
end
end
end
end
end
if (sv == 1 && si == 1) || sv == 4 && si == 4)
  ssf1 = 1; else
  ssf1 = 0;
end
if ( sv == 4 && si == 1 ) || sv == 1 && si == 4)
  ssf2 = 1; else
  ssf2 = 0;
end
%
similar statements for ssf3 to ssf18.

. . 
if ( sv == 3 && si == 6 ) || sv == 6 && si == 3)
  ssf18 = 1; else
  ssf18 = 0;
end
8.3.2 OUTPUT VOLTAGE AND INPUT CURRENT SECTOR CALCULATOR: This is developed using MATLAB Function, a mux and a demux as shown in Fig. 8.5. The input to the mux are vout_angle and i_in_angle. The output from the demux are SV and SI. The source code to determine SV and SI is shown in Program Segment III.

8.3.3 OUTPUT VOLTAGE AND INPUT CURRENT REFERENCE ANGLE CALCULATOR: This is shown in Fig. 8.6. This uses two REM function blocks and SUBTRACT modules. The first REM block has the inputs v_out_angle and pi/(3). The second REM block has the inputs i_in_angle and pi/(3). The output of the first REM block is subtracted from pi/(6) to obtain angle alfa defined in Fig. 8.2(A). The output of the second REM block is subtracted from pi/(6), input p.f. angle phi_i and once again from pi/(6) to obtain beta as per the configuration defined in Fig. 8.2(B).

8.3.4 GATE PULSE TIMING CALCULATOR: This is shown in Fig. 8.7. The inputs in1 to in5 are A, B, C, D and E respectively. The individual gate pulse timing, ta, tb, t0, tc and td are respectively dIII*Ts/(2), dI*Ts/(2), d0*Ts/(2), dII*Ts/(2) and dIV*Ts/(2) when (SV+SI) is even and dI*Ts/(2), dIII*Ts/(2), d0*Ts/(2), dIV*Ts/(2) and dII*Ts/(2) when (SV+SI) is odd. This individual gate pulse duration is obtained as shown in equation 8.11 below:

\[
t_a = (A \& A) \\
t_b = (\neg A \& B) \\
t_0 = (\neg B \& C) \\
t_c = (\neg C \& D) \\
t_d = (\neg D \& E) \ldots \quad (8.11)
\]

In equation 8.11, symbols (\&) represents logical AND and (\neg) represents NOT operation respectively. To easily generate the MC gate pulse, the timing pulse in equation 8.11 are given to OR gates to obtain the following additional timing pulse:

\[
t_{ab} = (t_d | t_b)
\]

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Table 8.5 below:
The complete gate timing for the nine bidirectional switches using Direct ASVM algorithm is given in
equation 8.12, symbol (||) represents logical OR operation.

Thus the gate timing pulse for switch SAa can be expressed as in equation 8.13 below:

\[
S_{Sa} = \text{ssf1} \& \text{tab0cd})|\text{ssf2} \& (t0)| ... |\text{ssf18} \& (0)| (8.13)
\]

The complete gate timing for the nine bidirectional switches using Direct ASVM algorithm is given in
Table 8.5 below:

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>SV_SI</th>
<th>SSF_ X HIGH</th>
<th>SAA</th>
<th>SAB</th>
<th>SAc</th>
<th>SAb</th>
<th>SAc</th>
<th>SBr</th>
<th>SAc</th>
<th>SBe</th>
<th>SACc</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1, 1 or 4, 4</td>
<td>ssf1</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>tb0c</td>
<td>ta</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
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<td>1, 4 or 4, 1</td>
<td>ssf2</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
<td>tb0c</td>
<td>ta</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
</tr>
<tr>
<td>3</td>
<td>1, 5 or 4, 2</td>
<td>ssf3</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
<td>td</td>
<td>ta</td>
<td>tb0c</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
</tr>
<tr>
<td>4</td>
<td>1, 2 or 4, 5</td>
<td>ssf4</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
<td>td</td>
<td>ta</td>
<td>tb0c</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
</tr>
<tr>
<td>5</td>
<td>1, 3 or 4, 6</td>
<td>ssf5</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
<td>ta</td>
<td>tb0c</td>
<td>td</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
</tr>
<tr>
<td>6</td>
<td>1, 6 or 4, 3</td>
<td>ssf6</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
<td>ta</td>
<td>tb0c</td>
<td>td</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>2, 5 or 5, 1</td>
<td>ssf7</td>
<td>tb0c</td>
<td>td</td>
<td>ta</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>2, 1 or 5, 4</td>
<td>ssf8</td>
<td>tb0c</td>
<td>td</td>
<td>ta</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
</tr>
<tr>
<td>9</td>
<td>2, 2 or 5, 5</td>
<td>ssf9</td>
<td>td</td>
<td>ta</td>
<td>tb0c</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
</tr>
<tr>
<td>10</td>
<td>2, 5 or 5, 2</td>
<td>ssf10</td>
<td>td</td>
<td>ta</td>
<td>tb0c</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
</tr>
<tr>
<td>11</td>
<td>2, 6 or 5, 3</td>
<td>ssf11</td>
<td>ta</td>
<td>tb0c</td>
<td>td</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
</tr>
<tr>
<td>12</td>
<td>2, 3 or 5, 6</td>
<td>ssf12</td>
<td>ta</td>
<td>tb0c</td>
<td>td</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
</tr>
<tr>
<td>13</td>
<td>3, 1 or 6, 4</td>
<td>ssf13</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>tb0c</td>
<td>td</td>
<td>ta</td>
</tr>
<tr>
<td>14</td>
<td>3, 4 or 6, 1</td>
<td>ssf14</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
<td>tb0c</td>
<td>td</td>
<td>ta</td>
</tr>
<tr>
<td>15</td>
<td>3, 5 or 6, 2</td>
<td>ssf15</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
<td>td</td>
<td>ta</td>
<td>tb0c</td>
</tr>
<tr>
<td>16</td>
<td>3, 2 or 6, 5</td>
<td>ssf16</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
<td>td</td>
<td>ta</td>
<td>tb0c</td>
</tr>
<tr>
<td>17</td>
<td>3, 3 or 6, 6</td>
<td>ssf17</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
<td>ta</td>
<td>tb0c</td>
<td>td</td>
</tr>
<tr>
<td>18</td>
<td>3, 6 or 6, 3</td>
<td>ssf18</td>
<td>tab0cd</td>
<td>0</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
<td>ta</td>
<td>tb0c</td>
<td>td</td>
<td></td>
</tr>
</tbody>
</table>

8.3.5 GATE PULSE GENERATOR: The gate pulse generator for the MC is developed using Embedded MATLAB as shown in Fig. 8.3. The sector switch functions ssf1 to ssf18, gate pulse timing calculator outputs defined in equations 8.11 and 8.12 form the input modules and the outputs are the gate pulses for the nine bidirectional switches of the MC. In Table 8.5, the gate timing for the nine bidirectional switches are shown. The gate timing for switch SAa can be combined by logically ANDing the respective value with sector switch function ssf_x and ORing the value for each sector. Thus the gate timing pulse for switch SAa can be expressed as in equation 8.13 below:

\[
S_{Sa} = \text{ssf1} \& (\text{tab0cd})|\text{ssf2} \& (t0)| ... |\text{ssf18} \& (0) | (8.13)
\]

Program segment IV gives the method of generating the gate timing pulses for the nine bidirectional switches using the calculated sector timings given in Table 8.5.

8.4 SIMULATION RESULTS: The simulation of the Three Phase ASVM Matrix Converter was carried out in SIMULINK [ 51 ]. The parameters used for simulation are shown in Table 8.6. The ode15S(Stiff/NDF) solver was used. Simulation of the above three phase AC to three phase AC direct
ASVM of MC was carried out for two different output frequencies with all other parameters constant. The simulation results of the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage for a 50 Hz AC output voltage are shown in Fig. 8.8(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.9(A) to (D). Similarly the harmonic spectrum of the above in order for a 20 Hz AC output voltage are shown in Fig. 8.10(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.11(A) to (D). The simulation results are tabulated in Table 8.7.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>50 – 50</td>
<td>1.0271</td>
<td>1.6083</td>
<td>1.9736</td>
<td>0.2926</td>
</tr>
<tr>
<td>2</td>
<td>50 – 20</td>
<td>0.9559</td>
<td>1.1765</td>
<td>1.4765</td>
<td>0.3678</td>
</tr>
</tbody>
</table>

### TABLE 8.6: Model Parameters

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RMS Line to Neutral Input Voltage</td>
<td>220</td>
<td>V</td>
</tr>
<tr>
<td>2</td>
<td>Input Frequency fI</td>
<td>50</td>
<td>Hz</td>
</tr>
<tr>
<td>3</td>
<td>Modulation Index q</td>
<td>0.7</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>Output Frequency fO</td>
<td>50, 20</td>
<td>Hz</td>
</tr>
<tr>
<td>5</td>
<td>Carrier Sampling Frequency fsW</td>
<td>10</td>
<td>kHz</td>
</tr>
<tr>
<td>6</td>
<td>R-L-C Output Filter</td>
<td>10.01e-3, 25.356e-6</td>
<td>Ω, H, F</td>
</tr>
<tr>
<td>7</td>
<td>R-L Load</td>
<td>100, 500e-3</td>
<td>Ω, H</td>
</tr>
<tr>
<td>8</td>
<td>Input Phase Displacement ζi</td>
<td>0</td>
<td>Radians</td>
</tr>
</tbody>
</table>

### PROGRAM SEGMENT IV

```matlab
function [SAa,SBa,SCa,SAb,SBb,SCb,SAc,SBc,SCc] = fcn(ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12,ssf13,ssf14,ssf15,ssf16,ssf17,ta,      tb0,tc,tab,tb0c,tcd,tab0cd)
    %Narayanaswamy. P.R.Iyer.
    SAa = ssf1&(tab0cd)||ssf2&(t0)||ssf3&(0)||ssf4&(tcd)||ssf5&(0)||ssf6&(tab)||ssf7&(tb0c)||ssf8&(tb0c)||ssf9&(td)||ssf10&(td)||ssf11&(ta)||ssf12&(ta)||ssf13&(t0)||ssf14&(tab0cd)||ssf15&(tcd)||ssf16&(0)||ssf17&(tab)||ssf18&(0);
    SBa = ssf1&(0)||ssf2&(tcd)||ssf3&(0)||ssf4&(tab)||ssf5&(tab0cd)||ssf6&(t0)||ssf7&(td)||ssf8&(td)||ssf9&(ta)||ssf10&(ta)||ssf11&(tb0c)||ssf12&(tb0c)||ssf13&(tcd)||ssf14&(0)||ssf15&(tab)||ssf16&(0)||ssf17&(t0)|| ssf18&(tab0cd);
    SCa = ssf1&(0)||ssf2&(tab)||ssf3&(tab0cd)||ssf4&(t0)||ssf5&(0)||ssf6&(tcd)||ssf7&(ta)||ssf8&(ta)||ssf9&(tb0c)||ssf10&(tb0c)||ssf11&(td)||ssf12&(td)||ssf13&(tab)||ssf14&(0)||ssf15&(tab0cd)||ssf16&(tab0cd)||ssf17&(tcd)||ssf18&(ta);
    SAb = ssf1&(tb0c)||ssf2&(tb0c)||ssf3&(td)||ssf4&(td)||ssf5&(ta)||ssf6&(ta)||ssf7&(t0)||ssf8&(tab0cd)||ssf9&(tcd)||ssf10&(0)||ssf11&(tab)||ssf12&(0)||ssf13&(tab0cd)||ssf14&(t0)||ssf15&(0)||ssf16&(tcd)||ssf17&(0)||ssf18&(tab);
    SBb = ssf1&(td)||ssf2&(td)||ssf3&(ta)||ssf4&(ta)||ssf5&(tb0c)||ssf6&(tb0c)||ssf7&(tab0cd)||ssf8&(0)||ssf9&(tab)||ssf10&(0)||ssf11&(t0)||ssf12&(tab0cd)||ssf13&(0)||ssf14&(tcd)||ssf15&(0)||ssf16&(tab)||ssf17&(tab0cd)||ssf18&(t0);
    SCb = ssf1&(ta)||ssf2&(ta)||ssf3&(tb0c)||ssf4&(tb0c)||ssf5&(td)||ssf6&(td)||ssf7&(tab)||ssf8&(0)||ssf9&(tab)||ssf10&(tab0cd)||ssf11&(tab0cd)||ssf12&(t0)||ssf13&(0)||ssf14&(tab)||ssf15&(tab0cd)||ssf16&(tab0cd)||ssf17&(tb0c)||ssf18&(tb0c);
    SAc = ssf1&(t0)||ssf2&(tab0cd)||ssf3&(tcd)||ssf4&(0)||ssf5&(tab)||ssf6&(tab0cd)||ssf7&(tab0cd)||ssf8&(0)||ssf9&(0)||ssf10&(tcd)||ssf11&(tab0cd)||ssf12&(tab0cd)||ssf13&(tcd)||ssf14&(0)||ssf15&(tab0cd)||ssf16&(tab0cd)||ssf17&(0)||ssf18&(tab0cd);
    SBc = ssf1&(0)||ssf2&(tab0cd)||ssf3&(0)||ssf4&(tab0cd)||ssf5&(tab0cd)||ssf6&(tab0cd)||ssf7&(tab0cd)||ssf8&(tab0cd)||ssf9&(tab0cd)||ssf10&(tab0cd)||ssf11&(tab0cd)||ssf12&(tab0cd)||ssf13&(tab0cd)||ssf14&(tab0cd)||ssf15&(tab0cd)||ssf16&(tab0cd)||ssf17&(tab0cd)||ssf18&(tab0cd);
    SCc = ssf1&(tab0cd)||ssf2&(tab0cd)||ssf3&(tab0cd)||ssf4&(tab0cd)||ssf5&(tab0cd)||ssf6&(tab0cd)||ssf7&(tab0cd)||ssf8&(tab0cd)||ssf9&(tab0cd)||ssf10&(tab0cd)||ssf11&(tab0cd)||ssf12&(tab0cd)||ssf13&(tab0cd)||ssf14&(tab0cd)||ssf15&(tab0cd)||ssf16&(tab0cd)||ssf17&(tab0cd)||ssf18&(tab0cd);
```

8.5 MODEL OF DIRECT SYMMETRICAL SPACE VECTOR MODULATED THREE PHASE MATRIX CONVERTER: The SIMULINK model of the Direct Symmetrical Space Vector Modulated (DSSVM) three phase AC to three phase AC MC is shown in Fig. 8.12. The power circuit of the model is developed using the SimPowerSystems blockset in SIMULINK [51]. This mainly consists of three phase AC voltage source, bidirectional switch matrix, output filter and R-L load. The arrangement of the bidirectional switch matrix using IGBTs is the same as shown in Fig. 3.2 of Chapter III.

The modulation algorithm is developed in several sub units using Embedded MATLAB Function.
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FIG. 8.12: SIMULINK MODEL OF THREE PHASE AC TO THREE PHASE AC SSVM MATRIX CONVERTER
MATLAB Function, Math Function, Logical and Bit Operator and using Sources block set in SIMULINK [51]. The various sub units are explained below:

8.5.1 DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR: This is developed using Embedded MATLAB Function block in SIMULINK, as shown in Fig. 8.12. With peak line to neutral input voltage, desired peak output phase voltage, input frequency, output frequency, time, angular frequency of reference frame \( \omega_c \) as input parameters, the three phase output voltage can be resolved into dq-axis component voltages [42] and the absolute value of the angle of the output phase voltage, \( \text{vout_angle} \) can be calculated using the function \( \text{atan2(vq,vd)} \). Using input voltage and input phase displacement angle, a similar procedure is used to calculate the absolute value of the input current angle, \( \text{i_in_angle} \). The value of reference frame frequency \( \omega_c \) is zero. This is illustrated in Program segment I in Section 8.3.1 above. These two values of the angles are used to calculate the output voltage sector \( sv \), input current sector \( si \), \( \alpha \) and \( \beta \) values for output voltage and input current using MATLAB function, REM functions and SUBTRACT modules. Program segment V illustrates the MATLAB code for duty cycle sequencing and sector switch function generation. Duty-cycle \( dI \), \( dII \), \( dIII \), \( dIV \) and \( d0 \) are calculated using equations 8.5 to 8.8 and 8.10, assuming unity input power factor. With \((sv+si)\) even and odd, rule 1 and 2 for duty cycle are followed with zero vector duty cycle \( d0/3 \) introduced at the start, middle and at the end of the four duty cycles, \( dI \), \( dII \), \( dIII \), \( dIV \). This is used to calculate the timing \( A, B, C, D, E, F \) and \( G \), by comparison of the cumulative sector timing with a triangle carrier. This triangle carrier has a period \( Ts \), peak value \( Ts/2 \) Volts and minimum value zero, as shown in Fig. 8.4. Cumulative sector timing is obtained by appropriately adding the value of duty-ratio and multiplying by \( Ts/2 \), as per rules 1 and 2 given above. Sector switch functions ssf1 to ssf18 are determined using if-then-else statement. For example sector switch function ssf1 is HIGH only when \( sv = si =1 \) or \( sv = si = 4 \) and is LOW otherwise.

8.5.2 OUTPUT VOLTAGE AND INPUT CURRENT SECTOR CALCULATOR: This is developed using MATLAB Function, a mux and a demux as shown in Fig. 8.5 above. The input to the mux are \( \text{vout_angle} \) and \( \text{i_in_angle} \). The output from the demux are \( SV \) and \( SI \). The source code to determine \( SV \) and \( SI \) is shown in Program Segment III above.

8.5.3 OUTPUT VOLTAGE AND INPUT CURRENT REFERENCE ANGLE CALCULATOR: This is shown in Fig. 8.6 above. This uses two REM function blocks and SUBTRACT modules. The first REM block has the inputs \( \text{v_out_angle} \) and \( \pi/(3) \). The second REM block has the inputs \( \text{i_in_angle} \) and \( \pi/(3) \). The output of the first REM block is subtracted from \( \pi/(6) \) to obtain angle \( \text{alpha} \) defined in Fig. 8.2(A). The output of the second REM block is subtracted from \( \pi/(6) \), input p.f. angle \( \text{phi_i} \) and once again from \( \pi/(6) \) to obtain \( \text{beta} \) as per the configuration defined in Fig. 8.2(B).

8.5.4 GATE PULSE TIMING CALCULATOR: This is shown in Fig. 8.13. The inputs in1 to in7 are A, B, C, D, E, F and G respectively. The individual gate pulse timing, \( t01, ta, tb, t02, tc, td \) and
function(q,dI,dII,dIII,dIV,d0,A,B,C,D,E,ssf1,ssf2,ssf3,…ssf18)= fcn(Vom,fo,t,Vim,fi,wc,ph_i,alfa,beta,sv,si,Ts,vtri)
qu = Vom/Vim  %% Duty cycle calculations
dl = (2*q*cos(alfa - pi/(3))*cos(beta - pi/(3))/(sqrt(3)*cos(ph_i)));
dll = (2*q*cos(alfa - pi/(3))*cos(beta - pi/(3))/(sqrt(3)*cos(ph_i)));
dlv = (2*q*cos(alfa + pi/(3))*cos(beta + pi/(3))/(sqrt(3)*cos(ph_i)));
d0 = (1 - dI - dII - dIII - dIV);
if (rem((sv+si),2) == 0)  %%even sequence
if ( vtri <= (d0/(3))*Ts/(2))
   A = 1;    else
   A = 0;
if ( vtri <= (dIII + d0/(3))*Ts/(2))
   B = 1;    else
   B = 0;
if ( vtri <= (dIII + dI + d0/(3))*Ts/(2))
   C = 1;    else
   C = 0;
if ( vtri <= (dIII + dI + d0/(3) + d0/(3))*Ts/(2))
   D = 1;    else
   D = 0;
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII)*Ts/(2))
   E = 1;    else
   E = 0;
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
   F = 1;    else
   F = 0;
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
   G = 1;    else
   G = 0;
else
    %%odd sequence
if ( vtri <= (d0/(3))*Ts/(2))
   A = 1;    else
   A = 0;
if ( vtri <= (dI + d0/(3))*Ts/(2))
   B = 1;    else
   B = 0;
if ( vtri <= (dIII + dI + d0/(3))*Ts/(2))
   C = 1;    else
   C = 0;
if ( vtri <= (dIII + dI + d0/(3) + d0/(3))*Ts/(2))
   D = 1;    else
   D = 0;
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
   E = 1;    else
   E = 0;
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
   F = 1;    else
   F = 0;
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
   G = 1;    else
   G = 0;
end
end
PROGRAM SEGMENT V (CONTINUED)

if (sv == 1 && si == 1 || sv == 4 && si == 4)
    ssf1 = 1;
else
    ssf1 = 0;
end

if (sv == 4 && si == 1 || sv == 1 && si == 4)
    ssf2 = 1;
else
    ssf2 = 0;
end

% similar statements for ssf3 to ssf18.

if (sv == 3 && si == 6 || sv == 6 && si == 3)
    ssf18 = 1;
else
    ssf18 = 0;
end

t03 are respectively \((d0/3)*Ts/2\), \(dIII*Ts/(2)\), \(dI*Ts/(2)\), \((d0/3)*Ts/(2)\), \(dII*Ts/(2)\) and \((d0/3)*Ts/2\) when \((SV+SI)\) is even and \((d0/3)*Ts/2\), \(dI*Ts/(2)\), \(dIII*Ts/(2)\), \((d0/3)*Ts/2\), \(dIV*Ts/(2)\), \(dII*Ts/(2)\) and \((d0/3)*Ts/2\) when \((SV+SI)\) is odd. This individual gate pulse duration is obtained as shown in equation 8.14 below:

\[
\begin{align*}
\tau_{01} &= (A \& A) \\
\tau_a &= (~A \& B) \\
\tau_b &= (~B \& C) \\
\tau_{02} &= (~C \& D) \\
\tau_c &= (~D \& E) \\
\tau_d &= (~E \& F) \\
\tau_{03} &= (~F \& G) \ldots \quad (8.14)
\end{align*}
\]

In equation 8.14, symbols \(\&\) represents logical AND and \((~)\) represents NOT operation respectively. To easily generate the MC gate pulse, the timing pulse in equation 8.14 are given to OR gates to obtain the following additional timing pulse:

\[
t_{01a} = (\tau_a || \tau_{01})
\]

Fig. 8.13
The complete gate timing for the nine bidirectional switches using Direct SSVM algorithm is given in Table 8.8 below:

Table 8.8: SSVM Gate Pulse Timing

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>SV_SI</th>
<th>SSF_X HIGH</th>
<th>SAa</th>
<th>SBa</th>
<th>SCa</th>
<th>SAb</th>
<th>SBB</th>
<th>SCh</th>
<th>SAC</th>
<th>SCb</th>
<th>SBc</th>
<th>SCc</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1, 1 or 4, 4</td>
<td>ssf1</td>
<td>tab02cd</td>
<td>t03</td>
<td>t01</td>
<td>t02</td>
<td>t03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1, 4 or 1</td>
<td>ssf2</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td>t02</td>
<td>t03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1, 5 or 4, 2</td>
<td>ssf3</td>
<td>t03</td>
<td>t01</td>
<td>tab02cd</td>
<td>t03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1, 2 or 4, 5</td>
<td>ssf4</td>
<td>tcd03</td>
<td>t01ab</td>
<td>t02</td>
<td>t03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1, 3 or 4, 6</td>
<td>ssf5</td>
<td>t01</td>
<td>tab02cd</td>
<td>t03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>1, 6 or 4, 3</td>
<td>ssf6</td>
<td>t01ab</td>
<td>t02</td>
<td>tcd03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>2, 4 or 5, 1</td>
<td>ssf7</td>
<td>tab02c</td>
<td>t03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td>t02</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>8</td>
<td>2, 1 or 5, 4</td>
<td>ssf8</td>
<td>tab02c</td>
<td>t03</td>
<td>t01a</td>
<td>tab02cd</td>
<td>t03</td>
<td>t01</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>2, 2 or 5, 5</td>
<td>ssf9</td>
<td>t01a</td>
<td>tab02c</td>
<td>t03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>2, 5 or 5, 2</td>
<td>ssf10</td>
<td>t03</td>
<td>t01a</td>
<td>tab02c</td>
<td>t03</td>
<td>t01a</td>
<td>tab02cd</td>
<td>t03</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>2, 6 or 5, 3</td>
<td>ssf11</td>
<td>t01a</td>
<td>tab02c</td>
<td>t03</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>2, 3 or 5, 6</td>
<td>ssf12</td>
<td>t01a</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td>t02</td>
<td>tcd03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>3, 1 or 4, 6</td>
<td>ssf13</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td>tab02cd</td>
<td>t03</td>
<td>t01</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>3, 4 or 6, 1</td>
<td>ssf14</td>
<td>t02</td>
<td>t01</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td>t02</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>3, 5 or 6, 2</td>
<td>ssf15</td>
<td>t01ab</td>
<td>t02</td>
<td>t03</td>
<td>t01ab</td>
<td>t02</td>
<td>t03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>3, 2 or 6, 5</td>
<td>ssf16</td>
<td>t01</td>
<td>t02</td>
<td>t03</td>
<td>t01ab</td>
<td>t02</td>
<td>t03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>3, 3 or 6, 6</td>
<td>ssf17</td>
<td>t01ab</td>
<td>t02</td>
<td>tcd03</td>
<td>t01ab</td>
<td>t02</td>
<td>t03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>3, 6 or 6, 3</td>
<td>ssf18</td>
<td>t01</td>
<td>tab02cd</td>
<td>t03</td>
<td>t01ab</td>
<td>t02</td>
<td>t03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The complete gate timing for the nine bidirectional switches using Direct SSVM algorithm is given in Table 8.8 below:

\[
\begin{align*}
    t_{01ab} &= (t_b || t_{01} || t_a) \\
    t_{b02c} &= (t_c || t_{02} || t_b) \\
    t_{ab02cd} &= (t_d || t_{b2} || t_c || t_d) \\
    t_{cd03} &= (t_d || t_{c03}) \\
\end{align*}
\]

In equation 8.15, symbol (||) represents logical OR operation.

8.5.5 GATE PULSE GENERATOR: The gate pulse generator for the MC is developed using Embedded MATLAB as shown in Fig. 8.12. The sector switch functions ssf1 to ssf18, gate pulse timing calculator outputs defined in equations 8.14 and 8.15 form the input modules and the outputs are the gate pulses for the nine bidirectional switches of the MC. In Table 8.8, the gate timing for the nine bidirectional switches are shown. The gate timing for switch SAa can be combined by logically ANDing the respective value with sector switch function ssf_x and ORing the value for each sector. Thus the gate timing pulse for switch SAa can be expressed as in equation 8.16 below:

\[
    \text{SAa} = \text{ssf1} \& (\text{tab02cd}) || \text{ssf2} \& (t02) || \text{ssf3} \& (t03) || \ldots || \text{ssf18} \& (t01) \ldots \ldots \quad (8.16)
\]

Program segment VI gives the method of generating the gate timing pulses for the nine bidirectional switches using the calculated sector timings given in Table 8.8.

8.6 SIMULATION RESULTS: The simulation of the Three Phase SSVM Matrix Converter was carried out in SIMULINK [ 51 ]. The parameters used for simulation are shown in Table 8.6. The
ode15s(Stiff/NDF) solver was used. Simulation of the above three phase AC to three phase AC direct SSVM of MC was carried out for two different output frequencies with all other parameters constant.

The simulation results of the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage for a 50 Hz AC output voltage are shown in Fig. 8.14(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.15(A) to (D). Similarly the harmonic spectrum of the above in order for a 20 Hz AC output voltage are shown in Fig. 8.16(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.17(A) to (D). The simulation results are tabulated in Table 8.9.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>50 – 50</td>
<td>0.9913</td>
<td>1.85</td>
<td>2.5136</td>
<td>0.4541</td>
</tr>
<tr>
<td>2)</td>
<td>50 – 20</td>
<td>0.8925</td>
<td>1.3041</td>
<td>1.5777</td>
<td>0.3867</td>
</tr>
</tbody>
</table>

8.7 MODEL OF CENTRE ZERO ASYMMETRICAL SPACE VECTOR MODULATED THREE PHASE MATRIX CONVERTER: This method is newly proposed here. This is a modification of the direct ASVM technique discussed in section 8.2 above. The Table 8.1, 8.2 and 8.3 and the rules 1 and 2 discussed in section 8.2 above are used here to develop the model of the new Centre Zero ASVM (CZASVM) three phase MC. The equations 8.5 to 8.10 are used to calculate the duty-ratios d0, dI, dII, dIII, dIV and d0. With regard to zero configuration for CZASVM, Table 8.3
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![Graph 1: Three Phase SVM 50 Hz AC to 50 Hz AC MC - Line to Neutral Output Voltage in Volts](image1)

![Graph 2: Fundamental (f=50 Hz) = 137.2, THD = 13.45%](image2)

![Graph 3: Three Phase SVM 50 Hz AC to 50 Hz AC SVM MC - Input Current in Amperes](image3)

![Graph 4: Fundamental (f=50 Hz) = 0.6245, THD = 137.89%](image4)

![Graph 5: Three Phase SVM 50 Hz AC to 50 Hz AC SVM MC - Load Current in Amperes](image5)

![Graph 6: Fundamental (f=50 Hz) = 1.146, THD = 38.67%](image6)

![Graph 7: Three Phase SVM 50 Hz AC to 50 Hz AC SVM MC - Line to Line Output Voltage in Volts](image7)

![Graph 8: Fundamental (f=50 Hz) = 125.5, THD = 9.25%](image8)
Chapter VIII: Direct Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter
shown above can be used. For example, considering output voltage vector in sector 1 and input current vector in sector 4 (i.e., SV = 1; SI = 4) within their respective hexagons, it can be seen that (SV + SI) is odd, rule 2 applies with \( \delta I \) and \( \delta IV \) having negative sign. Also using Table 8.3, the following is the only possible sequence that can be generated for CZASVM technique:

\[
\text{CCA – CAA – BAA – AAA} \quad \text{| AAA - BBA – BAA – CAA – CCA}
\]

\[\rightarrow \text{-------------Ts/2--------------------- \rightarrow}\]

where Ts is the sampling period.

The gate pulse pattern for CZASVM using Tables 8.1 to 8.3, rules 1 and 2 is shown in Table 8.10.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>(SV, SI)</th>
<th>SSF_X</th>
<th>BIDIRECTIONAL SWITCH GATE PULSE PATTERN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1, 1 or 4, 4</td>
<td>Even</td>
<td>ssf1 ACC ACC AAB ABB AAA</td>
</tr>
<tr>
<td>2</td>
<td>1, 4 or 4, 1</td>
<td>Odd</td>
<td>ssf2 CCA CAA BBA BBA AAA</td>
</tr>
<tr>
<td>3</td>
<td>1, 5 or 4, 2</td>
<td>Even</td>
<td>ssf3 BCB CCB CCA CAA CCC</td>
</tr>
<tr>
<td>4</td>
<td>1, 4 or 5, 4</td>
<td>Odd</td>
<td>ssf4 ABB CBB CBB CBB CBB</td>
</tr>
<tr>
<td>5</td>
<td>1, 3 or 4, 6</td>
<td>Even</td>
<td>ssf5 BAA BBA BCC BCC BBB</td>
</tr>
<tr>
<td>6</td>
<td>1, 6 or 4, 3</td>
<td>Odd</td>
<td>ssf6 AAB ABB CBB CCB BBB</td>
</tr>
<tr>
<td>7</td>
<td>2, 4 or 5, 1</td>
<td>Even</td>
<td>ssf7 CCA ACA ABA BBA AAA</td>
</tr>
<tr>
<td>8</td>
<td>2, 1 or 5, 4</td>
<td>Odd</td>
<td>ssf8 CAC AAC AAB BAB AAA</td>
</tr>
<tr>
<td>9</td>
<td>2, 2 or 5, 5</td>
<td>Even</td>
<td>ssf9 BBC CBC CAC AAC CCC</td>
</tr>
<tr>
<td>10</td>
<td>2, 5 or 5, 2</td>
<td>Odd</td>
<td>ssf10 BCB CCB CCA ACA CCC</td>
</tr>
<tr>
<td>11</td>
<td>2, 6 or 5, 3</td>
<td>Even</td>
<td>ssf11 AAB BAB BCB CCB BBB</td>
</tr>
<tr>
<td>12</td>
<td>2, 3 or 5, 6</td>
<td>Odd</td>
<td>ssf12 ABA BBA BBC CBC BBB</td>
</tr>
<tr>
<td>13</td>
<td>3, 1 or 6, 4</td>
<td>Even</td>
<td>ssf13 CAC CAA BAA BAB AAA</td>
</tr>
<tr>
<td>14</td>
<td>3, 4 or 6, 1</td>
<td>Odd</td>
<td>ssf14 ACC ACA ABA ABB AAA</td>
</tr>
<tr>
<td>15</td>
<td>3, 5 or 6, 2</td>
<td>Even</td>
<td>ssf15 BCB BCC ACC ACA CCC</td>
</tr>
<tr>
<td>16</td>
<td>3, 2 or 6, 5</td>
<td>Odd</td>
<td>ssf16 CBB CBC CAC CAA CCC</td>
</tr>
<tr>
<td>17</td>
<td>3, 3 or 6, 6</td>
<td>Even</td>
<td>ssf17 ABA ABB CBB CBC BBB</td>
</tr>
<tr>
<td>18</td>
<td>3, 6 or 6, 3</td>
<td>Odd</td>
<td>ssf18 BAA BAB BCB BCC BBB</td>
</tr>
</tbody>
</table>

The SIMULINK model of the direct Centre Zero Asymmetrical Space Vector Modulated (CZASVM) three phase AC to three phase AC MC is shown in Fig. 8.18. The power circuit of the model is developed using the SimPowerSystems blockset in SIMULINK [51]. This mainly consists of three phase AC voltage source, bidirectional switch matrix, output filter and R-L load. The arrangement of the bidirectional switch matrix using IGBTs is the same as shown in Fig. 3.2 of Chapter III.

The modulation algorithm is developed in several sub units using Embedded MATLAB Function, MATLAB Function, Math Function, Logical and Bit Operator and using Sources block set in SIMULINK [51]. The various sub units are explained below:

### 8.7.1 DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR:

This is developed using Embedded MATLAB Function block in SIMULINK, as shown in Fig. 8.18. With peak line to neutral input voltage, desired peak output phase voltage, input frequency, output frequency, time, angular frequency of reference frame \( \omega c \) as input parameters, the three phase output voltage can be resolved into dq-axis component voltages [42] and the absolute value of the angle of the output phase voltage, \( \text{vout\_angle} \) can be calculated using the function \( \text{atan2(vq,vd)} \). Using input voltage and input phase displacement angle, a similar procedure is used to calculate the absolute value of the input current angle, \( \text{i\_in\_angle} \). The value of reference frame frequency \( \omega c \) is zero. This
Chapter VIII: Direct Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

FIG. 8.18: SIMULINK MODEL OF THREE PHASE AC TO THREE PHASE AC CENTRE ZERO ASVM MATRIX CONVERTER

NOTE: THIS IS AN ACCURATE MODEL. BUT HARMONIC PERFORMANCE IS NOT AS GOOD AS CONVENTIONAL THREE PHASE ASVM MATRIX CONVERTER

Discrete, $T_s = 1 \times 10^{-5}$ s.

powergui

Three-Phase V-I Measurement

BIDIRECTIONAL SWITCH MATRIX

OUTPUT VOLTAGE AND INPUT CURRENT

SECTOR CALCULATOR

OUTPUT FILTER

Carrier Generator

signal rms

node 0

node 0

node 0

10 kHz Triangle

PHI_I

From

SV

ssi

tab0cd

tcd
	bc

tdc

tab

t0

td

tc
	b

ta

t

THREE PHASE AC VOLTAGE SOURCE

Embedded MATLAB Function

THREE PHASE MC CENTRE ZERO ASVM - GATE PULSE GENERATOR

DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR

Display
is illustrated in Program segment I above. These two values of \( v_{out\_angle} \) and \( i_{in\_angle} \) are used to calculate the output voltage sector \( sv \), input current sector \( si \), \( \alpha \) and \( \beta \) values for output voltage and input current using MATLAB function, REM functions and SUBTRACT modules.

Program segment VII illustrates the MATLAB code for duty cycle sequencing and sector switch function generation. Duty-cycle \( dI \), \( dII \), \( dIII \), \( dIV \) and \( d0 \) are calculated using equations 8.5 to 8.8 and 8.10 assuming unity input power factor. With \( (sv+si) \) even and odd, rule 1 and 2 for duty cycle are followed with zero vector duty cycle \( d0 \) introduced at the end of the four duty cycles, \( dI \), \( dII \), \( dIII \), \( dIV \). This is used to calculate the timing \( A, B, C, D \) and \( E \), by comparison of the cumulative sector timing with a triangle carrier \( V_{tri} \) as shown in Program Segment VII. This triangle carrier \( V_{tri} \) has a period \( Ts \), peak value \( Ts/2 \) Volts and minimum value zero, as shown in Fig. 8.4. Cumulative sector timing is obtained by appropriately adding the value of duty-ratio and multiplying by \( Ts/2 \), as per rules 1 and 2 given above. Sector switch functions \( ssf1 \) to \( ssf18 \) are determined using if-then-else statement. For example sector switch function \( ssf1 \) is HIGH only when \( sv = si = 1 \) or \( sv = si = 4 \) and is LOW otherwise.

### 8.7.2 OUTPUT VOLTAGE AND INPUT CURRENT SECTOR CALCULATOR:

This is developed using MATLAB Function, a mux and a demux as shown in Fig. 8.5 above. The input to the mux are \( v_{out\_angle} \) and \( i_{in\_angle} \). The output from the demux are \( SV \) and \( SI \). The source code to determine \( SV \) and \( SI \) is shown in Program Segment III above.

### 8.7.3 OUTPUT VOLTAGE AND INPUT CURRENT REFERENCE ANGLE CALCULATOR:

This is shown in Fig. 8.6 above. This uses two REM function blocks and SUBTRACT modules. The first REM block has the inputs \( v_{out\_angle} \) and \( \pi/3 \). The second REM block has the inputs \( i_{in\_angle} \) and \( \pi/3 \). The output of the first REM block is subtracted from \( \pi/6 \) to obtain angle \( \alpha \) defined in Fig. 8.2(A). The output of the second REM block is subtracted from \( \pi/6 \), input p.f. angle \( \phi_i \) and once again from \( \pi/6 \) to obtain \( \beta \) as per the configuration defined in Fig. 8.2(B).

### 8.7.4 GATE PULSE TIMING CALCULATOR:

This is shown in Fig. 8.19. The inputs \( in1 \) to \( in5 \) are \( A, B, C, D \) and \( E \) respectively. The individual gate pulse timing, \( ta, tb, tc, td \) and \( t0 \) are respectively \( dIII*Ts/(2), dI*Ts/(2), dII*Ts/(2), dIV*Ts/(2) \) and \( d0*Ts/(2) \), when \( (SV+SI) \) is even and \( dI*Ts/(2), dIII*Ts/(2), dIV*Ts/(2), dII*Ts/(2) \) and \( d0*Ts/(2) \), when \( (SV+SI) \) is odd. This individual gate pulse duration is obtained as shown in equation 8.17 below:

\[
\begin{align*}
    t_a &= (A \& A) \\
    t_b &= (~A \& B) \\
    t_c &= (~B \& C) \\
    t_d &= (~C \& D) \\
    t_0 &= (~D \& E) \ldots 
\end{align*}
\] (8.17)
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PROGRAM SEGMENT VII

function(q,dI,dII,dIII,dIV,d0,A,B,C,D,E,ssf1,ssf2,ssf3,…ssf18) =
fcn(Vom,fo,i,Vim,fi,wc_phi_i,alfa,sv,si,Ts,vtri)

%% Duty cycle calculations
\[ dI = \frac{2q \cdot \cos(\alpha - \frac{\pi}{3}) \cdot \cos(\beta - \frac{\pi}{3})}{\sqrt{3} \cdot \cos(\phi_i)} \]
\[ dII = \frac{2q \cdot \cos(\alpha - \frac{\pi}{3}) \cdot \cos(\beta + \frac{\pi}{3})}{\sqrt{3} \cdot \cos(\phi_i)} \]
\[ dIII = \frac{2q \cdot \cos(\alpha + \frac{\pi}{3}) \cdot \cos(\beta - \frac{\pi}{3})}{\sqrt{3} \cdot \cos(\phi_i)} \]
\[ dIV = \frac{2q \cdot \cos(\alpha + \frac{\pi}{3}) \cdot \cos(\beta + \frac{\pi}{3})}{\sqrt{3} \cdot \cos(\phi_i)} \]
\[ d0 = 1 - dI - dII - dIII - dIV \]

if (rem(sv+si,2) == 0)
%% even sequence
if (vtri <= dIII*Ts/(2))
\[ A = 1 \]
else
\[ A = 0 \]
end
if (vtri <= (dIII + dI)*Ts/(2))
\[ B = 1 \]
else
\[ B = 0 \]
end
if (vtri <= (dIII + dI + dII)*Ts/(2))
\[ C = 1 \]
else
\[ C = 0 \]
end
if (vtri <= (dIII + dI + dII + dIV)*Ts/(2))
\[ D = 1 \]
else
\[ D = 0 \]
end
if (vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
\[ E = 1 \]
else
\[ E = 0 \]
end
else
%% odd sequence
if (vtri <= dI*Ts/(2))
\[ A = 1 \]
else
\[ A = 0 \]
end
if (vtri <= (dIII + dI)*Ts/(2))
\[ B = 1 \]
else
\[ B = 0 \]
end
if (vtri <= (dIII + dI + dIV)*Ts/(2))
\[ C = 1 \]
else
\[ C = 0 \]
end
if (vtri <= (dIII + dI + dII + dIV)*Ts/(2))
\[ D = 1 \]
else
\[ D = 0 \]
end
if (vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
\[ E = 1 \]
else
\[ E = 0 \]
end
end
if (sv == 1 && si == 1 || sv == 4 && si == 4)
%% sector 1. sector switch function ssf1.
ssf1 = 1; else
ssf1 = 0;
end
if (sv == 4 && si == 1 || sv == 1 && si == 4)
%% sector 2. sector switch function ssf2.
ssf2 = 1; else
ssf2 = 0;
end
if (sv == 1 && si == 6 || sv == 6 && si == 1 || sv == 4 && si == 4)
%% sector 3. sector switch function ssf3.
ssf3 = 1; else
ssf3 = 0;
end
...
The complete gate timing for the nine bidirectional switches using CZASVM algorithm is given in Table 8.11 below:

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>SV.SL</th>
<th>SSF_X HIGH</th>
<th>SAa</th>
<th>SBa</th>
<th>SCa</th>
<th>Sab</th>
<th>SBb</th>
<th>SCb</th>
<th>SAC</th>
<th>SBc</th>
<th>SCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1,1</td>
<td>ssf1</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>tbo0c</td>
<td>td</td>
<td>ta</td>
<td>t0</td>
<td>tbo0c</td>
<td>tab0cd</td>
</tr>
<tr>
<td>2</td>
<td>1,2</td>
<td>ssf2</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
<td>tbo0c</td>
<td>td</td>
<td>ta</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>1,3</td>
<td>ssf3</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
<td>td</td>
<td>ta</td>
<td>tbo0c</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
</tr>
<tr>
<td>4</td>
<td>1,4</td>
<td>ssf4</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
<td>td</td>
<td>ta</td>
<td>tbo0c</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
</tr>
<tr>
<td>5</td>
<td>1,5</td>
<td>ssf5</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
<td>ta</td>
<td>tbo0c</td>
<td>td</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
</tr>
<tr>
<td>6</td>
<td>1,6</td>
<td>ssf6</td>
<td>t0</td>
<td>tcd</td>
<td>ta</td>
<td>tbo0c</td>
<td>td</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>2,1</td>
<td>ssf7</td>
<td>tbo0c</td>
<td>td</td>
<td>ta</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>2,2</td>
<td>ssf8</td>
<td>tbo0c</td>
<td>td</td>
<td>ta</td>
<td>t0</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>t0</td>
<td>tcd</td>
</tr>
<tr>
<td>9</td>
<td>2,3</td>
<td>ssf9</td>
<td>td</td>
<td>ta</td>
<td>tbo0c</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
</tr>
<tr>
<td>10</td>
<td>2,4</td>
<td>ssf10</td>
<td>td</td>
<td>ta</td>
<td>tbo0c</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
</tr>
<tr>
<td>11</td>
<td>2,5</td>
<td>ssf11</td>
<td>ta</td>
<td>tbo0c</td>
<td>td</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
</tr>
<tr>
<td>12</td>
<td>2,6</td>
<td>ssf12</td>
<td>ta</td>
<td>tbo0c</td>
<td>td</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
</tr>
<tr>
<td>13</td>
<td>3,1</td>
<td>ssf13</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>tbo0c</td>
<td>td</td>
<td>ta</td>
</tr>
<tr>
<td>14</td>
<td>3,2</td>
<td>ssf14</td>
<td>tab0cd</td>
<td>0</td>
<td>0</td>
<td>t0</td>
<td>tcd</td>
<td>tab</td>
<td>tbo0c</td>
<td>td</td>
<td>ta</td>
</tr>
<tr>
<td>15</td>
<td>3,3</td>
<td>ssf15</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
<td>td</td>
<td>ta</td>
<td>tbo0c</td>
</tr>
<tr>
<td>16</td>
<td>3,4</td>
<td>ssf16</td>
<td>0</td>
<td>0</td>
<td>tab0cd</td>
<td>tcd</td>
<td>tab</td>
<td>t0</td>
<td>td</td>
<td>ta</td>
<td>tbo0c</td>
</tr>
<tr>
<td>17</td>
<td>3,5</td>
<td>ssf17</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
<td>tab0cd</td>
<td>0</td>
<td>ta</td>
<td>tbo0c</td>
<td>td</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>3,6</td>
<td>ssf18</td>
<td>0</td>
<td>tab0cd</td>
<td>0</td>
<td>tab</td>
<td>t0</td>
<td>tcd</td>
<td>ta</td>
<td>tbo0c</td>
<td>td</td>
</tr>
</tbody>
</table>

8.7.5 GATE PULSE GENERATOR: The gate pulse generator for the MC is developed using Embedded MATLAB as shown in Fig. 8.18. The sector switch functions ssf1 to ssf18, gate pulse timing calculator outputs defined in equations 8.17 and 8.18 form the input modules and the outputs are the gate pulses for the nine bidirectional switches of the MC. In Table 8.11, the gate timing for the nine bidirectional switches are shown. The gate timing for switch SAa can be combined by logically ANDing the respective value with sector switch function ssf_x and ORing the value for each sector. Thus the gate timing pulse for switch SAa can be expressed as in equation 8.19 below:

\[ SAa = ssf1 \& (tab0cd) || ssf2 (t0) || ssf3 (0) || \ldots \ldots || ssf18 (0) \ldots (8.19) \]
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Program segment VIII gives the method of generating the gate timing pulses for the nine bidirectional switches using the calculated sector timings given in Table 8.11.

**PROGRAM SEGMENT VIII**

```
function [SAa,SBa,SCa,SAb,SBb,SCb,SAc,SBc,SCc] = fcn(ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12,ssf13,ssf14,ssf15,ssf16,ssf17,ssf18,tab0c,tab0cd,tab1c,tab1cd,tab0c1,tab0cd1,tab1c1,tab1cd1)

%%%Narayanaswamy. P.R.Iyer.

SAa = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
SBa = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
SCa = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
SAb = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
SBb = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
SCb = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
SAc = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
SBc = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
SCc = sssf1&(tab0c)&(tab0cd1)\&(ssf13&(tab0cd)&ssf14&(tab)&ssf15&(tab0c)&ssf16&(tab1cd)&ssf17&(tab1c)&ssf18&(tab0c1);
```

8.8 SIMULATION RESULTS: The simulation of the Three Phase CZASVM Matrix Converter was carried out in SIMULINK [51]. The parameters used for simulation are shown in Table 8.6. The ode15s(Stiff/NDF) solver was used. Simulation of the above three phase AC to three phase AC direct CZASVM of MC was carried out for two different output frequencies with all other parameters constant. The simulation results of the harmonic spectrum of line to neutral output voltage, input current, load current and load line to line output voltage for a 50 Hz AC output voltage are shown in Fig. 8.20(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.21(A) to (D). Similarly the harmonic spectrum of the above in order for a 20 Hz AC output voltage are shown in Fig. 8.22(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.23(A) to (D). The simulation results are tabulated in Table 8.12.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>50 – 50</td>
<td>1.5989</td>
<td>2.8457</td>
<td>0.8002</td>
<td>3.9414</td>
<td>0.8002</td>
</tr>
<tr>
<td>2)</td>
<td>50 – 20</td>
<td>1.2932</td>
<td>2.2127</td>
<td>0.3569</td>
<td>3.8462</td>
<td>0.3569</td>
</tr>
</tbody>
</table>

TABLE 8.12: CZASVM Simulation Results 3

8.9 DISCUSSION OF RESULTS: The Centre Zero ASVM (CZASVM) is a newly proposed Space Vector Modulation technique. The THD of line to neutral and line to line output voltage, input current and load current decreases as the output frequency is reduced. However for ASVM technique the THD of load current increases as the output frequency is reduced. Although CZASVM technique is presented here, from the point of harmonic performance of the MC, it is found to be inferior to
Chapter VIII: Direct Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

![Graph](image1)

![Graph](image2)

![Graph](image3)

![Graph](image4)
Chapter VIII: Direct Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter
three phase ASVM and S SVM techniques. The input power factor is assumed to be unity in this analysis. In all the three SVM techniques, it is seen from the simulation results that all the harmonic components are centred around the integral multiples of carrier switching frequency. The ASVM and CZASVM have eight commutations, whereas SSVM has twelve commutations per carrier switching period.

8.10 CONCLUSIONS: The model of the three phase AC to three phase AC MC has been developed in SIMULINK using the Duty-Cycle Space Vector approach. All possible switching combinations are represented by space vectors. The SVM technique for three phase MC is considered an optimal solution. Owing to its intrinsic two degrees of freedom, SVM technique represents the general solution of the matrix converter modulation problem and can be considered the best solution for achieving the highest voltage transfer ratio and optimizing the switching pattern through a suitable use of the zero configurations. Placing of the zero vector at the centre of the sampling interval which is named here as CZASVM technique is inferior to the ASVM and SSVM techniques from the point of view of harmonic performance of line to neutral, line to line output voltages, input current and load currents. With SVM technique modulation ratio as high as 0.866 can be achieved. The SSVM technique is found to be better from the point of view of harmonic performance of the MC as compared to ASVM and CZASVM techniques.

A8.1 APPENDIX: Using the line to line to line to neutral voltage transformation, we have the following transformation matrix:

\[
\begin{bmatrix}
V_{an} \\
V_{bn} \\
V_{cn}
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
1 & 0 & -1 \\
-1 & 1 & 0 \\
0 & -1 & 1
\end{bmatrix} \cdot \begin{bmatrix}
V_{ab} \\
V_{bc} \\
V_{ca}
\end{bmatrix} \quad \text{(A8.1.1)}
\]

From serial number 1 of Table 8.1, from the output states column, we have

\[
\begin{align*}
V_{ab} &= V_{AB} \\
V_{bc} &= 0 \\
V_{ca} &= -V_{AB}
\end{align*} \quad \text{(A8.1.2)}
\]

Using equation A8.1.2 in A8.1.1 and simplifying, we have

\[
\begin{align*}
V_{an} &= \frac{2 * V_{AB}}{3} \\
V_{bn} &= -\frac{2\pi V_{AB}}{3} \\
V_{cn} &= -\frac{4\pi V_{AB}}{3}
\end{align*} \quad \text{(A8.1.3)}
\]

The output phase voltage reference is \(V_{an}\) in equation A8.1.3, which corresponds to column 4 of Table 8.1.

Similarly corresponding to serial number 12 of Table 8.1, we have

\[
\begin{align*}
V_{ab} &= V_{CA} \\
V_{bc} &= -V_{CA} \\
V_{ca} &= 0
\end{align*} \quad \text{(A8.1.4)}
\]

Using equation A8.1.4 in A.1 and simplifying, we have
The output phase voltage reference is $V_{bn}$ in equation A8.1.5, which corresponds to column 4 of Table 8.1.

For serial number 17 of Table 8.1, we have

$$
V_{ab} = 0 \\
V_{bc} = -V_{CA} \\
V_{ca} = V_{CA}
$$

Using equation A8.1.6 in A8.1.1 and simplifying, we have

$$
V_{an} = -V_{CA} / \frac{0}{3} \\
V_{bn} = -V_{CA} / \frac{2\pi}{3} \\
V_{cn} = -V_{CA} / \frac{4\pi}{3}
$$

The output phase voltage reference is $V_{ca}$ in equation A8.1.7, which corresponds to column 4 of Table 8.1. Similar transformation applies to input current vector, as shown below:

For phase current to line current transformation assume that the three phase load connected to the MC are in DELTA and the three phase load currents are $i_{ab}$, $i_{bc}$ and $i_{ca}$ and the input line currents are $i_A$, $i_B$ and $i_C$ respectively. Then the following transformation apply:

$$
\begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = (-) \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_{ab} \\
i_{bc} \\
i_{ca}
\end{bmatrix} \quad (A8.1.8)
$$

For serial number 1 of Table 8.1, we have $i_{ab} = i_a/\sqrt{3}$; $i_{bc} = -i_a/\sqrt{3}$; $i_{ca} = 0$. Using this values of phase currents in equation A8.1.8, we have the following:

$$
i_A = -i_a/\sqrt{3}/\pi/2; i_B = 2*i_a/\sqrt{3}/_{-\pi/6}; i_C = -i_a/\sqrt{3}/_{-5\pi/6}... \quad (A8.1.9)
$$

Similarly for serial number 12 of Table 8.1, we have $i_{ab} = i_b/\sqrt{3}$; $i_{bc} = 0$; $i_{ca} = i_a/\sqrt{3}$. Using this values of phase currents in equation A8.1.8, we have the following:

$$
i_A = -2*i_b/\sqrt{3}/_{7\pi/6}; i_B = i_b/\sqrt{3}/_{\pi/2}; i_C = -i_b/\sqrt{3}/_{-\pi/6}... \quad (A8.1.10)
$$

Similarly for serial number 17 of Table 8.1, we have $i_{ab} = -i_c/\sqrt{3}$; $i_{bc} = 0$; $i_{ca} = i_c/\sqrt{3}$. Using this values of phase currents in equation A8.1.8, we have the following:

$$
i_A = 2*i_c/\sqrt{3}/_{7\pi/6}; i_B = -i_c/\sqrt{3}/_{\pi/2}; i_C = -i_c/\sqrt{3}/_{-\pi/6}... \quad (A8.1.11)
$$

Equations A8.1.9, A8.1.10, A8.1.11 confirms with Table 8.1 column 4.

**A8.2 APPENDIX:** Proof of equations 8.1 and 8.2 are given below. Referring to Fig. A8.2.1, the line voltage $V_{v}$ from origin can be expressed as follows:
Chapter VIII: Direct Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

Thus \( v_{o\beta} \) from the origin can be expressed as follows:

\[
v_{o\beta} = \frac{V_o}{\cos\left(\frac{\pi}{3}\right)} = \frac{2}{\sqrt{3}} V_o \cos\left(\frac{\pi}{3} - \alpha\right) \quad \text{(A8.2.1)}
\]

The expression \( e^{j(S_r-1)\frac{\pi}{3}} \) in equation 8.1 gives the location of \( v_{o\beta} \) as the output voltage sector number changes from 1 to 6. Thus in sector 1, \( v_{o\beta} \) is having \( \pi/3 \) radians and in sector 6, this value is \( 2\pi \) radians.

Similarly resolving \( v_o \) in a direction perpendicular to \( v_{o\beta} \), we have the following equation for \( V_h \) from the origin:

\[
V_h = V_o * \cos\left(\frac{\pi}{3} + \alpha\right) \quad \text{(A8.2.2)}
\]

The expression \( e^{j(S_r-1)\frac{\pi}{3}} \) in equation 8.2 gives the location of \( v_{oa} \) as the output voltage sector number changes from 1 to 6. Thus in sector 1, \( v_{oa} \) is having zero radians and in sector 6, this value is \( 5\pi/3 \) radians.

The solution of equations 8.1 and 8.3, to find the duty cycle \( \delta^I \) and \( \delta^{II} \) for the first two switching configurations are given below:

\[
\delta^I = \left[ \begin{array}{c} \frac{2}{\sqrt{3}} v_o * \cos\left(\alpha - \frac{\pi}{3}\right) * e^{j(S_r-1)\frac{\pi}{3}} \v_o \n \frac{2}{\sqrt{3}} v_o * e^{j(S_r-1)\frac{\pi}{3}} \end{array} \right] \quad \text{(A8.2.5)}
\]

Simplifying and rewriting equation A8.2.5, we have the following:

\[
\delta^I = \left[ \begin{array}{c} \frac{2}{\sqrt{3}} v_o * i_{I^*} * \cos\left(\alpha - \frac{\pi}{3}\right) * e^{j(S_r+S_r-2)\frac{\pi}{3}} \v_o \n \frac{2}{\sqrt{3}} v_o * e^{j(S_r-1)\frac{\pi}{3}} \end{array} \right] \quad \text{(A8.2.6)}
\]

Considering the real part, the denominator of equation A8.2.6 gives the output power delivered. This is also the input power neglecting switching losses. Thus the denominator of equation A8.2.6 can be replaced by the following:

\[
V_v = V_o * \cos\left(\frac{\pi}{3} - \alpha\right) \quad \text{(A8.2.1)}
\]
Simplifying and rewriting equation A8.2.13, we have the following:

\[
\frac{-\frac{V_o}{i_l} * e^{j[(S_i - 1)\frac{\pi}{3} + \beta]} - \frac{V_o}{i_l} * e^{j[(S_i - 1)\frac{\pi}{3} + \beta]} = V_i * I_i * \cos(\phi_i)}{\cos(\phi_i)} \quad \text{(A8.2.7)}
\]

In equation A8.2.6, \(\frac{V_o}{i_l} \) and \(\frac{V_o}{i_l} \) are the value of \(I_i \) for the first and second switching configuration. Thus using equation A8.2.6 and A8.2.7, duty-cycle \(\delta^I \) can be expressed as follows:

\[
\delta^I = \frac{2}{\sqrt{3}} * q * \cos \left(\alpha - \frac{\pi}{3}\right) * \cos \left[(S_v + S_i - 2)\frac{\pi}{3} + \frac{\pi}{3} + \beta\right] \quad \text{(A8.2.8)}
\]

Similarly solving for duty-cycle \(\delta^{II} \) we have the following equation:

\[
\delta^{II} = \frac{2}{\sqrt{3}} * \frac{V_o}{i_l} * e^{j[(S_i + 1)\frac{\pi}{3}]} - \frac{V_o}{i_l} * e^{j[(S_i - 1)\frac{\pi}{3} + \beta]} \quad \text{(A8.2.9)}
\]

\[i.e., \quad \delta^{II} = \frac{2}{\sqrt{3}} * q * \cos \left(\alpha - \frac{\pi}{3}\right) * \cos \left[(S_v + S_i - 1)\beta - \pi/3\right] \quad \text{(A8.2.10)}\]

Duty-cycle \(\delta^I \) corresponds to the case when \((S_v+S_i)\) is odd. Thus when \((S_v+S_i)\) is 3, using equation A8.2.8, \(\cos(\beta+2\pi/3)\) can be expressed as \(\cos(\pi + (\beta - \pi/3))\) which is \((-1) \cos(\beta - \pi/3)\). Thus equation A8.2.8 can be expressed as follows:

\[
\delta^I = \frac{(-1)(S_v+S_i) * 2}{\sqrt{3}} * q * \cos \left(\alpha - \frac{\pi}{3}\right) * \cos(\beta + \pi/3) \quad \text{(A8.2.11)}
\]

Duty-cycle \(\delta^{II} \) corresponds to the case when \((S_v+S_i)\) is even. Thus when \((S_v+S_i)\) is 2, using equation A8.2.9, we have the following:

\[
\delta^{II} = \frac{(-1)(S_v+S_i+1) * 2}{\sqrt{3}} * q * \cos \left(\alpha - \frac{\pi}{3}\right) * \cos(\beta - \pi/3) \quad \text{(A8.2.12)}
\]

In equations A8.2.11 and A8.2.12, \(q\) is the voltage transfer ratio \(v_o/v_i\). Similar derivations hold good for \(\delta^{III} \) and \(\delta^{IV} \), as given below:

The solution of equations 8.2 and 8.4, to find the duty cycle \(\delta^{III} \) and \(\delta^{IV} \) for the third and fourth switching configurations are given below:

\[
\delta^{III} = \begin{bmatrix}
\frac{2}{\sqrt{3}} * \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} \\
0 & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} \\
\frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} \\
\frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} \\
\end{bmatrix} \quad \text{(A8.2.13)}
\]

Simplifying and rewriting equation A8.2.13, we have the following:

\[
\delta^{III} = \begin{bmatrix}
\frac{2}{\sqrt{3}} * \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} \\
0 & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} \\
\frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} \\
\frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} & \frac{V_o}{i_l} * e^{j[(S_v - 1)\frac{\pi}{3}]} \\
\end{bmatrix} \quad \text{(A8.2.14)}
\]
Considering the real part, the denominator of equation A8.2.14 gives the output power delivered. This is also the input power neglecting switching losses. Thus the denominator of equation A8.2.14 can be replaced by the following:
\[
\frac{v_i^*}{i_i^*} \cdot e^{j[(s_i-1)\frac{\pi}{2} + \beta]} - \frac{v_o^*}{i_i^*} \cdot e^{j[(s_i-1)\frac{\pi}{2} + \beta]} = V_i \cdot I_i \cdot \cos(\phi_i) \quad \text{(A8.2.15)}
\]

In equation A8.2.14, \(i_i^{III}, i_i^{IV}\) are the value of \(I_i\) for the third and fourth switching configuration. Thus using equation A8.2.14 and A8.2.15, duty-cycle \(\delta^{III}\) can be expressed as follows:
\[
\delta^{III} = \frac{2}{\sqrt{3}} \cdot q \cdot \cos \left( \alpha + \frac{\pi}{3} \right) \cdot \cos \left( (S_v + S_i - 2) \cdot \frac{\pi}{3} + \beta \right) \cdot \frac{\cos(\phi_i)}{\cos(\phi_i)} \quad \text{(A8.2.16)}
\]

Similarly solving for duty-cycle \(\delta^{IV}\) we have the following equation:
\[
\delta^{IV} = \frac{2}{\sqrt{3}} \cdot q \cdot \cos \left( \alpha - \frac{\pi}{3} \right) \cdot \cos \left( (S_v + S_i - 2) \cdot \frac{\pi}{3} + \frac{\pi}{3} + \beta \right) \cdot \frac{\cos(\phi_i)}{\cos(\phi_i)} \quad \text{(A8.2.17)}
\]

Thus when \((S_v+S_i)\) is even. Thus when \((S_v+S_i)\) is 4, using equation A8.2.14, \(\cos(\beta + 2\pi/3)\) can be expressed as \(\cos[\pi + (\beta - \pi/3)]\) which is \((-1)^{*}\cos(\beta - \pi/3)\). Thus equation A8.2.16 can be expressed as follows:
\[
\delta^{III} = \frac{(-1)^{(S_v+S_i+1)}}{\sqrt{3}} \cdot q \cdot \cos \left( \alpha + \frac{\pi}{3} \right) \cdot \cos(\phi_i) \quad \text{(A8.2.19)}
\]

Duty-cycle \(\delta^{IV}\) corresponds to the case when \((S_v+S_i)\) is odd. Thus when \((S_v+S_i)\) is 3, using equation A8.2.17, we have the following:
\[
\delta^{IV} = \frac{(-1)^{(S_v+S_i)}}{\sqrt{3}} \cdot q \cdot \cos \left( \alpha + \frac{\pi}{3} \right) \cdot \cos(\phi_i) \quad \text{(A8.2.20)}
\]

Equations A8.2.19 and A8.2.20 well agree with equations 8.7 and 8.8 respectively.
Chapter IX

Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

9.1 INTRODUCTION: Three Phase AC to Three Phase AC Matrix Converter has advantages over the conventional three phase rectifier-inverter frequency converters in the sense that the former directly converts AC voltage at any given frequency to AC output voltage of any other magnitude and frequency without the need for a DC link capacitor storage element and with a regeneration capability [25-30]. In the proposed voltage Space Vector PWM control of MCs, the Indirect Transfer Function (ITF) approach is used where the input AC voltage is first rectified to create a fictitious DC voltage which is then inverted at the required output frequency [25-30]. For low harmonic distortion, the inverter operation is achieved by Space Vector Modulation (SVM) simultaneously with input current SVM for rectification [25-30]. The simultaneous output voltage-input current SVM algorithm is reviewed here and the model of the 3 X 3 MC is derived based on this algorithm using SIMULINK. The simulation results are presented.

9.2 PRINCIPLE OF INDIRECT SPACE VECTOR MODULATION: The three phase AC to three phase AC Conventional Matrix Converter (CMC) is shown in Fig. 9.1 with the load represented as a current source connected in delta. The equivalent circuit of this CMC is shown in Fig. 9.2. The CMC can be considered equivalent to a three phase rectifier forming a virtual DC link output voltage which is then inverted using a three phase inverter to get the required AC output voltage and frequency [25-30]. The model equivalence of Fig. 9.1 and Fig. 9.2 can be expressed as follows:
Using this Table 3.1 and Fig. 9.1, the following expressions for the output line voltage and input phase are obtained:

\[
\begin{bmatrix}
S_A \quad S_B \quad S_C
\end{bmatrix}
\begin{bmatrix}
S_a \\
S_b \\
S_c
\end{bmatrix}
= \begin{bmatrix}
S_7 \\
S_9 \\
S_{11}
\end{bmatrix}
\cap
\begin{bmatrix}
S_1 \\
S_3 \\
S_5
\end{bmatrix}
= \begin{bmatrix}
(s_7 \cap s_1) \cup (s_8 \cap s_2) \\
(s_7 \cap s_1) \cup (s_8 \cup s_4) \\
(s_7 \cap s_1) \cup (s_8 \cup s_6)
\end{bmatrix}
\]

(9.1)

where \( \cap = \text{Logical AND} \) \( \cup = \text{Logical OR} \).

The basic idea of the indirect SVM (ISVM) technique is to decouple the control of the input current and the control of the output voltage. Modeling the matrix converter in this way enables the well-known space vector PWM to be applied for a rectifier as well as an inverter stage independently [25-30, 41].

### 9.3 INDIRECT SPACE VECTOR MODULATION ALGORITHM:

The 3 X 3 matrix converter shown in Fig.9.1 connects the three phase ac source to the three phase load. The switching function for a 3 X 3 matrix converter can be defined as in equations 3.1 and 3.2 under section 3.2 in Chapter III. Also the twenty seven switching states of the 3 X 3 MC is presented in Table 3.1 in Chapter III. Using this Table 3.1 and Fig. 9.1, the following expressions for the output line voltage and input phase currents are obtained:

\[
\begin{bmatrix}
V_{ab} \\
V_{bc} \\
V_{ca}
\end{bmatrix} = \begin{bmatrix}
(S_a - S_b) \\
(S_b - S_c) \\
(S_c - S_a)
\end{bmatrix}
\begin{bmatrix}
S_a \\
S_b \\
S_c
\end{bmatrix}
\begin{bmatrix}
V_{AO} \\
V_{BO} \\
V_{CO}
\end{bmatrix}
+ \begin{bmatrix}
V_{AO} \\
V_{BO} \\
V_{CO}
\end{bmatrix}
= \begin{bmatrix}
V_{oa} \\
V_{ob} \\
V_{oc}
\end{bmatrix}
\begin{bmatrix}
S_a \\
S_b \\
S_c
\end{bmatrix}
\begin{bmatrix}
V_{AO} \\
V_{BO} \\
V_{CO}
\end{bmatrix}
\]

(9.2)

\[
\text{i.e. } V_{oa} = [T_{phl}]^T \cdot V_{iph}
\]

(9.3)

\[
\text{and } i_{iph} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix}
\]

(9.4)

\( T_{phl} \) is the instantaneous input phase to output line Transfer Function matrix of the three phase MC.

\[
\begin{bmatrix}
V_{ph} \\
V_{bo} \\
V_{co}
\end{bmatrix} = \begin{bmatrix}
S_a \\
S_b \\
S_c
\end{bmatrix}
\begin{bmatrix}
V_{AO} \\
V_{BO} \\
V_{CO}
\end{bmatrix}
\]

(9.5)

\[
\text{and } i_{iph} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix} = \begin{bmatrix}
i_A \\
i_B \\
i_C
\end{bmatrix}
\]

(9.6)

\( T_{iph} \) is the instantaneous input phase to output phase matrix. To use the HF synthesis, the switching frequency must be higher than the frequency of the input voltages and output currents. The switching function \( S_{kj} \) is the duty-cycle of the switch \( S_{kj} \) and is denoted by \( M_{kj} \). The LF equivalents are given below:

\[
0 \leq M_{kj} \leq 1 \text{ where } K \in A, B, C \text{ and } j \in a, b, c \quad (9.7)
\]

\[
M_{Aj} + M_{Bj} + M_{Cj} = 1 \text{ for } j \in a, b, c \quad (9.8)
\]

The remaining LF equivalents are given in equations 9.4 to 9.7. Equations for \( T_{phl} \) and \( T_{iph} \) can now be rewritten as follows:

\[
\begin{bmatrix}
T_{phl}
\end{bmatrix} = \begin{bmatrix}
(M_{AA} - M_{Ab}) \\
(M_{Ba} - M_{BB}) \\
(M_{Ca} - M_{Cb}) \\
(M_{AB} - M_{Ac}) \\
(M_{BB} - M_{bc}) \\
(M_{CBB} - M_{Cc}) \\
(M_{Ac} - M_{Ab}) \\
(M_{bc} - M_{ba}) \\
(M_{Cbc} - M_{Ca})
\end{bmatrix}
\]

(9.9)
Chapter IX: Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

Let the input phase voltage be expressed as follows:

\[ v_{\text{iph}} = V_{\text{im}} \begin{bmatrix} \cos(\omega_1 t) \\ \cos(\omega_1 t - 120^\circ) \\ \cos(\omega_1 t + 120^\circ) \end{bmatrix} \] (9.11)

The averaged output line voltage is expressed as follows:

\[ v_{\text{OL}} = \begin{bmatrix} v_{\text{ab}} \\ v_{\text{bc}} \\ v_{\text{ca}} \end{bmatrix} = \sqrt{3} * V_{\text{om}} \begin{bmatrix} \cos(\omega_0 t - \varphi_0 + 30^\circ) \\ \cos(\omega_0 t - \varphi_0 + 30^\circ - 120^\circ) \\ \cos(\omega_0 t - \varphi_0 + 30^\circ + 120^\circ) \end{bmatrix} \] (9.12)

where \( \varphi_0 \) is the output phase displacement angle. The input phase to output line transfer matrix is chosen as follows:

\[ [T_{\text{phL}}] = m * \begin{bmatrix} \cos(\omega_0 t - \varphi_0 + 30^\circ) & \cos(\omega_0 t - \varphi_L) \\ \cos(\omega_0 t - \varphi_0 + 30^\circ - 120^\circ) & \cos(\omega_0 t - \varphi_L - 120^\circ) \\ \cos(\omega_0 t - \varphi_0 + 30^\circ + 120^\circ) & \cos(\omega_0 t - \varphi_L + 120^\circ) \end{bmatrix}^T \] (9.13)

where \( 0 \leq m \leq 1 \) is the modulation index and \( \varphi_L \) is the input phase displacement angle.

Equations 9.11 to 9.13 satisfy equation 9.3 for value of \( V_{\text{om}} \) given below:

\[ V_{\text{om}} = \frac{\sqrt{3}}{2} * V_{\text{im}} * m * \cos(\varphi_L) \] (9.14)

The proof of equation 9.14 is given in A9.1Appendix. The output line current is assumed sinusoidal and is given below:

\[ i_{\text{OL}} = \begin{bmatrix} i_{\text{ab}} \\ i_{\text{bc}} \\ i_{\text{ca}} \end{bmatrix} = \frac{I_{\text{om}}}{\sqrt{3}} \begin{bmatrix} \cos(\omega_0 t - \varphi_0 - \varphi_L + 30^\circ) \\ \cos(\omega_0 t - \varphi_0 - \varphi_L + 30^\circ - 120^\circ) \\ \cos(\omega_0 t - \varphi_0 - \varphi_L + 30^\circ + 120^\circ) \end{bmatrix} \] (9.15)

where \( \varphi_L \) is the load displacement angle. At the output frequency \( f_0 \) Hz. If equations 9.14 and 9.15 are substituted in equation 9.4, the local averaged input currents are obtained as given below:

\[ i_{\text{iph}} = \begin{bmatrix} i_{\text{a}} \\ i_{\text{b}} \\ i_{\text{c}} \end{bmatrix} = I_{\text{im}} \begin{bmatrix} \cos(\omega_1 t) \\ \cos(\omega_1 t - 120^\circ) \\ \cos(\omega_1 t + 120^\circ) \end{bmatrix} \] (9.16)

where

\[ I_{\text{im}} = \frac{\sqrt{3}}{2} * I_{\text{om}} * m * \cos(\varphi_L) \] (9.17)

The proof of equation 9.17 is given in A9.2Appendix. Unity input displacement factor is obtained by letting \( \varphi_L \) equal to zero which from equation 9.14 results in a voltage gain of 0.866 for unity modulation index. The HF synthesis requires determination of the value of duty-cycle \( M_k \) and the position of the switching pulses such that the constraint given by equations 9.7 and 9.8 are satisfied and the required transfer matrix given by equation 9.13 is implemented. For the control of three phase AC to three phase MC, indirect and direct Transfer Function approaches are used. Here Indirect Transfer Function (ITF) approach is discussed below:

Equation 9.13 represents the ITF approach. The transfer matrix \( T_{\text{phL}} \) may be expressed as follows:

\[ [T_{\text{phL}}] = [T_{\text{VSI}}(\omega_0)] * [T_{\text{VSR}}(\omega_1)]^T \] (9.18)
Multiplying $[T_{VSR}(\omega_i)]^T$ with input phase voltage vector given by equation 9.11, the following is obtained:

$$[T_{VSR}(\omega_i)]^T * v_{iph} = \frac{3}{2} * V_{im} * \cos(\varphi_i) \quad (9.19)$$

This constant voltage given by equation 9.19 represents the operation of a Voltage Source Rectifier (VSR). Equation 9.19 is derived in A9.3 Appendix. Multiplying equation 9.19 with $[T_{VSI}(\omega_D)]$, the operation of a Voltage Source Inverter (VSI) is obtained. Therefor ITF approach emulates a VSR-VSI combination as shown in Fig. 9.2. From Fig. 9.2, it is clear that the three phase to three phase matrix converter falls to one of the six possible subtopologies with $Vdc \in [V_{ab}, V_{bc}, V_{ca}, V_{ba}, V_{cb}, V_{ac}]$. It can be seen that for each allowed switching combination in Fig. 9.2, there is only one allowed switching combination in Table 3.1 of chapter III that results in the same output voltage and input current. The ITF approach enables application of well known VSR-VSI PWM technique for three phase AC to three phase AC MC control.

Here based on the ITF approach, Space Vector Modulation (SVM) is simultaneously employed for both VSR and VSI part of the MC. The procedure for VSI SVM and VSR SVM are reviewed and their LF transfer functions are derived. The steps for HF synthesis of the simultaneous output voltage and input current SVM are derived and the representation of the modulation process in the complex plane is given.

**9.3.1 VOLTAGE SOURCE INVERTER OUTPUT VOLTAGE SVM:** Consider the voltage source inverter part of Fig. 9.2, supplied by a DC voltage source $v_{pn} = V_{dc}$. The VSI can assume six non-zero and two zero output voltage values. The resulting output line voltage space vector is defined below:

$$v_{ol} = \frac{2}{3} * (v_{ab} + v_{bc}e^{+j120} + v_{ca}e^{-j120}) \quad (9.20)$$

The output line voltage space vector can assume seven discrete Voltage Switching Space Vectors.
Chapter IX: Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

(SSV’s) Vo – V6 shown in Fig. 9.3. The desired output line voltage space vector is given below:

\[ v_{ol} = \sqrt{3} * V_{om} * e^{j(\omega_0 t - \phi_0 + 30)} \]  

(9.21)

The line voltage space vector can be resolved into \( V_\mu, V_\lambda, \) and \( V_0 \) using PWM as shown in Fig. 9.4. In Fig. 9.4, \( V_{out} \) is the sampled value of \( v_{ol} \) at any instant within the switching period \( T_s \). The duty-cycles of the two SSVs are given below:

\[ d_\mu = \frac{T_\mu}{T_s} = m_V * \sin\left(\frac{\pi}{3} - \theta_{inv}\right) \]  

(9.22)

\[ d_A = \frac{T_A}{T_s} = m_V * \sin(\theta_{inv}) \]  

(9.23)

\[ d_{ov} = \frac{T_{ov}}{T_s} = (1 - d_\mu - d_A) \]  

(9.24)

Where \( m_V \) is the voltage modulation index whose range is defined below:

\[ 0 \leq m_V \leq \frac{\sqrt{3} \cdot V_{om}}{V_{dc}} \leq 1 \]  

(9.25)

The sectors of the VSI hexagon in Fig. 9.3 correspond to the six 60 degree segments within a period of the desired three phase output line voltages shown in Fig. 9.5. In Fig. 9.6, the line voltage during the period \( T_\mu \) correspond \( V_6(p,n,p), T_\lambda \) correspond to \( V_1(p,n,n) \) and \( T_0 \) correspond to zero voltage vector in Fig. 9.3. When the switching in Fig. 9.2 correspond to \( V_6(p,n,p) \), the line to line output voltages \( V_{ab}, V_{bc} \) and \( V_{ca} \) are \(+V_{dc}, -V_{dc} \) and zero and when this switching is \( V_1(p,n,n) \) the corresponding line to line output voltages are \(+V_{dc}, \) zero and \(-V_{dc} \) respectively. These values are shown in Fig. 9.6. The local averaged output line voltages are given below:

\[
\begin{bmatrix}
 v_{ab} \\
 v_{bc} \\
 v_{ca}
\end{bmatrix} = \begin{bmatrix}
 d_\mu + d_A \\
 -d_\mu \\
 -d_A
\end{bmatrix} * V_{dc} \]  

(9.26)

Using equation 9.22 to 9.23 in 9.26, the following:

\[
\begin{bmatrix}
 v_{ab} \\
 v_{bc} \\
 v_{ca}
\end{bmatrix} = m_V * \begin{bmatrix}
 \cos(\theta_{inv} - 30^\circ) \\
 -\sin(60^\circ - \theta_{inv}) \\
 -\sin(\theta_{inv})
\end{bmatrix} * V_{dc} \]  

(9.27)

For the first sixty degree segment

\[-30^\circ \leq (\omega_0 t - \phi_0 + 30^\circ) \leq 30^\circ \]

\[ \theta_{inv} = (\omega_0 t - \phi_0 + 30^\circ) + 30^\circ \]  

(9.28)

Using equation 9.28 in equation 9.27, we have the following:

\[
\begin{bmatrix}
 v_{ab} \\
 v_{bc} \\
 v_{ca}
\end{bmatrix} = m_V * \begin{bmatrix}
 \cos(\omega_0 t - \phi_0 + 30^\circ) \\
 \cos(\omega_0 t - \phi_0 + 30^\circ - 120^\circ) \\
 \cos(\omega_0 t - \phi_0 + 30^\circ + 120^\circ)
\end{bmatrix} * V_{dc} = T_{VSI} * V_{dc} \]  

(9.29)

\( T_{VSI} \) in equation 9.29 is the LF transfer matrix of VSI. Using equation 9.25 in equation 9.29, equation 9.12 is obtained. The local averaged input current is defined as follows:
\[ i_{dc} = [T_{VSI}]^T \cdot i_{OL} = \frac{\sqrt{3}}{2} \cdot I_{em} \cdot m_c \cdot \cos(\varphi_L) \quad (9.30) \]

### 9.3.2 VOLTAGE SOURCE RECTIFIER INPUT CURRENT SVM:

Consider the VSR part of Fig.9.2 as a standalone VSR loaded by a DC current generator \( I_{dc} \). The VSR input current hexagon is similar to VSI output voltage hexagon except that the subscripts \( \mu, \lambda \) and \( \text{inv} \) are replaced by \( \alpha, \beta \) and \( \text{rect} \) respectively. The VSR hexagon is shown in Fig. 9.7. The input current space vector is shown in Fig. 9.8. The VSR duty-cycles are defined below:

\[
\begin{align*}
    d_\alpha &= \frac{T_a}{T_s} = m_c \cdot \sin \left( \frac{\pi}{3} - \theta_{\text{rect}} \right) \quad (9.31) \\
    d_\beta &= \frac{T_\beta}{T_s} = m_c \cdot \sin(\theta_{\text{rect}}) \quad (9.32) \\
    d_{\alpha v} &= \frac{T_{\alpha v}}{T_s} = \left( 1 - d_\alpha - d_\beta \right) \quad (9.33)
\end{align*}
\]

Where \( m_c \) is the VSR modulation index whose range is defined below:

\[ 0 \leq m_c \leq \frac{I_{im}}{I_{dc}} \leq 1 \quad (9.34) \]

The local averaged input phase currents in the first sector of VSR hexagon are given below:

\[ \begin{bmatrix} i_\alpha \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} d_\alpha + d_\beta \\ -d_\alpha \\ -d_\beta \end{bmatrix} \cdot I_{dc} \quad (9.35) \]

\[ = m_c \cdot \begin{bmatrix} 
    \cos(\theta_{\text{rect}} - 30^\circ) \\
    -\sin(60^\circ - \theta_{\text{rect}}) \\
    -\sin(\theta_{\text{rect}})
\end{bmatrix} \cdot I_{dc} \quad (9.36) \]

But \( \theta_{\text{rect}} \) in the first sector of input current hexagon can be expressed as follows:

\[ \theta_{\text{rect}} = (\omega_i \cdot t - \varphi_i + 30^\circ) \quad (9.37) \]

\[ -30^\circ \leq (\omega_i \cdot t - \varphi_i) \leq +30^\circ \]

Using equation 9.37 in equation 9.36, the LF transfer matrix \( T_{VSR} \) for the first sector of input current hexagon is defined as follows:

\[ \begin{bmatrix} i_\alpha \\ i_B \\ i_C \end{bmatrix} = m_c \cdot \begin{bmatrix} 
    \cos(\omega_i \cdot t - \varphi_i) \\
    \cos(\omega_i \cdot t - \varphi_i - 120^\circ) \\
    \cos(\omega_i \cdot t - \varphi_i + 120^\circ)
\end{bmatrix} \cdot I_{dc} = T_{VSR} \cdot I_{dc} \quad (9.38) \]
Using equation 9.34 in 9.38, equation 9.16 is obtained. The VSR local averaged output voltage \( v_{pn} = V_{dc} \) in Fig. 9.2 is obtained as follows:

\[
v_{pn} = V_{dc} = \left[ T_{VSR} \right]^T v_{iph} = \frac{3}{2} V_{in} m_c \cos(\varphi_i) \quad (9.39)
\]

### 9.3.3 MATRIX CONVERTER OUTPUT VOLTAGE AND INPUT CURRENT SVM:

The local averaged output voltage of the SVM VSR given in equation 9.39 and that for the input current SVM VSI given in equation 9.30 are constants and hence can be directly interconnected. Also it is seen that the product \([T_{VSR}]^T[T_{VSI}]^T\) from equation 9.38 and 9.29 correspond to \(T_{phL}\) in equation 9.13 where \(m\) corresponds to the product \(m_v^*m_c\). For simplicity \(m_v\) is chosen as one and \(m_v\) is chosen to be the value of \(m\).

There are six sectors each for the VSI and VSR hexagons and hence thirty six operating modes are possible. Consider the instant when the first 60 degree segment for both the output voltage and input current are active. Then using equation 9.27 and 9.36, the following expression for LF transfer matrix is obtained:

\[
T_{phL} = m \begin{bmatrix}
\cos(\theta_{inv} - 30^\circ) \\
-\sin(60^\circ - \theta_{inv}) \\
-\sin(\theta_{inv})
\end{bmatrix}
\begin{bmatrix}
\cos(\theta_{rect} - 30^\circ) \\
-\sin(60^\circ - \theta_{rect}) \\
-\sin(\theta_{rect})
\end{bmatrix}^T
\]

(9.40)

where \(m = m_v^*m_c\). Using equations 9.26 and 9.35 in equation 9.3, we have the following:

\[
\begin{bmatrix}
v_{ab} \\
v_{bc} \\
v_{ca}
\end{bmatrix} = \begin{bmatrix}
d_{\mu} + d_{\lambda} \\
-d_{\mu} \\
-d_{\lambda}
\end{bmatrix} \begin{bmatrix}
d_{\mu} + d_{\lambda} \\
-d_{\mu} \\
-d_{\lambda}
\end{bmatrix}^T \begin{bmatrix}
v_{AO} \\
v_{BO} \\
v_{CO}
\end{bmatrix}
\]

(9.41)

Equation 9.41 simplifies to the following:

\[
\begin{bmatrix}
v_{ab} \\
v_{bc} \\
v_{ca}
\end{bmatrix} = \begin{bmatrix}
(d_{\mu} + d_{\lambda}) \\
-d_{\mu} \\
-d_{\lambda}
\end{bmatrix} \begin{bmatrix}
(d_{\mu} + d_{\lambda}) \\
-d_{\mu} \\
-d_{\lambda}
\end{bmatrix}^T \begin{bmatrix}
v_{AB} \\
v_{AC}
\end{bmatrix}
\]

(9.42)

where

\[
v_{AB} = v_{AO} - v_{BO} \quad (9.43)
\]

\[
v_{AC} = v_{AO} - v_{CO} \quad (9.44)
\]

\[
d_{\mu} = d_{\mu} * d_{\mu} = m * \sin(\frac{\pi}{3} - \theta_{rect}) * \sin(\frac{\pi}{3} - \theta_{inv}) = \frac{T_{\mu}}{T_3} \quad (9.45)
\]

\[
d_{\lambda} = d_{\mu} * d_{\lambda} = m * \sin(\frac{\pi}{3} - \theta_{rect}) * \sin(\theta_{inv}) = \frac{T_{\lambda}}{T_3} \quad (9.46)
\]

\[
d_{\beta_\mu} = d_{\beta} * d_{\mu} = m * \sin(\theta_{rect}) * \sin(\frac{\pi}{3} - \theta_{inv}) = \frac{T_{\beta_\mu}}{T_3} \quad (9.47)
\]

\[
d_{\beta_\lambda} = d_{\beta} * d_{\lambda} = m * \sin(\theta_{rect}) * \sin(\theta_{inv}) = \frac{T_{\beta_\lambda}}{T_3} \quad (9.48)
\]

The derivation equation 9.42 is given in A9.4 Appendix. From equation 9.42, it is clear that the standard output voltage and input current SVM can be implemented in two VSI sub topologies. When the VSI SVM sub topology corresponds to \(v_{p_m} = V_{dc} = v_{AB}\), then the two duty-cycles of the two adjacent voltage vectors are \(d_{\mu}\) and \(d_{\lambda}\). When the VSI SVM sub topology corresponds to \(v_{p_m} =
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\[ V_{dc} = vac, \] then the two duty-cycles of the adjacent output voltage vectors are \( d_{\beta\mu} \) and \( d_{\beta\lambda} \). During the remaining part of the switching period, the output line voltage is zero and the duty-cycle corresponds to the following:

\[ d_0 = 1 - d_{a\mu} - d_{a\lambda} - d_{\beta\mu} - d_{\beta\lambda} = \frac{T_0}{T_S} \]  

(9.49)

Finally it is the selection of the zero switching state vector from Group III of Table 3.1 of Chapter III and the order of arrangement of the five switching state vectors (SSVs). The pattern followed for arrangement of the state switching vectors is: \( d_{a\mu} \rightarrow d_{\beta\mu} \rightarrow d_{\beta\lambda} \rightarrow d_{a\lambda} \rightarrow d_0 \). The optimum zero switching state vector is used for each of the thirty six switching combinations.

The thirty six switching combinations are tabulated as shown in Table 9.1 to Table 9.6, each with six sub tables. In Table 9.1 to 9.6, \( S_i \) and \( S_v \) corresponds to the input current and output voltage hexagon sector number. Also in Table 9.1 to 9.6, serial number 1 to 5 corresponds to the timing \( T_{a\mu} \rightarrow T_{\beta\mu} \rightarrow T_{\beta\lambda} \rightarrow T_{a\lambda} \rightarrow T_0 \). Also it is seen from Table 9.1 to 9.6 that with reference to VSI output voltage switching combination, there are eighteen pair of identical sub tables. If output voltage vol and input current iph are both in the first sector of respective hexagon, then referring Fig. 9.3, 9.4, 9.7 and 9.8, the SSV pair using the above duty-cycle sequence will be I6-V6, I1-V6, I1-V1, I6-V1 and Io-Vo. Similar procedure is used to complete all the sector combinations of the output voltage and input current. Corresponding to I6-V6 SSV pair, from Fig. 9.7 and 9.8, \( p=A \) and \( n=B \). From Fig. 9.3 and 9.4, \( p=a \), \( n=b \) and \( p=c \). As \( p \) and \( n \) correspond to input phase A and B, it follows that the output voltage VSI switching combination is A, B, A which has an ON duration \( d_{a\mu} * T_S \). Table 9.1 to 9.6 shows the ON duration for all the thirty six switching combinations. The method of completing Table 9.1 to 9.6 is shown in A9.5 Appendix.

9.4 MODEL OF INDIRECT SPACE VECTOR MODULATED THREE PHASE MATRIX CONVERTER: The model of the three phase AC to three phase AC Indirect SVM MC was developed in SIMULINK [51]. This model is shown in Fig. 9.9. The individual subsystems are explained below:

The power circuit of the model is shown in in Fig. 9.9. This is developed using the SimPowerSystems blockset in SIMULINK [51]. This mainly consists of three phase AC source, bidirectional switch matrix, output filter and R-L load. The arrangement of the bidirectional switch matrix using IGBTs is shown in Fig. 3.2 of chapter III.

The modulation algorithm is developed in several sub units using Embedded MATLAB Function, MATLAB Function, Math Function, Logical and Bit Operator and using Sources block set in SIMULINK [51]. The various sub units are explained below:

9.4.1 DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR: This is developed using Embedded Matlab Function block in SIMULINK, as shown in Fig. 9.9. With peak
### Chapter IX: Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

#### Table 9.1

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>SSV Pair</th>
<th>Switching Combinations p a b c</th>
<th>Sl.No</th>
<th>SSV Pair</th>
<th>Switching Combinations p a b c</th>
<th>Sl.No</th>
<th>SSV Pair</th>
<th>Switching Combinations p a b c</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>I6-V6</td>
<td>A B A B A</td>
<td>1</td>
<td>I6-V1</td>
<td>A B A B A</td>
<td>1</td>
<td>I6-V2</td>
<td>A B A B A</td>
</tr>
<tr>
<td>2</td>
<td>I1-V6</td>
<td>A C A C A</td>
<td>2</td>
<td>I1-V1</td>
<td>A C A C A</td>
<td>2</td>
<td>I1-V2</td>
<td>A C A C A</td>
</tr>
<tr>
<td>3</td>
<td>I1-V1</td>
<td>A C A C C</td>
<td>3</td>
<td>I1-V2</td>
<td>A C A C C</td>
<td>3</td>
<td>I1-V3</td>
<td>A C A C C</td>
</tr>
<tr>
<td>5</td>
<td>Io-V6</td>
<td>A A A A A</td>
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<td>Io-V1</td>
<td>A A A A A</td>
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#### Table 9.2 (Continued)

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<th>Switching Combinations p a b c</th>
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<th>SSV Pair</th>
<th>Switching Combinations p a b c</th>
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<td>I6-V5</td>
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<td>A C A C A</td>
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<td>I1-V5</td>
<td>A C A C A</td>
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<td>I1-V4</td>
<td>A C A C C</td>
<td>3</td>
<td>I1-V5</td>
<td>A C A C C</td>
<td>3</td>
<td>I1-V6</td>
<td>A C A C C</td>
</tr>
<tr>
<td>5</td>
<td>Io-V6</td>
<td>A A A A A</td>
<td>5</td>
<td>Io-V1</td>
<td>A A A A A</td>
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<td>Io-V2</td>
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#### Table 9.3

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<th>Sl.No</th>
<th>SSV Pair</th>
<th>Switching Combinations p a b c</th>
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<th>SSV Pair</th>
<th>Switching Combinations p a b c</th>
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<tbody>
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<td>I3-V2</td>
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<td>I3-V3</td>
<td>B A A A B</td>
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<td>Io-V1</td>
<td>A A A A A</td>
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#### Table 9.4

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<th>Switching Combinations p a b c</th>
<th>Sl.No</th>
<th>SSV Pair</th>
<th>Switching Combinations p a b c</th>
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<th>SSV Pair</th>
<th>Switching Combinations p a b c</th>
</tr>
</thead>
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<td>I4-V6</td>
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<td>C A A C C</td>
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<td>I4-V2</td>
<td>C A A C C</td>
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<td>I5-V6</td>
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<td>I5-V1</td>
<td>C B C C C</td>
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<td>I5-V2</td>
<td>C B C C C</td>
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<td>I5-V1</td>
<td>C B C C C</td>
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<td>C B C C C</td>
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<td>I5-V3</td>
<td>C B C C C</td>
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</table>
input current angle, \( i_{\text{in\_angle}} \). The value of reference frame frequency can be calculated using MATLAB function and \( \theta_{\text{inv}} \) in Program segment I in section 8.3.1 of chapter VIII. These two values of the angles are used to find the line to neutral input voltage, desired peak output phase voltage, input frequency, output frequency, time, angular frequency of reference frame \( \omega_c \) as input parameters, the three phase output voltage can be resolved into \( dq \)-axis component voltages [42] and the absolute value of the angle of the output phase voltage, \( \text{vout\_angle} \) can be calculated using the function \( \text{atan2}\left(v_{oq},v_{od}\right) \). Using input voltage and input phase displacement angle, a similar procedure is used to calculate the absolute value of the input current angle, \( i_{\text{in\_angle}} \). The value of reference frame frequency \( \omega_c \) is zero. This is illustrated in Program segment I in section 8.3.1 of chapter VIII. These two values of the angles are used to calculate the output voltage sector SV, input current sector SI using MATLAB function and \( \theta_{\text{inv}} \) in Table 9.4.

### Table 9.4 (Continued)

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<td>I4-V3</td>
<td>CA A CA A</td>
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<td>2</td>
<td>I5-V4</td>
<td>CB B CB C</td>
<td>2</td>
<td>I5-V3</td>
<td>CB B CB C</td>
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<td>I5-V5</td>
<td>CB B CB C</td>
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<td>I5-V4</td>
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</tr>
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### Table 9.5

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<th>Switching Combinations p n a b c</th>
<th>Sl.No</th>
<th>SSV</th>
<th>Switching Combinations p n a b c</th>
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<td>I2-V1</td>
<td>BC B BC C</td>
<td>1</td>
<td>I2-V2</td>
<td>BC B BC C</td>
</tr>
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<td>I3-V6</td>
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<td>I3-V3</td>
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<td>AB A AB A</td>
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### Table 9.6 (Continued)

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<th>Switching Combinations p n a b c</th>
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<th>SSV</th>
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</thead>
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<td>I5-V1</td>
<td>CB C CB C</td>
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<td>I5-V2</td>
<td>CB C CB C</td>
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<td>I6-V1</td>
<td>AB A AB A</td>
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<td>I6-V2</td>
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<td>I5-V6</td>
<td>CB C CB C</td>
<td>4</td>
<td>I5-V2</td>
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<td>I5-V3</td>
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### Table 9.6 (Continued)

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<th>SSV</th>
<th>Switching Combinations p n a b c</th>
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<td>I5-V1</td>
<td>CB C CB C</td>
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<td>I5-V2</td>
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<td>I6-V1</td>
<td>AB A AB A</td>
<td>2</td>
<td>I6-V2</td>
<td>AB A AB A</td>
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<td>AB A AB A</td>
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<td>I6-V3</td>
<td>AB A AB A</td>
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<tr>
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<td>I5-V6</td>
<td>CB C CB C</td>
<td>4</td>
<td>I5-V2</td>
<td>CB C CB C</td>
<td>4</td>
<td>I5-V3</td>
<td>CB C CB C</td>
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<td>I5-V2</td>
<td>CB C CB C</td>
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<td>I5-V3</td>
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</tr>
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### Table 9.1 to 9.6: PH3 AC to PH3 AC ISVM MC – Switching Sequence Table

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FIG. 9.9: THREE PHASE AC TO THREE PHASE AC INDIRECT SPACE VECTOR MODULATED MATRIX CONVERTER
and theta_rect using the REM and SUBTRACT modules. Program Segment II illustrates part of the MATLAB code for duty cycle sequencing and sector switch function generation. Duty-cycle dni, dni, dIII, dIV and d0 are calculated using equations 9.45, 9.47, 9.48, 9.46 and 9.49 respectively, assuming unity input power factor. This is used to calculate the timing A, B, C, D and E by comparison of the cumulative sector timing with a triangle carrier as shown in Program Segment II. This triangle carrier has a period Ts, peak value Ts/2 Volts and minimum value zero, as shown in Fig. 8.4 of chapter VIII. The PWM signal timing is shown in Fig. 9.10. Cumulative sector timing is obtained by appropriately adding the value of duty-ratios and multiplying by Ts/2, as shown in Program Segment II. Sector switch functions ssf1 to ssf18 are determined using if-then-else statement. For example sector switch function ssf1 is HIGH only when sv = si = 1 or sv = si = 4 and is LOW otherwise.

%%PROGRAM SEGMENT II
%%Narayanaswamy, P.R. Iyer
Function [m,dI,dII,dIII,dIV,d0,A,B,C,D,E,ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12,ssf13,ssf14,ssf15, ssf16,ssf17, ssf18] = fcn(vom,fo,t,vim,fi,wc,phi_i,theta_inv,theta_rect,sv,si,Ts,vtri)
m = vo/vim;
dI = (m*sin(pi/(3)-theta_rect)*sin(pi/(3)-theta_inv));%%d_alfa_meu
dII = (m*sin(theta_rect)*sin(pi/(3)-theta_inv));%%d_beta_meu
dIII = (m*sin(theta_rect)*sin(theta_inv));%%d_beta_lamda
dIV = (m*sin(pi/(3)-theta_rect)*sin(theta_inv));%%d_alfa_lamda
d0 = (1 - dI - dII - dIII - dIV);
if ( vtri <= dI*Ts/(2))
    A = 1;    else
    A = 0;
end
if ( vtri <= (dII + dI)*Ts/(2))
    B = 1;    else
    B = 0;
end
if ( vtri <= (dIII + dII + dI)*Ts/(2))
    C = 1;   else
    C = 0;
end
if ( vtri <= (dIV + dIII + dII + dI)*Ts/(2))
    D = 1;  else
    D = 0;
end
if ( vtri <= (dIV + dIII + dII + dI + d0)*Ts/(2))
    E = 1;  else
    E = 0;
end
if (sv == 1 && si == 1 || sv == 4 && si == 4)
    %%sector 1. sector switch function ssf1.
    ssf1 = 1;
else
    ssf1 = 0;
end
if ( sv == 2 && si == 1 || sv == 5 && si == 4 )
    %%sector 2. sector switch function ssf2.
    ssf2 = 1;
else
    ssf2 = 0;
end
%%Similar statement for ssf3 to ssf18.
if ( sv == 6 && si == 3 || sv == 3 && si == 6 )
    %%sector 18. sector switch function ssf18.
    ssf18 = 1;
else
    ssf18 = 0;
end
9.4.2 OUTPUT VOLTAGE AND INPUT CURRENT SECTOR CALCULATOR: This is developed using MATLAB Function, a mux and a demux as shown in Fig. 8.5 of chapter VIII. The input to the mux are \( v_{\text{out\_angle}} \) and \( i_{\text{in\_angle}} \). The output from the demux are SV and SI. The source code to determine SV and SI is shown in Program Segment III in section 8.3.1 of chapter VIII.

9.4.3 OUTPUT VOLTAGE AND INPUT CURRENT REFERENCE ANGLE CALCULATOR: This is shown in Fig. 9.11. This uses two REM function blocks and SUBTRACT modules. The first REM block has the inputs \( v_{\text{out\_angle}} \) and \( \pi/(3) \). The output of the first REM block gives \( \theta_{\text{inv}} \) defined in Fig. 9.4. The second REM block has the inputs \( i_{\text{in\_angle}} \) and \( \pi/(3) \). The output of the second REM block is subtracted from input p.f. angle \( \phi_i \) to obtain \( \theta_{\text{rect}} \) defined in Fig. 9.8.

9.4.4 GATE PULSE TIMING CALCULATOR: This is shown in Fig. 9.12. The inputs in1 to in5 are A, B, C, D and E respectively. The individual gate pulse timing, \( t_a \), \( t_b \), \( t_c \), \( t_d \) and \( t_0 \) are respectively \( d_1^*Ts/(2) \), \( d_2^*Ts/(2) \), \( d_3^*Ts/(2) \), \( d_4^*Ts/(2) \) and \( d_0^*Ts/(2) \) where each duty-cycle \( d_1 \), \( d_2 \), \( d_3 \), \( d_4 \) and \( d_0 \) respectively correspond to \( d_{\alpha} \), \( d_{\beta} \), \( d_{\beta_\lambda} \), \( d_{\alpha_\lambda} \) and \( d_0 \) as defined in equations 9.45, 9.47, 9.48, 9.46 and 9.49. This individual gate pulse duration is obtained as shown in equation 9.50 below:

\[
\begin{align*}
  t_a &= (A \& A) \\
  t_b &= (\neg A \& B)
\end{align*}
\]
Chapter IX: Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

\[ t_c = (\sim B \& C) \]
\[ t_d = (\sim C \& D) \]
\[ t_0 = (\sim D \& E) \ldots \quad (9.50) \]

In equation 9.50, symbols (\&) represents logical AND and (\sim) represents NOT operation respectively.

To easily generate the MC gate pulse, the timing pulse in equation 9.50 are given to OR gates to obtain the following additional timing pulse:

\[ t_{ab} = (t_a||t_b) \]
\[ t_{bed} = (t_1||t_c||t_d) \]
\[ t_{ad} = (t_a||t_d) \]
\[ t_{be} = (t_b||t_c) \]
\[ t_{abo} = (t_a||t_b||t_0) \]
\[ t_{cd0} = (t_c||t_d||t_0) \]
\[ t_{abcd0} = (t_a||t_b||t_c||t_d||t_0) \ldots \ldots (9.51) \]

In equation 9.51, symbol (\|) represents logical OR operation.

The complete gate timing for the nine bidirectional switches using Indirect SVM algorithm is given in Tables 9.7 and 9.8 below:

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>SI, SV</th>
<th>SSF_X HIGH</th>
<th>BIDIRECTIONAL SWITCH GATE PULSE PATTERN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I, I or IV, IV</td>
<td>ssf1</td>
<td>ABA</td>
</tr>
<tr>
<td>2</td>
<td>I, II or IV, V</td>
<td>ssf2</td>
<td>ABB</td>
</tr>
<tr>
<td>3</td>
<td>I, III or IV, VI</td>
<td>ssf3</td>
<td>AAB</td>
</tr>
<tr>
<td>4</td>
<td>I, IV or IV, I</td>
<td>ssf4</td>
<td>BAB</td>
</tr>
<tr>
<td>5</td>
<td>IV or IV, II</td>
<td>ssf5</td>
<td>BAA</td>
</tr>
<tr>
<td>6</td>
<td>LVI or IV, III</td>
<td>ssf6</td>
<td>BBA</td>
</tr>
<tr>
<td>7</td>
<td>II, I or I, IV</td>
<td>ssf7</td>
<td>ACA</td>
</tr>
<tr>
<td>8</td>
<td>II, II or V, V</td>
<td>ssf8</td>
<td>ACC</td>
</tr>
<tr>
<td>9</td>
<td>II, III or V, VI</td>
<td>ssf9</td>
<td>AAC</td>
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<td>ssf10</td>
<td>CAC</td>
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<td>II, V or V, II</td>
<td>ssf11</td>
<td>CAA</td>
</tr>
<tr>
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<td>II, VI or V, III</td>
<td>ssf12</td>
<td>CCA</td>
</tr>
<tr>
<td>13</td>
<td>III, I or VI, IV</td>
<td>ssf13</td>
<td>BCB</td>
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<td>III, VI or VI, III</td>
<td>ssf18</td>
<td>CCB</td>
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</table>

**TABLE 9.7: Switching Pattern**

**9.4.5 GATE PULSE GENERATOR:** The gate pulse generator for the MC is developed using Embedded MATLAB as shown in Fig. 9.9. The sector switch functions ssf1 to ssf18, gate pulse timing calculator outputs defined in equations 9.50 and 9.51 form the input modules and the outputs are the gate pulses for the nine bidirectional switches of the MC. In Table 9.8, the gate timing for the nine bidirectional switches are shown. The gate timing for switch SAA can be combined by logically ANDing the respective value with sector switch function ssf_x and ORing the value for each sector. Thus the gate timing pulse for switch SAA can be expressed as in equation 9.52 below:

\[ SAA = ssf1\&(tabcd0)||ssf2\&(tabcd0)||\ldots||ssf18\&(tb) \ldots (9.52) \]
Program segment IV gives the method of generating the gate timing pulses for the nine bidirectional switches using the calculated sector timings given in Table 9.8.

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>SL. SV</th>
<th>SSP_X HIGH</th>
<th>SAa</th>
<th>SBa</th>
<th>SCa</th>
<th>SAb</th>
<th>SBB</th>
<th>SCb</th>
<th>SAc</th>
<th>SBe</th>
<th>SCc</th>
</tr>
</thead>
<tbody>
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<td>I, I or I, IV</td>
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<td>tabcd0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ta</td>
<td>tbc</td>
<td>tab0</td>
<td>td</td>
<td>tc</td>
</tr>
<tr>
<td>2</td>
<td>I, II or I, V</td>
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<td>tabcd0</td>
<td>0</td>
<td>0</td>
<td>ta</td>
<td>ta</td>
<td>tbc</td>
<td>tab0</td>
<td>td</td>
<td>tbc</td>
</tr>
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<td>I, III or I, VI</td>
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<td>tab0</td>
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<td>tb</td>
<td>tbc</td>
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<td>tab0</td>
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<td>tab0</td>
<td>td</td>
<td>tbc</td>
<td></td>
<td></td>
</tr>
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<td>tcb</td>
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<td></td>
<td></td>
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<td>tab0</td>
<td>td</td>
<td>tcb</td>
<td>tab0</td>
<td>td</td>
<td>tbc</td>
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<td>tab0</td>
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<td>tbc</td>
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<td>tab0</td>
<td>td</td>
<td>tbc</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>16</td>
<td>III, IV or VI, I</td>
<td>ssf16</td>
<td>tab0</td>
<td>td</td>
<td>tcb</td>
<td>tab0</td>
<td>td</td>
<td>tbc</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>17</td>
<td>III, V or VI, II</td>
<td>ssf17</td>
<td>tab0</td>
<td>td</td>
<td>tcb</td>
<td>tab0</td>
<td>td</td>
<td>tbc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>III, VI or VI, III</td>
<td>ssf18</td>
<td>tab0</td>
<td>td</td>
<td>tcb</td>
<td>tab0</td>
<td>td</td>
<td>tbc</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PROGRAM SEGMENT IV

function [SAa,SBa,SCa,SAb,SBb,SCb,SAc,SBe,SCc] = fcn(ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12, ssf13,ssf14,ssf15,ssf16,ssf17,ss18,ta,tc,t0,tab0,tad,tbcd,tabcd0)

9.5 SIMULATION RESULTS: The simulation of the Three Phase ISVM MC was carried out in SIMULINK [51]. The parameters used for simulation are shown in Table 9.9. The ode15S(Stiff/NDF) solver was used. Simulation was carried out for two different output frequencies with all other parameters constant. The simulation results for the harmonic spectrum of line to neutral...
Chapter IX: Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter
Chapter IX: Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter
ral output voltage, input current, load current and line to line output voltage for 50 Hz output frequency are shown in Fig. 9.13(A) to (D) and their respective oscilloscope waveforms are shown in Fig. 9.14(A) to (D) above. The same results in the above order for 20 Hz output frequency are shown in Fig. 9.15(A) to (D) and Fig. 9.16(A) to (D) above respectively. The simulation results are tabulated in Table 9.10 below:

![Table 9.10: Simulation Results](image)

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>1) 2)</td>
<td>50 – 50 50 – 20</td>
<td>1.2558</td>
<td>2.1108</td>
<td>2.6486</td>
<td>0.4921</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.198</td>
<td>1.6563</td>
<td>1.6865</td>
<td>0.2733</td>
</tr>
</tbody>
</table>

9.6 DISCUSSION OF RESULTS: Indirect space vector modulation for three phase MC assumes the three phase MC to be considered equivalent to a three phase rectifier inverter converter and the SVM technique to be applied separately to the three phase rectifier and inverter and the combined duty-cycle timing for the MC is the product of the corresponding individual duty-cycle timing for the three phase rectifier and three phase inverter. It is also seen from Table 9.10 that as the output frequency is reduced, the THD of the line to neutral output voltage, line to line output voltages, input current and load current are reduced. The indirect SVM has eight commutations per carrier switching period. Also it is seen from the simulation results that the harmonic components of line to neutral output voltage, line to line output voltage, input current and load current tend to concentrate at integral multiples of carrier switching frequency.

9.7 CONCLUSIONS: This chapter presents an easy method of modeling a three phase Indirect SVM MC using Embedded MATLAB function, MATLAB function, Math blockset, Logic and Bit Operations toolbox and Sources block set. The input current, load current, Line to Neutral and Line to Line output voltage harmonic distortions are reduced with reduction in the output frequency. The three phase AC to three phase AC output voltage – input current SVM algorithm is systematically reviewed. A simple geometric presentation of the three phase AC to three phase AC MC SVM procedure is given. The indirect SVM algorithm uses eight commutations per carrier switching period. Harmonic components of line to neutral output voltage, line to line output voltage, input current and load current tend to concentrate at integral multiples of switching frequency. The model can be easily adapted for hardware implementation.

A9.1 APPENDIX: The matrix $T_{phL}$ in equation 9.13 can be expressed as follows:
Chapter IX: Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

\[ T_{phl} = m \begin{bmatrix} \cos(\omega_L t - \varphi_a + 30^\circ) \\ \cos(\omega_L t - \varphi_a + 30^\circ - 120^\circ) \\ \cos(\omega_L t - \varphi_a + 30^\circ + 120^\circ) \end{bmatrix} \times \begin{bmatrix} \cos(\omega_L t - \varphi_1) & \cos(\omega_L t - \varphi_1 - 120^\circ) & \cos(\omega_L t - \varphi_1 + 120^\circ) \end{bmatrix} \]  
\hspace{1cm} (A9.1.1)

Let \((\omega_L t - \varphi_a) = \alpha\) and \((\omega_L t - \varphi_1) = \beta\)  
\hspace{1cm} (A9.1.2)

Simplifying using equations A9.1.1 and A9.1.2, we have the following equation:

\[ T_{phl} = \begin{bmatrix} m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta) & m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta - 120^\circ) & m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta + 120^\circ) \\ m \cdot \cos(\alpha - 90^\circ) \cdot \cos(\beta) & m \cdot \cos(\alpha - 90^\circ) \cdot \cos(\beta - 120^\circ) & m \cdot \cos(\alpha - 90^\circ) \cdot \cos(\beta + 120^\circ) \\ m \cdot \cos(\alpha + 150^\circ) \cdot \cos(\beta) & m \cdot \cos(\alpha + 150^\circ) \cdot \cos(\beta - 120^\circ) & m \cdot \cos(\alpha + 150^\circ) \cdot \cos(\beta + 120^\circ) \end{bmatrix} \]  
\hspace{1cm} (A9.1.3)

Using equations 9.3, 9.11, 9.11 and A9.1.3, we have the following:

\[ v_{ab} = \sqrt{3} \cdot V_{in} \cdot \cos(\alpha + 30^\circ) = V_{in} \cdot m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta - 120^\circ) + V_{in} \cdot m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta + 120^\circ) \]  
\hspace{1cm} (A9.1.4)

i.e., \(v_{ab} = \sqrt{3} \cdot V_{in} \cdot \cos(\alpha + 30^\circ) = V_{in} \cdot m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta - 120^\circ) + \cos(\beta + 120^\circ) \cdot \cos(\beta - 120^\circ) + \cos(\beta + 120^\circ)\)  
\hspace{1cm} (A9.1.5)

Simplifying equation A9.1.5, we have the following:

\[ \sqrt{3} \cdot V_{in} \cdot \cos(\alpha + 30^\circ) = \frac{1}{2} \cdot V_{in} \cdot m \cdot \cos(\phi) \]  
\hspace{1cm} (A9.1.6)

\[ V_{in} = \frac{\sqrt{3}}{2} \cdot V_{in} \cdot m \cdot \cos(\phi) \]  
\hspace{1cm} (A9.1.7)

A9.2 APPENDIX: In equation 9.15, let \((\omega_L t - \varphi_1 - \varphi_a) = \gamma\)  
\hspace{1cm} (A9.2.1)

\[ i_{al} = \frac{l_{im}}{\sqrt{3}} \cdot \begin{bmatrix} \cos(\gamma + 30^\circ) \\ \cos(\gamma - 90^\circ) \\ \cos(\gamma + 150^\circ) \end{bmatrix} \]  
\hspace{1cm} (A9.2.2)

\[ T_{phl}^T = \begin{bmatrix} m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta) & m \cdot \cos(\alpha - 90^\circ) \cdot \cos(\beta) & m \cdot \cos(\alpha + 150^\circ) \cdot \cos(\beta) \\ m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta - 120^\circ) & m \cdot \cos(\alpha - 90^\circ) \cdot \cos(\beta - 120^\circ) & m \cdot \cos(\alpha + 150^\circ) \cdot \cos(\beta - 120^\circ) \\ m \cdot \cos(\alpha + 30^\circ) \cdot \cos(\beta + 120^\circ) & m \cdot \cos(\alpha - 90^\circ) \cdot \cos(\beta + 120^\circ) & m \cdot \cos(\alpha + 150^\circ) \cdot \cos(\beta + 120^\circ) \end{bmatrix} \]  
\hspace{1cm} (A9.2.3)

Using equation 9.4 and A9.2.3, we have the following:

\[ \begin{bmatrix} i_{a} \\ i_{b} \end{bmatrix} = T_{phl}^T \cdot \begin{bmatrix} \frac{l_{im}}{\sqrt{3}} \cdot \cos(\gamma + 30^\circ) \\ \frac{l_{im}}{\sqrt{3}} \cdot \cos(\gamma - 90^\circ) \\ \frac{l_{im}}{\sqrt{3}} \cdot \cos(\gamma + 150^\circ) \end{bmatrix} \]  
\hspace{1cm} (A9.2.4)

Simplifying for \(i_a\), we have the following:

\[ i_a = m \cdot \cos(\beta) \cdot \frac{l_{im}}{\sqrt{3}} \cdot [[\cos(\alpha + 30^\circ) \cdot \cos(\gamma + 30^\circ)] + \cos(\alpha - 90^\circ) \cdot \cos(\gamma - 90^\circ)] + \cos(\alpha + 150^\circ) \cdot \cos(\gamma + 150^\circ)] \]  
\hspace{1cm} (A9.2.5)

i.e., \(i_a = m \cdot \cos(\beta) \cdot \frac{l_{im}}{\sqrt{3}} \cdot \left[ \frac{1}{2} \cdot \cos(\alpha + \gamma + 60^\circ) + \frac{1}{2} \cdot \cos(\alpha - \gamma) + \frac{1}{2} \cdot \cos(\alpha + \gamma - 180^\circ) + \frac{1}{2} \cdot \cos(\alpha - \gamma) + \frac{1}{2} \cdot \cos(\alpha + \gamma + 120^\circ) + \frac{1}{2} \cdot \cos(\alpha - \gamma - 120^\circ) \right] \)  
\hspace{1cm} (A9.2.6)

simplifying, \(i_a = \frac{l_{im}}{\sqrt{3}} \cdot \frac{1}{2} \cdot m \cdot \cos(\beta) \cdot \cos(\alpha - \gamma) \)  
\hspace{1cm} (A9.2.7)

Substituting for \(\alpha, \beta\) and \(\gamma\) and further simplifying, we have the following:

\[ l_{im} = \frac{\sqrt{7}}{2} \cdot l_{im} \cdot m \cdot \cos(\phi) \]  
\hspace{1cm} (A9.2.8)

A9.3 APPENDIX: From equation 9.13, \([T_{VSR}(\omega_L)]^T\) is given in equation A9.3.1 below:

\[ [T_{VSR}(\omega_L)]^T = \begin{bmatrix} \cos(\omega_L t - \varphi_1) & \cos(\omega_L t - \varphi_1 - 120^\circ) & \cos(\omega_L t - \varphi_1 + 120^\circ) \end{bmatrix} \]  
\hspace{1cm} (A9.3.1)

Multiplying equation A9.3.1 with equation 9.11, we have the following:
\[ [T_{VSR}(\omega_i)]^T \cdot v_{oph} \]

\[ = V_{lm} \]

\[ \cdot [\cos(\omega_i t) \]

\[ \cdot \cos(\omega_i t - \varphi_i) + \cos(\omega_i t - 120^\circ) \]

\[ \cdot \cos(\omega_i t - \varphi_i - 120^\circ) + \cos(\omega_i t + 120^\circ) * \cos(\omega_i t - \varphi_i + 120^\circ)] \]

\[ = \frac{V_{lm}}{2} \cdot [\cos(2\omega_i t - \varphi_i) + \cos(2\omega_i t - 240^\circ - \varphi_i) + \cos(2\omega_i t + 240^\circ - \varphi_i) + 3 \cdot \cos(\varphi_i)] \quad A9.3.2 \]

\[ = \frac{3}{2} \cdot V_{lm} \cdot \cos(\varphi_i) \quad A9.3.3 \]

**A9.4 APPENDIX:** Equation 9.41 can be rewritten as follows:

\[
\begin{bmatrix}
v_{ab} \\
v_{bc} \\
v_{ca}
\end{bmatrix} = \begin{bmatrix}
(d_\mu + d_x) \cdot (d_\mu + d_y) & (d_\mu + d_x) \cdot (-d_y) & (-d_y) \cdot (d_\mu + d_y) \\
(-d_y) \cdot (d_\mu + d_y) & d_\mu \cdot d_y & d_y \cdot d_\mu \\
(-d_x) \cdot (d_\mu + d_y) & d_x \cdot d_y & d_y \cdot d_x
\end{bmatrix} \cdot \begin{bmatrix}
v_{a0} \\
v_{b0} \\
v_{c0}
\end{bmatrix} \quad (A9.4.1)
\]

Simplifying, we have the following:

\[ v_{ab} = (d_\mu + d_x) \cdot [d_\mu + v_{ab} + d_\beta \cdot v_{ac}] \quad (A9.4.2) \]

\[ v_{bc} = (-d_y) \cdot [d_\mu + v_{ab} + d_\beta \cdot v_{ac}] \quad (A9.4.3) \]

\[ v_{ca} = (-d_y) \cdot [d_\mu + v_{ab} + d_\beta \cdot v_{ac}] \quad (A9.4.4) \]

Let

\[ d_\mu \cdot d_\mu = d_{\mu \mu} \]

\[ d_x \cdot d_\mu = d_{x \mu} \]

\[ d_\mu \cdot d_\beta = d_{\mu \beta} \]

\[ d_\beta \cdot d_\beta = d_{\beta \beta} \quad (A9.4.6) \]

Using equation A9.4.6 in A9.4.5, we have the following:

\[
\begin{bmatrix}
v_{ab} \\
v_{bc} \\
v_{ca}
\end{bmatrix} = \begin{bmatrix}
(d_\mu + d_x) \cdot (d_\mu + d_x) \\
(d_\mu + d_x) \cdot (-d_\beta) \\
(-d_\beta) \cdot (d_\mu + d_x)
\end{bmatrix} \cdot \begin{bmatrix}
v_{a0} \\
v_{b0} \\
v_{c0}
\end{bmatrix} \quad (A9.4.7)
\]

Equation A9.4.7 corresponds to equation 9.42.

**A9.5 APPENDIX:** Table 9.1 to 9.6 are derived using the phasor diagram of the output voltage and input current for each sector as given in Fig. A9.5.1(A) to A9.5.1(F) for the former and Fig. A9.5.2(A) to A9.5.2(F) for the latter. Their sector numbers are marked in the diagram. For example let the reference output voltage and input current vectors are in sector II and sector IV respectively, then SV = II and SI = IV and hence Fig. A9.5.1(B) and Fig. A9.5.2(D) must be considered. The switching time order sequence is \( T_{up}, T_{up}, T_{up}, T_{up}, T_{up} \) and \( T_{up} \) respectively. Referring to Fig. A9.5.1(B) and Fig. A9.5.2(D), during \( T_{up} \), time interval, corresponding to \( I_{p-v_\mu} \) vector 13-V1, input phase B correspond to positive terminal p of rectifier and input phase A correspond to negative terminal n of rectifier. Three phase output voltage vector V1 is p,n,n and therefore output phase a correspond to input phase B and the output phase b and c correspond to input phase A and A or a,b,c is connected to B,A,A respectively. Similarly during time interval \( T_{up} \), for \( I_{p-v_\mu} \) vector corresponding to 14-V1, input phase C and A correspond to p and n terminal of rectifier, V1 correspond to p,n,n and the output phase a, b and c are connected to C,A,A
Chapter IX: Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

respectively. During $T_{\beta\lambda}$ and $T_{\alpha\lambda}$ time interval, the vectors are $I_4-V_2$ and $I_3-V_2$ respectively. During time interval $T_{\beta\lambda}$, input phase C and A are connected to p and n terminal of rectifier, V2 correspond to p,p,n and the output phases a,b,c are connected to C,C,A respectively. In the same way during $T_{\alpha\lambda}$ time interval, input phase B and A are connected to p and n terminal of rectifier, and as output voltage V2 correspond to p,p,n, output phases a,b,c are connected to B,B,A respectively. During time interval $T_{O}$, as the current vector SI is in IVth quadrant, the output phase a,b,c are connected to A,A,A respectively, as A is the common terminal to I3 and I4 input current vector. The Table 9.1 to 9.6 is filled in this way.

\begin{center}
\begin{tikzpicture}
\node (V1) at (0,0) {$V_{\lambda}$};
\node (V2) at (-2,-1) {$V_{\mu}$};
\node (V3) at (2,-1) {$V_{\mu}$};
\node (V4) at (-4,-2) {$V_1(p,n,n)$};
\node (V5) at (-2,-2) {$V_2(p,p,n)$};
\node (V6) at (2,-2) {$V_3(n,p,n)$};
\node (V7) at (-6,-3) {$V_4(n,p,p)$};
\node (V8) at (-4,-3) {$V_5(n,n,p)$};
\node (V9) at (2,-3) {$V_6(p,n,p)$};
\node (V10) at (-8,-4) {$I_{B}$};
\node (V11) at (-6,-4) {$I_{A}$};
\node (V12) at (-4,-4) {$I_{C}$};
\node (V13) at (-2,-4) {$I_{D}$};
\node (V14) at (0,-4) {$I_{E}$};
\node (V15) at (2,-4) {$I_{F}$};
\node (V16) at (-10,-5) {$FIG. A9.5.1(A)$};
\node (V17) at (-8,-5) {$FIG. A9.5.1(B)$};
\node (V18) at (-6,-5) {$FIG. A9.5.1(C)$};
\node (V19) at (-4,-5) {$FIG. A9.5.1(D)$};
\node (V20) at (-2,-5) {$FIG. A9.5.1(E)$};
\node (V21) at (0,-5) {$FIG. A9.5.1(F)$};
\node (V22) at (-10,-6) {$FIG. A9.5.2(A)$};
\node (V23) at (-8,-6) {$FIG. A9.5.2(B)$};
\node (V24) at (-6,-6) {$FIG. A9.5.2(C)$};
\node (V25) at (-4,-6) {$FIG. A9.5.2(D)$};
\node (V26) at (-2,-6) {$FIG. A9.5.2(E)$};
\node (V27) at (0,-6) {$FIG. A9.5.2(F)$};
\end{tikzpicture}
\end{center}
Chapter X

Dual Programmable AC to DC Rectifier Using Three Phase AC to Three Phase AC Matrix Converter Topology

10.1 INTRODUCTION: Three Phase AC to Three Phase AC Matrix Converter based dual AC to DC rectifier is reported in the literature [43-45]. But these reports only indicate that dual DC output voltages with fixed value is possible by setting the desired AC output voltage phase angle leading by 30 degrees and the frequency of output voltage zero in the model [43-44]. Detailed modelling studies using SIMULINK reveals that with the frequency of desired AC output voltage set to zero, as the AC output voltage phase angle is varied from 0 to $+\pi$ and 0 to $-\pi$, dual DC output voltages in multitude of combinations are possible such as a) Both voltages positive and unequal, b) Both voltages positive and equal, c) Any one voltage zero and the other positive, d) Any one Voltage positive and the other negative with unequal modulus value, e) Any one voltage positive and the other negative with equal modulus value, f) Any one Voltage zero and the other negative, g) Both voltages negative and unequal, h) Both voltages negative and equal. In this chapter, a detailed insight into this discovery is made with a mathematical derivation for the dual DC output voltage magnitude. Theoretical finding is confirmed by SIMULINK model simulation. The model is extended to verify the speed control, acceleration and braking of separately excited DC motors. Applications of this separately excited DC motor and Permanent Magnet DC (PMDC) motor for Hybrid Electric Vehicles (HEVs) and Electric Traction are highlighted.

10.2 OUTPUT VOLTAGE AMPLITUDE LIMIT OF DIRECT AC TO AC CONVERTERS: The three phase AC to three phase AC MC is shown in Fig. 3.1 of Chapter III. The model of the three phase AC to three phase AC MC in terms of modulation duty-cycle has been derived in equations 3.5 to 3.8 in section 3.2 of Chapter III. Venturini modulation algorithm which gives the solution of the modulation duty-cycle for the MC is also presented in equations 3.13 to 3.17 in section 3.2 of Chapter III. Now consider the three phase AC input voltage and desired three phase AC output voltage of the MC as defined in equations 3.9 and 3.11 in section 3.3 of chapter III. In order that the three phase output voltage waveform is synthesised or reconstructed from the three phase input voltage waveform without distortion, it is necessary to switch the bidirectional switches of the MC at a high sampling rate or carrier frequency much higher than the input frequency and the desired output frequency. It is also a requirement that the output voltage waveform so synthesised or reconstructed from the input voltage waveform must lie within the upper and lower bounds of the input voltage waveform at every instant of time. This requirement can be expressed as follows [2-3]:

\[ v_{i,UB}(t) \leq v(t) \leq v_{i,LB}(t) \]  

(10.1)

where \( v_{i,lb}(t) \) and \( v_{i,ub}(t) \) represents the Lower and Upper Bounds of the input voltage \( v(t) \).
Now considering the general case of the three phase input and three phase output voltage waveform defined in equations 3.9 and 3.11 in section 3.3 of chapter III, where the input and output frequency \( \omega_i \) and \( \omega_o \) are not correlated, the equation 10.1 can be expressed as follows [2-3]:

\[
\frac{v_{i,\text{UB}}(t)}{v_{\text{min}}} \geq \frac{v_{O,\text{UB}}(t)}{v_{\text{max}}} \tag{10.2}
\]

where

\[
\frac{v_{O,\text{UB}}}{v_{\text{max}}} \text{ is the maximum value of output voltage upper bound}
\]

\[
\frac{v_{i,\text{UB}}}{v_{\text{min}}} \text{ is the minimum value of input voltage upper bound}
\]

The condition given by equation 10.2 is shown in Fig. 10.1. Thus for a distortion less synthesis or reconstruction of the output voltage waveform from the three phase input voltage, the maximum value of the output voltage at any time should not exceed the input voltage value where \( v_{iA} = v_{iB} = v_{iC} \) or at the intersecting point of the three phase input voltages. This can be expressed as follows:

\[
V_{\text{im}} \cdot \cos(\omega_i t) = V_{\text{im}} \cdot \cos\left(\omega_i t - \frac{2\pi}{3}\right) = V_{\text{im}} \cdot \cos\left(\omega_i t - \frac{4\pi}{3}\right) \tag{10.3}
\]

Equation 10.3 is valid at intervals of \( \pi/3 \) radians and the magnitude at the intersecting point of the three phase input voltages is \( 0.5*V_{\text{im}} \) [2-3]. This is illustrated in Fig. 10.1. The condition given in equation 10.2 requires the following equation to be valid [2-3]:

\[
\frac{v_{O}(t)}{V_{\text{om}}} \leq 0.5 \cdot \frac{v_{i}(t)}{V_{\text{im}}} \tag{10.4}
\]

Equation 10.4 is independent of the conversion algorithm used. The maximum value of the output amplitude is obtained when the maximum value of the difference between the output voltage upper bound and output voltage lower bound coincides with minimum value of the difference between the input voltage upper bound and the input voltage lower bound. Referring to Fig. 10.1, the maximum value of the upper bound of the output voltage \( V_{oa} \) varies from 0 to \( 0.5*V_{\text{im}} \) with respect to time while for the other two output phases \( V_{ob} \) and \( V_{oc} \) the lower bound of the output voltage varies from

![Diagram of Three Phase Cosine Wave Input and Output Voltages](image-url)
0.5\*Vim to -0.5\*Vim and -0.5\*Vim to +0.5\*Vim respectively. At any instant of time during the positive half cycle of the output voltage \(V_{oa}\), this maximum value of the difference between the upper and lower bounds of the output voltage is therefor the phasor difference between \(V_{oa}\) and \(V_{ob}\) or \(V_{oa}\) and \(V_{oc}\) which can be expressed as follows [2-3]:

\[
\left(\frac{V_{O_{UB}}(t) - V_{O_{LB}}(t)}{\text{MAX}}\right) = \left(\bar{V}_{oa} - \bar{V}_{ob}\right) = \left(\bar{V}_{oa} - \bar{V}_{oc}\right) = \left(\sqrt{3}\right) \cdot V_{om} \quad (10.5)
\]

Equation 10.5 gives the maximum value of the line to line output voltage. From Fig. 10.1, for the three phase input voltage, the minimum value of the lower bound for \(V_{iA}\) is \(-Vim\) and the minimum value of the upper bound for the input voltages \(V_{iB}\) and \(V_{iC}\) are \(+0.5\*Vim\) respectively which can be expressed as follows [2-3]:

\[
\left(\frac{v_{i_{UB}} - v_{i_{LB}}}{\text{MIN}}\right) = \left[+0.5\*V_{im} - (-V_{im})\right] = \frac{3\*V_{im}}{2} \quad (10.6)
\]

Equating equations 10.5 and 10.6, the maximum output voltage amplitude obtainable can be expressed as follows [2-3]:

\[
\begin{align*}
V_{om} &= \frac{\sqrt{3}}{2} \cdot V_{im} = 0.866 \cdot V_{im} \\
V_{O} &= 0.866 \cdot V_{i}
\end{align*} \quad (10.7)
\]

Equation 10.7 gives the maximum output voltage amplitude obtainable for a three phase AC to three Phase AC MC.

10.3 PRINCIPLE OF DUAL PROGRAMMABLE AC TO DC RECTIFIER: For the three phase AC input voltage and the output voltage as defined in equations 3.9 and 3.11, Venturini modulation algorithm for Modulation Duty-Cycle which satisfies equations 3.11 and 3.12 assuming Unity Input Phase Displacement Factor is given in equation 3.17 in section 3.3 of Chapter III. For the above three phase MC to work as an AC to DC rectifier, the output frequency \(f_o\) is to be set to zero [43-44]. This makes equation 3.10 and 3.11 given in section 3.3 of chapter III as follows:

\[
\begin{align*}
i_o &= \frac{[i_a, i_b, i_c]}{i_{om}} = I_{om} \cdot \begin{bmatrix} \cos(\varphi_o) \\
\cos(\varphi_o - \frac{2\pi}{3}) \\
\cos(\varphi_o + \frac{2\pi}{3}) \end{bmatrix} \quad (10.8) \\
v_o &= \frac{[v_a, v_b, v_c]}{q \cdot V_{im}} = Q \cdot V_{im} \cdot \begin{bmatrix} \cos(\varphi_o) \\
\cos(\varphi_o - \frac{2\pi}{3}) \\
\cos(\varphi_o + \frac{2\pi}{3}) \end{bmatrix} \quad (10.9)
\end{align*}
\]

In equation 10.9, if the output voltage phase angle \(\varphi_o\) is set to +30 degrees, it is seen that the output voltage \(v_b\) becomes zero, where as \(v_a\) and \(v_c\) have equal magnitude [43-44]. In any three phase AC to three phase AC matrix converter, the intrinsic output voltage limit irrespective of control algorithm
used is given by equation 10.7 [2-3]. In the linear region of the modulation index $q$, the input-output voltage relation in an MC can be expressed as follows:

$$v_o = q \cdot v_i \quad (10.10)$$

Combining equations 10.7 and 10.10, we have the following:

$$v_{om} = 0.866 \cdot q \cdot V_{im} \quad (10.11)$$

Three phase output voltage in equation 3.11 of chapter III is shown in Fig. 10.2(A). With $b$ as virtual ground or virtual reference point, for any arbitrary angular frequency $\omega_o$ of the output voltage, $v_{ab}$ and $v_{cb}$ which correspond to $v_{o1}$ and $v_{o2}$, leads $v_a$ by $\pi/6$ and $\pi/2$ radians respectively. Now noting that for the three phase MC to work as a dual AC to DC rectifier the output frequency $\omega_o$ is zero, combining equation 10.11 and noting the phase lead of $v_{ab}$ and $v_{cb}$ with respect to $v_a$, equations 10.12 and 10.13 follows:

$$V_{ab} = V_{o1} = 0.866 \cdot q \cdot V_{im} \cdot \cos \left( \varphi_o + \frac{\pi}{6} \right) \quad (10.12)$$

$$V_{cb} = -V_{bc} = V_{o2} = 0.866 \cdot q \cdot V_{im} \cdot \cos \left( \varphi_o + \frac{\pi}{2} \right) \quad (10.13)$$

Equations 10.12 and 10.13 are discussed in A10.1 Appendix. When a practical implementation is considered, a question arises whether the three phase AC voltage generated by the grid is a sine wave or cosine wave? Evidently it is a sine wave of the form $V_{iK} = V_{im} \sin(\omega_i t - \gamma)$ where $\gamma = 0, 2\pi/3, 4\pi/3$ for $K = A, B, C$ respectively. Considering this factor, a phase lag of $\pi/2$ radians is given to the three phase AC input and output voltage defined in equations 3.9 and 3.11 of chapter III. This permits three phase sine wave AC input voltage to be used for practical implementation. With a phase lag of $\pi/2$ radians given to the three phase output voltage defined in equation 3.11 of chapter III, the new phasor diagram is shown in Fig. 10.2(B). The new position of $v_a$, $v_b$ and $v_c$ are marked $v_a'$, $v_b'$ and $v_c'$ respectively. The new position of $v_{ab}$ and $v_{cb}$ are marked $v_{ab}'$ and $v_{cb}'$ which lag the original position of $v_{ab}$ and $v_{cb}$ in Fig. 10.2(A) by $\pi/2$ radians. Thus the new position of $v_{ab}'$ and $v_{cb}'$ in Fig. 10.2(B), lag the original position of $v_a$ in Fig. 10.2(A) by $\pi/3$ and zero radians respectively. Now noting that for the three phase MC to work as a dual AC to DC rectifier the output frequency $\omega_o$ is
zero, combining equation 10.11 and noting the phase lag of \( v_{ab}' \) and \( v_{cb}' \) with respect to \( v_a \), equations 10.14 and 10.15 follows:

\[
V'_{ab} = V_{o1} = 0.866 \times q \times V_{im} \times \cos \left( \phi_o - \frac{\pi}{3} \right) \quad (10.14)
\]
\[
V'_{cb} = -V'_{bc} = V_{o2} = 0.866 \times q \times V_{im} \times \cos(\phi_o) \quad (10.15)
\]

As can be seen from equations 10.14 and 10.15, when \( \phi_o \) is varied from 0 to +\( \pi \) and 0 to –\( \pi \), multitude of combination of dual DC output voltages are possible. Thus by suitable changing the value of \( \phi_o \) in the model of three phase MC, dual programmable DC output voltages can be obtained.

### 10.4 MODEL OF DUAL PROGRAMMABLE AC TO DC RECTIFIER:

The model of the Dual programmable AC to DC rectifier is shown in Fig.10.3. The model is developed in SIMULINK [51]. Here Venturini algorithm for unity input phase displacement factor is assumed in generating the gate pulses for the bidirectional switches. Also three phase sine wave input and output voltages are used for developing the model. The above algorithm is proved valid for three phase sine wave input and output voltage in A3.3 Appendix in Chapter III. The model consists of:

- a) Bidirectional switch gate pulse generator
- b) Output voltage phase angle varying device
- c) Three phase sine wave AC voltage source
- d) MC bidirectional switch matrix
- e) RLC output filter
- f) RL load.

The parameters used for the model is given in Table 10.1.

<table>
<thead>
<tr>
<th>TABLE 10.1: Dual Programable AC to DC Rectifier – SIMULINK Model Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>SL.No.</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>7</td>
</tr>
</tbody>
</table>

Bidirectional switch gate pulse generator is shown in Fig. 10.4(A). This consists of two embedded MATLAB functions. The first MATLAB function generates the nine modulation functions according to equations 3.17 of Chapter III, using inputs q, Vim, fi, fo, phi_0 and the time module. The second MATLAB function generates the gate timing pulse for the nine bidirectional switches, by comparison of the modulation functions with a saw-tooth carrier vsaw. The code for generating the timing pulse for the bidirectional switches connected between input phase A, B, C and output phase a, b, c is given in section 3.4.1 of Chapter III. Output Voltage Phase Angle Varying Device is shown in Fig.10.3. This is using slider gain block. The constant block with value +\( \pi/12 \) is given as input to the slider gain block whose multiplication constant can be varied from -12 to +12. Appropriate gain multiplier value is entered in the current value field of slider gain block. The output of slider gain provides the variable output voltage phase angle \( \phi_o \) in radians. Three Phase AC Sine Wave voltage Source is shown in Fig. 10.4(B). This three phase AC sine wave source is from the SimPowerSystems blockset. This three phase sine wave AC source generates three phase voltage with a line to line RMS value of.
FIG. 10.3: DUAL PROGRAMMABLE AC TO DC RECTIFIER USING THREE PHASE MATRIX CONVERTER TOPOLOGY
381.04 Volts and frequency 50 Hz. The nine
MC Bidirectional Switch Matrix using IGBTs
and diodes is shown in Fig. 10.4(C). RLC
Output Filter is shown in Fig. 10.4(D). The L
and C values are so chosen to resonate at the
carrier switching frequency of 2 kHz. The
output voltage is tapped across the filter
kapacitor. RL Load is shown in Fig. 10.4(E).

The theoretically computed value of the dual
DC output voltages Vo1 and Vo2 using
equations 10.14 and 10.15 for the parameters shown in Table 10.1 is given in Table 10.2 for various
values of output voltage phase angle $\phi_o$ radians.

10.4.1 SIMULATION RESULTS: The simulation of the Dual Programmable AC to DC rectifier
was carried out in SIMULINK [51]. The ode15s(Stiff/NDF) solver is used. The simulation results for
the value of $\phi_o$ shown in the order in Table 10.2 are shown in Fig. 10.5(A) to (X). The simulation
results are shown in Table 10.3. The model simulation results indicate that the magnitude and sign of
vo1 and vo2 closely agree with the theoretically computed value shown in Table 10.2.
### TABLE 10.2: Theoretically Computed Values

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>( \phi \text{ radians} )</th>
<th>Vo1 Volts</th>
<th>Vo2 Volts</th>
<th>Sl.No.</th>
<th>( \phi \text{ radians} )</th>
<th>Vo1 Volts</th>
<th>Vo2 Volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>67.34</td>
<td>134.64</td>
<td>13</td>
<td>( \pm \pi )</td>
<td>-67.34</td>
<td>-134.69</td>
</tr>
<tr>
<td>2</td>
<td>+( \pi/12 )</td>
<td>95.24</td>
<td>130.107</td>
<td>14</td>
<td>-11( \pi/12 )</td>
<td>-95.24</td>
<td>-130.107</td>
</tr>
<tr>
<td>3</td>
<td>+( \pi/6 )</td>
<td>116.64</td>
<td>116.64</td>
<td>15</td>
<td>-5( \pi/6 )</td>
<td>-116.64</td>
<td>-116.64</td>
</tr>
<tr>
<td>4</td>
<td>+( \pi/4 )</td>
<td>130.1</td>
<td>95.24</td>
<td>16</td>
<td>-3( \pi/4 )</td>
<td>-130.107</td>
<td>-95.24</td>
</tr>
<tr>
<td>5</td>
<td>+( \pi/3 )</td>
<td>134.69</td>
<td>67.34</td>
<td>17</td>
<td>-2( \pi/3 )</td>
<td>-134.69</td>
<td>-67.34</td>
</tr>
<tr>
<td>6</td>
<td>+5( \pi/12 )</td>
<td>130.107</td>
<td>34.86</td>
<td>18</td>
<td>-7( \pi/12 )</td>
<td>-130.107</td>
<td>-34.86</td>
</tr>
<tr>
<td>7</td>
<td>+( \pi/2 )</td>
<td>116.64</td>
<td>0</td>
<td>19</td>
<td>-( \pi/2 )</td>
<td>-116.64</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>+7( \pi/12 )</td>
<td>95.24</td>
<td>-34.8</td>
<td>20</td>
<td>-5( \pi/12 )</td>
<td>-95.24</td>
<td>34.86</td>
</tr>
<tr>
<td>9</td>
<td>+2( \pi/3 )</td>
<td>67.34</td>
<td>-67.34</td>
<td>21</td>
<td>-( \pi/3 )</td>
<td>-67.34</td>
<td>67.34</td>
</tr>
<tr>
<td>10</td>
<td>+3( \pi/4 )</td>
<td>34.86</td>
<td>-95.24</td>
<td>22</td>
<td>-( \pi/4 )</td>
<td>-34.86</td>
<td>95.24</td>
</tr>
<tr>
<td>11</td>
<td>+5( \pi/6 )</td>
<td>0</td>
<td>-116.64</td>
<td>23</td>
<td>-( \pi/6 )</td>
<td>0</td>
<td>116.64</td>
</tr>
<tr>
<td>12</td>
<td>+11( \pi/12 )</td>
<td>-34.86</td>
<td>-130.107</td>
<td>24</td>
<td>-( \pi/12 )</td>
<td>34.86</td>
<td>130.107</td>
</tr>
</tbody>
</table>

### TABLE 10.3: Model Simulation Results

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>( \phi \text{ radians} )</th>
<th>Vo1 Volts</th>
<th>Vo2 Volts</th>
<th>Sl.No.</th>
<th>( \phi \text{ radians} )</th>
<th>Vo1 Volts</th>
<th>Vo2 Volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>67.5</td>
<td>135</td>
<td>13</td>
<td>( \pm \pi )</td>
<td>-67.5</td>
<td>-135</td>
</tr>
<tr>
<td>2</td>
<td>+( \pi/12 )</td>
<td>95.1</td>
<td>130</td>
<td>14</td>
<td>-11( \pi/12 )</td>
<td>-95</td>
<td>-130</td>
</tr>
<tr>
<td>3</td>
<td>+( \pi/6 )</td>
<td>117</td>
<td>117</td>
<td>15</td>
<td>-5( \pi/6 )</td>
<td>-116.5</td>
<td>-116.5</td>
</tr>
<tr>
<td>4</td>
<td>+( \pi/4 )</td>
<td>130</td>
<td>95.5</td>
<td>16</td>
<td>-3( \pi/4 )</td>
<td>-130</td>
<td>95</td>
</tr>
<tr>
<td>5</td>
<td>+( \pi/3 )</td>
<td>135</td>
<td>67.5</td>
<td>17</td>
<td>-2( \pi/3 )</td>
<td>-135</td>
<td>-67.5</td>
</tr>
<tr>
<td>6</td>
<td>+5( \pi/12 )</td>
<td>130</td>
<td>35</td>
<td>18</td>
<td>-7( \pi/12 )</td>
<td>-130</td>
<td>-35</td>
</tr>
<tr>
<td>7</td>
<td>+( \pi/2 )</td>
<td>116</td>
<td>0</td>
<td>19</td>
<td>-( \pi/2 )</td>
<td>-116.5</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>+7( \pi/12 )</td>
<td>95</td>
<td>-35</td>
<td>20</td>
<td>-5( \pi/12 )</td>
<td>-95</td>
<td>35</td>
</tr>
<tr>
<td>9</td>
<td>+2( \pi/3 )</td>
<td>67.5</td>
<td>-67.5</td>
<td>21</td>
<td>-( \pi/3 )</td>
<td>-67.5</td>
<td>67.5</td>
</tr>
<tr>
<td>10</td>
<td>+3( \pi/4 )</td>
<td>35</td>
<td>-95</td>
<td>22</td>
<td>-( \pi/4 )</td>
<td>-35</td>
<td>95</td>
</tr>
<tr>
<td>11</td>
<td>+5( \pi/6 )</td>
<td>0</td>
<td>-117</td>
<td>23</td>
<td>-( \pi/6 )</td>
<td>0</td>
<td>117</td>
</tr>
<tr>
<td>12</td>
<td>+11( \pi/12 )</td>
<td>-35</td>
<td>-130</td>
<td>24</td>
<td>-( \pi/12 )</td>
<td>35</td>
<td>130</td>
</tr>
</tbody>
</table>

### 10.5 Model of Dual Programmable AC to DC Rectifier Fed Separately Excited DC Motors:

The model of the Dual programmable AC to DC rectifier fed DC Motor
is shown in Fig.10.6. The model is developed in SIMULINK [51]. Here Venturini algorithm for unity input phase displacement factor is assumed in generating the gate pulses for the bidirectional switches. Also three phase sine wave input and output voltages are used for developing the model. The above algorithm is proved valid for three phase sine wave input and output voltage in A3.3 Appendix in Chapter III. The model consists of a) Bidirectional switch gate pulse generator b) Output voltage phase angle varying device c) Three phase sine wave AC voltage source d) MC bidirectional switch matrix e) RLC output filter f) Two Separately Excited DC Motor Loads. The parameters used for the model excluding the two R-L loads are shown in Table 10.1. The parameters of the two separately excited DC Motors are shown in Table 10.4. In the model sub units given above, item a, c, d, and e have already been explained in Section 10.4 above.

The output voltage phase angle varying device is shown in Fig. 10.6. This is a multiport switch. The first port at the top is the control port and the remaining ports are data ports. Here the number of data ports are eight, numbered from top to bottom. The sequence generator connected to the control port has the numbers from one to eight at specified intervals of time. Depending on the number displayed at a specific time by the sequence generator, the input corresponding to that data port number appears at the output of the multiport switch. For example if the number at any time interval displayed by the sequence generator is six, then $\frac{8\pi}{12}$ appears at the output of multiport switch.

The two separately excited DC motors have parameters as shown in Table 10.4 [51]. The above DC motor model is shown in Fig. 10.7.

### TABLE 10.4: DC Motors

<table>
<thead>
<tr>
<th>SLNo.</th>
<th>Parameters</th>
<th>DC Machine 1 Value</th>
<th>Unit</th>
<th>DC Machine 2 Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power Output</td>
<td>10</td>
<td>HP</td>
<td>5</td>
<td>HP</td>
</tr>
<tr>
<td>2</td>
<td>Rated Terminal Voltage</td>
<td>500</td>
<td>Volts</td>
<td>240</td>
<td>Volts</td>
</tr>
<tr>
<td>3</td>
<td>Speed</td>
<td>1750</td>
<td>RPM</td>
<td>1750</td>
<td>RPM</td>
</tr>
<tr>
<td>4</td>
<td>Field Voltage</td>
<td>300</td>
<td>Volts</td>
<td>300</td>
<td>Volts</td>
</tr>
<tr>
<td>5</td>
<td>Armature Resistance</td>
<td>4.712</td>
<td>Ohms</td>
<td>2.581</td>
<td>Ohms</td>
</tr>
<tr>
<td>6</td>
<td>Armature Inductance</td>
<td>0.0527</td>
<td>H</td>
<td>0.028</td>
<td>H</td>
</tr>
<tr>
<td>7</td>
<td>Field Resistance</td>
<td>180</td>
<td>Ohms</td>
<td>281.3</td>
<td>Ohms</td>
</tr>
<tr>
<td>8</td>
<td>Field Inductance</td>
<td>71.4</td>
<td>H</td>
<td>156</td>
<td>H</td>
</tr>
<tr>
<td>9</td>
<td>Field-Armature Mutual Inductance</td>
<td>1.345</td>
<td>H</td>
<td>0.9483</td>
<td>H</td>
</tr>
<tr>
<td>10</td>
<td>Total Inertia</td>
<td>0.0425</td>
<td>kg-m/2</td>
<td>0.0221</td>
<td>kg-m/2</td>
</tr>
<tr>
<td>11</td>
<td>Damping Coefficient</td>
<td>0.0034</td>
<td>Nw-m-s</td>
<td>0.0029</td>
<td>Nw-m-s</td>
</tr>
</tbody>
</table>

10.5.1 SIMULATION RESULTS: The simulation of the Dual Programmable AC to DC rectifier fed separately excited DC motors was carried out in SIMULINK [51]. The ode15s(Stiff/NDF) solver is used. At intervals of 0.2 seconds, the numbers from 1 to 8 are given as input to control port of multiport switch. The output of $\varphi_0$ during this time intervals are $+\pi/12$, $+\pi/6$, $+\pi/4$, $+7\pi/12$, 0, $+2\pi/3$, $-\pi/6$, $-\pi/4$, $-7\pi/12$.
Chapter X: Dual Programmable AC to DC Rectifier Using Three Phase AC to Three Phase AC Matrix Converter Topology

Fig. 10.6: Model of Dual Programmable AC to DC Rectifier Fed Separately Excited DC Motors
Chapter X: Dual Programmable AC to DC Rectifier Using Three Phase AC to Three Phase AC Matrix Converter Topology

The output voltage $V_{o1}$ and $V_{o2}$ for DC machines 1 and 2 can be obtained from Table 10.3. These values from Table 10.3 indicate that DC machine 1 is accelerating, decelerating, coasting, and braking whereas DC machine 2 is accelerating, reduced acceleration or decelerating, braking, accelerating, braking, accelerating and braking. The simulation result for the motor speed of DC machines 1 and 2 is shown in Fig. 10.8 above, which confirm the above finding using Table 10.3. The variation of the two DC output voltages $V_{o1}$ and $V_{o2}$ with respect to $\phi_o$ is shown in Fig. 10.9.

FIG. 10.7

FIG. 10.8

FIG. 10.9
10.6 REAL TIME IMPLEMENTATION: Simulation results in Section 10.5.1 indicates that this Dual programmable AC to DC rectifier can be used for the speed control of either two separately excited DC motor drives or else two Permanent Magnet DC Motor Drives thus rendering them suitable for Hybrid Electric Vehicle [63] and Electric Traction applications. Some of these applications are highlighted in Fig. 10.10(A), (B), (C) and (D). The dSPACE implementation scheme of the gate drive for the bidirectional switches of the three phase MC used as Dual Programmable AC to DC rectifier is shown in Fig. 10.10(E).

Fig. 10.11 shows one method of developing a output voltage phase angle device using two op.amps. When the switch SS1 is thrown to A or B, the output of the first op.amp. will be $+\pi$ or $-\pi$ Volts respectively. The second op.amp. has $12E3$ (12 K) Ohms as the input resistor and twelve $1E3$ (1 K) Ohms in series as feedback resistor with tappings for each feedback resistor. By throwing the switch SS2 from position 1 to 12, output voltage in the range $\pm\pi/12$ to $\pm\pi$ can be obtained in steps of $\pm\pi/12$ Volts.
Fig. 10.12 shows one of several methods of generating a 2 kHz saw-tooth carrier pulse with a peak value of 1 volt and minimum value of zero. The astable multi using NE555 by Texas Instruments generates a 2 kHz square pulse with peak value of 5 Volts, ON time of 495 microseconds and OFF
time of 5 microseconds. This output is compared using an Op.Amp. comparator with a +1 Volt DC voltage obtained using a +10 Volts power supply and potential divider. The output of this comparator drives a pair of N and P MOSFET switches in series with a 25 Kilohms resistor connected to the +10 Volts power supply. Across the P channel MOSFET switch a capacitor of 0.18984e-6 Farads capacitor is connected. The simulation Fig. 10.12 using PSIM with the NE555 astable multi replaced by a 2 kHz square clock pulse generator with ON and OFF duration of 495e-6 and 5e-6 seconds is shown in Fig. 10.13.

Another method of generating the 2 kHz saw-tooth carrier generator using PIC16F84A microcontroller is shown in Appendix I.

10.7 DISCUSSION OF RESULTS: Dual Programmable AC to DC rectifier is a new concept hitherto NOT reported in the literature references. The simulation results of the Dual Programmable AC to DC rectifier well agree with the theoretically computed results. As the dual DC output voltages varies in magnitude and takes both positive and negative values with the variation of output voltage phase angle $\varphi_O$, this method is suitable for speed control, acceleration and braking of Separately Excited DC Motors and Permanent magnet DC Motors. Practical applications for HEV[63] and Electric traction are highlighted. One method of implementing the above rectifier in real time using dSPACE is shown. Although only one simulation result is shown in Fig. 10.8 for one set of output
voltage phase angle \( \phi_0 \) value, it is possible to have number of combination of \( \phi_0 \) values to suit the individual requirement. By looking at Fig. 10.9, it is possible to select the output phase angle \( \phi_0 \) required for either acceleration or deceleration or braking of the two DC motors. This Dual Programmable AC to DC rectifier is sure to find applications involving the speed control of Separately Excited DC Motors and Permanent Magnet DC Motors such as in Hybrid Electric Vehicles (HEVs)[63] and in Electric Traction.

10.8 CONCLUSIONS: A novel concept of Dual Programmable AC to DC rectifier using three phase AC to three phase AC MC topology is presented in this chapter. Simulation results and theoretically computed values closely well agree. Venturini algorithm for the maximum output voltage magnitude of direct AC to AC converter forms the basis for the behaviour of dual programmable AC to DC rectifier. The proposed scheme can be implemented in real time as this has applications in the speed control, acceleration and breaking by plugging of separately excited DC motor and Permanent Magnet DC Motor.

A10.1 APPENDIX: Equations 10.12 and 10.13 are derived using three phase cosine wave input and output voltages. The three phase source used is from the Electrical Source library in the SimPowerSystems blockset of SIMULINK. Here in the box corresponding to Phase Angle of Phase A (degrees), a value of 90 is entered. All other boxes are filled with appropriate values as used in the above model. The simulation results obtained for various values of \( \phi_0 \) are tabulated in Table A10.1. The plot of \( v_{o1} \) and \( v_{o2} \) for a \( \phi_0 \) of \(+\pi/6\) radians is shown in Fig. A10.1. From Fig. A10.1 it is clear that for the output voltage phase angle \( \phi_0 \) of \(+\pi/6\) radians, simulation results for \( V_{o1} \) and \( V_{o2} \) are +67.5 Volts and -67.5 Volts respectively which closely agree with the theoretically computed value given in Table A10.1.

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>( \phi_0 ) radians</th>
<th>( V_{o1} ) (Volts)</th>
<th>( V_{o2} ) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>116.64</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>(+\pi/6)</td>
<td>67.34</td>
<td>-67.34</td>
</tr>
<tr>
<td>3</td>
<td>(+\pi/4)</td>
<td>34.86</td>
<td>-95.24</td>
</tr>
<tr>
<td>4</td>
<td>(+\pi/3)</td>
<td>0</td>
<td>-116.64</td>
</tr>
<tr>
<td>5</td>
<td>(+\pi/2)</td>
<td>-67.34</td>
<td>-134.69</td>
</tr>
<tr>
<td>6</td>
<td>(+2\pi/3)</td>
<td>-116.64</td>
<td>-116.64</td>
</tr>
<tr>
<td>7</td>
<td>(+5\pi/6)</td>
<td>-134.69</td>
<td>-67.34</td>
</tr>
<tr>
<td>8</td>
<td>(\pm\pi)</td>
<td>-116.64</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>(-5\pi/6)</td>
<td>-67.34</td>
<td>67.34</td>
</tr>
<tr>
<td>10</td>
<td>(-2\pi/3)</td>
<td>0</td>
<td>116.64</td>
</tr>
<tr>
<td>11</td>
<td>(-\pi/2)</td>
<td>67.34</td>
<td>134.69</td>
</tr>
<tr>
<td>12</td>
<td>(-\pi/3)</td>
<td>116.64</td>
<td>116.64</td>
</tr>
<tr>
<td>13</td>
<td>(-\pi/4)</td>
<td>130.1</td>
<td>95.24</td>
</tr>
<tr>
<td>14</td>
<td>(-\pi/6)</td>
<td>134.69</td>
<td>67.34</td>
</tr>
</tbody>
</table>
Chapter XI

Delta-Sigma Modulation of Three Phase AC to Three Phase AC Matrix Converter

11.1 INTRODUCTION: Matrix converter directly converts the AC input voltage at any given frequency to AC output voltage with arbitrary amplitude at any unrestricted frequency without the need for a dc link capacitor storage element at the input side. Since inception, several carrier based modulation techniques have been proposed for matrix converter. All these techniques use either a saw-tooth carrier[1-8] or a triangle carrier voltage signal[13-14, 16-17] to be compared with modulation voltage signals to generate gate switching pulses for the bidirectional switches of matrix converter. These modulation voltage signals are generated using Venturini algorithm [1-5] or using other recently proposed algorithms [11-14, 16-17]. This chapter examines the recently proposed delta-sigma modulation technique for matrix converter [46-49]. A model of the three phase AC to three phase AC matrix converter (MC) using delta-sigma modulation technique is developed in SIMULINK [51]. Both Venturini[1-5] as well as advanced modulation algorithm [13-14, 16-17] are used for generating the modulation voltage signals. Simulation is carried out for a given sampling frequency. It is seen from simulation results that voltage harmonic peaks are reduced at integral multiples of sampling frequency[46-48]. Also simulation of three phase Induction Motor (IM) fed by MC using delta-sigma modulation is presented. The delta-sigma modulation technique can reduce noise peaks in the output voltage as compared to conventional PWM technique and has the advantage of maintaining noise regulation.

11.2 REVIEW OF MATRIX CONVERTER GATE PULSE GENERATION: The three phase AC to three phase MC is shown in Fig. 3.1 of Chapter III. Gate pulses for three phase matrix converter bidirectional switches have to be generated to comply with some specific requirement. Referring to Fig. 3.1 of Chapter III, it is seen that if two or more bidirectional switches connected to same output phase such as SAa, SBa and SCa are turned ON simultaneously, there will be a dead short circuit. These gate pulses have to be on in sequence, one after the other. Also it is required that one of the above bidirectional switches should remain closed. This is achieved by carrier PWM technique [1-5] and also by Delta-Sigma modulation technique [46-48].

11.2.1 SAW-TOOTH CARRIER PWM TECHNIQUE: In carrier PWM technique, the nine modulation functions defined in equation 3.17 of Chapter III are developed using Embedded MATLAB Function in SIMULINK [51]. These are then compared with a saw-tooth carrier voltage signal using comparators and the resulting output is given to logic gates. The method of generating the gate pulses for output phase a is shown in Fig. 11.1(A). Gate pulses tAa, tBa and tCa correspond to bidirectional switches SAa, SBa and SCa respectively. Similar hardware circuit applies to output phase b and c.
11.2.2 TRAPEZOIDAL CARRIER PWM TECHNIQUE: In triangle carrier PWM, the nine modulation functions defined in equation 4.40 of Chapter IV are derived using Embedded MATLAB Function in SIMULINK [51]. These are then compared with a triangle carrier voltage signal using comparators and the resulting output is given to logic gates. The method of generating the gate pulses for output phase a is shown in Fig. 11.1(B). Gate Pulses tAa, tBa and tCa correspond to bidirectional switches SAa, SBa and SCa respectively. Similar hardware circuit applies to output phase b and c.

11.2.3 DELTA-SIGMA PWM TECHNIQUE: This is a recently proposed technique for three phase Matrix Converters [46-48]. In Delta-Sigma modulation high frequency noise peaks in the output voltages due to switching operation does not occur and this becomes an advantage for clearing noise regulations [46-48]. Fig. 11.1(C) and (D) shows the first order Delta-Sigma modulator [49]. Analysis of Fig. 11.1(C) gives the following:

$$X(z) - z^{-1} \cdot Y(z) + z^{-1} \cdot E(z) = E(z) \quad (11.1)$$

Analysis of Fig. 11.1(D) gives the following:

$$X(z) - z^{-1} \cdot Y(z) + z^{-1} \cdot E(z) = E(z) \quad (11.2)$$

In sample time, equations 11.1 and 11.2 can be expressed as follows:

$$x(k) - y(k-1) + e(k-1) = e(k) \quad (11.3)$$

Equations 11.1 and 11.2 agree well and there for Fig. 11.1(C) and (D) are identical.
Quantizer characteristics can be expressed as follows:

\[ y(k) = sgn[e(k)] \quad (11.4) \]

The quantizer output is +1 if its input exceeds the threshold and -1 if its input is below threshold value. The quantizer output is used to control the bidirectional switches.

11.3 DELTA-SIGMA MODULATOR INTERFACE: This section discusses the implementation aspects of a Delta-Sigma modulator for a three phase matrix converter. The Delta-Sigma modulator for the output phase a of three phase matrix converter is shown in Fig. 11.2. Similar circuit applies to output phase b and c of the matrix converter. In Fig. 11.2, the quantizer output is given to comparator. The comparator output is HIGH when its input greater than or equal to zero, else the output is LOW.

The comparator outputs A, B and C form the input to the combinational logic circuit which generates the gate pulse for the bidirectional switches. The combinational logic circuit must be so designed to comply with the gate drive requirement specified under section 11.2 above. Table 11.1 shows one method of generating the gate pulse for the bidirectional switches connected to output phase a. Gate pulse tAa, tBa and tCa can be expressed as follows:

\[
tAa = (A \cap B) \cup (\overline{B} \cap \overline{C}) \quad (11.5)
\]
\[
tBa = (\overline{A} \cap B) \quad (11.6)
\]
\[
tCa = (B \cap C) \quad (11.7)
\]

Gate pulse expressions for bidirectional switches connected to output phase b and c can be expressed as follows:
\[ tAb = (D \cap \overline{F}) \quad (11.8) \]
\[ tBb = (\overline{D} \cap F) \cup (E \cap F) \quad (11.9) \]
\[ tCb = (\overline{E} \cap F) \quad (11.10) \]
\[ tAc = (G \cap \overline{I}) \quad (11.11) \]
\[ tBc = (\overline{G} \cap H) \quad (11.12) \]
\[ tCc = (G \cap I) \cup (\overline{G} \cap \overline{H}) \quad (11.13) \]

In equations 11.5 to 11.13, the symbols \( \cap \), \( \cup \), \( \neg \) represent logical AND, OR and NOT operation respectively. For the output phase b and c, inputs to delta-sigma modulator in Fig. 11.2, MAa, MBa and MCa are replaced by MAb, MBb, MCb and MAc, MBc, MCc respectively. Similarly the inputs A, B, C to the combinational logic circuit in Fig. 11.2 are replaced by D, E, F for output phase b and G, H, I for output phase c for the sake of clarity.

### 11.4 Venturini Model of Three Phase Matrix Converter Using Delta-Sigma Modulation

The Venturini model of the three phase AC to three phase AC MC using delta-sigma modulation is shown in Fig. 11.3. The Embedded MATLAB Function generates the nine modulation duty-cycles as defined in equation 3.17 of Chapter III. These nine modulation functions are applied as inputs to first order Delta-Sigma modulators as shown in Fig. 11.2. The combinational logic interface are designed as described in Section 11.3 above. The principle of operation of the Delta-Sigma modulator is explained in Section 11.2.3 above. The nine gate pulses from the output of combinational logic circuit is applied to the respective gates of the bidirectional switches.

### 11.4.1 Simulation Results

The simulation of the delta-sigma modulated MC shown in Fig. 11.3 was carried out using SIMULINK [51]. The simulation parameters are shown in Table 11.2. The simulation results are tabulated in Table 11.3.

#### TABLE 11.2: Delta-Sigma Modulated PH3 AC to PH3 AC MC – SIMULINK Model Parameters

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>RMS Line to Neutral Input Voltage</td>
<td>220</td>
<td>Volts</td>
</tr>
<tr>
<td>2)</td>
<td>Input Frequency</td>
<td>50</td>
<td>Hz</td>
</tr>
<tr>
<td>3)</td>
<td>Output Frequency</td>
<td>50, 10</td>
<td>Hz</td>
</tr>
<tr>
<td>4)</td>
<td>Sampling Frequency</td>
<td>5</td>
<td>kHz</td>
</tr>
<tr>
<td>5)</td>
<td>Modulation Index</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>6)</td>
<td>RL Load</td>
<td>50, 0.5</td>
<td>( \Omega ), H</td>
</tr>
</tbody>
</table>

The ode15s(Stiff/NDF) solver was used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage and their respective oscilloscope waveforms for an output frequency of 50 Hz are shown in Fig. 11.4(A) to (D) and Fig. 11.5(A) to (D) respectively. The same harmonic spectrum and waveforms in the above order for an output frequency of 10 Hz are shown in Fig. 11.6(A) to (D) and Fig. 11.7(A) to (D) respectively. The simulation results are tabulated in Table 11.3.

#### TABLE 11.3: SIMULINK Model Simulation Results

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Frequency Input-Output Hz</th>
<th>Line to Neutral Output THD (p.u.)</th>
<th>Line to Line Output Voltage THD (p.u.)</th>
<th>Input current THD (p.u.)</th>
<th>Load current THD (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>50 – 50</td>
<td>1.14</td>
<td>1.195</td>
<td>1.198</td>
<td>0.1155</td>
</tr>
<tr>
<td>2)</td>
<td>50 – 10</td>
<td>2.36</td>
<td>2.22</td>
<td>1.165</td>
<td>0.449</td>
</tr>
</tbody>
</table>
FIG. 11.3 VENTURINI MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING DELTA-SIGMA MODULATION
Chapter XI: Delta-Sigma Modulation of Three Phase AC to Three Phase AC Matrix Converter

![Graph 1: Line to Neutral Output Voltage](Image)

![Graph 2: Fundamental (50Hz)](Image)

![Graph 3: Phase A Input Current](Image)

![Graph 4: Load Current](Image)

![Graph 5: Load Current](Image)

![Graph 6: Line to Line Output Voltage](Image)

![Graph 7: Fundamental (50Hz)](Image)
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11.5 ADVANCED MODEL OF THREE PHASE MATRIX CONVERTER USING DELTA-SIGMA MODULATION: A novel carrier-based modulation scheme is proposed which requires no sector information and look-up table to calculate duty ratios, with output voltage amplitude 0.866 times that of the input voltage and the input power factor controllable [13, 16-17]. This has already been explained under section 4.4 of Chapter IV. The advanced model of the MC using delta-sigma modulation technique is shown in Fig. 11.8. The Embedded MATLAB Function along with the min and max block generates the nine modulation duty-cycles as defined in equation 4.40 of Chapter IV. These nine modulation functions are applied as inputs to first order Delta-Sigma modulators as shown in Fig. 11.2. The combinational logic interface are designed as described in section 11.3 above. The principle of operation of the Delta-Sigma modulator is explained in Section 11.2.3 above. The nine gate pulses from the output of combinational logic circuit is applied to the respective gates of the bidirectional switches.

11.5.1 SIMULATION RESULTS: The simulation of the delta-sigma modulated MC shown in Fig. 11.8 was carried out using SIMULINK [51]. The simulation parameters are shown in Table 11.4.

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Input RMS Line to Neutral Voltage</td>
<td>220</td>
<td>Volts</td>
</tr>
<tr>
<td>2)</td>
<td>Input Frequency</td>
<td>50</td>
<td>Hz</td>
</tr>
<tr>
<td>3)</td>
<td>Output Frequency</td>
<td>50, 10</td>
<td>Hz</td>
</tr>
<tr>
<td>4)</td>
<td>Sampling Frequency</td>
<td>5</td>
<td>kHz</td>
</tr>
<tr>
<td>5)</td>
<td>Modulation Index k</td>
<td>0.26667</td>
<td>---</td>
</tr>
<tr>
<td>6)</td>
<td>RL Load</td>
<td>50, 20E-3</td>
<td>Ω, H</td>
</tr>
</tbody>
</table>

The ode15s(Stiff/NDF) solver was used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage and their respective oscilloscope waveforms for an output frequency of 50 Hz are shown in Fig. 11.9(A) to (D) and Fig. 11.10(A) to (D) respectively. The same harmonic spectrum and waveforms in the above order for an output frequency of 10 Hz are shown in Fig. 11.11(A) to (D) and Fig. 11.12(A) to (D) respectively. The simulation results are tabulated in Table 11.5.

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>Frequency Input-Output Hz</th>
<th>Line to Neutral Output voltage THD (p.u.)</th>
<th>Line to Line Output Voltage THD (p.u.)</th>
<th>Input current THD (p.u.)</th>
<th>Load current THD (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>50 – 50</td>
<td>0.8267</td>
<td>0.5823</td>
<td>0.5982</td>
<td>0.4626</td>
</tr>
<tr>
<td>2)</td>
<td>50 – 10</td>
<td>4.90</td>
<td>3.56</td>
<td>1.049</td>
<td>3.267</td>
</tr>
</tbody>
</table>

11.6 THREE PHASE INDUCTION MOTOR LOAD: A three phase cage Induction motor is used as load to the Venturini model and also the advanced model of MC using delta-sigma modulation. The parameters of the cage I.M. rated 4 kW, 400 Volts, Three Phase, 50 Hz, 4 poles, 1430 r.p.m. are given in Table 11.6 [51]. The Venturini model of the Delta-Sigma modulated MC driving the three phase IM is shown Fig. 11.13. The R-L load in the model shown in Fig. 11.3 is disconnected and a three phase cage IM whose parameters are in Table 11.6 is connected as load. The simulation results of stator currents, rotor speed and e.m. torque of the three phase IM as load is shown in Fig. 11.14 for zero external mechanical load.
FIG. 11.8 MODEL OF DELTA-SIGMA MODULATED THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING ADVANCED MODULATION ALGORITHM
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FIG. 11.15 MODEL OF DELTA-SIGMA MODULATED THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING ADVANCED MODULATION ALGORITHM DRIVING THREE PHASE INDUCTION MOTOR.
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TABLE 11.6: PH3 IM Parameters

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
<th>Sl.No.</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Stator Resistance Rs</td>
<td>1.405</td>
<td>Ohms</td>
<td>5)</td>
<td>Mutual Inductance Llm</td>
<td>0.1722</td>
<td>H</td>
</tr>
<tr>
<td>2)</td>
<td>Rotor Resistance Rr’</td>
<td>1.395</td>
<td>Ohms</td>
<td>6)</td>
<td>Rotor Inertia</td>
<td>0.0131</td>
<td>Kg-m^2</td>
</tr>
<tr>
<td>3)</td>
<td>Stator Leakage Inductance Lls</td>
<td>0.005839</td>
<td>H</td>
<td>7)</td>
<td>Damping constant</td>
<td>0.002985</td>
<td>N.m.s</td>
</tr>
<tr>
<td>4)</td>
<td>Rotor Leakage Inductance Llr’</td>
<td>0.005839</td>
<td>H</td>
<td>8)</td>
<td>No. of Poles</td>
<td>4</td>
<td>---</td>
</tr>
</tbody>
</table>

The Advanced model of the Delta-Sigma modulated MC driving the three phase IM is shown Fig. 11.15. The R-L load in the model shown in Fig. 11.8 is disconnected and a three phase cage IM whose parameters are in Table 11.6 is connected as load. The simulation results of stator currents, rotor speed and e.m. torque of the three phase IM as load is shown in Fig. 11.16 for zero external mechanical load.

11.7 DISCUSSION OF RESULTS: Comparison of the simulation results for the harmonic spectrum of line to neutral and line output voltages as well as for input and load currents for the venturini model of MC using delta-sigma modulation with that of carrier based modulation given in Chapter III indicates the absence harmonic voltage components at integral multiples of sampling frequency. Similar comparison of the harmonic spectrum for the above values for advanced model of MC using delta-sigma modulation with that of carrier based modulation given in chapter IV indicates the absence of harmonic voltage components at integral multiples of sampling frequency. The proposed method suppress noise peaks in the output voltage and is found to be suitable for clearing noise regulation. As for the simulation results of three phase IM, it is seen that in both cases the stator starting current is high and finally settles to the no load value. Similarly the e.m. torque in both cases are initially high and finally settles to zero corresponding to the externally applied mechanical load. As for the rotor speed, it is seen that in both cases the rotor reaches close to the no load speed of 1430 r.p.m. which is 149.6 mech.rad per second. However the rate of rise of rotor speed is slow for the advanced model as compared to the Venturini model.

11.8 CONCLUSIONS: A method of modeling MC using delta-sigma modulation technique is presented. Comparison of the THD of line to neutral and line output voltages indicates that for a 50 Hz output frequency, the advanced model has low THD compared to Venturini model both with delta-sigma modulation. However with 10 Hz output frequency, the above results are just reversed. The absence of harmonic components of voltages at integral multiples of sampling frequency responsible for noise peak is worth noting. For the input current advanced model gives lower THD compared to Venturini model with delta-sigma modulation. The proposed method suppress noise peaks in the output voltage and is found to be suitable for clearing noise regulation. As for three phase IM performance. It is seen that with both Venturini and advanced model, the rotor reaches rated no load speed with zero external load, the rate of rise of speed being faster for the former as compared to the later model. !
Chapter XII

Single Phase AC to Three Phase AC Matrix Converter

12.1 INTRODUCTION: For single phase AC to three phase AC power conversion, three phase indirect method is used where the single phase AC is first rectified to DC and this DC link voltage is inverted to AC using three phase inverter. A control and designing method of the capacitance of the compensation capacitor for a direct single phase AC to three phase AC matrix converters with application to a variable speed induction motor is reported in the literature [50]. The amplitude of the compensation capacitor voltage is controlled to absorb the single phase power fluctuation along with the load power. A method is proposed to decide the input side parameters such as the capacitance of the compensation capacitor, considering the input voltage and the power of the IM [50]. A circuit configuration with a compensation capacitor in the input side is introduced which absorbs the fluctuating power due to the single phase AC power. Here the single phase AC source is connected to an LC filter and compensating capacitor [50]. The two nodes of the LC filter and the compensating capacitor end terminals are connected to nine bidirectional switches [50]. Indirect virtual rectifier-inverter analysis is used. Derivations for modulation ratio and output power flow are presented [50]. A method of designing and selecting the compensating capacitor is given in terms of the output phase voltage, output power flow and input frequency [50]. In this chapter a detailed analysis of the single phase AC to three phase AC MC is presented. A model of this single phase AC to three phase AC MC is developed in SIMULINK [51]. Simulation results of the single phase AC to three phase AC MC is presented for both R-L load and three phase IM load.

12.2 ANALYSIS OF SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER:
The single phase AC to three phase AC MC is shown in Fig. 12.1. Here the junction of the input filter inductor and capacitor is connected to input phase A, the junction of the input filter capacitor and compensation capacitor is connected to input phase B and the end of the compensation capacitor is connected to input phase C of the 3 X 3 MC consisting of nine bidirectional switches [50]. The
equivalent circuit of Fig. 12.1 is shown in Fig. 12.2 which is a virtual indirect three phase rectifier-inverter circuit [50]. The relationship between switches of Fig. 12.1 and Fig. 12.2 is given by equation 9.1 in chapter IX. The following analysis for the design of compensation capacitor $C_C$ is based on reference 50.

12.2.1 CONTROL OF VIRTUAL RECTIFIER: The rectifier stage in Fig. 12.2 is a Current Source Converter (CSC). Referring to Fig. 12.2, the input voltage is expressed below:

\[
v_S = \sqrt{2} V_S \sin(\omega_i t) \quad (12.1)
\]

\[
V_s = \text{RMS value of input voltage}
\]

Assuming unity input power factor, the reference input current $i_S^*$ is given below:

\[
i_S^* = \sqrt{2} I_S \sin(\omega_i t) \quad (12.2)
\]

\[
I_S = \text{RMS value of input current}
\]

Modulation signal $m_S$ for the switch $S_1$ and $S_2$ in Fig. 12.2 is given below:

\[
m_S = M_S \sin(\omega_i t) \quad (12.3)
\]

\[
M_S = \text{Modulation ratio of modulation signal } m_S
\]

The fundamental component of the current $i_{pf}$ of current $i_p$ in Fig. 12.2 is given below:

\[
i_{pf} = M_S i_d \sin(\omega_i t) \quad (12.4)
\]

\[
i_d = \text{DC Link Current}
\]

When the current $i_{pf} = i_S^*$, we have the following equation by equating equation 12.2 and 12.3:

\[
I_S = \frac{M_S i_d}{\sqrt{2}} \quad (12.5)
\]

Input power $p_i$ is obtained by multiplying equations 12.1 and 12.2 which is given below:

\[
p_i = 2 V_S I_S \sin^2(\omega_i t)
\]

\[
= V_S I_S - V_S I_S \cos(2 \omega_i t) \quad (12.6)
\]

Compensating capacitor current reference $i_{CC}^*$ is gen below:

\[
i_{CC}^* = \sqrt{2} I_{CC} \sin\left(\omega_i t + \frac{\pi}{4}\right) \quad (12.7)
\]

\[
I_{CC} = \text{RMS value of compensating capacitor current}
\]

A modulation signal $m_C$ for switches $S_5$ and $S_6$ in Fig. 12.2 to control $i_{CC}$ is given below:

\[
m_C = M_C \sin\left(\omega_i t + \frac{\pi}{4}\right) \quad (12.8)
\]

\[
M_C = \text{Modulation ratio of modulation signal } m_C
\]

Fundamental frequency component of compensation capacitor current $i_{CC}$ is given below:
\[ i_{CC} = M_C \cdot i_d \cdot \sin \left( \alpha_i t + \frac{\pi}{4} \right) \quad (12.9) \]

\[ i_d = DC \quad Link \quad Current \]

Compensation capacitor voltage \( v_{CC} \) is given below:

\[ v_{CC} = \frac{1}{C_C} \left( \int i_{CC}^* \cdot dt \right) = -\frac{M_C \cdot i_d^* \cdot \cos \left( \alpha_i t + \frac{\pi}{4} \right)}{\omega_i \cdot C_C} \quad (12.10) \]

\[ i_d = DC \quad Link \quad Current \]

Power input to compensating capacitor is obtained by multiplying equation 12.9 with 12.10 which is given below:

\[ P_C = -\frac{M_C^2 \cdot i_d^2 \cdot \sin \left( \alpha_i t + \frac{\pi}{4} \right) \cdot \cos \left( \alpha_i t + \frac{\pi}{4} \right)}{\omega_i \cdot C_C} \]

\[ = -\frac{M_C^2 \cdot i_d^2}{2 \cdot \omega_i \cdot C_C} \cdot \cos \left( 2 \cdot \alpha_i t \right) \quad (12.11) \]

When the fluctuating power is compensated, then the second term on the R.H.S. of equation 12.6 equal to equation 12.11. Thus equating second term of equation 12.6 with equation 12.11 and using equation 12.5 for the value of \( I_S \), we have the following equation for \( M_C \):

\[ V_S \cdot I_S \cdot \cos \left( 2 \cdot \alpha_i t \right) = \frac{M_C^2 \cdot i_d^2}{2 \cdot \omega_i \cdot C_C} \cdot \cos \left( 2 \cdot \alpha_i t \right) \]

\[ V_S \cdot I_S = \frac{M_C^2 \cdot i_d^2}{2 \cdot \omega_i \cdot C_C} \]

\[ V_S \cdot M_S \cdot i_d = \frac{M_C^2 \cdot i_d^2}{2 \cdot \omega_i \cdot C_C} \]

\[ M_C = \sqrt{\frac{2 \cdot \omega_i \cdot C_C \cdot M_S \cdot V_S}{i_d}} \quad (12.12) \]

12.2.2 CONTROL OF VIRTUAL INVERTER: Referring to Fig. 12.2, when any one of switch S1, S3 and S5 of the virtual rectifier is ON, the p rail of DC link is \(+V_{T\text{max}}\) and when any one of switch S2, S4 and S6 is ON, the n rail of DC link is \(-V_{T\text{max}}\) where \( V_T \) is the RMS value of the output phase voltage of the virtual inverter in Fig. 12.2. Assume that the neutral of the load connected to the virtual inverter is grounded (NOT shown in Fig. 12.2). Then assuming that the modulation ratio of the switches of the virtual inverter is \( M_T \), with reference the neutral ground of the load connected to the virtual inverter, inverter output phase voltage can be expressed as follows:

\[ \left[ +V_{T\text{max}} - \left( -V_{T\text{max}} \right) \right] = V_{dc} \cdot M_T \]

\[ V_{\text{rms}} = V_T = \frac{V_{dc} \cdot M_T}{2 \cdot \sqrt{2}} \quad (12.13) \]
12.2.3 CALCULATION OF MODULATION RATIO: Balancing the input power and output power is required for the proper operation of the single phase AC to three phase AC MC. The virtual DC link voltage is obtained from equation 12.13, as given below:

\[ V_{dc} = \frac{2\sqrt{2} \cdot V_T}{M_T} \]  

(12.14)

The sum of the constant and fluctuating component of the virtual DC link voltage \( V_{dc} \) is given by multiplying equation 12.1 with equation 12.3, as given below:

\[
V_{dcf} = \sqrt{2} \cdot V_S \cdot \frac{M_S}{\sqrt{2}} \cdot \sin^2(\omega t)
= \left( \frac{V_S \cdot M_S}{\sqrt{2}} \right) \left( \frac{V_S \cdot M_S \cdot \cos(2\omega t)}{\sqrt{2}} \right) \]

(12.15)

When the fluctuating component of DC link voltage \( V_{dcf} \) is compensated fully, the second term on the R.H.S. of equation 12.15 is zero and under this circumstances, equating the first term of equation 12.15 with equation 12.14, the modulation ratio \( M_S \) of the switches S1 and S2 can be expressed as follows:

\[
M_S = \frac{4 \cdot V_T}{V_S \cdot M_T} \]  

(12.16)

If the single phase fluctuating input power is compensated, then the output power \( P_O \) is a constant and is equal to the virtual DC link voltage \( V_{dc} \) multiplied by the DC link current \( i_d \) of the rectifier. This is given below:

\[
P_O = V_{dc} \cdot i_d = \frac{2 \cdot \sqrt{2} \cdot V_T}{M_T} \cdot i_d
\]

\[ i_d = \frac{P_O \cdot M_T}{2 \cdot \sqrt{2} \cdot V_T} \]  

(12.17)

Using equations 12.16 and 12.17 in equation 12.12, the modulation ratio \( M_C \) can be expressed as follows:

\[
M_C = \sqrt{\frac{\sqrt{2} \cdot \omega_i \cdot C_S \cdot 4 \cdot V_T \cdot V_S \cdot 2 \cdot \sqrt{2} \cdot V_T}{P_O \cdot M_T \cdot V_S \cdot M_T}}
= \sqrt{\frac{16 \cdot \omega_i \cdot C_S \cdot V_T^2}{P_O \cdot M_T^2}} \]  

(12.18)

The modulation ratio \( M_C \) of the switches S5 and S6 is a function of output power \( P_O \) and the virtual inverter output phase voltage \( V_T \). The DC link voltage \( V_{dc} \), is proportional to the ratio of \( V_T \) to \( M_T \).
The RMS compensation capacitor voltage $V_{CC}$ is dependent on output power $P_O$. By designating RMS output phase voltage of the virtual inverter as $V_T^*$, the three phase reference output voltage of the inverter for an output frequency of $\omega_O$ can be expressed as follows:

$$
\begin{align*}
    v_a^* &= \sqrt{2} V_T^* \sin(\omega_O t) \\
    v_b^* &= \sqrt{2} V_T^* \sin\left(\omega_O t - \frac{2\pi}{3}\right) \\
    v_c^* &= \sqrt{2} V_T^* \sin\left(\omega_O t - \frac{4\pi}{3}\right)
\end{align*}
$$

(12.19)

The output power $P_O$ is calculated as follows:

$$
P_O = v_a^* i_a + v_b^* i_b + v_c^* i_c
$$

(12.20)

The modulation function $M_S$ is calculated by substituting $V_T^*$ to $V_T$ in equation 12.16 and $M_C$ is calculated by using equations 12.18 and substituting $P_O$ from equation 12.20. All modulation ratios $M_S$, $M_C$ and $M_T$ lie in the range 0 to 1.

12.3 DESIGN OF COMPENSATION CAPACITOR: The capacitance of the compensating capacitor $C_C$ is an important factor for the proper operation of single phase AC to three phase AC MC. The compensating power in the compensation capacitor is dependent on output power and the output voltage of MC is restricted by the compensation capacitor voltage. The compensation capacitor $C_C$ decides the characteristics of the output power versus output phase voltage in a single phase to three phase MC. The compensation capacitor $C_C$ is designed based on the relation between output power $P_O$ and the output phase voltage $V_T$ of the single phase to three phase MC with IM load to drive inertial load at constant acceleration. The maximum value of input phase voltage for the IM $V_{Tmax}$ is decided by the maximum values of modulation ratios $M_C$ and $M_T$ given by equation 12.18. Output power $P_O$ is determined by motor torque $T_{em}$ and rotor angular speed $\omega_{re}$. Using IM parameters and the IM RMS input phase voltage reference $V_T^*$, the IM torque $T_{em}$ can be calculated. Using this $T_{em}$ and rotor inertia $J$ and damping constant $B$, the theoretical rotor speed $\omega_{ret}$ can be calculated.

Using RMS input voltage reference to the IM, the compensation capacitor $C_C$ can be calculated using equation 12.18, where $M_C$ and $M_T$ are given the maximum value unity. Thus $C_C$ and $V_T^*$ and $V_{Tmax}$ are related as follows:

$$
V_T^* \leq V_{Tmax} = \frac{1}{4} \sqrt{\frac{P_O}{\omega_i \cdot C_C}}
$$

(12.21)

$$
C_C \leq \frac{P_O}{16 \cdot V_T^* \cdot \omega_i}
$$

(12.22)

Using equations 12.10, 12.17 and 12.21 and for the maximum value of $M_C$ and $M_T$, the RMS value of the compensation capacitor voltage $V_{CC}$ can be expressed as follows:
Chapter XII: Single Phase AC to Three Phase AC Matrix Converter

\[ V_{CC} = \sqrt{\frac{P_O}{\omega i * C_C}} \quad (12.23) \]

From equation 12.23 and 12.21, it is clear that the RMS value of the compensation capacitor voltage \( V_{CC} \) is four times greater than the maximum output phase voltage \( V_{T_{max}} \).

12.4 MODEL DEVELOPMENT: The model of the Single phase AC to three phase AC MC fed IM drive was developed in SIMULINK [51]. The parameter of the three phase IM rated 4 kW, 400 V, 50 Hz, 4 poles, 1430 rpm is shown in Table 12.1.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Stator Resistance Rs</td>
<td>1.405</td>
<td>Ohms</td>
</tr>
<tr>
<td>2</td>
<td>Rotor Resistance Rr'</td>
<td>1.395</td>
<td>Ohms</td>
</tr>
<tr>
<td>3</td>
<td>Stator Leakage Inductance Lls</td>
<td>0.005839</td>
<td>H</td>
</tr>
<tr>
<td>4</td>
<td>Rotor Leakage Inductance Llr'</td>
<td>0.005839</td>
<td>H</td>
</tr>
<tr>
<td>5</td>
<td>Mutual Inductance Lm</td>
<td>0.1722</td>
<td>H</td>
</tr>
<tr>
<td>6</td>
<td>Rotor Inertia</td>
<td>0.0131</td>
<td>Kg-m^2</td>
</tr>
<tr>
<td>7</td>
<td>Damping constant</td>
<td>0.002985</td>
<td>N.m.s</td>
</tr>
</tbody>
</table>

**FIG. 12.3 THREE PHASE INDUCTION MOTOR UNDER NO LOAD TEST**
To design the compensating capacitor value, the three phase IM was first driven on no load at rated input voltage. The model of the three phase IM and its no load characteristics are shown in Fig. 12.3 and Fig. 12.4(A) and (B) respectively. From Fig. 12.4(A) it is seen that the time taken by the three phase IM to reach a no load speed of 149.67 mech.rad. per second which corresponds to a frequency slightly less than 50 Hz is 25 milliseconds. For this time of 25 milliseconds it is seen that from Fig. 12.4 (B) the RMS value of terminal voltage per phase rises to 230 Volts. Thus a $V_T^*$ of 230 Volts is assumed and the given output power $P_O$ is 1333.33 Watts. Using equation 12.22, the value of the Compensating capacitor $C_C$ is found to be 5.017E-6 Farads. The input filter inductor $L_f$ and filter capacitor $C_f$ are taken to be 1E-3 H and 8E-6 Farads respectively.

12.4.1 MODEL OF SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER FED INDUCTION MOTOR DRIVE: The model of the single phase AC to three phase AC MC driving the IM is shown in Fig. 12.5. Here the gate pulses for the nine bidirectional switches are generated using Venturini modulation algorithm assuming unity input phase displacement factor given by equation 3.17 in section 3.3 of chapter III. This algorithm is also proved to be valid for three phase sine wave input voltages as given in A3.3 Appendix of Chapter III. In this model a saw-tooth carrier frequency of 10 kHz is used. The single phase AC input voltage source has an RMS value of 231 Volts and frequency 50 Hz. Two Embedded MATLAB Function blocks are used to generate the gate pulses. The method of generating this gate pulses and the source code used are already explained in Section 3.4.1 of Chapter III. The gate pulses drive the nine bidirectional switches of the MC.

12.4.2 SIMULATION RESULTS: The simulation of the single phase AC to three phase AC MC driving the IM is carried out in SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation parameters are given in Table 12.2 below. An output R-L-C filter to resonate at 10 kHz carrier switching frequency is used. The simulation results for the three phase 50 Hz line to line output voltage is shown in Fig. 12.6(A) and the stator current, rotor speed and electromagnetic torque of the three phase IM are shown in Fig. 12.6(B), for zero externally applied mechanical load.
FIG. 12.5: MODEL OF SINGLE PHASE AC TO THREE PHASE AC TO MATRIX CONVERTER FED I.M. DRIVE
TABLE 12.2: PH1 AC to PH3 AC MC Model Parameters

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
<th>Sl.No</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Single Phase RMS Line to Ground Input Voltage $V_s$</td>
<td>231</td>
<td>V</td>
<td>5</td>
<td>Modulation Index</td>
<td>0.5</td>
<td>--</td>
</tr>
<tr>
<td>2</td>
<td>Input Frequency $f_i$</td>
<td>50</td>
<td>Hz</td>
<td>6</td>
<td>Compensation capacitor</td>
<td>5.017E-6</td>
<td>F</td>
</tr>
<tr>
<td>3</td>
<td>Output Frequency $f_o$</td>
<td>50</td>
<td>Hz</td>
<td>7</td>
<td>Input Filter Inductor</td>
<td>1E-3</td>
<td>H</td>
</tr>
<tr>
<td>4</td>
<td>Saw-tooth Carrier Frequency $f_{sw}$</td>
<td>10</td>
<td>kHz</td>
<td>8</td>
<td>Input Filter Capacitor</td>
<td>8E-6</td>
<td>F</td>
</tr>
</tbody>
</table>

12.4.3 MODEL OF SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER:
The model of the single phase AC to three phase AC MC connected to an R-L load is shown in Fig. 12.7. The model is already explained under section 12.4.1 above.

12.4.4 SIMULATION RESULTS:  The simulation of the single phase AC to three phase AC MC
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NARAYANASWAMY. P.R. IYER
RESEARCH CANDIDATE
DEPT. OF ECE
CURTIN UNIVERSITY OF TECHNOLOGY
PERTH, WA - 6845
AUSTRALIA.

FIG. 12.7: MODEL OF SINGLE PHASE AC TO THREE PHASE AC TO MATRIX CONVERTER FED I.M. DRIVE
The simulation parameters used are the same as in Table 12.2 above. The R-L load used is 50 Ω and 0.5 Henries. An output R-L-C filter to resonate at 10 kHz carrier switching frequency is used. The simulation results for the three phase line to line output voltage and load current for 50 Hz and 20 Hz output frequencies are shown in Fig. 12.8(A) and Fig. 12.8(B) respectively.

12.5 DISCUSSION OF RESULTS: The simulation results for the case of three phase I.M. load shows unbalanced output voltage and load current. The speed pick up for the I.M. is very slow. As for static R-L load also unbalanced output voltages and load current are observed.

12.6 CONCLUSIONS: The model of a new technique for single phase AC to three phase AC MC is presented. Simulation results for three phase IM as well as for static R-L load shows conversion of single phase AC voltage to three phase AC voltage at the same frequency as the input or a different frequency. However the three phase output voltages and load current are found to be unbalanced by model simulation.
Chapter XIII

A Novel AC To AC Converter Using A DC Link

13.1 INTRODUCTION: A novel method of generating a Pulse Width Modulated single phase and three phase variable frequency, variable voltage AC from the normal 220 Volts/440 Volts, single phase/three phase 50 Hz AC supply mains using a step down transformer and an intermediate DC link is presented here.

13.2 SINGLE PHASE AC TO SINGLE PHASE AC CONVERTER USING A DC LINK: The block diagram of the single phase AC to single phase AC converter is shown in Fig. 13.1. The block diagram is explained below:

- The supply mains is a 220 Volts, 50 Hz AC.
- The step down transformer 230/6 V is connected to the supply mains.
- The secondary 6 V is connected to the op.amplifier zero crossing comparator.
- The output of the zero crossing comparator forms the gate drive input to all the four MOSFET switches forming the bipolar dual output inverter.
- The bipolar dual output inverter consists of two legs. Each leg is a pair of N and P type MOSFETs connected in series. The two parallel legs of the inverter are connected to the DC source which forms the DC link. The two outputs of this inverter are V/0 and V/-180 with a frequency of 50 Hz, where 2V is the DC link voltage. These two outputs are fed to the two IGBT bidirectional switches.
The four gates of the two IGBT bidirectional switches are cross connected. This is different from the mode of connection used in conventional matrix converter. The output of this bidirectional switches is connected to the load.

The clock generator output is a square pulse having a frequency of $f_o$ Hz with 50% duty cycle. This frequency $f_o$ Hz is variable.

The carrier generator output is a square pulse having a pre-calculated fixed frequency of $f_c$ Hz with a variable duty-cycle. The carrier frequency $f_c$ Hz must be at least two times greater than the desired output frequency of $f_o$ Hz.

The load voltage $V_o$ is a Pulse Width Modulated square wave AC with a peak to peak value of 2V Volts and frequency $f_o$ Hz.

By varying the duty-cycle of the square pulse carrier generator, the magnitude of the output voltage $V_o$ can be controlled.

13.3 MODEL OF A PWM SINGLE PHASE AC TO SINGLE PHASE AC CONVERTER: The schematic of the novel PWM Single phase AC to single phase AC converter is shown in Fig. 13.2.

![Schematic of the novel PWM Single phase AC to single phase AC converter](image)

**FIG. 13.2 A NOVEL PWM SINGLE PHASE AC SINGLE PHASE AC CONVERTER**

The 230 Volts, 50 Hz single phase AC supply is stepped down to 6 Volts and given as input to the non-inverting input of op.amp. zero crossing comparator. The MOSFETs M1 and M2 are N and P MOSFET pair and so is the case with M3 and M4. This zero crossing comparator drives the four MOSFET switches M1 to M4 to produce bipolar dual output voltages which are given as inputs to four IGBT switches Q1 to Q4. The opto isolation circuit is NOT shown in Fig.13.2 due to simulation difficulty in PSIM9. The 10Hz ($f_o$ Hz) square pulse with 50% duty-cycle and its inverted output pulse are ANDeD using a 10 kHz ($f_c$ Hz) modulating square wave voltage signal with variable duty-cycle which drives the four bidirectional IGBT switches Q1 to Q4 as shown in Fig. 13.2, whose variable voltage output having frequency $f_o$ Hz is given to the load. By changing the frequency $f_o$ of the square pulse generator the frequency of output voltage can be controlled. The modulating signal frequency $f_c$ Hz must be at least twice greater than the desired output frequency $f_o$ Hz. The detailed principle of operation of the above converter is shown in Appendix A13.1
13.4 RMS OUTPUT VOLTAGE: A typical output voltage waveform of the above converter is shown in Fig. 13.3 below. This is uniform pulse width modulation. Let $D_C$ be the duty cycle of the square pulse carrier and $T_C = 1/f_C$ be its period. Let $T_0 = 1/f_o$ be the period of the output voltage waveform. Let $V$ be the peak value of the output PWM voltage waveform. The following derivation for RMS output voltage waveform holds good:

Number of PWM square pulses for one half cycle of the PWM output voltage $n_p = \frac{T_o}{2T_C}$ (13.1)

Let $V_{rms}$ be the RMS value of the output voltage and $T_1$ be the time of starting of the first pulse measured from the origin.

$$V_{rms}^2 = \frac{2 \times n_p}{T_0} \left[ \int_{T_1}^{T_1+D_CT_C} V^2 \, dt \right]$$

(13.2)

$$V_{rms} = V \times \sqrt{\frac{2n_pD_CT_C}{T_0}}$$

(13.3)

$$V_{rms} = V \times \sqrt{2n_pD_CT_C/T_0}$$

(13.4)

Equations 13.4 and 13.5 gives the RMS value of the PWM output voltage waveform.

13.5 SIMULATION RESULTS: To verify the performance of the proposed single phase PWM AC to single phase AC converter, a model of this was developed in PSIM9, as shown in Fig. 13.2. The DC link voltage is 100 Volts. The carrier frequency is 10 kHz. The clock generator frequency is 1 kHz with 50 % duty cycle. The duty cycle for the carrier generator was initially set to 0.8. The simulation results are shown in Fig. 13.4(A) to (G ). The duty cycle of the carrier generator was then set to 0.5 and the simulation results are shown in Fig. 13.5(A) to Fig. 13.5(G ). The simulation results with the duty cycle of the carrier generator set to 0.2 are shown in Fig. 13.6(A) to Fig. 13.6(G). To study the output frequency variation capability, the simulation of the above converter was carried out for a $f_o$ value of 10 Hz. The clock frequency was set to 10 Hz with a duty cycle of 50 %. The carrier frequency was chosen to be 1 kHz. The duty cycles of the carrier generator used for simulation were 0.8, 0.5 and 0.2 respectively. The simulation results for these three values of duty cycles are shown above in Fig. 13.7(A) to Fig. 13.7(G), Fig. 13.8(A) to Fig. 13.8(G) and Fig. 13.9(A) to Fig. 13.9(G) respectively.
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FIG. 13.4 (A)

FIG. 13.4 (B)

FIG. 13.4 (C)

FIG. 13.4 (D)

FIG. 13.4 (E)

FIG. 13.4 (F)
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FIG. 13.4(G)

FIG. 13.5(A)

FIG. 13.5(B)

FIG. 13.5(C)

FIG. 13.5(D)
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FIG. 13.6(C)

FIG. 13.6(D)

FIG. 13.6(E)

FIG. 13.6(F)

FIG. 13.6(G)
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13.6 DISCUSSION OF RESULTS: From the simulation results it is seen that a variable frequency Pulse Width Modulated variable voltage output is obtained at the load terminal from a constant 50 Hz frequency AC input voltage. The variable frequency at the load terminal is obtained by selecting the appropriate clock frequency to drive the IGBT bidirectional switches. The variable voltage magnitude at the load terminal is obtained by varying the duty-cycle of the carrier switching frequency.

13.7 THREE PHASE AC TO THREE PHASE AC CONVERTER USING A DC LINK: The block diagram of the Three Phase fixed supply frequency AC to Three Phase variable frequency AC converter using an intermediate DC link is shown in Fig.13.10. The block diagram is explained below:
• The supply mains is a 220 Volts (Line to Neutral), 50 Hz Three Phase AC.
• The step down transformer 230/6 V is connected to each phase of the supply mains.
• The secondary 6 V of each phase is connected to op. amplifier zero crossing comparator.
• The output of the zero crossing comparator forms the gate drive input to all the four MOSFET switches forming the bipolar dual output inverter in each phase.
• The bipolar dual output inverter in each phase consists of two legs. Each leg is a pair of N and P type MOSFETs connected in series. The two parallel legs of the inverter are connected to the DC source which forms the DC link. The two outputs of this inverter in each phase are $VA=V/\_0$, $VA=V/\_-180$, $VB=V/\_-120$, $VB=V/\_-300$ and $VC=V/\_-240$, $VC=V/\_-420$ with a frequency of 50 Hz, where $2V$ is the DC link voltage. These two outputs of inverter in each phase are fed to the IGBT bidirectional switches corresponding to each output phase.
• There are two IGBT bidirectional switches in each output phase. The four gates of the two IGBT bidirectional switches in each output phase are cross connected. This is different from the mode of connection used in conventional matrix converter. The output of this bidirectional switches is connected to the three phase load.
• The three phase clock generator output is a square pulse for each phase having a frequency of $f_o$ Hz with 50 % duty cycle. The clock QA, QB and QC corresponding to each output phase are separated from each other by a phase difference of $T_o/3$ seconds, where $T_o = 1/f_o$. This frequency $f_o$ Hz is variable.
• The carrier generator output is a square pulse having a pre-calculated fixed frequency of $f_c$ Hz with a variable duty-cycle. The carrier frequency $f_c$ Hz must be at least two times more greater than the desired output frequency of $f_o$ Hz.
• The load voltage $V_o$ is a Pulse Width Modulated square wave AC with a peak to peak value of $2V$ Volts and frequency $f_o$ Hz.
• By varying the duty-cycle of the square pulse carrier generator, the magnitude of the output voltage $V_o$ can be controlled.

13.8 MODEL OF A PWM THREE PHASE AC TO THREE PHASE AC CONVERTER: The model schematic of the novel PWM Three Phase AC to three phase AC converter is shown in Fig. 13.11. One op.amp. zero crossing comparator (ZCC) for each input phase drives the four MOSFET switches corresponding to each input phase to produce bipolar dual output voltages which are respectively given to four IGBTs forming two bidirectional switches connected to each output phase. In Fig. 13.11, MOSFETs M1 and M2 and N and P type respectively. Similar is the case with M3-M4, M5-M6, M7-M8, M9-M10 and M11-M12 pair of MOSFETs. In Fig.13.11, the isolation transformers are not shown next to op.amp. ZCC due to simulation difficulty in PSIM9. The three phase square clock pulse with 50 % duty-cycle and frequency $f_o$ Hz is modulated using a variable duty-cycle square pulse carrier signal generator. Three phase clock and its inverted pulse are ANDe'd with square pulse carrier wave and these pair of gate pulses drive the two pairs of bidirectional IGBT switches corresponding to each output phase whose variable frequency variable three phase voltage output is given to the load. The gates of the IGBTs Q1-Q4, Q5-Q8 and Q9-Q12 are cross connected.
FIG. 13.11: A NOVEL PWM THREE PHASE AC TO THREE PHASE AC CONVERTER
The three phase clock of frequency \( f_0 \) Hz is developed here as given below:

A modulo six counter which counts from 0 to 5 in the continuous up sequence is developed using D flip-flop. The truth table for designing the modulo six counter using D flip-flops is shown in Table 13.1. For D flip-flops the next state is mapped to find the three control logic for the D input of C, B and A. The control logic for the D input of flip-flops A, B and C are derived using K-maps as shown in Fig. 13.12(a), (b) and (c). The clock input to this counter has a frequency of \( 6f_0 \), where \( f_0 \) Hz is the desired output frequency. The three bit output of the counter is decoded using three 8 line to 1 line Multiplexer. Each of these multiplexers give a logic HIGH output corresponding to the minimum terms \( \Sigma_m(0,1,2), \Sigma_m(2,3,4), \Sigma_m(4,5,0) \). The output of these MUX and their corresponding inverted output drives the four bidirectional switches in each of the three output phase. Another method of switching the gates of IGBTs Q1-Q12 using PIC16F84A microcontroller is given in Appendix I.

### Table 13.1: D-Flip-flop Truth Table

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>C</th>
<th>B</th>
<th>A</th>
<th>C</th>
<th>B</th>
<th>A</th>
</tr>
</thead>
<tbody>
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<td>1</td>
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<td>0</td>
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<td>0</td>
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</tr>
<tr>
<td>6</td>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

A input map. \( D_A = /A \) (A)

B input map. \( D_B = /C.B.A + B./A \) (B)

C input map. \( D_C = /C.\bar{A} + B.A \) (C)

**FIG. 13.12: K_Map for Modulo Six Counter**

#### 13.9 SIMULATION RESULTS:
To verify the performance of the proposed PWM three phase AC to three phase AC converter, a model of this was developed in PSIM9, as shown in Fig. 13.11. The DC link voltage is 100 Volts. The carrier frequency is 10 kHz. The clock frequency was set to 6 kHz so that frequency of the square pulse used for driving the bidirectional switches is 1 kHz with 50% duty-cycle. The output frequency is 1 kHz. The duty cycle for the carrier generator was initially set to 0.2. The simulation results are shown in Fig. 13.13(A) to (C) and Fig. 13.14(A) to (C) for the three phase line to neutral and line to line output voltages respectively. The duty cycle of the carrier generator was then set to 0.8 and the simulation results in the above order are shown in Fig. 13.15(A) to (C) and Fig. 13.16(A) to (C). To study the output frequency variation capability, the simulation of the above converter was carried out for an output frequency value of 10 Hz. The clock frequency was set to 60 Hz, so that the frequency of the square pulse driving the bidirectional switches is 10 Hz with 50% duty-cycle. The carrier frequency was chosen to be 1 kHz with variable duty-cycle. The duty cycles of the carrier generator used for simulation were 0.2 and 0.8 respectively. The simulation
results for these two values of duty cycles in the above order are shown above in Fig. 13.17(A) to (C), Fig. 13.18(A) to (C) Fig. 13.19(A) to (C) and Fig. 13.20(A) to (C) respectively.

13.10 DISCUSSION OF RESULTS: From the simulation results it is seen that a variable frequency Pulse Width Modulated Three Phase variable voltage output is obtained at the load terminal from a constant 50 Hz frequency Three Phase AC input. The variable frequency at the load terminal is obtained by selecting the appropriate clock frequency to drive the IGBT bidirectional switches. The variable voltage magnitude at the load terminal is obtained by varying the duty-cycle of the carrier square wave switching pulse.

Both the single phase AC to single phase AC and the three phase AC to three phase AC converter presented above converts the fixed supply frequency AC voltage to variable frequency AC output voltage. This is a new method in the sense the topology of connecting the IGBT bidirectional switches and its gate connections are much different from the conventional matrix converter. The above topology presents a new method of obtaining variable frequency AC output voltage from a supply frequency input voltage. The gate drive can be easily implemented using analog and digital ICs or microcontrollers whereas gate drive for conventional matrix converters require algorithms to be implemented in dSPACE or using Digital Signal Processors.

13.11 CONCLUSIONS: A novel method of generating a variable frequency variable single phase and variable Three Phase AC output voltage across the load from a single phase and three phase 50 Hz AC input voltage is presented. The PWM scheme used is well known. The topology of the DC to 50 Hz AC single phase and three phase dual inverter using N and P MOSFETs with 180 degree phase difference in the output voltage and the topology of the IGBT bidirectional switches and their gate connection of the single phase AC to single phase AC and Three Phase AC to Three Phase AC converter are new.

A13.1 APPENDIX: Referring to Fig. 13.2, the working of the dual MOSFET inverter using N and P MOSFETs in series is explained below:

The 220 Volts single phase 50 Hz sine wave AC input voltage and the 6V transformer secondary output voltage are shown in Fig. A13.1. During the positive half cycle of the transformer secondary input voltage, the output OA of the Op.Amplifier zero crossing comparator (ZCC) is driven to positive saturation and it is +10 V and during the negative half cycle of this input voltage, the ZCC output OA is driven to negative saturation and it is -10V. This is shown in Fig.A13.1. During the positive half cycle of the ZCC output OA, N MOSFETs M1 and M4 conducts, the output VA and VB with respect to DC link ground are respectively +Vdc/2 (+50 V) and –Vdc/2 (-50 V) respectively, where Vdc is the DC link voltage. Similarly during the negative half cycle of the ZCC output OA, P MOSFETs M2 and M3 conducts, the output VA and VB with respect to DC link ground are respectively -Vdc/2 (-50 V) and +Vdc/2 (+50 V) respectively. This is shown in Fig. A13.1.
Chapter XIII: A Novel AC to AC Converter Using A DC Link
Referring to Fig. 13.2, the working principle of the IGBT bidirectional switch inverter is given below:

Now consider that the period of the input voltage $VA$ and $VB$ is $T$ and that of the clock switching the IGBT bidirectional switches is $To$ with 50% duty-cycle. Assume that there is no carrier modulation involved. Referring to Fig. 13.2, the following analysis hold good:

**Case A:** Let $T \gg To$. Consider interval $0 < t \leq To/2$. Gate pulse for Q1 and Q4 are HIGH and that for Q2 and Q3 are LOW. Then the following argument is valid:
- Input voltage $VA$ is $+V_{dc}/2$ ($+50$ V) Volts and $VB$ is $-V_{dc}/2$ ($-50$ V) Volts.
- IGBT Q1 is ON and Q2, Q3 and Q4 are OFF.
- IGBT Q1 and the diode across Q2 conducts.
- Output voltage $V_{OUT}$ is $+V_{dc}/2$ ($+50$ V) Volts.

**Case B:** Let $T \gg To$. Consider interval $To/2 < t \leq To$. Gate pulse for Q2 and Q3 are HIGH and that for Q1 and Q4 are LOW. Then the following argument is valid:
- Input voltage $VA$ is $+V_{dc}/2$ ($+50$ V) Volts and $VB$ is $-V_{dc}/2$ ($-50$ V) Volts.
- IGBT Q3 is ON and Q1, Q2 and Q4 are OFF.
- IGBT Q3 and the diode across Q4 conducts.
- Output voltage $V_{OUT}$ is $-V_{dc}/2$ ($-50$ V) Volts.

**Case C:** Let $T \gg To$. Consider interval $0 < t \leq To/2$. Gate pulse for Q1 and Q4 are HIGH and that for Q2 and Q3 are LOW. Then the following argument is valid:
- Input voltage $VA$ is $-V_{dc}/2$ ($-50$ V) Volts and $VB$ is $+V_{dc}/2$ ($+50$ V) Volts.
- IGBT Q4 is ON and Q1, Q2 and Q3 are OFF.
- IGBT Q4 and the diode across Q3 conducts.
- Output voltage $V_{OUT}$ is $+V_{dc}/2$ ($+50$ V) Volts.

**Case D:** Let $T \gg To$. Consider interval $To/2 < t \leq To$. Gate pulse for Q2 and Q3 are HIGH and that for Q1 and Q4 are LOW. Then the following argument is valid:
- Input voltage $VA$ is $-V_{dc}/2$ ($-50$ V) Volts and $VB$ is $+V_{dc}/2$ ($+50$ V) Volts.
- IGBT Q2 is ON and Q1, Q3 and Q4 are OFF.
- IGBT Q2 and the diode across Q1 conducts.
- Output voltage $V_{OUT}$ is $-V_{dc}/2$ ($-50$ V) Volts.

Period of output voltage $V_{OUT}$ is $To$. Case A to D are shown in Fig. A13.2.

**Case E:** Let $T \ll To$. Consider interval $0 < t \leq To/2$. Gate pulse for Q1 and Q4 are HIGH and that for Q2 and Q3 are LOW. Then the following argument is valid:
- When $VA$ is $+V_{dc}/2$ ($+50$ V) Volts and $VB$ is $-V_{dc}/2$ ($-50$ V) Volts, IGBT Q1 and the diode across Q2 conducts. Output $V_{OUT}$ is $+V_{dc}/2$ ($+50$ V) Volts.
When VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts, IGBT Q4 and the diode across Q3 conducts. Output VOUT is +Vdc/2 (+50 V) Volts.

**Case F:** Let T << To. Consider interval To/2 < t <= To. Gate pulse for Q1 and Q4 are LOW and that for Q2 and Q3 are HIGH. Then the following argument is valid:
- When VA is +Vdc/2 (+50 V) Volts and VB is -Vdc/2 (-50 V) Volts, IGBT Q3 and the diode across Q4 conducts. Output VOUT is -Vdc/2 (-50 V) Volts.
- When VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts, IGBT Q2 and the diode across Q1 conducts. Output VOUT is -Vdc/2 (-50 V) Volts.

**Case G:** Let T << To. Consider interval 0 < t <= To/2. Gate pulse for Q1 and Q4 are LOW and that for Q2 and Q3 are HIGH. Then the following argument is valid:
- When VA is +Vdc/2 (+50 V) Volts and VB is -Vdc/2 (-50 V) Volts, IGBT Q3 and the diode across Q4 conducts. Output VOUT is -Vdc/2 (-50 V) Volts.
- When VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts, IGBT Q2 and the diode across Q1 conducts. Output VOUT is -Vdc/2 (-50 V) Volts.

**Case H:** Let T << To. Consider interval To/2 < t <= To. Gate pulse for Q1 and Q4 are HIGH and that for Q2 and Q3 are LOW. Then the following argument is valid:
- When VA is +Vdc/2 (+50 V) Volts and VB is -Vdc/2 (-50 V) Volts, IGBT Q1 and the diode across Q2 conducts. Output VOUT is +Vdc/2 (+50 V) Volts.
- When VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts, IGBT Q4 and the diode across Q3 conducts. Output VOUT is +Vdc/2 (+50 V) Volts.

The period of the output voltage VOUT is To. Case E to H are shown in Fig. A13.3.
Also Case A to H described above are diagrammatically shown in Fig. A13.4 (A), (B), (C) and (D).

![Diagram of bidirectional IGBT inverter conducting modes](image)

**FIG. A13.4: BIDIRECTIONAL IGBT INVERTER CONDUCTING MODES**

Fig. A13.4(A), (B), (C) and (D) respectively correspond to cases A, E and H; cases B, F and G; cases C, E and H; and cases D, F and G discussed in Appendix A13.1 above.

The same principle of operation holds good for the three phase AC to three phase AC Converter using a DC link discussed in section 13.7 above.
Chapter XIV

Verification of Models of Three Phase AC To Three Phase AC Matrix Converter

14.1 INTRODUCTION: This chapter provides the verification of models of selected three phase AC to three phase AC Matrix Converter (MC) topologies discussed in the previous chapters using either PSIM or PSCAD software [52-53].

14.2 MATRIX CONVERTER MODEL USING VENTURINI MODULATION ALGORITHM:
The model of a three phase AC to three phase AC MC using Venturini second method is discussed in Section 3.4.3 of Chapter III. The data given in Table 3.2 of Chapter III is used to solve the above problem using PSCAD [53]. Here equation 3.17 of Chapter III is used to generate the nine modulation functions for the bidirectional switches of the MC. The PSCAD model is shown in Fig. 14.1 and the simulation results are shown in Fig. 14.2. The simulation results are tabulated in Table 14.1.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Algorithm</th>
<th>THD of Line to Neutral Output Voltage (p.u.)</th>
<th>THD Line to Line Output Voltage (p.u.)</th>
<th>THD of Input Current (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Venturini Second Method</td>
<td>2.19</td>
<td>1.3896</td>
<td>2.331</td>
</tr>
</tbody>
</table>

14.3 MATRIX CONVERTER MODEL USING SUNTER-CLARE MODULATION ALGORITHM: The Sunter-Clare modulation algorithm is discussed in Section 4.2 of Chapter IV. The data given in Table 3.2 of Chapter III is used to develop the model of the three phase AC to three phase AC MC using Sunter-Clare modulation algorithm in PSCAD. This PSCAD model is shown in Fig. 14.3 and the simulation results are in Fig. 14.4. The simulation results are tabulated in Table 14.2.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Algorithm</th>
<th>THD of Line to Neutral Output Voltage (p.u.)</th>
<th>THD Line to Line Output Voltage (p.u.)</th>
<th>THD of Input Current (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Sunter-Clare</td>
<td>2.217</td>
<td>1.101</td>
<td>3.164</td>
</tr>
</tbody>
</table>

14.4 MODEL OF MATRIX CONVERTER USING NED MOHAN MODULATION ALGORITHM: The Ned Mohan modulation algorithm is discussed in Section 4.4 of Chapter IV. The data given in Table 3.2 of Chapter III is used to develop the model of the three phase AC to three phase AC MC using Ned Mohan modulation algorithm in PSCAD. The value of modulation index k is 0.26667. This PSCAD model is shown in Fig. 14.5 and the simulation results are in Fig. 14.6. The simulation results are tabulated in Table 14.3.
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter

FIG. 14.2  SIMULATION RESULTS FOR THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING VENTURINI ALGORITHM
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter

FIG. 14.3  MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING SUNTER-CLARE ALGORITHM
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FIG. 14.4  THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING SUNTER-CLARE ALGORITHM - SIMULATION RESULTS
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FIG. 14.6  THREE PHASE 50 Hz AC TO THREE PHASE 50 Hz AC MC USING NED MOHAN ALGORITHM - SIMULATION RESULTS
14.5 MODEL OF MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE: The development model for the multilevel matrix converter with three flying capacitors per output phase using Venturini modulation algorithm has already been discussed in Section 7.2 of Chapter VII. In this section the model of the three phase MMC with three FC is re-examined using PSIM9 software [52]. The PSIM model of the three phase MMC with three FC is shown in Fig. 14.7. The parameters are given in Table 7.3 of Chapter VII. The simulation results using PSIM9 are shown in Figs. 14.8(A) to 14.8(L). The simulation results are tabulated in Table 14.4.

In addition the line to neutral output voltage \(v_a\) of phase a and the Phase A input current \(i_A\) are theoretically calculated using equations 7.4 and 7.5 of Chapter VII. The relevant logic gates, multiplication and summing blocks to theoretically calculate \(v_a\) and \(i_A\) are shown in Fig. 14.7. This theoretical value and actual value by simulation are tabulated in Table 14.5.

14.6 MODEL OF MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE: Three phase AC to three phase AC MMC with six FC per output phase using Venturini algorithm is already discussed in Section 7.9 of Chapter VII. In this section the model of the three phase MMC with six FC per output phase is re-examined using PSIM9 software [52]. The PSIM model of the three phase MMC with six FC is shown in Fig. 14.9. The parameters are given in Table 7.3 of Chapter VII. The simulation results using PSIM9 are shown in Figs. 14.10(A) to 14.10(J). The simulation results are tabulated in Table 14.6.
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter

14.7 MODEL OF DUAL PROGRAMMABLE AC TO DC RECTIFIER: The principle of operation relating to the discovery of the dual programmable AC to DC rectifier and its modelling is discussed in Section 10.3 and 10.4 of Chapter X. In this chapter this model performance is re-examined using PSCAD [53]. The model of the dual programmable AC to DC rectifier is shown in Fig. 14.11. The simulation results for the above rectifier for various output voltage phase angle $\phi_o$ is shown in Fig. 14.12(A) to (N). The PSCAD simulation results are tabulated in Table 14.7.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Topology</th>
<th>Parameters</th>
<th>$\phi_o$ radians</th>
<th>$V_{o1}$ Volts</th>
<th>$V_{o2}$ Volts</th>
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<tr>
<td>1)</td>
<td>Three Phase MMC With SIX FC</td>
<td>Table 7.3</td>
<td>0</td>
<td>67.5</td>
<td>135</td>
</tr>
<tr>
<td>2)</td>
<td>+$\pi$/6</td>
<td>116.5</td>
<td>116.5</td>
<td>0</td>
<td>135</td>
</tr>
<tr>
<td>3)</td>
<td>+$\pi$/3</td>
<td>135</td>
<td>67.5</td>
<td>9</td>
<td>135</td>
</tr>
<tr>
<td>4)</td>
<td>+$\pi$/2</td>
<td>116.5</td>
<td>0</td>
<td>10</td>
<td>67.5</td>
</tr>
<tr>
<td>5)</td>
<td>+2$\pi$/3</td>
<td>67.5</td>
<td>-67.5</td>
<td>12</td>
<td>-67.5</td>
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<tr>
<td>6)</td>
<td>+3$\pi$/4</td>
<td>35</td>
<td>-95</td>
<td>13</td>
<td>-95</td>
</tr>
<tr>
<td>7)</td>
<td>+5$\pi$/6</td>
<td>0</td>
<td>-116.5</td>
<td>14</td>
<td>-116.5</td>
</tr>
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</table>

14.8 DELTA-SIGMA MODULATED MATRIX CONVERTER USING VENTURINI ALGORITHM: The model of three phase AC to three phase AC MC delta-sigma modulated using Venturini algorithm is already explained in Section 11.3 and 11.4 of Chapter XI. Here the model of the above MC is developed in PSIM[52]. This PSIM model of the above MC is shown in Fig. 14.13. The simulation parameters are shown in Table 11.2 of Chapter XI. The simulation results using PSIM are shown in Fig. 14.14(A) to 14.14(L) and in Fig. 14.15(A) to 14.15(L). The simulation results are also tabulated in Table 14.8.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Frequency Input-Output Hz</th>
<th>Line to Neutral Output Voltage THD (p.u.)</th>
<th>Line to Line Output Voltage THD (p.u.)</th>
<th>Input current THD (p.u.)</th>
<th>Load current THD (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>50 – 50</td>
<td>1.632</td>
<td>1.5129</td>
<td>6.522</td>
<td>0.392</td>
</tr>
<tr>
<td>2)</td>
<td>50 – 10</td>
<td>1.650</td>
<td>1.5123</td>
<td>6.959</td>
<td>2.788</td>
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</table>
FIG. 14.7 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
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FIG. 14.9 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH SIX FC
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
14.9 DELTA-SIGMA MODULATED MATRIX CONVERTER USING ADVANCED MODULATION ALGORITHM: A novel carrier-based modulation scheme is proposed which requires no sector information and look-up table to calculate duty ratios, with output voltage amplitude 0.866 times that of the input voltage and the input power factor controllable [13, 16-17]. This has already been explained under Section 4.4 of Chapter IV. The model of three phase AC to three phase AC MC delta-sigma modulated using Ned Mohan algorithm is already explained in Section 11.5 and 11.6 of Chapter XI. Here the model of the above MC is developed in PSIM9[52]. This PSIM model of the above MC is shown in Fig. 14.16. The simulation parameters are shown in Table 11.4 of Chapter XI. The simulation results using PSIM are shown in Fig. 14.17(A) to 14.17(L) and Fig. 14.18(A) to 14.18(L). The simulation results are also tabulated in Table 14.9.

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Frequency Input-Output Hz</th>
<th>Line to Neutral Output Voltage THD (p.u.)</th>
<th>Line to Line Output Voltage THD (p.u.)</th>
<th>Input current THD (p.u.)</th>
<th>Load current THD (p.u.)</th>
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<td>50 – 50</td>
<td>2.379</td>
<td>1.986</td>
<td>4.462</td>
<td>1.491</td>
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<td>2)</td>
<td>50 – 10</td>
<td>1.770</td>
<td>2.144</td>
<td>3.926</td>
<td>2.190</td>
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</table>
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter

**Table**

<table>
<thead>
<tr>
<th>Phase</th>
<th>Freq (Hz)</th>
<th>Mag (V)</th>
<th>Cos (°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHI_A</td>
<td>50.0</td>
<td>210.0</td>
<td>90.0</td>
</tr>
<tr>
<td>PHI_B</td>
<td>330.0</td>
<td>210.0</td>
<td>90.0</td>
</tr>
<tr>
<td>PHI_C</td>
<td>0.0</td>
<td>0.0</td>
<td>90.0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Phase</th>
<th>Freq (Hz)</th>
<th>Mag (V)</th>
<th>Sin (°)</th>
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</thead>
<tbody>
<tr>
<td>PHI_A</td>
<td>50.0</td>
<td>-120.0</td>
<td>90.0</td>
</tr>
<tr>
<td>PHI_B</td>
<td>120.0</td>
<td>210.0</td>
<td>90.0</td>
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<tr>
<td>PHI_C</td>
<td>220.0</td>
<td>210.0</td>
<td>90.0</td>
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</tbody>
</table>

**Results**

FIG. 14.11 MODEL OF A DUAL PROGRAMMABLE AC TO DC RECTIFIER USING THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER TOPOLOGY
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
14.10 THREE PHASE INDUCTION MOTOR LOAD: The three phase delta-sigma modulated MC using Venturini and Advanced Modulation algorithm driving a three phase Induction Motor (IM) load are already discussed in Section 11.6 of Chapter XI. The parameters of the IM are given in Table 11.6 of Chapter XI. In this section the model of the above MC driving an IM is reviewed using PSIM9 [52].

The PSIM model of the delta-sigma modulated MC using Venturini modulation algorithm driving the IM is shown in Fig. 14.19. The simulation results are shown in Fig. 14.20. The PSIM model of the delta-sigma modulated MC using Advanced modulation algorithm driving the IM is shown in Fig.
14.21. The simulation results are shown in Fig. 14.22. In both cases the external mechanical load applied is zero.

14.11 SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER: The detailed analysis, design of compensation capacitor and modelling of a single phase AC to three phase AC MC has already been discussed in Chapter XII. In this chapter the modelling of the above MC is reviewed using PSIM9 [52]. The parameters of the three phase Induction Motor and the values of the parameters used for the three phase input voltage, input and output frequency, saw-tooth carrier frequency, modulation index, filter inductor, filter capacitor and compensation capacitor are given in Table 12.1 and 12.2 of Chapter XII respectively. The PSIM model of the above MC driving the IM is shown in Fig. 14.23 and the simulation results are shown in Fig. 14.24(A) and Fig. 14.24 (B). The PSIM model of the above MC connected to a static R-L load is shown in Fig. 14.25 and the simulation results are shown in Fig. 14.26(A) for an output frequency of 50 Hz and in Fig. 14.26(B) for an output frequency of 20 Hz respectively.

14.12 DIRECT SPACE VECTOR MODULATION OF MATRIX CONVERTER: The modelling of MC using Direct Asymmetrical Space Vector Modulation (ASVM) technique is discussed in Section 8.2 and 8.3 of Chapter VIII. The modelling of three phase ASVM MC using PSIM9 [52] is reviewed here. The model of the Direct ASVM three phase AC to three phase AC MC is developed using PSIM in the same way as discussed in Section 8.3 of Chapter VIII. This model is shown in Fig. 14.27. The parameters are shown in Table 8.6 of Chapter VIII. The simulation results for output frequencies of 50 Hz and 20 Hz are shown in Figs. 14.28(A) to 14.28(I) and in Fig. 14.29(A) to 14.29(I) respectively. The simulation results are tabulated in Table 14.10.

<table>
<thead>
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<td>1)</td>
<td>50 – 50</td>
<td>0.720</td>
<td>0.136</td>
<td>0.182</td>
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<td>2)</td>
<td>50 – 20</td>
<td>0.950</td>
<td>0.166</td>
<td>0.320</td>
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</table>

The model of the Direct Symmetrical Space Vector Modulated (SSVM) MC using SIMULINK is already discussed in Section 8.5 of Chapter VIII. The model of the three phase Direct SSVM MC using PSIM9 [52] is reviewed here. The PSIM model of three phase Direct SSVM MC is shown in Fig. 14.30. This model is developed in the same way as discussed in Section 8.5 of Chapter VIII. The simulation results for output frequencies of 50 Hz and 20 Hz are shown in Figs. 14.31(A) to 14.31(I) and in Figs. 14.32(A) to 14.32(I) respectively. The simulation results are tabulated in Table 14.11.

<table>
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<td>1)</td>
<td>50 – 50</td>
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<td>0.406</td>
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<td>0.4188</td>
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</tbody>
</table>
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
FIG. 14.16 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC - DELTA SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM
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Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
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FIG. 14.19 MODEL OF THREE PHASE 50 Hz AC TO THREE PHASE 50 Hz AC MC - DELTA SIGMA MODULATED USING VENTURI Algorithm DRIVING A THREE PHASE DC LOAD
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FIG 14.21 MODEL OF THREE PHASE AC TO THREE PHASE AC INTERCONNECTION USING ADVANCED MODULATION ALGORITHM DRIVING THREE PHASE DM LOAD
FIG. 14.23 MODEL OF SINGLE PHASE AC TO THREE PHASE AC MC DRIVING THE I.M.
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14.13 INDIRECT SPACE VECTOR MODULATION OF MATRIX CONVERTER: The model of the Indirect Space Vector Modulated (ISVM) MC using SIMULINK is already discussed in Section 9.4 of Chapter IX. The model of the three phase Indirect SVM MC using PSIM9 [52] is reviewed here. The PSIM model of three phase Indirect SVM MC is shown in Fig. 14.33. This model is developed in the same way as discussed in Section 9.3 and 9.4 of Chapter IX. The simulation results for output frequencies of 50 Hz and 20 Hz are shown in Figs. 14.34(A) to 14.34(I) and in Figs. 14.35(A) to 14.35(I) respectively. The simulation results are tabulated in Table 14.12.

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<tbody>
<tr>
<td>1)</td>
<td>50 – 50</td>
<td>1.0814</td>
<td>1.5897</td>
<td>0.3738</td>
</tr>
<tr>
<td>2)</td>
<td>50 – 20</td>
<td>1.0435</td>
<td>1.7125</td>
<td>0.3554</td>
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</table>

14.14 DISCUSSION OF RESULTS: In this section the SIMULINK model performance for the respective category of the MC is compared with the relevant performance obtained by either PSCAD or PSIM presented in this chapter. The percentage error is calculated on the basis of SIMULINK model performance in the format given below:

\[
\text{Percentage Error} = \frac{(\text{SIMULINK Model Result} - \text{PSCAD/PSIM Model Result}) \times 100}{\text{SIMULINK Model Result}}
\]

Venturini algorithm assuming unity input power factor gives a percentage error of 3.94, -3.7 and 16.78 for the line to neutral output voltage, line to line output voltage and input current respectively. Sunter-Clare algorithm for MC gives a percentage error of -29.27, 15.5 and -28.61 for the line to neutral, line to line output voltages and input current respectively. Ned Mohan algorithm for MC gives a percentage error of -18.42, -11.32 and 30.47 for the line to neutral, line to line and input current respectively.

The simulation of three phase Multilevel MC (MMC) with three Flying capacitors (FC) per output phase is first carried out by SIMULINK and then this is also done by PSCAD and PSIM. Comparing the simulation using SIMULINK with PSIM, the percentage errors are -11.6, -29.2 and 76.21 for the line to neutral, line to line output voltages and input current respectively. The simulation of three phase MMC with six FC per output phase is carried out using PSCAD and PSIM only and hence the percentage error is NOT calculated.

The simulation of three phase Direct ASVM MC for an input and output frequency of 50 Hz respectively gives percentage error of 29.36, 29.89 and 37.79 for the line to neutral, line to line output voltages and load current respectively. For this Direct ASVM MC, the percentage error in the above order for an input and output frequency of 50 Hz and 20 Hz are -41.77, 0.6172 and 12.99 respectively. The simulation results for the Direct SSVM MC for an input and output frequency of 50 Hz respectively gives percentage error of 5.4, 15.58 and 10.59 in the above order. For this Direct SSVM MC the percentage error in the above order for an input and output frequency of 50 Hz and 20 Hz are
FIG. 14.27 MODEL OF DIRECT SVM THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER
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The simulation of the three phase Indirect SVM of MC for an input and output frequency of 50 Hz gives percentage error of 24.68, 13.88 and 24.04 for the line to neutral, line to line output voltages and load current respectively. For this three phase Indirect SVM MC the values of percentage error for an input and output frequency of 50 Hz and 20 Hz in the above order are -3.39, 12.89 and -30.04 respectively.

The simulation results of the Dual Programmable AC to DC rectifier shown in Table 10.3 of Chapter X closely well agree with the simulation results using PSCAD shown in Table 14.7 above and the discrepancy is negligible. This confirms the success of the discovery of the Dual Programmable AC to DC rectifier using three phase AC to three phase AC MC topology.

The simulation results for the three phase Delta-Sigma modulated MC using Venturini algorithm shows that for an input and output frequency of both 50 Hz, the percentage error for the line to neutral, line to line output voltages, input current and load current are -43.15, -26.56, -444.40 and -239.39 respectively. For the above delta-sigma modulated MC with an input and output frequency of 50 Hz and 20 Hz, the percentage error in the above order are 30.08, 31.87, -497.33 and -520.93 respectively. The simulation results for the three phase Delta-Sigma modulated MC using Ned Mohan algorithm shows that for an input and output frequency of both 50 Hz, the percentage error for
FIG. 14.30 MODEL OF DIRECT SSVM THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
the line to neutral, line to line output voltages, input current and load current are -187.77, -241.06, -645.90 and -222.30 respectively. For the above delta-sigma modulated MC using Ned Mohan algorithm, with an input and output frequency of 50 Hz and 20 Hz, the percentage error in the above order are 63.87, 39.77, -274.26 and 32.96 respectively. Also it is seen that with IM load, for both cases of the algorithm with delta-sigma modulated MC the speed of the IM tries to reach the no load speed. The simulation time used with PSIM and SIMULINK model in Chapter XI are different and hence the rated no load speed of the IM can’t be observed with PSIM model.

Comparing the simulation results of the single phase AC to three phase AC MC using SIMULINK in Chapter XII with that of the PSIM model of single phase AC to three phase AC MC, it is seen that with IM load in both cases three phase 50 Hz line to line output voltages are obtained from single phase 50 Hz AC supply and that the IM picks up speed. Also with R-L load, three phase 50 Hz as well as 20 Hz line to line output voltages are obtained in both cases with SIMULINK and PSIM software. The three phase 50 Hz stator current of the IM are NOT well balanced in both cases.

14.15 CONCLUSIONS: This chapter provides a verification of the performance of the selected models using SIMULINK discussed in the previous chapters. Both PSIM and PSCAD softwares are used for verification. Verification of the three phase MC performance using Venturini, Sunter-Clare and Ned Mohan algorithm shows a reasonable value for the error. Model verification for three phase Mutilevel MC with three FC shows reasonable error for the line to neutral and line to line output volt-
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
Chapter XIV: Verification of Models of Three Phase AC to Three Phase AC Matrix Converter
ages and a large value of error for the input current. The SIMULINK models for three phase MMC with three and six FC have been replaced by software PSCAD and the results verified by PSIM and found to have error within reasonable limit. The three phase MMC with six FC is a novel contribution. In the case of three phase Direct ASVM, SSVM and Indirect SVM of MC, reasonable errors are found for the line to neutral output voltage, line to line output voltage and load current. In the case of three phase delta-sigma modulated MC using both Venturini and Ned Mohan algorithm, it is seen that unreasonably large values of errors are observed for three phase input current and load current by model verification using PSIM. One of the greatest achievements of this research project is the discovery of the Dual Programmable AC to DC rectifier using three phase AC to three phase AC MC topology and the model verification using PSCAD results in close agreement with the performance using SIMULINK model. This opens up a new path way for the development of Hybrid Electric Vehicle and Electric Traction and associated control using dSPACE which can be used to drive separately excited DC motor and Permanent Magnet DC Motor. Also model verification using PSIM reveals possibility of generating three phase AC from single phase AC directly using MC without the need for AC to DC rectification and then DC to AC inversion.
Chapter XV
Conclusions

15.1 INTRODUCTION: This chapter provides the summary of contributions and conclusions drawn from the simulation results or performance of the three phase Matrix Converter (MC) models discussed in the previous chapters.

15.2 SUMMARY OF CONTRIBUTIONS AND DERIVED CONCLUSIONS: This thesis presents the modelling of three phase AC to three Phase AC Matrix Converter (MC) starting from the fundamental Venturini, Optimum Venturini algorithms [1-5] to the recent algorithms proposed by Sunter-Clare [11-12] and the one by Ned Mohan [13-14, 16-17] for switching three phase AC to three phase AC MC.

The application of the above mentioned algorithms for switching three phase AC to three phase AC MC driving Vector Controlled Induction Motor (IM) drive [15] is also successfully presented in this thesis. Simulation results indicate that accurate speed control of three phase vector controlled IM drive is possible with the rotor speed reaching the set point value in spite of mechanical load variation.

Real time control of a three phase AC to single phase AC MC hardware assembled using IGBT bidirectional switches, switched by gate pulses from model of the above MC using SIMULINK and dSPACE blockset interfaced to dSPACE DS1104 hardware controller board is successfully presented and the experimental result obtained is compared with model performance.

Three Phase AC to Three Phase AC Multilevel Matrix Converters (MMCs) with two and three Flying Capacitors (FCs) have been proposed in the literature to improve the harmonic performance of the three phase MC [18-19]. In this thesis models have been developed for three phase MMC with three and six FCs. The model of three phase MMC with six FC is a novel and an original contribution in this thesis. It is found by model simulation that the harmonic performance of three phase MMC with three and six FCs are found to be superior to that of the conventional three phase MC. Another special feature of this thesis and an original contribution is that for three phase MMC with three FC, modelling equations for three phase output voltage and input current are presented in matrix form as a Boolean logic expression in terms of the MC switch states such as whether a MC switch state is ON (logic 1) or OFF (logic 0).

Based on the method presented for the Direct Asymmetrical and Direct Symmetrical Space Vector Modulation of three phase AC to three phase AC MC in the literature [31-38] references, models have been presented in this thesis for the direct Asymmetrical Space Vector Modulation (ASVM) and also for the direct Symmetrical Space Vector Modulation (SSVM) of three phase AC to three phase AC MC. A notable original contribution in this thesis is the development of the model for the direct
Asymmetrical Centre Zero Space Vector Modulation (CZSVM) which shows how the location of the zero output voltage vector can be relocated. Various locations for the zero output voltage vector can be tried for optimum performance of the MC.

The Indirect Space Vector Modulation (ISVM) assumes a three phase AC to three Phase AC MC consisting of a three phase AC to DC rectifier and a DC to three phase AC Inverter [25-30]. In this thesis models have been successfully developed for three phase AC to three phase AC ISVM MC.

Dual fixed AC to DC rectifier using three phase AC to three phase AC MC topology is available in the literature [43-45]. One of the greatest achievements of this research thesis is the discovery of the model for Dual Programmable AC to DC rectifier using three phase AC to three phase AC MC topology and the mathematical derivation based on phasor diagram for the performance of the above Dual programmable AC to DC rectifier. This is a highly original contribution in this thesis which is NOT hitherto reported in the literature references. Model performance is verified by theoretical calculations using derived equations and found to be successful. This dual programmable AC to DC rectifier applications in the speed control and brake by plugging of separately excited DC motor and Permanent Magnet DC Motor is also presented and its real time applications using dSPACE in Hybrid Electric Vehicle and electric traction are highlighted which is also an original contribution in this thesis.

Sample time based modulation also known as Delta-Sigma modulation applied to three phase AC to three phase AC MC is reported in the literature [46-48]. In this thesis, models have been presented for Delta-Sigma modulated three phase AC to three phase AC MC using both Venturini algorithm [1-5] and Advanced Modulation algorithm proposed by Ned Mohan [13-14, 16-17]. The Delta-Sigma Modulated three phase AC to three phase AC MC using Advanced Modulation algorithm is an original contribution in this thesis.

Direct conversion of Single phase fixed frequency AC voltage to three phase variable frequency AC voltage using MC without an intermediate capacitor storage element is reported in the literature [50]. Based on this literature reference, model has been developed for single phase AC to three phase AC MC and the performance of the model successfully tested for two different output frequencies with both R-L load and three phase IM load.

A Novel Pulse Width Modulated AC to AC Converter using a DC link is a new idea developed by the author of this thesis. In this, single phase as well as three phase supply frequency AC to single phase as well as three phase variable frequency AC using NMOSFET-PMOSFET pair combination and bidirectional switches using IGBTs are presented along with successful simulation results using hardware components for the gate drive. The author of this thesis presumes that this is an original contribution.
Chapter XV: Conclusions

Above all, selected SIMULINK models from all the previous chapters have been verified for performance using either PSCAD or PSIM software and this verification report is presented.

Three appendices are presented. The first appendix gives the application of PIC microcontroller for saw-tooth carrier waveform generation and switching novel three phase AC to three phase AC converter using a DC link. The second appendix provides the model for speed control and brake by plugging of three phase IM fed by matrix converter, scheme for real time implementation of this model using dSPACE DS1104 hardware controller board and possible applications of this model for Hybrid Electric Vehicles and Electric traction. This model of three phase IM fed by MC with ability to control the speed and brake by reversing the phase sequence of the three phase applied voltage to the terminals of the IM and the scheme for real time implementation using dSPACE are original contribution in this thesis. The third appendix provides the list of publications from this thesis.

15.3 SUGGESTION FOR FURTHER WORK: A lot of further research work is possible in the following areas:

1) Dual Programmable AC to DC rectifier using Three Phase AC to Three Phase AC MC topology and real time speed control and brake by plugging of separately excited and Permanent Magnet DC motors using dSPACE hardware controller board.
2) Speed control and brake by plugging of three phase IM fed by MC in real time using dSPACE hardware controller board.
3) Delta-sigma modulation of three phase AC to three phase AC MC in real time using dSPACE hardware controller board.
4) Three Phase AC to Three Phase AC Multilevel MC and its real time implementation using dSPACE hardware controller board.
5) Implementation of Direct and Indirect Space Vector Modulation of three phase AC to three phase AC MC in real time using dSPACE hardware controller board.
6) Implementation of three phase Vector Controlled IM drive fed by MC in real time using dSPACE hardware controller board.
7) Implementation of single phase AC to three phase AC MC in real time using dSPACE hardware controller board.
Appendix I

PIC Microcontroller Applications

AI.1 INTRODUCTION: This appendix provides the PIC microcontroller approach for a) Designing the 2 kHZ saw-tooth carrier generator and b) Designing a gate drive for a 10 kHZ three phase inverter which can also be used as gate drive for the novel three phase AC to three phase AC converter using a DC link. The former one can be used to replace the 2 kHZ saw-tooth carrier generator using IC NE555 discussed in Chapter X of this thesis. The later one can be used to replace the modulo six counter and multiplexer used for switching the bidirectional switches of the AC to AC converter using a DC link discussed in Chapter XIII of this thesis.

AI.2 OVERVIEW OF PIC MICROCONTROLLER PIC 16F84A: The details of the PIC microcontroller PIC16F84A is available in the data sheet given in reference AI.6[1] below. Nevertheless for the purpose of systematically designing the above mentioned saw-tooth carrier and the three phase inverter gate drive, this data sheet is briefly reviewed here. The pin layout, register file map, STATUS register, OPTION register and INTCON register are briefly shown here in Fig. AI.1. Only essential Information required for this design are given in Fig. AI.1.
AI.3 DESIGN OF A 2 KHz SAW-TOOTH CARRIER GENERATOR: The saw-tooth carrier generator is designed in the same way as given in chapter X of this thesis. Here IC NE555 is replaced by a PIC microcontroller PIC16F84A to generate a 2 kHz square pulse with an ON time of 494E-6 seconds and an OFF time of 6E-6 seconds.

The program is developed here using TMR0 as a timer to generate time delays of 494 and 6 microseconds respectively. A 4 MHz external clock source is used which is connected to RA4/TOCKI pin of PIC16F84A. A divide by eight prescaler is chosen. The following calculations are made to preset the count in TMR0 register to create the above time delays.

\[
\text{Clock Frequency} = \frac{4 \times 10^6}{8} = 0.5 \times 10^6 \text{ Hz (AI.1)}
\]

\[
\text{Clock Period} = \frac{1}{0.5 \times 10^6} = 2 \times 10^{-6} \text{ Seconds (AI.2)}
\]

For 494E-6 Seconds time delay:

\[
2 \times 10^{-6} \times \text{clock cycle1} = 494 \times 10^{-6}
\]

Clock cycle1 = 247 (AI.3)

For 6E-6 Seconds time delay:

\[
2 \times 10^{-6} \times \text{clock cycle2} = 6 \times 10^{-6}
\]

Clock cycle2 = 3 (AI.4)

Preset TMR0 for a delay of 494e−6 seconds = (256 − 247) = 9 (AI.5)

Preset TMR0 for a delay of 6e−6 seconds = (256 − 3) = 253 (AI.6)

TMR0 is an eight bit register and the maximum count is FF hex which is 255. At 256th count TMR0 register overflows and the TMR0 overflow interrupt flag in the INTCON register set HIGH. Thus TMR0 is preset to count 9 and count 253 to create delays of 494e-6 seconds and 6e-6 seconds respectively. The flow-chart and source code for generating the square pulse with the above ON and OFF time using PIC16F84A is shown in Fig. AI.2. The 2 kHz saw-tooth carrier generator using PIC16F84A is shown in Fig. AI.3.

AI.4 DESIGN OF A GATE DRIVE FOR A THREE PHASE AC TO THREE PHASE AC CONVERTER USING A DC LINK: The design of the three phase AC to three phase AC converter using a DC link is shown in Fig. 13.10 of Chapter XIII where a modulo six counter and a multiplexer is used to generate the variable frequency 50% duty-cycle three phase clock generator. In this section same variable frequency 50% duty-cycle clock generator is developed using PIC16F84A microcontroller. The Pulse width modulation has to be added as shown in Fig. 13.10 and 13.11 of Chapter XIII. Here the frequency chosen for the variable frequency 50% duty-cycle three phase clock generator is 10 kHz. The design procedure is the same as that for a conventional three phase two level inverter. Therefor for the purpose of clarity, the bidirectional switches in Fig. 13.11 of Chapter XIII is replaced by conventional switches in a three phase two level inverter. The design is illustrated below:
The three phase inverter using conventional switches is shown in Fig. AI.4 and the gate drive waveform is shown in Fig. AI.5. Table AI.1 shows the method of connecting the port B of the micro-

---

The PIC16F84A source code is given below to generate clock pulse with 494 microseconds ON time and 6 microseconds OFF time.

```assembly
; The PIC16F84A source code is given below to generate clock pulse with 494 microseconds ON time and 6 microseconds OFF time.

.include pic16f84a.inc

org 00h

bsf status, 5 ; select bank 1
movlw 0x01     ; RA0 is input and RA3-RA0 are output ports
movlw 0x10     ; RA0 is input and RA3-RA0 are output ports
movlw 0x11     ; RA0 is input and RA3-RA0 are output ports
movwf option_reg ; TM10 external clock input and divide by eight prescale
bsf status, 5 ; select bank 0
bsf intcon, 7 ; Enable global interrupt
bsf intcon, 5 ; Enable time0 overflow interrupt
; introduce delay of 494 microseconds
clrf 494     ; bcf intcon, 2 ; clear TM10 interrupt flag
movlw 0x11111111b
movwf TMR0
xorw PORTA     ; PORTA R40 is HIGH for 494-6 seconds
movlw 0x4f
movwf TMR0
; Load decimal 9 to TM10 to start counting 494-6 seconds
loop1         ; bcf intcon, 2
goto loop1    ; bcf intcon, 2
movlw 0x00000000f
movwf PORTA    ; R40 is LOW for 6-6 seconds
movlw 0x2f
movwf TMR0
; loop2         ; bcf intcon, 2
goto loop2    ; goto delay494
end
```

---

FIG. AI.2: FLOW-CHART AND SOURCE CODE FOR SAW-TOOTH WAVEFORM GENERATOR
controller to the three phase inverter gate drive. Table AL2 shows the bit pattern obtained from Fig. AL5. Here an output frequency of 10 kHz is assumed. Therefore period of the inverter output frequency is 100e-6 seconds and 60 degree time interval correspond to 16.6667e-6 seconds. Assume that the external clock connected to RA4/TOCKI pin of PIC16F84A has a frequency of 4 MHz and that a prescale of divide by two is used. The TMR0 register is used to create a time delay of 16.6667e-6 seconds. The TMR0 count preset is calculated below:
Appendix I: PIC Microcontroller Applications

\[
\text{Clock} \quad \text{Frequency} = 2\text{MHz}
\]

\[
\text{Clock} \quad \text{Period} = \frac{1}{2 \times 10^6} = 0.5 \times 10^{-6} \text{ seconds} \quad (AI.7)
\]

\[
0.5 \times 10^{-6} \times N_1 \text{ clock cycle} = 16.6667 \times 10^{-6}
\]

\[
N_1 = 33
\]

\[
\text{Preset TMR0 for } 16.6667e-6 \text{ seconds} \quad \text{time delay} = (256 - 33) = 223 \quad (AI.8)
\]

The source code for generating the 10 kHz three phase inverter gate drive is shown in Fig. AI.6. By varying the TMR0 count preset, any required output frequency for the three phase inverter can be obtained. The 10 kHz three phase inverter gate drive using PIC16F84A is shown in Fig. AI.7. The gate drive for switches S1 to S6 in Fig. AI.7 correspond to the gate drive for the bidirectional IGBT switches from top to bottom in order shown in Fig. 13.11 in Chapter XIII.

The source code for the 10 kHz three phase inverter is given below.

```
; The PIC16F84A source code is given below for 10 kHz three phase inverter
; Narayanaswamy, P.R. Iyer
#include pic16f84a.inc
;port A RA4 input port
;RA4/TOCKI pin 4 MHz clock
;port B output port
;port A RA3-RA0 are output ports
status equo 03
porta equo 05
portb equo 06
trisa equo 85
trish equo 86
intcon equo 0B
option_reg equo 81
tmr0 equo 01
org 00
bsf status, 5 ; select bank 1
movlw B'00010000'
movwf trisa ; RA4 is input and RA3-RA0 are output ports
movlw B'00000000'
movwf trish ; All port B pins are output ports
movlw B'00110000'
movwf option_reg ; TMR0 external clock input at RA4/TOCKI and divide by two prescale
bsf status, 5 ; select bank 0
bsf intcon, 7 ; Enable global interrupt
bsf intcon, 5 ; Enable TMR0 overflow interrupt
loop1 movlw B'99h'
movwf portb
call delay
movlw B'9Fh'
movwf portb
call delay
movlw B'A4h'
movwf portb
call delay
movlw B'6Fh'
movwf portb
call delay
movlw B'68h'
movwf portb
call delay
movlw B'S8h'
movwf portb
call delay
movlw B'00h'
movwf portb
call delay
goto loop1
delay bcf intcon, 2 ; clear TMR0 FF
movlw B'D223'
movwf tmr0 ; load TMR0 for a delay of 16.6667s-6 seconds
loop2 btfss intcon, 2
goto loop2
return
```

Fig. AI.6: Source code for three phase AC to AC converter using a DC link.

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AI.5 CONCLUSIONS: The present trend is to use microcontrollers in the place of analog and digital ICs for waveform generation and for three phase and single phase inverter gate drive. By assigning suitable value for TMR0 count preset value required time delay and required output frequency can be obtained. Also externally changing the clock frequency within the range allowable for PIC16F84A, required output frequency for the inverter and also for the square pulse waveform ON and OFF time can be obtained. Also by using any neighbouring output gate drive such as the gate drive for S1 and S2 in Fig. AI.7, the same source code and circuit connection in Fig. AI.7 can be used for single phase AC to single phase AC converter using a DC link discussed in Chapter XIII.

AI.6 REFERENCES:
Appendix II

Speed Control and Brake by Plugging of Three Phase Induction Motor Fed by Matrix Converter

AII.1 INTRODUCTION: Three phase induction motor (IM) fed by Matrix Converters (MCs) can be used for speed control and brake by plugging or by reversing the phase sequence of the three phase applied voltage. This can be accomplished in the SIMULINK MC model and can be implemented in dSPACE. Thus three phase IM fed by MC can be used in Hybrid Electric Vehicle and also in electric traction. This section explores this application.

AII.2 MODEL OF THREE PHASE INDUCTION MOTOR FED BY MATRIX CONVERTER: The SIMULINK model of the three phase IM fed by MC with provision for speed control and brake by plugging is shown in Fig. AII.1. Braking of a three phase IM by plugging involves reversing the phase sequence of the three phase applied voltage to the stator terminals of the IM. This is done manually using three pole double throw switch. In the method using SIMULINK model this can be done by varying the model parameter such as the modulation index and the phase of the desired three phase output voltage. The model shown in Fig. AII.1 is developed using Venturini Second method assuming unity input phase displacement factor explained in section 3.4.3 of chapter III. Only relevant changes in the model for speed control and braking is explained below:

Speed control is achieved by varying the magnitude of the three phase output voltage of the MC which is applied to the terminals of the IM. Magnitude variation is possible by changing the modulation index $q$ in the range from 0 to 0.5. In Fig. AII.1, this value of $q$ is varied using a multiport switch. For braking, three phase output voltage phase sequence has to be reversed. Referring to equation 3.11 of chapter III, the phase sequence of output voltage $v_b$ and $v_c$ can be changed by swapping the phase $2\pi/3$ with proper sign. In Fig. AII.1, this is achieved by using a repeating sequence block. The three phase IM used has the parameter shown in Table 5.1 of chapter V.

AII.3 SIMULATION RESULTS: The simulation of the model shown in Fig. AII.1 is carried out using SIMULINK [51]. The ode15s(Stiff/NDF) solver is used. The simulation results are shown in Fig. AII.2(A) to AII.2(D).

AII.4 REAL TIME IMPLEMENTATION: The real time implementation scheme using SIMULINK model in conjunction with dSPACE hardware controller board is shown in Fig. AII.3(A) to (C). The scheme in Fig. AII.3(A) and (B) are with DC generator and three phase alternator mode respectively. Fig. AII.3(C) is the scheme for dSPACE gate drive for MC. Fig. AII.4 shows the hard-
FIG. AII.1: SPEED CONTROL AND BRAKE BY PLUGGING OF THREE PHASE IM FED BY MC
Appendix II: Speed Control and Brake by Plugging of Three Phase Induction Motor Fed by Matrix Converter
Appendix II: Speed Control and Brake by Plugging of Three Phase Induction Motor Fed by Matrix Converter

FIG. AII.3

FIG. AII.4 SAW-TOOTH CARRIER GENERATOR (A), OUTPUT VOLTAGE PHASE VALUE SWAPPING DEVICE (B) AND MODULATION INDEX VARYING DEVICE (C)
ware implementation for the saw-tooth carrier generator, output voltage phase value (2*PI/3) swapping device and the modulation index varying device. The hardware realization for saw-tooth carrier generator is already explained in chapter X and also Appendix I. The phase value swapping device and the modulation index varying device use op.amps and resistor network as shown in Fig. AII.4 (B) and (C) respectively.

AII.5 DISCUSSION OF RESULTS: For the purpose of illustration of acceleration, retardation and braking by plugging or phase sequence reversal, the modulation index q is assumed to vary from 0 to 0.5 in steps of 0.1 every 20e-3 seconds in the forward increasing order and then in the reverse decreasing order. At 100e-3 seconds simulation time the phase value changes from +2π/3 to -2π/3 radians and similarly at 210e-3 seconds simulation time, this phase value changes from -2π/3 to +2π/3 radians respectively. From the rotor speed in Fig. AII.2(D) it is seen that the IM accelerates for the initial 100e-3 seconds, then retards or decelerates and reverses direction of rotation from 100e-3 seconds to 210e-3 seconds. From the stator current and line to line output voltage waveform in Fig. AII.2(D), it is clear that phase sequence reversal takes place after 100e-3 seconds simulation time. Also in Fig. AII.2(D), the rotor E.M. torque is found to be negative from 100e-3 seconds simulation time. This simulation illustrates the speed control, acceleration, retardation and braking of three phase IM. Fig. AII.3 and AII.4 shows how this method can be implemented in real time using dSPACE DS1104 hardware controller board. The three phase IM fed by three phase AC to three phase AC MC can be used for Hybrid Electric Vehicle (HEV) [63] and Electric Traction applications.

AII.6 CONCLUSIONS: Here one method of speed control and brake by plugging of a three phase IM is illustrated by simulation of the SIMULINK model, by varying the modulation index and by swapping the phase value of the three phase output voltage in the model. A hardware realization scheme for real time application using dSPACE DS1104 hardware controller board is also presented. This provides a new method of real time speed control and brake by plugging of three phase IM drive suitable for Hybrid Electric Vehicle and electric traction applications.
Appendix II

Speed Control and Brake by Plugging of Three Phase Induction Motor Fed by Matrix Converter

AII.1 INTRODUCTION: Three phase induction motor (IM) fed by Matrix Converters (MCs) can be used for speed control and brake by plugging or by reversing the phase sequence of the three phase applied voltage. This can be accomplished in the SIMULINK MC model and can be implemented in dSPACE. Thus three phase IM fed by MC can be used in Hybrid Electric Vehicle and also in electric traction. This section explores this application.

AII.2 MODEL OF THREE PHASE INDUCTION MOTOR FED BY MATRIX CONVERTER: The SIMULINK model of the three phase IM fed by MC with provision for speed control and brake by plugging is shown in Fig. AII.1. Braking of a three phase IM by plugging involves reversing the phase sequence of the three phase applied voltage to the stator terminals of the IM. This is done manually using three pole double throw switch. In the method using SIMULINK model this can be done by varying the model parameter such as the modulation index and the phase of the desired three phase output voltage. The model shown in Fig. AII.1 is developed using Venturini Second method assuming unity input phase displacement factor explained in Section 3.4.3 of Chapter III. Only relevant changes in the model for speed control and braking is explained below:

Speed control is achieved by varying the magnitude of the three phase output voltage of the MC which is applied to the terminals of the IM. Magnitude variation is possible by changing the modulation index \( q \) in the range from 0 to 0.5. In Fig. AII.1, this value of \( q \) is varied using a multiport switch. For braking, three phase output voltage phase sequence has to be reversed. Referring to equation 3.11 of Chapter III, the phase sequence of output voltage \( v_b \) and \( v_c \) can be changed by swapping the phase \( \frac{2\pi}{3} \) with proper sign. In Fig. AII.1, this is achieved by using a repeating sequence block. The three phase IM used has the parameter shown in Table 5.1 of Chapter V.

AII.3 SIMULATION RESULTS: The simulation of the model shown in Fig. AII.1 is carried out using SIMULINK [51]. The ode15s(Stiff/NDF) solver is used. The simulation results are shown in Fig. AII.2(A) to AII.2(D).

AII.4 REAL TIME IMPLEMENTATION: The real time implementation scheme using SIMULINK model in conjunction with dSPACE hardware controller board is shown in Fig. AII.3(A) to (C). The scheme in Fig. AII.3(A) and (B) are with DC generator and three phase alternator mode respectively. Fig. AII.3(C) is the scheme for dSPACE gate drive for MC. Fig. AII.4 shows the hard-
FIG. AII.1: SPEED CONTROL AND BRAKE BY PLUGGING OF THREE PHASE IM FED BY MC
ware implementation for the saw-tooth carrier generator, output voltage phase value \((2\pi/3)\) swapping device and the modulation index varying device. The hardware realization for saw-tooth carrier generator is already explained in Chapter X and also in Appendix I. The phase value swapping device and the modulation index varying device use op.amps and resistor network as shown in Fig. AII.4 (B) and (C) respectively.

**AII.5 DISCUSSION OF RESULTS:** For the purpose of illustration of acceleration, retardation and braking by plugging or phase sequence reversal, the modulation index \(q\) is assumed to vary from 0 to 0.5 in steps of 0.1 every 20e-3 seconds in the forward increasing order and then in the reverse decreasing order. At 100e-3 seconds simulation time the phase value changes from +2\(\pi/3\) to -2\(\pi/3\) radians and similarly at 210e-3 seconds simulation time, this phase value changes from -2\(\pi/3\) to +2\(\pi/3\) radians respectively. From the rotor speed in Fig. AII.2(D) it is seen that the IM accelerates for the initial 100e-3 seconds, then retards or decelerates and reverses direction of rotation from 100e-3 seconds to 210e-3 seconds. From the stator current and line to line output voltage waveform in Fig. AII.2(D), it is clear that phase sequence reversal takes place after 100e-3 seconds simulation time. Also in Fig. AII.2(D), the rotor E.M. torque is found to be negative from 100e-3 seconds simulation time. This simulation illustrates the speed control, acceleration, retardation and braking of three phase IM. Fig. AII.3 and AII.4 shows how this method can be implemented in real time using dSPACE DS1104 hardware controller board. The three phase IM fed by three phase AC to three phase AC MC can be used for Hybrid Electric Vehicle (HEV) [63] and Electric Traction applications.

**AII.6 CONCLUSIONS:** Here one method of speed control and brake by plugging of a three phase IM is illustrated by simulation of the SIMULINK model, by varying the modulation index and by swapping the phase value of the three phase output voltage in the model. A hardware realization scheme for real time application using dSPACE DS1104 hardware controller board is also presented. This provides a new method of real time speed control and brake by plugging of three phase IM drive suitable for Hybrid Electric Vehicle and electric traction applications.
Appendix III
List of Publications

AIII.1 INTRODUCTION: The following are the list of publications from this research work:

AIII.2 LIST OF PUBLICATIONS:


References


References:


References:


References:


