FPGA Implementation of Wideband IQ Imbalance Correction in OFDM Receivers

Rajitha Bandara Palipana and Kah-Seng Chung

Abstract—**This paper describes the implementation of a digital compensation scheme, called CSAD, for correcting the effects of wideband gain and phase imbalances in dual-branch OFDM receivers. The proposed scheme is implemented on a Xilinx Virtex-4 field programmable gate array (FPGA). The flexible architecture of the implementation makes it readily adaptable for different broadband applications, such as DVB-T/H, WLAN, and WiMAX. The proposed correction scheme is resilient against multipath fading and frequency offset. When applied to DVB-T, it is shown that an 11-bit arithmetic precision is sufficient to achieve the required BER of $2x10^{-4}$ at an SNR of 16.5 dB. Using this bit-precision, the implementation consumes 1686 Virtex-4 slices equivalent to about 42600 gates.**

Index Terms—**direct-conversion receiver, gain and phase imbalances, field programmable gate array, orthogonal frequency division multiplexing.**

I. INTRODUCTION

A dual-branch direct-conversion receiver architecture is attractive as it supports very high level of integration. With this architecture, radio frequency signals are down-converted to in-phase (I) and quadrature (Q) signal components in one single step. However, for correct operation, the I and Q signal branches must maintain equal gain and quadrature phase.

In wideband applications, precise matching of gain and phase is very difficult if not impossible to achieve over the entire signal bandwidth. As a result, this gives rise to frequency dependent gain and phase errors, known as wideband IQ imbalances. Moreover, direct-conversion receivers require very large baseband amplification, often in excess of 60 dB, before signal digitization and demodulation. This large gain requirement makes accurate matching of gain and phase even more difficult to achieve. In practice, a well designed wideband dual-branch receiver is likely to encounter average frequency dependent gain and phase imbalances in the order of 0.5 - 1 dB and ±3°- 5º, respectively [1]. When such a receiver is used to demodulate a high order modulation scheme, such as 64-QAM, the resulting bit error rate will be degraded. For example, the presence of 1 dB gain and 5° phase deviations will give rise to about 2.5 dB degradation in SNR when 64-QAM is adopted in conjunction with an error correction code of rate 2/3 [2]. This degradation in SNR increases to over 10 dB when a code rate of 7/8 is used [2].

This problem of gain and phase imbalances needs to be overcome in order for a dual-branch receiver to successfully operate with high order modulation schemes. There are a number of IQ compensation techniques published in the literature, but most of them target a single particular application [3, 4]. It is envisaged that future applications will call for a single receiving device to be able to operate with different modulation schemes, preferably with only software modifications. This suggests that any proposed architecture for the mismatch compensation scheme must be sufficiently flexible to allow such changes to be made through minor modifications in software. Furthermore, such a compensation scheme has to be robust. One such compensation scheme, called complex symmetric adaptive de-correlation (CSAD), has been proposed and analyzed in [5]. This paper focuses on the hardware implementation of this gain and phase imbalance compensation scheme.

This paper is organized as follows. Section II provides an introduction to the effects of receiver impairments in a direct conversion receiver operating with an orthogonal division frequency division multiplexing (OFDM) signal. This is followed by a methodical approach for correcting such adverse affects. Section III describes the hardware implementation of the CSAD scheme. Finally, results obtained through hardware-in-the-loop testing are presented in Section IV.

II. CORRECTION OF FRONT-END IMPAIRMENTS

For a direct-conversion receiver, the discrete time representation of the received baseband OFDM signal in the presence of multi-path, AWGN, frequency offset, and gain and phase imbalances can be expressed as [5]

$$r_1[n] = g_1[n] \otimes m_1[n] + g_2[n] \otimes m_1{}^*[n] \quad (1)$$

where

$$m_1[n] = (h[n] \otimes c[n] + \eta[n]) e^{-j2\pi\Delta fn/Nf_s}, \quad (1.a)$$

$$g_1[n] = \left(\alpha e^{-j\theta_1} g_I[n] + \beta e^{-j\theta_2} g_Q[n]\right)/2, \quad (1.b)$$

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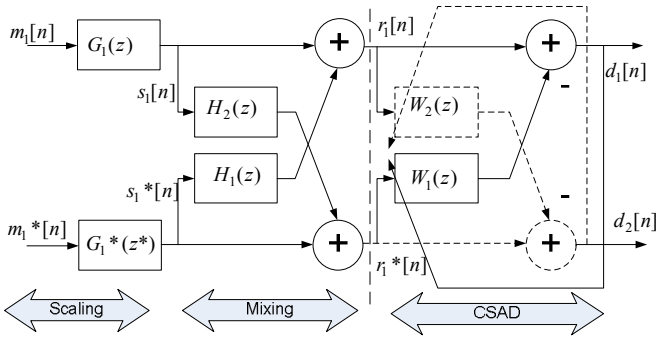

Fig. 1 The use of CSAD filter for compensating the effects of gain and phase imbalances

$$g_2[n] = \left(\alpha e^{j\theta_1} g_I[n] - \beta e^{j\theta_2} g_Q[n]\right)/2 . \qquad (1.c)$$

$g_1[n]$ and $g_2[n]$ denote the contributions of gain and phase imbalances. Frequency independent gain an phase errors are given by α/β and $(\theta_1 - \theta_2)$, respectively. $g_I[n]$ and $g_Q[n]$ are used to model the frequency dependent imbalances. The frequency offset is Δf, and f_s is the sub-carrier spacing. $h[n]$, $c[n]$ and $\eta[n]$ are the channel impulse response, the complex envelope of the transmitted signal, and additive white Gaussian noise (AWGN), respectively. It is assumed that OFDM signals are generated using N - point inverse discrete Fourier transform (IDFT).

Now consider the received signal $r_1[n]$ given in (1). This signal consists of two components, the desired signal $m_1[n]$ and the undesired $m_1{}^*[n]$, which is the complex conjugate of the desired signal. This observation enables the gain and phase mismatch problem to be treated as a signal separation problem with scaling and mixing of the sources $m_1[n]$ and $m_1{}^*[n]$ as shown in Fig. 1. The mixing transfer functions are indicated by $H_1(z)$ and $H_2(z)$. The CSAD filter, as shown in Fig. 1, can be used to separate the signals $s_1[n]$ and $s_1{}^*[n]$. An additional equalizer is required to recover $m_1[n]$ from $s_1[n]$.

A signal de-correlation method, such as the CSAD, may be used to recover the desired signal $m_1[n]$ from a mixture of signals containing $m_1[n]$ and $m_1{}^*[n]$, provided that $m_1[n]$ and $m_1^*[n]$ are uncorrelated. It is shown in [5] that $m_1[n]$ and $m_1{}^*[n]$ are indeed uncorrelated even in the presence of frequency offset and multipath fading. According to [5], the CSAD filter algorithm operates as follow:

I. Obtain the signal estimates

$$d_1[n] = r_1[n] - \mathbf{w}_1{}^H[n]\mathbf{r}_1{}^*[n] \qquad (2.a)$$

$$d_2[n] = r_1{}^*[n] - \mathbf{w}_2{}^H[n]\mathbf{r}_1[n] \qquad (2.b)$$

II. Update the weights

$$\mathbf{w}_1[n+1] = \mathbf{w}_1[n] + 2\lambda_1 \mathbf{d}_2[n] d_1{}^*[n] \qquad (2.c)$$

$$\mathbf{w}_2[n+1] = \mathbf{w}_1{}^*[n+1] . \qquad (2.d)$$

Note that the bold face letters denote vectors of length L, where L is the length of the de-correlating adaptive filters $\mathbf{w}_1[n]$ and $\mathbf{w}_2[n]$. $\{\ \}^H$ denotes a Hermitian transpose. λ_1 is the adaptive filter step size. $d_1[n]$ and $d_2[n]$ are the outputs of the CSAD filter. The desired output signal from the CSAD filter is $d_1[n]$, given by

$$d_1[n] = h_o[n] \otimes (h[n] \otimes c[n] + \eta[n]) e^{-j2\pi\Delta f n / Nf_s} \qquad (3)$$

where

$$h_o[n] = g_1[n] \otimes \left(1 - h_1[n] \otimes h_2[n]\right) \qquad (3.a)$$

$$h_1[n] = IDFT\left\{G_2[k] / G_1{}^*[-k]\right\} \qquad (3.b)$$

$$h_2[n] = IDFT\left\{G_2{}^*[-k] / G_1[k]\right\} \qquad (3.c)$$

Now, assume that the frequency offset Δf is estimated accurately, its effect on $d_1[n]$ could then be eliminated by multiplying (3) with the factor $e^{j2\pi\Delta f n / Nf_s}$. The resulting signal becomes

$$d_{1f}[n] = h_{of}[n] \otimes (h[n] \otimes c[n] + \eta[n]) \qquad (4)$$

where $h_{of}[n] = h_o[n] e^{j2\pi\Delta f n / Nf_s}$. Note that $h_{of}[n]$ could be approximated by $h_o[n]$ when the length of the impulse response $h_o[n]$ is small and N is large. After this operation, the signal $d_{1f}[n]$ is given by

$$d_{1f}[n] = h_o[n] \otimes (h[n] \otimes c[n] + \eta[n]) \qquad (5)$$

In the case that the length of the impulse response, $h_o[n] \otimes h[n]$ is less than the length of the cyclic prefix of the OFDM signal, an estimate of the original signal $c[n]$ can be recovered using a pilot based LMS equalizer [5].

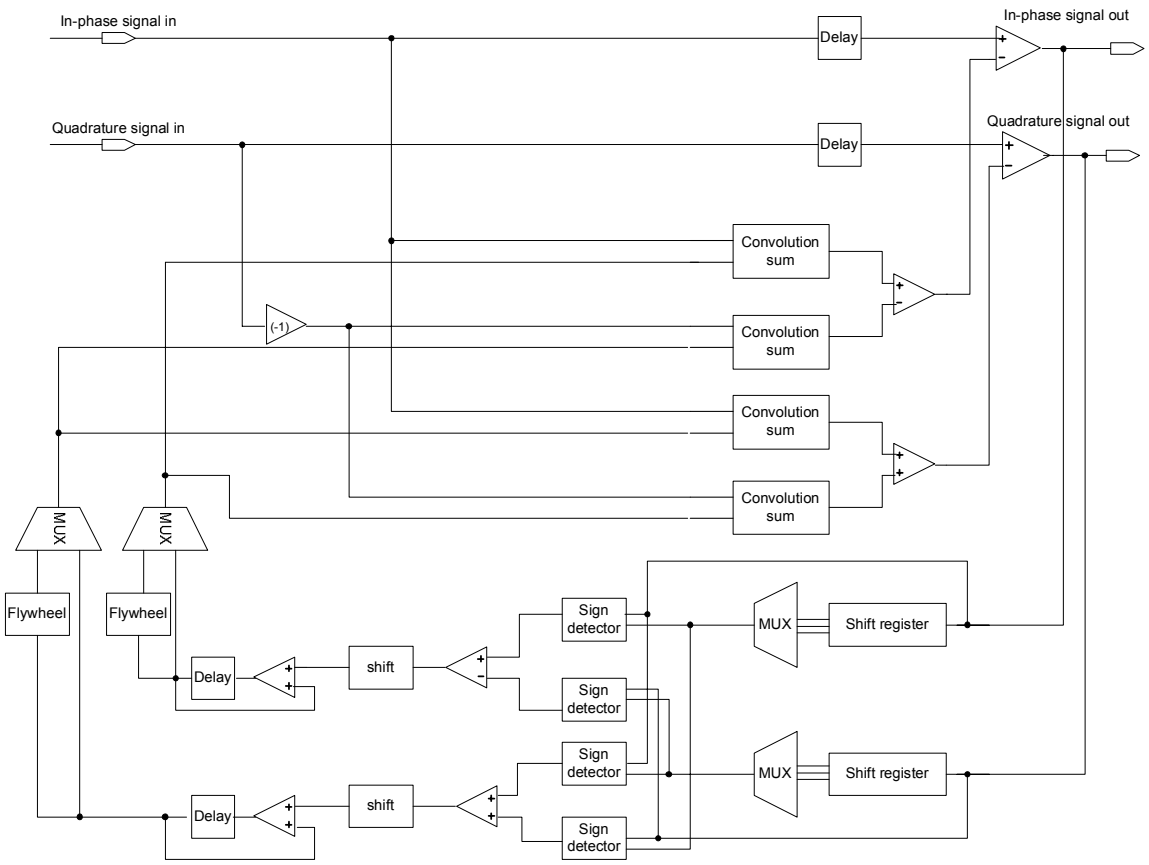

Fig. 2 CSAD filter implementation

III. FPGA IMPLEMENTATION OF THE CSAD FILTER

Figure 2 shows the various functional blocks for the FPGA implementation of the CSAD filter. The inputs to the CSAD filter, denoted by 'in-phase signal in' and 'quadrature signal in', are the real and imaginary signal components of $r_1[n]$, which is the received signal that has been corrupted by a combination of gain and phase imbalances, frequency offset, AWGN and multi-path fading. As given by (2.a), the desired signal $d_1[n]$ consists of $r_1[n]$ and its complex conjugate $\mathbf{r}_1{}^*[n]$, and the adaptive weight $\mathbf{w}_1[n]$. $\mathbf{r}_1{}^*[n]$ is obtained by negation of the imaginary part of $\mathbf{r}_1[n]$ as shown in Fig. 2. The convolution operation, $\mathbf{w}_1{}^H[n]\mathbf{r}_1{}^*[n]$ in (2.a) is carried out by the four 'convolution sum' blocks.

In wideband applications, the gain and phase imbalances are likely to vary differently over the signal bandwidth. Frequency dependent gain and phase imbalances introduce convolutive mixing of $m_1[n]$ and $m_1{}^*[n]$, as shown in (1). In order to correct for convolutive mixing, the length of the de-mixing adaptive CSAD filter, L, needs to be greater than one. This means that the calculation of $\mathbf{w}_1{}^H[n]\mathbf{r}_1{}^*[n]$ will involve 4L real multiplications. In order to reduce the actual number of multipliers needed, the same multipliers are reused. Suppose that the sampling period is T_s, and 4L real multiplications are required to be performed within this period. Now, by up-sampling the signals by a factor of L, a multiplication can be carried out within a time period of T_s/L. In this case, instead of 4L multipliers, this allows the use of only four multipliers, one each for calculating the real-real, imaginary-imaginary, real-imaginary, and imaginary-real products involved in the multiplication of two complex quantities. Each of the four 'convolution sum' blocks, shown in Fig. 2, contains an addressable shift register, a multiplexer, a real multiplier and an accumulator for calculating the convolution sum.

Next, consider the weight update operation, as given in (2.c). To obtain the updated weights at time index n+1, it requires knowledge of $d_1[n]$, $\mathbf{d}_2[n]$, and $\mathbf{w}_1[n]$. According to (2.d), the adaptive filter coefficients $\mathbf{w}_1[n]$ and $\mathbf{w}_2[n]$ are complex conjugates of one another. As a result, the signal $\mathbf{d}_2[n]$, is the complex conjugate of $\mathbf{d}_1[n]$. This observation suggests that the explicit calculations of $d_2[n]$ and $\mathbf{w}_2[n]$, based on (2.b) and (2.d) respectively, are not necessary. Thus, the implementation of the weight update is

significantly simplified.

In view of this observation, the computation of $\mathbf{w}_1[n+1]$ involving the evaluation of $2\lambda_1\mathbf{d}_2[n]d_1^*[n]$ then becomes $2\lambda_1\mathbf{d}_1^*[n]d_1^*[n]$. A further simplification of the implementation is to make the step size $2\lambda_1$ a power of two, so that the multiplication process can be replaced by a right shift of the binary point of the product $\mathbf{d}_1^*[n]d_1^*[n]$. Also, since CSAD is a form of gradient descent algorithms, the direction of motion in the quadratic error performance surface is determined by the signs of the respective real and imaginary parts of the product $\mathbf{d}_1^*[n]d_1^*[n]$. The calculation of the product $\mathbf{d}_1^*[n]d_1^*[n]$ involves 4L real multiplications. As before, if the signals $\mathbf{d}_1^*[n]$ and $d_1^*[n]$ are up sampled by a factor of L then the same multipliers could be reused. However, four real multipliers are still required for calculating the real-real, imaginary-imaginary, real-imaginary, and imaginary-real products involved in multiplying two complex quantities. On the other hand, each of the four real multipliers can now be replaced by a much simpler sign detection circuit. Suppose x and y are two inputs (real or imaginary components of $\mathbf{d}_1^*[n]$ and $d_1^*[n]$) applied to a sign detector circuit, its output, z, then takes on values according to Table 1.

TABLE 1 SIGN DETECTION CIRCUIT

x	y	z
> 0	> 0	x
< 0	< 0	-x
> 0	< 0	-x
< 0	> 0	x

Normally, gain and phase imbalances in a receiver are relatively time invariant. However, being an adaptive system, the weights of the CSAD filter will continue to be influenced by the instantaneous values of the received signal. When a large step size is used, the adaptive weights tend to vary somewhat about the average convergent value. This variation in weights can degrade the BER performance and make the signal equalization difficult. A flywheel or averaging circuit has therefore been implemented to smoothen out the instantaneous variations in the adaptive weights. The resultant smoothened weights are used to correct the signal while the weight updates continue to operate using the instantaneous values. A multiplexer is used here to switch between the instantaneous and averaged weight values.

The operation of the CSAD filter does not require synchronization of the OFDM signal to be achieved. Also, its insensitivity to the presence of frequency offset and multi-path fading suggests that the CSAD filter can operate directly on the digitised outputs of the down-converted in-phase and quadrature components of the received signal.

Often, the accuracy of a frequency offset estimator is affected by the presence of gain and phase imbalances, especially when a short cyclic prefix is used to estimate the frequency offset. In this situation, it is beneficial for the gain and phase imbalances to be first compensated using the CSAD filter prior to estimation of any residual frequency offset [5].

IV. RESULTS

The setup used for the hardware-in-the-loop testing is shown in Fig. 3. The test signal used is DVB-T operating in the 2k mode with non-hierarchical 64-QAM modulation and a convolutional code rate of 2/3 [6]. Pilot insertion, inverse Fourier transform and cyclic prefix attachment are carried out in the OFDM TX block. Baseband in-phase and quadrature signal components, corrupted by IQ imbalances and frequency offset, are saved in two data files along with the timing information. These files are accessed by the FPGA through a JTAG interface.

The CSAD filter is implemented on a Xilinx ML401 development board [7] using Xilinx System Generator v8.1 and Xilinx ISE foundation edition 8.1. After the in-phase and quadrature components have been processed by the CSAD filter, the resultant signals are output via the JTAG interface and stored in another data file on a PC. This data file is then imported to Matlab where frequency offset correction (FOC), cyclic prefix removal, FFT and channel equalization (CEQ) are carried out. The correction of the frequency offset is performed by multiplying the CSAD filtered signal by $e^{j2\pi\Delta fn/Nf_s}$. The residual scaling introduced by the CSAD filter and the multi-path channel is then corrected by a frequency domain LMS filter [5].

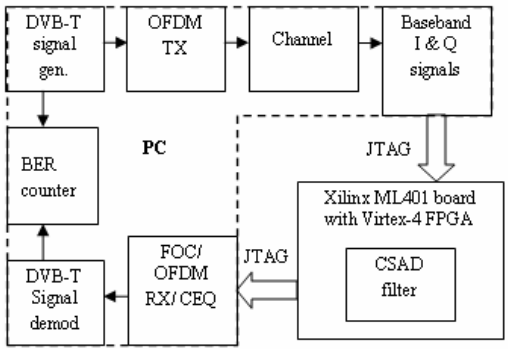

Fig. 3 The setup used for the hardware-in-the-loop testing

The computational complexity of the CSAD filter is proportional to the number of adaptive weights, L. According to [2], the average BER performance is relatively insensitive to L once it is chosen to be larger than a certain minimum value. For practical values of gain and phase imbalances, L = 3 is adequate. For the test, the gain and phase imbalances are allowed to vary by ± 1.5 dB and $\pm 10^\circ$, respectively, over the DVB-T signal bandwidth of 7.61 MHz. These variations are produced by combining the constant gain and phase imbalances of 1 dB and 5º together with the frequency dependent values derived from $G_I(z) = 0.01 + z^{-1} + 0.01z^{-2}$ & $G_Q(z) = 0.01 + z^{-1} + 0.2z^{-2}$ [8].

In the implementation, the performance of the CSAD filter as a function of bit-precision is studied using the average BER as the performance metric. In this case, all the mathematical operations required by the CSAD filter are carried out with the same bit-precision. Fig. 4 shows the average bit error rates achieved with different values of bit precision, ranging from 8 bits to 16 bits, in the presence of AWGN. For quasi-error free reception in DVB-T, it is specified that the bit error rate after Viterbi decoding has to be less than 2×10^{-4} at an SNR of 16.5 dB (Table A.1 in [6]). This level of performance could just be achieved using a wordlength of 11 bits.

Next, the performance of the CSAD filter operating in the Ricean channel as given in the DVB-T standard [6] is investigated in the presence of a frequency offset close to half the sub-carrier spacing, i.e., 2000 Hz. The BER curve obtained after the corrections of the gain and phase imbalances, and the frequency offset is shown in Fig. 5. When compared with the BER curve obtained assuming no circuit impairments, the degradation in SNR is less than 0.3 dB at the required BER of 2×10^{-4}. For this example, the CSAD filter is implemented with 11-bit precision.

To provide an indication on the hardware complexity of the CSAD filter, the Xilinx tool called XFLOW is used to obtain the gate count for implementing a given bit precision. Table 2 shows the number of lookup tables (LUTs) and flip-flops used by the design for four different precision levels, ranging from 11 bits to 16 bits. It is shown that a 12-bit implementation consumes only about 10 % of the gate resources offered by the Virtex-4 FPGA, which has a total of 21504 LUTs and 21504 flip-flops.

V. CONCLUSIONS

This paper describes an FPGA implementation of a digital IQ imbalance compensation scheme based on an CSAD filter. It is shown that the required BER of less than 2×10^{-4} specified for DVB-T reception can be met when the CSAD filter is implemented with a bit precision of at least 11 bits. This is achieved in the presence of severe gain and phase imbalances of ±1.5 dB and $\pm10^{\circ}$, respectively, varying over a bandwidth of 7.61 MHz. Furthermore, the operation of the CSAD filter does not depend on the synchronization of the OFDM signal being achieved. In fact, the CSAD can operate on any Gaussian like signals, including those OFDM signals associated with WLAN and WiMAX.

TABLE 2 HARDWARE DESIGN SUMMARY

Precision (bits)	Flip-Flops	LUTs	Gate count
11	1972	1983	42567
12	2033	2179	45461
14	2267	2510	51166
16	2439	2736	56180

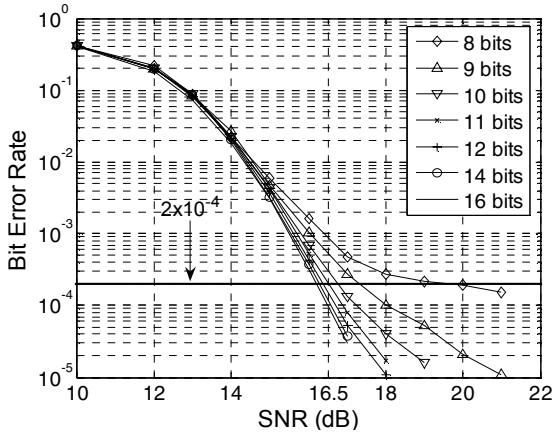

Fig. 4 The influence of bit-precision of the CSAD filter on the average BER

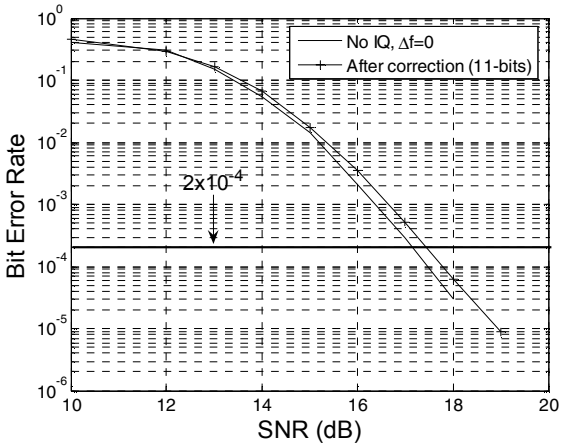

Fig. 5. The average BER achieved with the CSAD filter operating in the Ricean channel given in [6] and in the presence of 2000 Hz frequency offset

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