Experimental Evaluation of the MPPT Hardware for Vehicle Solar Arrays with Silicon Junction Cells

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***Abstract*-This paper studies the design of the solar vehicle distributed Maximum Power Point Tracking (MPPT) hardware intended for silicon junction cell applications. The MPPT hardware operates in an input voltage range from 0.9 V to 1.8 V and is suited for a power tracking group of four series connected silicon cells. The finished MPPT hardware measures 17 mm by 21 mm and has a nominal power rating of 600 mW. The power loss measurement through the calorimetric method verifies a power conversion efficiency of 93.9%. An analogue solar cell simulator is also employed to evaluate the performance of the MPPT hardware. The experimental results are shown at the end of the paper and confirm that high tracking accuracy has been achieved under both the static and the dynamic insolation conditions.**

I. INTRODUCTION

To solve the crisis in fossil fuel and global warming, the research and development efforts in hybrid and electric vehicles have drastically increased over the last decade. Automotive manufacturers are selling more hybrid vehicles and these will certainly become a core segment of the automotive market in the near future [1], [2]. Solar arrays present the opportunities to serve as the additional energy input or the range extender in the hybrid and electric vehicles [3], [4].

A highly distributed Maximum Power Point Tracking (MPPT) scheme has been previously proposed for the vehicular applications, where the solar cells have curvature and are subject to rapid insolation changes caused by road-side vegetation and structures [5]. A single-cell MPPT device based on the current sensorless Incremental Conductance (IncCond) method has been also developed [6]. This device is designed specifically for the high performance triple junction solar cells. The cell voltage of a triple junction cell at Maximum Power Point (MPP) under one sun insolation and 28°C is higher than 2 V as show in Fig. 1 [7]. Since the MPP cell voltages of the triple junction cell under most environmental conditions are greater than 1.8 V, a 1.8-V microprocessor, Texas Instrument MSP430, is used in that design and can be powered directly by a single cell. However, the crystalline silicon technology accounts for about 90% of the world solar cell production [8]. The I-V curve of the silicon solar cells under one sun insolation and 28°C is shown in Fig. 2 [9]. The MPP cell voltage of the silicon junction cell is significantly lower that that of the triple junction cell and can be as low as 0.3 V [10]. Therefore, at least seven or eight silicon cells must be series connected to supply one MPPT device and the benefit of the highly distributed MPPT scheme will be greatly undermined.

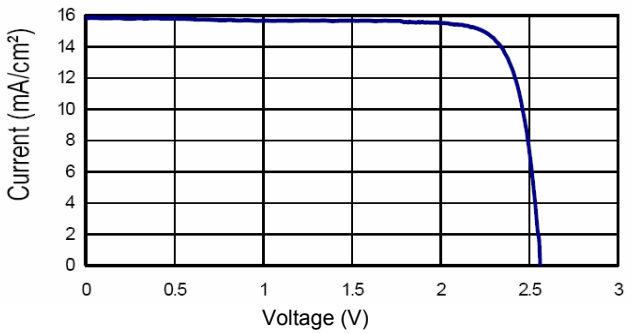

Fig. 1. Triple Junction Cell I-V Curve in [7]

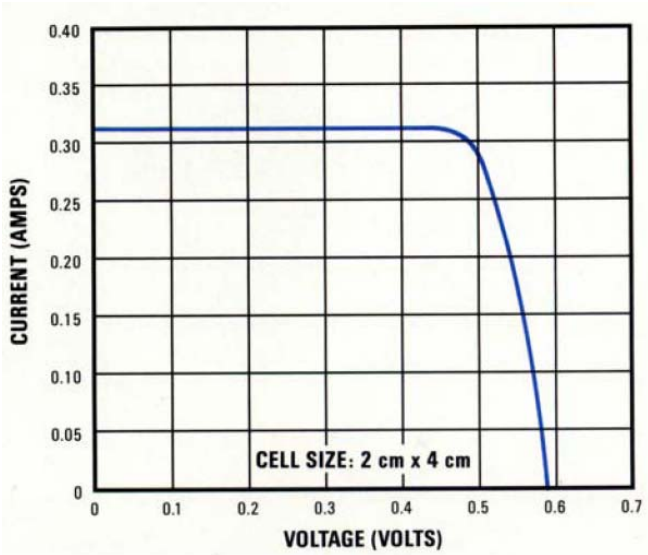

Fig. 2. Silicon Junction Cell I-V Curve in [9]

In order to improve the overall MPPT performance and reduce the number of cells for each MPPT device, this paper studies the design of the MPPT hardware suited for an input voltage from 0.9 V to 1.8 V. This input voltage range will enable a group of three to four series connected silicon cells to supply one MPPT device. The component selection process is discussed in detail. Significant effort has been made to reduce the size and the cost while maintaining the overall performance. The calorimetric method is used to establish the power loss of the 600-mW converter with 20-kHz switching frequency. The MPPT hardware has also achieved excellent performances under a set of static and dynamic tests through the solar cell simulator and the results are provided at the end of the paper.

II. MPPT Circuit Diagram

Individual MPPT device employs the buck converter topology therefore multiple buck converters can be connected in series and share a common inductor on the load side [11]. The MPPT algorithm is based on the IncCond method but removes the need for the current sensor [12]-[14]. A low-power Texas Instrument microprocessor MSP430, with a supply voltage range from 1.8 V to 3.6 V, handles both voltage sensing and switching duty ratio calculation tasks in order to track the MPP of the solar cell. In the design of the MPPT hardware for the triple junction solar cells, the microprocessor is directly supplied from the single triple junction cell. The microprocessor then drives a four-stage diode capacitor charge pump to supply the MOSFET gate driver [11].

However, this design cannot be applied to the silicon junction cells due their much lower cell voltages unless seven or eight cells are connected in series to supply the microprocessor. In order to achieve a reasonable cost and good performance in the MPPT device for the silicon junction cells, a variation of the original design is proposed. Fig. 3 shows the circuit diagram for the new MPPT hardware. A high efficiency charge pump, Texas Instruments TPS60310, is able to transform the input voltage between 0.9 V and 1.8 V to an output voltage of 3.3 V and supply the microprocessor MSP430. The microprocessor then drives a two-stage diode capacitor charge pump circuit to supply the drive circuit for the MOSFETs in the buck converter. This design variation will not increase the size of the MPPT hardware significantly as the charge pump TPS60310 is available in 10-pin MSOP package, which has a physical size of 3.05 mm × 4.98 mm (0.12 in × 0.20 in) [15].

III. Component Selection Process

In the component selection process, only the surface mount components are considered due to their small sizes and low profiles. The other two overwhelming factors including the power losses and the prices are also considered.

In the selection of the microprocessor, the Texas Instrument ultra-low power microcontroller family, MSP430, is considered. MSP430 microprocessors have a supply voltage ranging between 1.8 V and 3.6 V and an active operation current ranging between 160 μA and 400 μA. Since an Analogue Digital Converter (ADC) is a must and the program size is less 1 KB, MSP430F1122 with 4 KB flash memory is selected. This microprocessor is not equipped with a hardware multiplier therefore the cost can be minimised.

The conduction power loss in the input capacitor C_1 can be estimated by:

$$P_{C1} = I_{C,rms}^2 R_C \tag{1}$$

where I_C is the capacitor effective current and R_C is the Equivalent Series Resistance (ESR) of the capacitor.

The dynamic performance tests have also shown that at least 200-μF capacitance is required at the converter input to achieve a fast response [16]. Therefore, two 100-μF tantalum capacitors with 150-mΩ ESR each are used. A bonus of this arrangement is that the equivalent resistance is halved by connecting two capacitors in parallel. Recently, 100-μF ceramic multilayer capacitors, such as Kemet C1210C107M9PAC-TU, have become available. They will be a better replacement of the tantalum capacitors due to their longer lifetime and lower ESR. However, their price is currently higher than $1 US each and this makes them not suitable for the low-cost MPPT hardware implementation [17], [18].

The selected dc-dc charge pump converter TPS60310 is able to achieve a high power conversion efficiency with only four additional 1-μF capacitors compared with the original design for triple junction cells. No inductors are required and this contributes to the cost and space saving in the MPPT converter design.

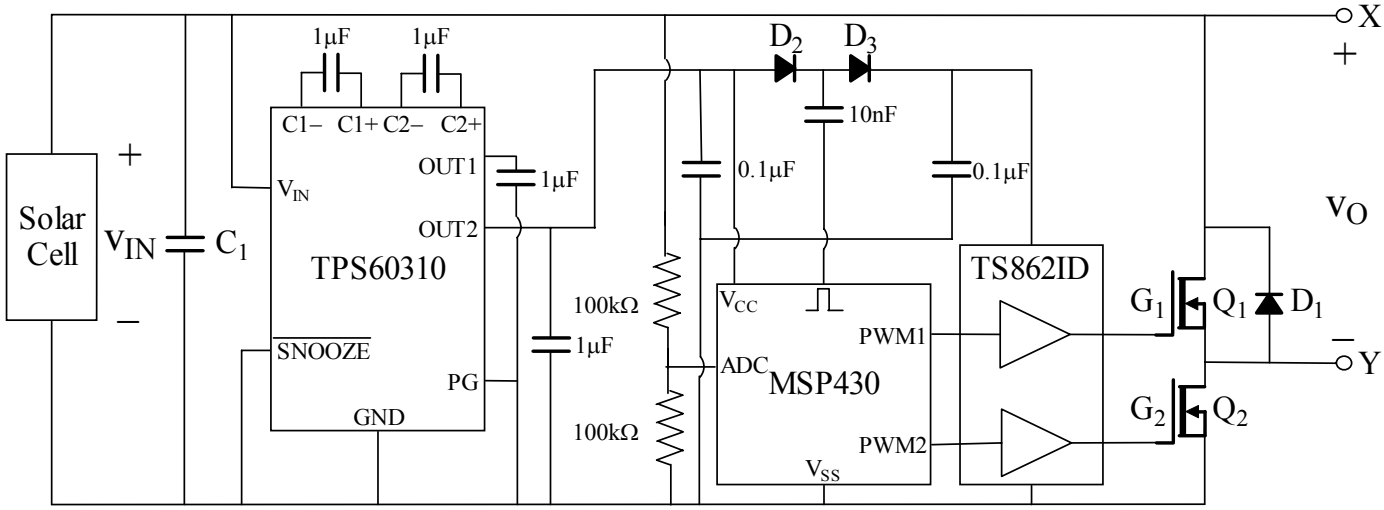

Fig. 3. MPPT Hardware Circuit Diagram

In order to maximise the efficiency of the diode-capacitor charge pump circuit, both low forward voltage drop and low junction capacitance are the important criteria in the selection of the diodes D_2 and D_3. Schottky diode, BAS125-07W, is selected as it features a standard forward voltage drop of 0.385 V and an extremely low junction capacitance of 1.1 pF.

The MOSFET gate driver must also have a low power consumption therefore CMOS comparator TS862ID is selected. Two comparators are integrated into one package and the design features an ultra-low current consumption of 6 μA per comparator at 2.7-V supply voltage. The push pull output of the comparator also removes the need for the pull up resistors when connecting to the MOSFET gate.

The power loss in the MOSFET includes both driving and conduction losses. The gate driving power loss in each MOSFET is:

$$P_{Q,drive} = C_G V_{drive}^2 f_s \tag{2}$$

where C_G is the MOSFET gate capacitance, V_{drive} is the driver supply voltage and f_s is the MOSFET switching frequency. As the MOSFET gate capacitance is not a constant, the power loss in Equation (2) can be better approximated by:

$$P_{Q,drive} = Q_G V_{drive} f_s \tag{3}$$

where Q_G is the MOSFET total gate charge.

The conduction power loss in each MOSFET is:

$$P_{Q,cond} = I_{Q,rms}^2 R_{DS(on)} \tag{4}$$

where $I_{Q,rms}$ is the MOSFET effective current and $R_{DS(on)}$ is the MOSFET drain source on resistance.

Finally, the MOSFET IRF7821 is selected with a maximum drain source on resistance of 12.5 mΩ and a maximum total gate charge of 14 mC.

In order to reduce the power loss during the dead time when both MOSFETs Q_1 and Q_2 are turned off, a Schottky diode is connected in reverse parallel with the synchronous MOSFET to provide the current path. The reverse recovery performance of the Schottky diode is much superior to that of the MOSFET embedded body diode. The conduction loss in the diode D_1 can be estimated by:

$$P_D = I_D V_F T_{dead} f_s \tag{5}$$

where I_D is the current in the diode D_1, V_F is the forward voltage drop and T_{dead} is the dead time.

Finally the diode 10BQ015 is selected due to its low price and its forward voltage drop is 0.35 V. The dead time is determined by the clock frequency of the microprocessor. It is one cycle of the clock, which is 0.02 s in this design.

The costs of the key components discussed above are shown in Table I. These prices are based on an order quantity of 10,000 units from three suppliers including Avnet, Digi-Key and Newark InOne [17]-[19]. The total cost of the key components is $6.06 US. The actual manufacturing cost will be slightly higher than this considering the cost of the ancillary surface mount components including two resistors and seven capacitors as well as the Printed Circuit Board (PCB) cost. The photo of the prototype MPPT hardware built in the laboratory is shown in Fig. 4. It has achieved a size of 17 mm × 21 mm (0.67 in × 0.83 in). Due to the design optimisation, this is slightly smaller than the size of the original converter for triple junction cell, 18 mm × 21 mm (0.71 in × 0.83 in) [6].

IV. Power Loss Measurement

The MPPT device has a power rating of 600 mW and the power loss is only a small percentage of the rated power. In addition, the converter employs an inductorless design therefore the output voltage and current will have significant switching frequency components. It becomes impossible to obtain an accurate power loss through the voltage and current measurement. Instead, the calorimetric method is employed [20], [21]. In order to achieve a good accuracy, the converter is submerged in the insulation oil inside a thermos flask. To maintain the temperature outside the thermos flask to be constant, the flask is located inside a beer cooler, which is placed inside an electronically controlled environmental chamber. The following two steps have been performed.

First, a calibration curve is obtained with a 1-kΩ resistor with 1% tolerance. A circuit made of a Wheatstone bridge with four platinum sensing resistors [22] and a precision operational amplifier MAX430 is used to convert the difference between the temperatures inside and outside of the thermos flask into a voltage measurement with a gain of 1000. The National Instrument LabVIEW software records the voltage readings every 15 minutes. The calibration curve is shown in Fig. 5, where the horizontal axis is the power loss in the resistive load and the vertical axis is the voltage output of the measurement circuit. The voltage values used in the calibration curve are the average values of the 12 data recorded in LabVIEW after the thermal equilibrium is reached. Error bars are also shown in Fig. 5. They have confirmed a maximum variation in the voltage measurement of 15 mV, which is equivalent to a variation of 0.08 °C in the temperature measurement.

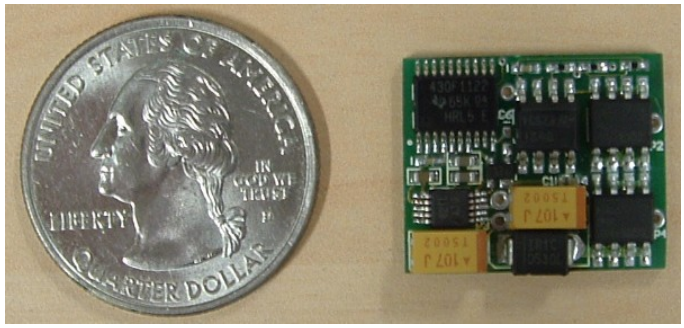

Fig. 4. Photo of the MPPT Hardware

TABLE I
KEY COMPONENT COSTS IN THE MPPT HARDWARE

Component	Manufacturer	Manufacturer Part Number	Unit Price (US$)	Supplier	Number of Components Required
Microprocessor	Texas Instrument	MSP430F1122IPW	2.40	Avnet	1
Capacitor C_1	AVX Corporation	TPSC107K006R0150	0.286	Avnet	2
Charge Pump	National Semiconductor	TPS60310DGSR	1.26	Avnet	1
Diodes D_2 and D_3	Infineon	BAS125-07W	0.1432	Avnet	1
Comparator	STMicroelectronics	TS862ID	0.806	Digi-Key	1
MOSFETs Q_1 and Q_2	International Rectifier	IRF7821PBF	0.408	Avnet	2
Diode D_1	International Rectifier	10BQ015	0.066	Digi-Key	1
Total	-	-	6.06	-	-

In the second step, the system under test remains undisturbed while the calibration resistive load is disconnected from the power supply and the MPPT converter is turned on. The converter operates under an input voltage of 1.794 V and an input current of 0.313 A, which are close to the MPP conditions of four series connected silicon solar cells used in due course. A total power loss of 34.0 mW in the converter has been observed. Under the input power of 561.5 mW, this is equivalent to an overall efficiency of 93.9%.

V. TRACKING PERFORMANCES

A solar simulator made of a switched current source and a solar panel consisting of four silicon cells is built to evaluate the tracking performance of the MPPT hardware as shown in Fig. 6. The solar simulator I-V and P-V characteristics are obtained by charging a capacitor from the short circuit to the open circuit conditions and respectively shown in Figs. 7 and 8, where three different line types respectively model the 0.1-sun, 0.5-sun and 1-sun insolation conditions of the silicon solar cell panel.

Table II shows the MPP voltages, currents and powers under the three set insolation conditions of the solar simulator obtained from the I-V and the P-V curves and Table III shows those obtained from the MPPT hardware. It can be confirmed that good static tracking efficiencies can be obtained under the three insolation conditions

The dynamic tracking performance test simulates the solar cell travelling at 20 ms^{-1} across alternate 1-m light and 1-m shadow sections under two of the three set insolation conditions shown in Table II. The experimental waveforms of the cell powers when the cell is subject to step insolation changes between 1 and 0.5 sun are shown in Figs. 9 and 10 and those when the cell is subject to step insolation changes between 1 and 0.1 sun are shown in Figs. 11 and 12. In Figs. 9 to 12, the solid, the dashed and the dashed-dotted lines respectively represent the actual, the maximum available and 90% of the maximum available cell powers. The energy and power losses are calculated with MATLAB and shown in Table IV. Compared with the data in Table II, the power losses represent respectively 2.5% or 8.5% under insolation changes between 1 and 0.5 sun or 1 and 0.1 sun.

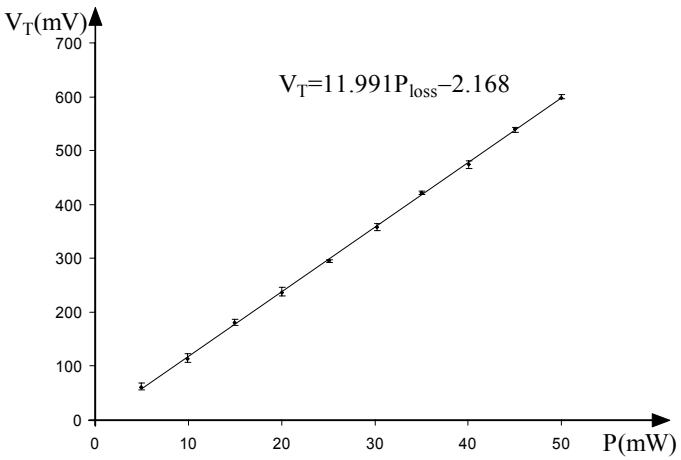

Fig. 5. Calorimetric Calibration Curve

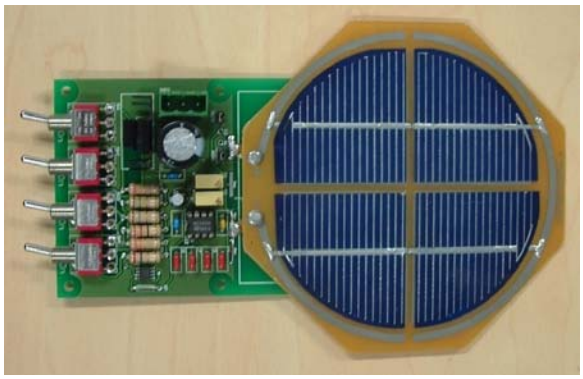
Fig. 6. Solar Simulator with Four Silicon Cells

TABLE II
SOLAR SIMULATOR MPP CHARACTERISTICS

Insolation	Voltage (V)	Current (A)	Power (W)
0.1 Sun	1.353	0.026	0.036
0.5 Sun	1.677	0.156	0.261
1 Sun	1.774	0.323	0.573

TABLE III
MEASURED MPPS AT THREE INSOLATION LEVELS

Insolation	Voltage (V)	Current (A)	Power (W)	Tracking Efficiency
0.1 Sun	1.235	0.027	0.034	94.4%
0.5 Sun	1.713	0.146	0.250	95.8%
1 Sun	1.777	0.315	0.562	98.1%

TABLE IV
MPPT HARDWARE DYNAMIC LOSSES

Initial and Final Insolation Conditions	1 and 0.5 Sun	1 and 0.1 Sun
Energy Loss in Step Down (mJ)	0.346	0.508
Energy Loss in Step Up (mJ)	0.714	2.228
Power Loss (mW)	10.6	27.4

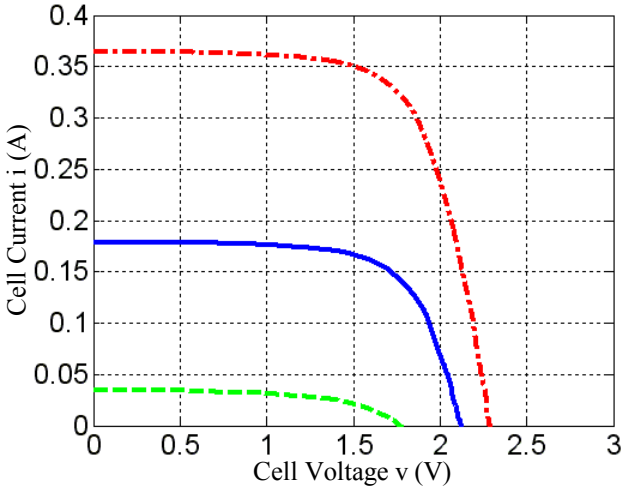

Fig. 7. Solar Simulator I-V Curve

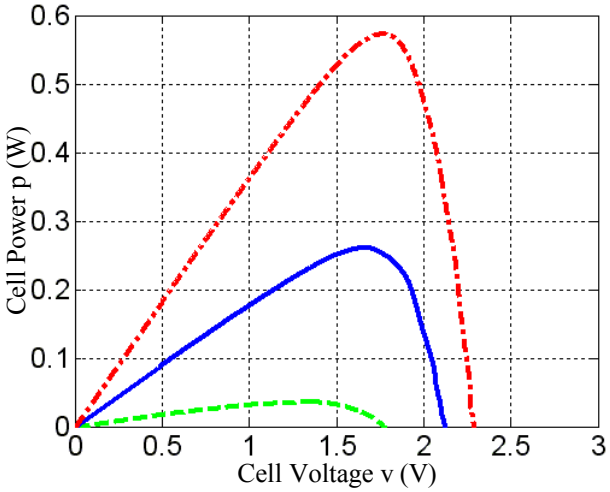

Fig. 8. Solar Simulator P-V Curve

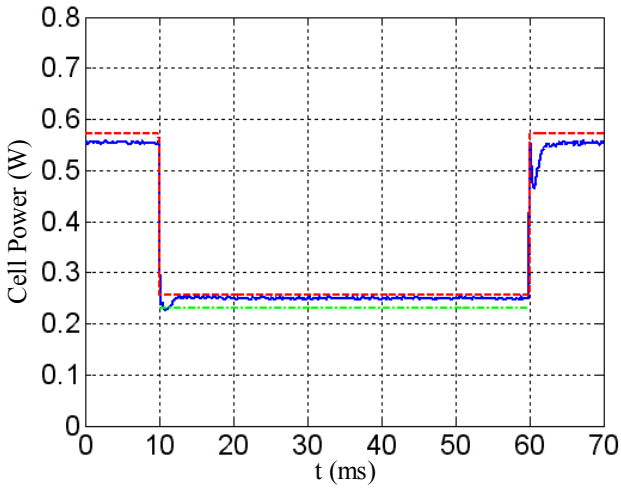

Fig. 9. Cell Power over 1-m Shadow (1 to 0.5 Sun)

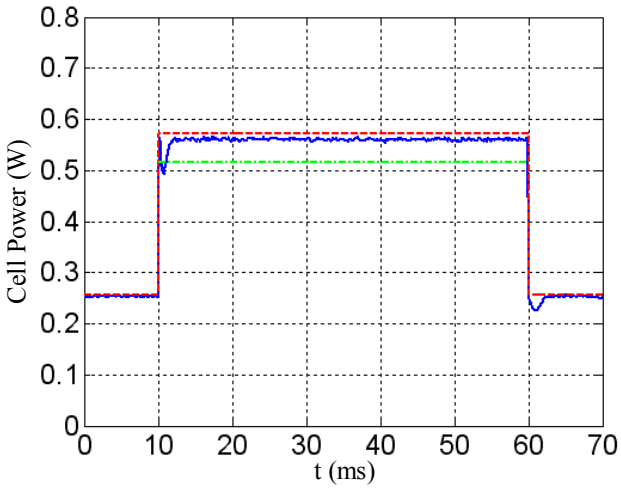

Fig. 10. Cell Power over 1-m Gap (1 to 0.5 Sun)

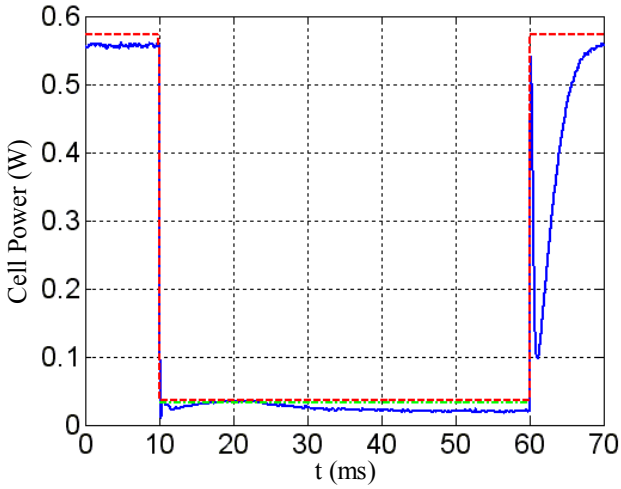

Fig. 11. Cell Power over 1-m Shadow (1 to 0.1 Sun)

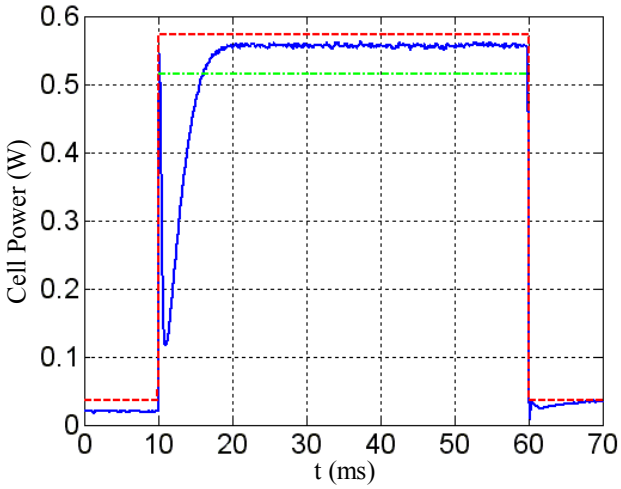

Fig. 12. Cell Power over 1-m Gap (1 to 0.1 Sun)

VI. Conclusions

In this paper, a maximum power point tracker with a 0.9 to 1.8 V input voltage is proposed. The MPPT device is specifically designed for vehicle arrays with silicon junction cells and the individual MPPT hardware can be supplied from a group of three to four solar cells. The component selection process considering the size, the power loss and the cost is studied in detail and the finished design has a size of 17 mm × 21 mm (0.67 in × 0.83 in) at a cost close to $6 US. The MPPT hardware has also achieved a high power conversion efficiency of 93.9%, a minimum static tracking efficiency of 94.4% and a maximum dynamic power loss of 8.5% under the three set insolation conditions of the solar simulator.

Acknowledgement

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