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The Power Loss Optimization of a Current Fed ZVS Two-Inductor Boost Converter With a Resonant Transition Gate Drive

Quan Li, *Member, IEEE*, and Peter Wolfs, *Senior Member, IEEE*

***Abstract*—This paper develops a power loss optimization method in a current fed zero-voltage switching (ZVS) two-inductor boost converter, which is suitable for the module integrated converter applications in grid interactive photovoltaic systems. The paper conducts the numerical analysis of the variable power loss components and establishes a set of the circuit parameters for an optimized operating point with a minimized average power loss. The ZVS two-inductor boost cell is fed from a sinusoidally modulated two-phase synchronous buck converter with an interphase transformer and produces a rectified sinusoidal voltage, which can be applied to an unfolding stage to generate the grid compatible voltage. The boost cell is also equipped with a resonant transition gate drive circuit to reduce the power loss in the drive circuit under high frequency operations. The experimental results for a prototype 1-MHz 100-W ZVS two-inductor boost converter are presented at the end of the paper.**

***Index Terms*—Interphase transformer (IPT), module integrated converter (MIC), photovoltaic (PV), zero-voltage switching (ZVS).**

I. Introduction

THE TWO-inductor boost converter possesses significant advantages in the applications where a boost topology is required. Other than the high dc voltage gain, the converter also compares favorably with other current fed converters in regard to the switch voltage stress, the switch conduction loss and the transformer utilization [1], [2]. Therefore, the two-inductor boost converter has many applications where low dc input voltages need to be transformed to high dc output voltages [3]–[6], [23]. Recently, module integrated converters (MICs) have been proposed as an attractive alternative in the grid interactive photovoltaic (PV) applications [7]. In such applications, a high power density is certainly one of the most desirable features, which calls for high switching frequency operations. However, a high switching loss, together with the switch over voltage at turn-off caused by the transformer leakage inductance, becomes an inherent barrier for the hard-switched converter to obtain an acceptable efficiency under high switching frequency operations. In order to remove the switching loss and actively utilize the transformer leakage inductance, a zero-voltage switching (ZVS) two-inductor boost converter has been developed as a dc–dc conversion stage in the MICs [8]. Fig. 1 shows the ZVS two-inductor boost converter with an inverter. In the soft-switched two-inductor boost converter, the parasitic components including the transformer leakage inductance and the metal–oxide–semiconductor field-effect transistor (MOSFET) output capacitance are absorbed into the resonant network. This enables the MOSFET to switch at zero voltage, resulting in a theoretical zero switching loss. A major loss issue in the hard switched converter is the switching loss in the output rectifier diode. The ZVS cell provides soft switching conditions for the diodes. It is tolerant of switching device capacitance and delivers limited di/dt and dv/dt for the diodes making operation at high frequencies possible with the loss in the diodes being nearly entirely conduction related. In hard-switched converters, the diode reverse recovery loss is potentially more than the primary side MOSFET conduction loss.

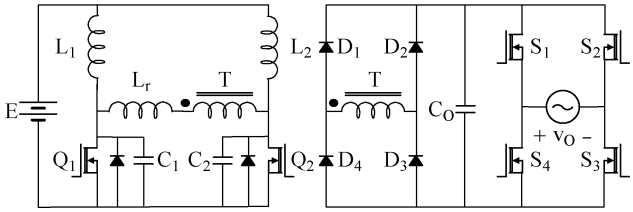

Fig. 1. ZVS two-inductor boost converter with an inverter.

In this voltage fed converter, the dc gain of the dc–dc conversion stage is a constant and the dc link offers a fixed voltage to the following dc–ac inversion stage. In order to generate low frequency grid compatible voltage waveforms, pulsewidth modulation (PWM) must be employed in the inversion stage. However, this design suffers from the high switching loss in the dc–ac inversion stage as well as a complex control circuitry required by the PWM technique.

This paper proposes a resonant two-inductor boost converter, where a two-phase synchronous buck converter acts as a variable current source for the ZVS boost cell, as shown in Fig. 2. The buck and the boost stages are combined through an interphase transformer (IPT). The resonant two-inductor boost cell operates under ZVS conditions and produces an output with a rectified sinusoidal waveform. This reduces the following dc–ac inversion stage to an unfolder with simple grid frequency control. Although the proposed converter requires four additional MOSFETs compared with the solution shown in Fig. 1, they appear only on the low-voltage side of the dc–dc converter and can be implemented by the MOSFETs with low voltage ratings. Therefore, the overall cost of the converter will not be significantly increased.

This paper identifies the power loss components that vary against the circuit parameters and numerically analyzes the av-

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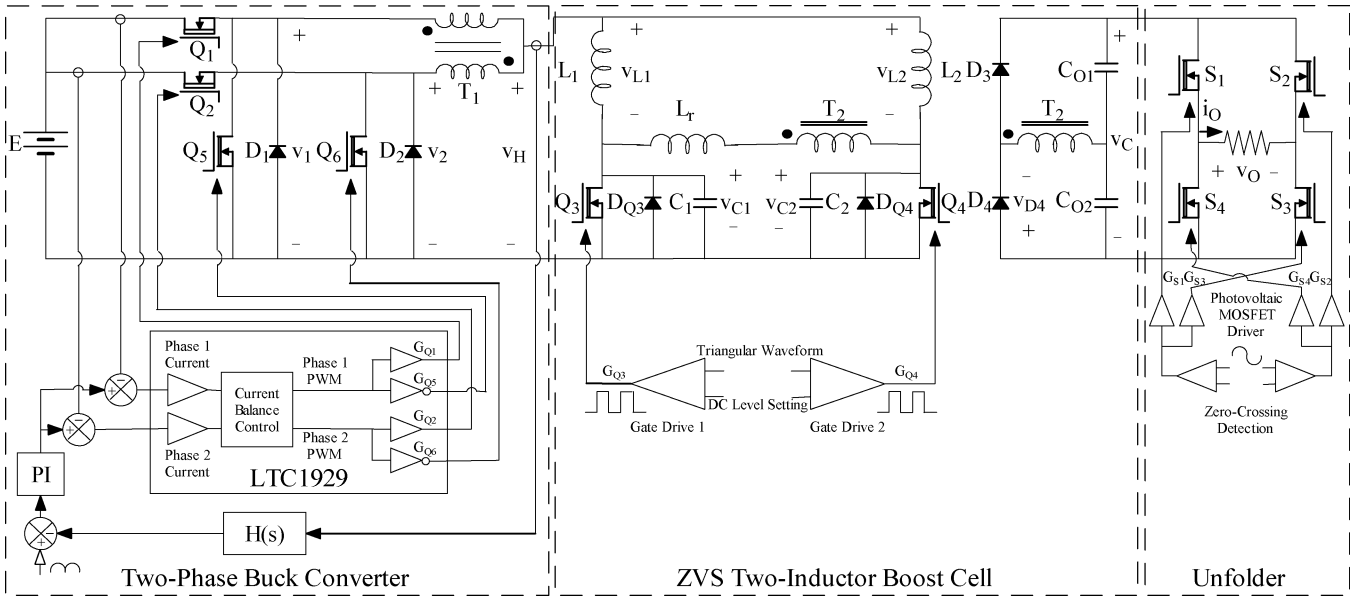

Fig. 2. ZVS two-inductor boost converter with an unfolder.

erage variable power loss in the ZVS two-inductor boost cell operating under different circuit parameters. Then power loss optimization in the ZVS boost cell can be carried out with the visual surface plots established through MATLAB. A resonant transition gate drive with theoretical zero power loss is also employed to drive the two MOSFETs in the boost stage. The experimental results for a 1-MHz 100-W prototype converter are provided at the end of the paper to prove the theoretical analysis.

II. Current Fed ZVS Two-Inductor Boost Converter

Although the voltage fed ZVS two-inductor boost converter is able to operate with a variable dc gain under variable frequency control [9], a wide output voltage range including zero is not possible as it is a boost-derived converter. In order to achieve a variable output including zero voltage, a buck stage must be added. In the proposed converter shown in Fig. 2, a two-phase synchronous buck converter with an IPT functions as a variable current source to the ZVS boost cell so that a zero voltage can be achieved on the dc link. The employment of the IPT doubles the switching frequency of the buck conversion stage and avoids the penalty of the potential higher switching losses in the hard-switched buck converter. The converter input voltage is 20 V. The switching frequencies for the buck and the boost stages are, respectively, $f_{\rm buck} = 250$ kHz and $f_{\rm boost} = 500$ kHz. The buck stage duty ratio $D_{\rm buck}$ is modulated in the sinusoidal manner and the boost stage duty ratio $D_{\rm boost}$ can be fixed at a constant value.

In the ZVS two-inductor boost cell, the transformer leakage inductance and the MOSFET output capacitance are used as part of the resonant inductor and capacitors. The resonance between the resonant inductor and capacitors creates a ZVS condition for the MOSFETs and the switching loss can be completely removed [8]. The resonance of the converter can be analyzed using the equivalent circuit shown in Fig. 3 within one boost stage switching period, when the input current to the two-inductor

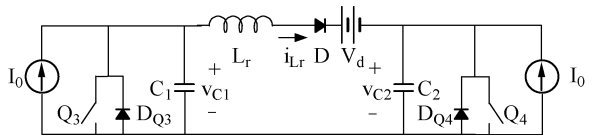

Fig. 3. Equivalent resonant circuit.

boost cell can be considered as a constant. $L_{\rm r}$ is the effective resonant inductor and $C_1 = C_2 = C_{\rm r}$ are the effective resonant capacitors. $D_{\rm Q3}$ and $D_{\rm Q4}$ are the embedded reverse body diodes of the MOSFETs. The current source I_0 models the input inductor L_1 or L_2. The voltage source $V_{\rm d}$ is the voltage of the capacitor $C_{\rm O1}$ or $C_{\rm O2}$ reflected to the transformer T_2 primary winding and the diode D corresponds to the diodes in the voltage-doubler rectifier. The arrangement for $V_{\rm d}$ and D assumes a positive resonant inductor current $I_{\rm Lr}$ as illustrated and their polarities reverse when the resonant inductor current becomes negative.

Three important circuit parameters determine the resonant condition of the ZVS two-inductor boost cell.

- The load factor k, which is defined by $I_0 Z_0 = {\rm k}V_{\rm d}$, where $Z_0 = \sqrt{L_r/C_r}$ is the characteristic impedance of the resonant tank. It is required that k be greater than or equal to one to allow the resonant capacitor voltage to return to zero so that the ZVS condition can be maintained.
- The timing factor Δ_1, which determines the initial inductor current when the MOSFET Q_3 or Q_4 turns off.
- The delay angle $\alpha_{\rm d}$ is the angle between the instant when the inductor current falls to zero and the instant when the corresponding MOSFET turns off.

The state analysis is demonstrated below. Before Q_3 turns off, both Q_3 and Q_4 are on. At time $t = t_0$, Q_3 turns off and the converter will move up to four possible states before Q_4 turns off as shown in Fig. 4.

- State (a) $(t_0 \le t \le t_1)$.

This state starts when Q_3 turns off. The initial conditions in State (a) are $i_{\rm Lr}(t_0) = -\Delta_1 I_0$ and $V_{\rm C1}(t_0) = 0$. In this state,

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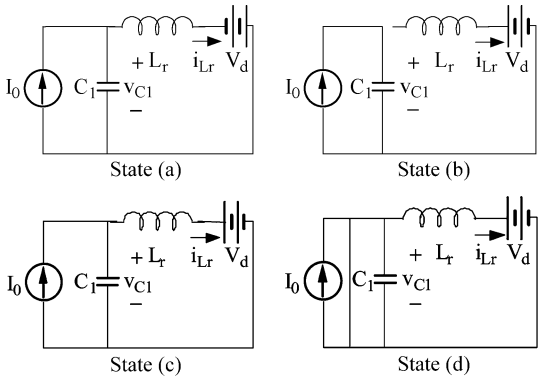

Fig. 4. Four possible states.

the current in the resonant inductor is still negative. This current and the current source I_0 charge the capacitor and the resonant inductor current decreases. The capacitor voltage $v_{\rm C1}$ and the inductor current $i_{\rm Lr}$ are, respectively

$$v_{C1}(t) = (1+\Delta_1)I_0 Z_0 \sin\omega_0(t-t_0) + V_d\cos\omega_0(t-t_0) - V_d \quad (1)$$

$$i_{Lr}(t) = \frac{V_d}{Z_0}\sin\omega_0(t-t_0) - (1+\Delta_1)I_0\cos\omega_0(t-t_0) + I_0 \quad (2)$$

where ω_0 is the angular resonance frequency of the resonant tank. This state does not exist if $\Delta_1 = 0$.

- State (b) $(t_1 \le t \le t_2)$.

This state starts when the current in the resonant inductor reaches zero and $V_{\rm d}$ reverses its polarity. If the capacitor voltage $v_{\rm C1}$ is still lower than $V_{\rm d}$, the diode D is reverse biased and the current source I_0 linearly charges the capacitor. The capacitor voltage $v_{\rm C1}$ and the inductor current $i_{\rm Lr}$ are, respectively

$$v_{C1}(t) = \frac{I_0}{C_r}(t-t_1) + v_{C1}(t_1) \quad (3)$$

$$i_{Lr}(t) = 0. \quad (4)$$

If the initial resonant inductor current in State (a) is sufficiently high to cause $v_{\rm C1}$ to exceed $V_{\rm d}$ at the end of State (a), this state will be bypassed.

- State (c) $(\mathrm{t}_2 \le \mathrm{t} \le \mathrm{t}_3)$.

This state starts when $v_{\rm C1}$ reaches $V_{\rm d}$ at the end of State (b) or $i_{\rm Lr}$ reaches zero if State (b) is bypassed. In this state, the capacitor resonates with the inductor. The capacitor voltage $v_{\rm C1}$ and the inductor current $i_{\rm Lr}$ are, respectively

$$v_{C1}(t) = I_0 Z_0 \sin\omega_0(t-t_2) + [v_{C1}(t_2) - V_d]\cos\omega_0(t-t_2) + V_d \quad (5)$$

$$i_{Lr}(t) = \frac{v_{C1}(t_2) - V_d}{Z_0}\sin\omega_0(t-t_2) - I_0\cos\omega_0(t-t_2) + I_0. \quad (6)$$

- State (d) $(t_3 \le t \le t_4)$.

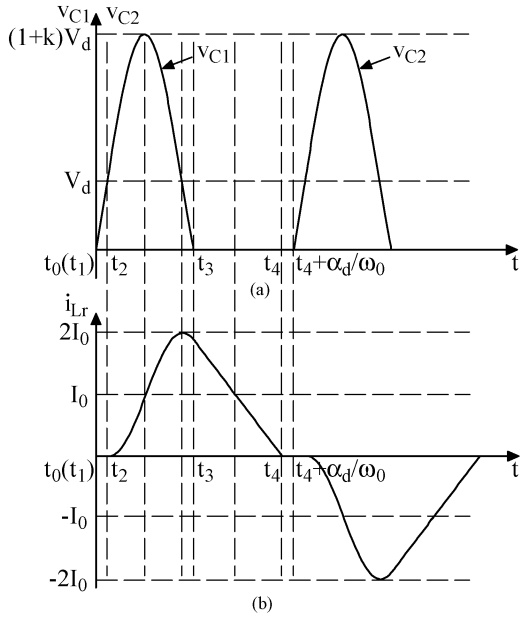

Fig. 5. Resonant waveforms in Region 1 (a) capacitor voltage and (b) inductor current.

This state starts when $v_{\rm C1}$ reaches zero. In this state, the resonant inductor is linearly discharged by $V_{\rm d}$. The capacitor voltage $v_{\rm C1}$ and the inductor current $i_{\rm Lr}$ are, respectively

$$v_{C1}(t) = 0 \quad (7)$$

$$i_{Lr}(t) = i_{Lr}(t_3) - \frac{V_d}{L_r}(t-t_3). \quad (8)$$

After Q_4 turns off, the above states repeat. The ZVS two-inductor boost cell is able to operate under two different regions: Region 1, where $\Delta_1 = 0$ and $\alpha_{\rm d} \ge 0$ and Region 2, where $\Delta_1 \ge 0$ and $\alpha_{\rm d} = 0$. A set of the resonant capacitor voltage and inductor current waveforms for Region 1 operation is shown in Fig. 5, where State (a) does not exist as $\Delta_1 = 0$ and t_0 and t_1 are overlapped with each other.

The theoretical gating waveforms of the MOSFETs Q_1 to Q_4 are drawn in Fig. 6, where the buck stage duty ratio $D_{\rm buck}$ is 20% and the buck stage switching period $T_{\rm buck}$ is twice the boost stage switching period $T_{\rm boost}$. The gate signal of Q_1 in the buck converter is synchronized with that of Q_3 in the ZVS boost cell. The IPT centre tap voltage $V_{\rm H}$ equals to the half converter input voltage when either Q_1 or Q_2 turns on. The voltage waveforms across the two input inductors L_1 and L_2 in the ZVS boost cell are respectively obtained from the difference of the cell input voltage $V_{\rm H}$ and the resonant capacitor voltage $V_{\rm C1}$ or $V_{\rm C2}$, which is given in the above state analysis. It is noteworthy that the inductor waveforms are not necessarily symmetric and vary with the buck stage duty ratio and the relative synchronization of the buck and the boost stages. The variation in the inductor waveforms will result in differences in the inductor current ripple.

In order to maintain the resonant condition of the current fed ZVS two-inductor boost converter, some attention must be paid to the non-linearity of the MOSFET output capacitance [10]. The low frequency term of the input current to the ZVS boost

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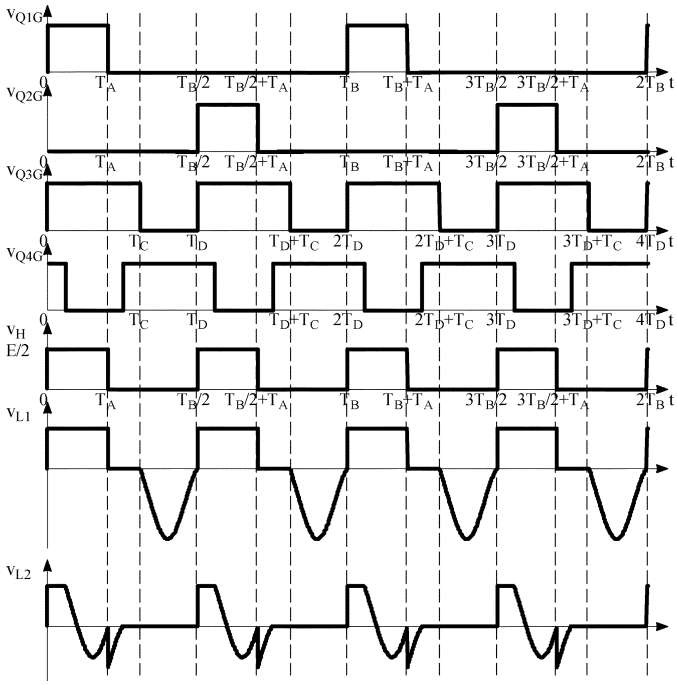

Fig. 6. Theoretical switching waveforms ($T_{\rm A} = D_{\rm buck}T_{\rm buck}$, $T_{\rm B} = T_{\rm buck}$, $T_{\rm C} = D_{\rm boost}T_{\rm boost}$, $T_{\rm D} = T_{\rm boost}$).

cell is a rectified sinusoidal waveform and this leads to different peak MOSFET drain source voltages over a low frequency cycle for a specific set of the circuit parameters. One simple solution is to select a switching frequency which requires a relatively large additional resonant capacitance therefore the MOSFET output capacitance only forms an insignificant portion of the total resonant capacitance. In this case, the variation of the MOSFET output capacitance can be safely neglected.

III. Power Loss Optimization of the ZVS Two-Inductor Boost Cell

In the current fed ZVS two-inductor boost converter, the buck conversion stage performs the wide range voltage control through the sinusoidal modulation of its switch duty ratio. Theoretically, the ZVS boost cell has the option to operate under any combinations of the three circuit parameters as the transformer turns ratio can be adjusted to provide the constant dc gain required in the boost conversion stage.

As different circuit parameters result in different resonant inductance and capacitance values under a specific load condition, the total power loss in the ZVS boost cell vary. The major power loss components in the ZVS two-inductor boost cell shown in Fig. 2 are listed below:

- the conduction loss in the two power MOSFETs Q_3 and Q_4;
- the power loss related to the series dc plus ac resistance of the resonant inductor $L_{\rm r}$;
- the power loss related to the equivalent series resistance (ESR) of the resonant capacitors C_1 and C_2;
- the copper and core loss in the two input inductors L_1 and L_2;
- the copper and core loss in the transformer T_2;
- the conduction loss in the two diodes D_3 and D_4 in the voltage-doubler rectifier.

In the physical construction of the ZVS two-inductor boost cell, the MOSFETs, the additional resonant inductor and the additional resonant capacitors are implemented by the components with the predetermined electrical characteristics. Therefore the first three power loss components vary with different circuit parameters. Under different circuit parameters, different resonant voltage and current waveforms are established in the ZVS cell and the power loss in each component varies. On the contrary, the last three power loss components can be kept constant. The input inductors and the transformer in the ZVS cell can be designed after the circuit parameters are selected and their windings can be configured to produce fixed total copper and core losses in the individual magnetic components. A major advantage of the ZVS two-inductor boost cell is the improvement in the operating conditions for the output rectifier diodes. The diode current falls with a di/dt which is controlled by the resonant inductor. The circuit is tolerant of the rectifier device capacitance and the reverse voltage reapplication rate is additionally limited. Limitations in both di/dt and dv/dt are important for high-frequency high-voltage applications. Hence, the power loss in the diodes is only load sensitive and will not vary significantly against different circuit parameters. Therefore in order to achieve a minimum total power loss in the ZVS two-inductor boost cell, only the variable power loss components in the MOSFETs, the resonant inductor and capacitors need to be considered. The three variable power loss components within a boost stage switching period is analyzed as follows.

- The power loss in the two MOSFETs $P_{\rm Q}$ is

$$P_Q = 2\left(I_{Q,rms}^2 R_{DS(on)} + I_{Q,avg} V_F\right) \tag{9}$$

  where $I_{\rm Q,rms}$ is the effective forward current in the MOSFET, $R_{\rm DS(on)}$ is the MOSFET drain source on resistance, $I_{\rm Q,avg}$ is the average reverse current in the MOSFET and $V_{\rm F}$ is the forward voltage drop of the MOSFET body diode. Both $R_{\rm DS(on)}$ and $V_{\rm F}$ can be obtained from the MOSFET datasheet.
- The power loss in the resonant inductor $P_{\rm Lr}$ is

$$P_{Lr} = I_{Lr,rms}^2 R_{Lr} \tag{10}$$

  where $I_{\rm Lr,rms}$ is the effective current in the resonant inductor and $R_{\rm Lr}$ is the series dc plus ac resistance of the resonant inductor.
- The power loss in the two resonant capacitors $P_{\rm Cr}$ is

$$P_{Cr} = 2I_{Cr,rms}^2 R_{Cr} \tag{11}$$

  where $I_{\rm Cr,rms}$ is the effective current in the resonant capacitor and $R_{\rm Cr}$ is the ESR of the resonant capacitors.

The total power loss $P_{\rm total,var}$ over a boost stage switching period which alters with different circuit parameters in the ZVS boost cell is

$$P_{\rm total,var} = P_Q + P_{Lr} + P_{Cr}. \tag{12}$$

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As the input voltage of the ZVS cell is modulated in the sinusoidal manner, the average power loss over a low frequency sinusoidal cycle, $P_{\mathrm{loss,avg}}$, must be established in order to identify the operating point with the minimum power loss in the ZVS cell. The process can be performed numerically with MATLAB.

In order to calculate the variable power loss components in the ZVS cell, a variety of the current terms and the equivalent series resistances of the resonant inductor and capacitors in (9)–(11) must be obtained. The current terms can be obtained through the state analysis as shown in Section II while the series resistance of the resonant inductor and the ESR of the resonant capacitors cannot be directly obtained. The resistance terms must be further derived with two other direct results through the state analysis

$$\gamma = \frac{\omega_0}{f_{\mathrm{boost}}} \tag{13}$$

$$Z_0 = \frac{kV_d}{I_0}. \tag{14}$$

The definitions of the series dc plus ac resistance of the resonant inductor, the ESR of the resonant capacitor and the characteristic impedance of the resonant tank are, respectively

$$R_{Lr} = \frac{2\pi f_{\mathrm{boost}} L_r}{Q} \tag{15}$$

$$R_{Cr} = \frac{DF}{2\pi f_{\mathrm{boost}} C_r} \tag{16}$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} = \omega_0 L_r = \frac{1}{\omega_0 C_r} \tag{17}$$

where Q is the quality factor of the resonant inductor and DF is the dissipation factor of the resonant capacitor.

Manipulations of (13)–(17) and solving for R_{Lr} and R_{Cr} yield

$$R_{Lr} = \frac{2\pi Z_0}{Q\gamma} \tag{18}$$

$$R_{Cr} = \frac{DF\gamma Z_0}{2\pi}. \tag{19}$$

In the numerical calculation of the average variable power loss in the ZVS boost cell, the following component parameters are used [11], [12]:

- $R_{\mathrm{DS(on)}} = 0.027\ \Omega$ and $V_{\mathrm{F}} = 1.5$ V for STB50NE10 MOSFETs;
- $Q = 96$ at 500 kHz for the air core toroidal inductor with Litz wire;
- $DF = 1/6000$ at 500 kHz for Cornell Dubilier surface mount mica capacitors.

The selection of a MOSFET with 100-V drain source voltage rating will be justified in due course as certain combinations of the circuit parameters will cause the peak MOSFET voltage to be greater than 100 V.

It is worth mentioning that as the transformer leakage inductance and the MOSFET output capacitance, respectively, forms part of the resonant inductor and capacitors, the actual power losses of these components will be different from the results obtained through (10) and (11) if the above component parameters are used. However, under the assumption that the values of the parasitic components are relatively small compared with the resonant inductance and capacitance values, the errors in the results of (10) and (11) are unlikely to be large.

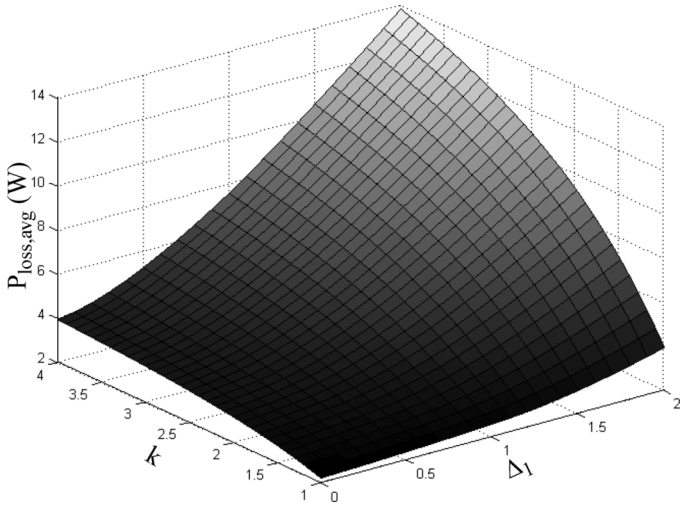

Fig. 7. Surface $P_{\mathrm{loss,avg}}$ in Region 2.

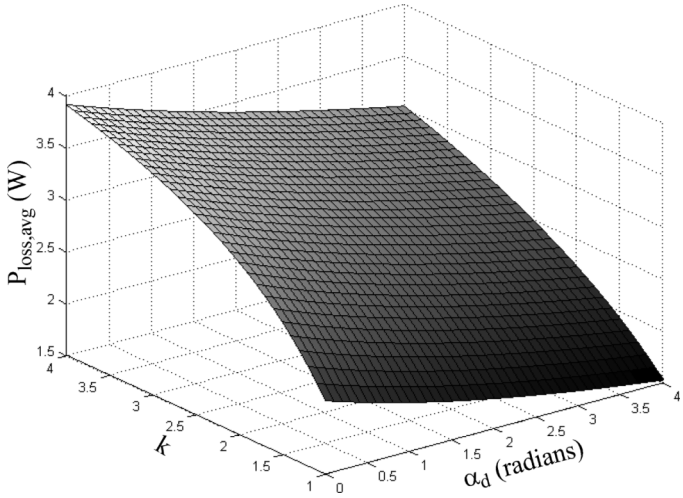

Fig. 8. Surface $P_{\mathrm{loss,avg}}$ in Region 1.

Figs. 7 and 8, respectively, shows the surface of the average variable power loss $P_{\mathrm{loss,avg}}$ in Regions 2 and 1 in the ZVS cell with an average output power of 100 W. Fig. 7 shows the average power loss when $1 \leq k \leq 4$ and $0 \leq \Delta_1 \leq 4$. In this region, the lowest average power loss occurs when $k = 1$ and $\Delta_1 = 0$, which is 2.21 W.

Fig. 8 shows the average power loss when $1 \leq k \leq 4$ and $0 \leq \alpha_{\mathrm{d}} \leq 4$. In this region, the average power loss can be further lowered. It can be observed that under the same k value, the greater the α_{d} value, the lower the average power loss. However, a higher peak switch voltage appears while α_{d} increases as shown by the surface V_{peak} in Fig. 9. A peak switch voltage of 100 V is set in the converter operation to obtain a low MOSFET forward resistance. MOSFET input capacitance increases considerably for the same value of the forward resistance at a higher

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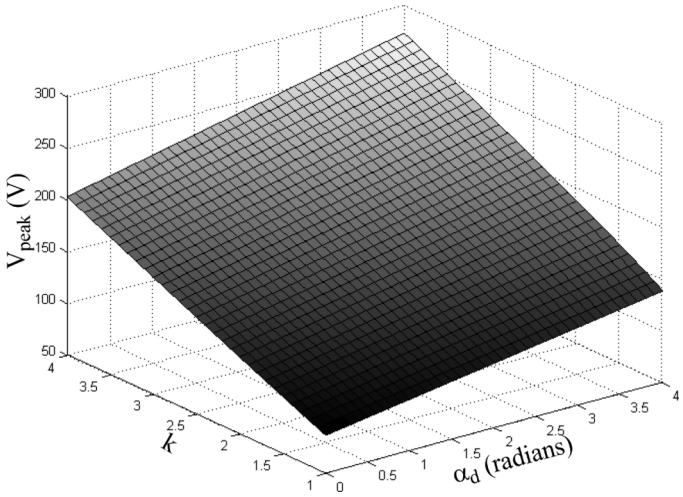

Fig. 9. Surface $V_{\rm peak}$ in Region 1.

voltage rating as the product of the input capacitance and forward resistance increases with drain-source voltage rating [13]. A larger MOSFET input capacitance demands a higher power from the drive circuit and lowers the converter overall efficiency. Another reason to choose a lower $\alpha_{\rm d}$ value is that the gradient of the surface $P_{\rm loss,avg}$ along the $\alpha_{\rm d}$ axis is very small. When $k = 1$ and $0 \leq \alpha_{\rm d} \leq 4$, the average gradient of the power loss against $\alpha_{\rm d}$ is -0.17 W/radian, while that of the peak switch voltage against $\alpha_{\rm d}$ is 12.9 V/radian. Figs. 8 and 9 show that the changes of the power loss and the peak switch voltage along the $\alpha_{\rm d}$ axis under the same k value are both monotonic. The ZVS operating condition requires $k \geq 1$. The final circuit parameters for the minimal power loss in the ZVS boost cell are $k = 1.1$, $\Delta_1 = 0$, and $\alpha_{\rm d} = 0$. Under this condition, the average power loss is 2.33 W and the peak switch voltage is 90 V. The safety margin for k to maintain the ZVS condition is justified by the numerical results from MATLAB, which show that the increase of k from 1 to 1.1 when $\Delta_1 = 0$ and $\alpha_{\rm d} = 0$ only raises the average power loss by an insignificant amount of 0.12 W. The power losses in the individual devices under the selected operating condition are given in Table I. It can be seen that the power losses in the two MOSFETs and the resonant inductor are the two major loss components as the dissipation factor of the resonant capacitor used in the resonant cell is extremely low.

Once the circuit parameters are determined, other important values in designing the ZVS cell can be obtained as the following:

- the resonant inductance is 1.40 μH;
- the resonant capacitance is 15.7 nF;
- the ratio of the transformer primary to the low frequency term of the input voltages in the ZVS two-inductor boost cell is 2.15.

IV. Resonant MOSFET Gate Drive Circuit

In the design of the ZVS two-inductor boost cell, care must be taken in selecting the MOSFETs as higher current and voltage stresses exist due to the resonant feature. MOSFETs with low drain source on resistances are preferred so that the increase in the conduction power loss, if there is any, will not cancel the reduction in the switching power loss. However, a low MOSFET drain source on resistance normally demands a large die size and the MOSFET input capacitance tends to be large [14]. In the conventional MOSFET gate drive circuit, the drive power loss is proportional to the switching frequency [15], [24]. Although the conventional MOSFET gate drivers have compact packages and are relatively easy to use, the drive power may become a significant portion of the total power loss when the switching frequency is high and this could reduce the converter overall efficiency remarkably. For example, if the above selected MOSFET STB50NE10 is used in the ZVS boost cell, only $\rm CV^2$ loss of the two MOSFETs will be 1.5 W at 500-kHz switching frequency with 12-V power supply. The actual drive power loss could be much higher than this as the losses due to the cross conduction and the hard-switching condition in the drive circuit are also contributing factors, which cannot be ignored [16]. Therefore, the selection of a MOSFET drive circuit which is capable of avoiding these power loss components plays an important role in the design of the ZVS two-inductor boost cell.

TABLE I
Power Losses of the Individual Devices at the Optimized Operating Point

Device	Average Power Loss (W)
MOSFETs Q_3, Q_4	1.51
Resonant Inductor L_r	0.80
Resonant Capacitors C_1, C_2	0.02
Total	2.33

In order to combat the high drive power loss, many types of the resonant gate drive circuits have been proposed over the years. In [16], [17], and [25], higher than normal charging or discharging current due to the resonant operation flows through the transistors in the drive circuit and the conduction power loss is still high. In [15], [18], [19], and [24], the power loss of the drive circuit cannot be minimized as the transistors in the gate drive circuit still switch under the hard-switching conditions. In [13] and [20], an ideally lossless gate drive circuit has been proposed. Both of the MOSFET turn-on and turn-off are achieved by using a small inductor to provide current to charge and discharge the input capacitance of the MOSFET and a capacitor is also required to maintain a dc level equal to the average gate voltage.

In the two-inductor boost cell, the gate signals of the two MOSFETs are 180° out of phase and this allows the gate charging inductor to be shared by the two drive circuits and the dc level setting capacitor to be performed by the MOSFET input capacitance. Fig. 10 shows the proposed resonant transition gate drive circuit for the two-inductor boost cell. Compared with the conventional MOSFET gate drive circuit, only one small inductor $L_{\rm G}$ is introduced between the gates of the MOSFETs Q_3 and Q_4. The operation of the resonant transition gate drive circuit can be explained using the waveforms shown in Fig. 11. The inductor current can be approximated as a constant outside the inductor linear charging and discharging duration as this duration is insignificantly short compared with the entire

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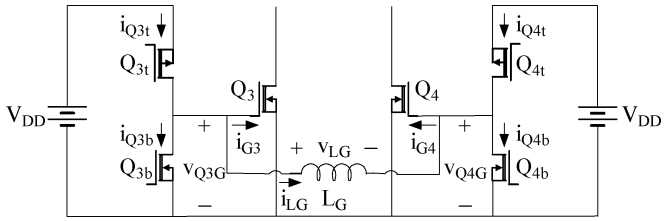

Fig. 10. Resonant transition gate drive for the two-inductor boost cell.

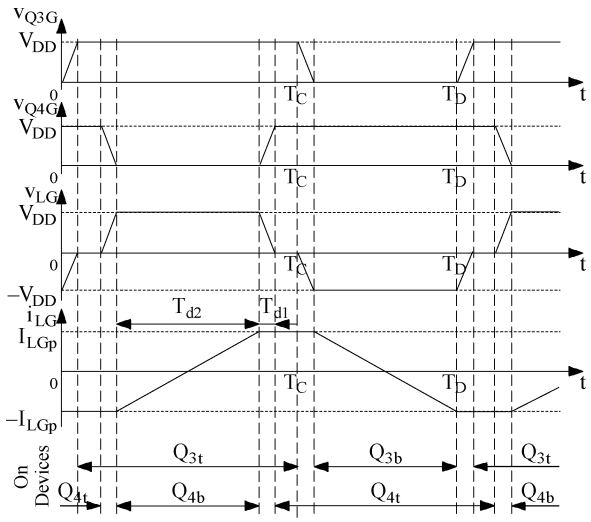

Fig. 11. Theoretical waveforms in the resonant transition gate drive ($T_{\rm C} = D_{\rm boost}T_{\rm boost}$, $T_{\rm D} = T_{\rm boost}$).

switching period $T_{\rm boost}$ if the switch duty ratio $D_{\rm boost}$ is not significantly larger than 50%. Therefore the MOSFET gate capacitances are charged and discharged linearly. During the time interval $T_{\rm d1}$, the gate capacitance of Q_4 is charged. The gate capacitance of Q_3 is later discharged over a time interval of the same length. Two P-type transistors $Q_{3\rm t}$ and $Q_{4\rm t}$ turn on and tie the gates of the power MOSFETs to the positive rail of the gate drive circuit power supply once the gate capacitances are charged to that level while two N-type transistors $Q_{3\rm b}$ and $Q_{4\rm b}$ turn on and tie the gates of the power MOSFETs to the ground once the gate capacitances are completely discharged. During the time interval $T_{\rm d2}$, when Q_3 is on and Q_4 is off, the inductor current linearly increases from the negative peak to the positive peak. Therefore the energy is transferred back and forth between two MOSFET gate capacitances through the inductor.

In the design of the resonant transition gate drive circuit, a dead time ratio ρ can be defined as:

$$\rho = \frac{T_{d1}}{T_{\rm boost}}. \tag{20}$$

Therefore the inductor linear charging or discharging interval can be obtained as

$$T_{d2} = (1 - D_{\rm boost} - \rho)T_{\rm boost}. \tag{21}$$

Assuming that the input capacitance of the MOSFET Q_3 or Q_4 is $C_{\rm iss}$, the peak inductor current $I_{\rm LGp}$ and the inductance $L_{\rm G}$ are, respectively

$$I_{LGp} = \frac{C_{iss}V_{DD}f_{\rm boost}}{\rho} \tag{22}$$

$$L_G = \frac{(1 - D_{\rm boost} - \rho)V_{DD}}{2I_{LGp}f_{\rm boost}}. \tag{23}$$

In the practical operation of the resonant transition gate drive circuit, the MOSFET gate charging and discharging currents follow the sinusoidal waveform due to the resonance between the gate inductance and the MOSFET input capacitance and their absolute values are higher than the absolute value of the inductor current $I_{\rm LG}$ at the end of its linear charging or discharging interval. Also, the MOSFET input capacitance includes gate-to-drain and gate-to-source capacitances. Due to the Miller Effect, the input capacitance is highly non-linear and the total gate charge $Q_{\rm G}$ is therefore a better parameter in determining the turn-on and the turn-off characteristics of the MOSFET [21]. Hence, the actual inductance value should be slightly larger than the value calculated from (23) if $I_{\rm LGp}$ is estimated by the MOSFET total gate charge as

$$I_{LGp} = \frac{Q_G f_{\rm boost}}{\rho}. \tag{24}$$

In the proposed resonant transition gate drive circuit, the MOSFET input capacitances are charged by the inductor current during the turn-on and the turn-off transitions and no $\rm CV^2$ loss occurs. Also a dead time $T_{\rm d1}$ is accomplished between the turn-on of the two transistors in the totem-pole to allow the buildup or the release of the charge on the power MOSFET input capacitances. This naturally prevents the cross conduction from happening. If the switch timing of the transistors in the gate drive circuit is carefully designed, they can turn on or off at zero voltage or zero current and the switching loss is absent. Therefore, a theoretical zero power loss can be achieved in the proposed resonant transition gate drive circuit. In the practical operation, however, a small amount of power loss does exist due to the parasitic components including the series dc plus ac resistance of the inductor, the internal gate resistance of the power MOSFET, the input capacitance and the drain source on resistance of the control transistors. The total power loss in the resonant transition gate drive circuit is

$$\begin{aligned} P_{\rm drive} = {} & R_{LG}I^2_{LG,rms} + 2R_G I^2_{G3,rms} \\ & + 2\left(R_{DS(on),t}I^2_{Q3t,rms} + R_{DS(on),b}I^2_{Q3b,rms}\right) \\ & + 2(C_{iss,t} + C_{iss,b})V^2_{DD}f_{\rm boost} \end{aligned} \tag{25}$$

where $R_{\rm LG}$ is the equivalent series dc plus ac resistance of $L_{\rm G}$, $R_{\rm G}$ is the internal gate resistance of the power MOSFET, $R_{\rm DS(on),t}$ and $R_{\rm DS(on),b}$ are, respectively, the drain source on resistances of the top and the bottom transistors, $I_{\rm LG,rms}$, $I_{\rm Q3t,rms}$, $I_{\rm Q3b,rms}$, and $I_{\rm G3,rms}$ are, respectively, the effective values of the currents in $L_{\rm G}$, $Q_{3\rm t}$, $Q_{3\rm b}$, and the charging and discharging current in the gate of Q_3, $C_{\rm iss,t}$ and $C_{\rm iss,b}$ are, respectively, the input capacitances of the top and the bottom

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TABLE II
COMPONENT LIST OF THE HARDWARE IMPLEMENTATION

COMPONENT	PART NUMBER	PARAMETERS	POWER LOSS (W)
L_G	Newport Component 2200 Series	Series Connection of two inductors of 1 µH: Q = 80 at 13 MHz and one inductor of 4.7 µH: Q = 75 at 13 MHz	0.12
Q_3, Q_4	STSTB50NE10	V_{DS}= 100 V, I_D = 50 A, $R_{DS(on)}$ = 0.027 Ω, Q_G = 123 nC, R_G = 1.5 Ω	0.23
Q_{3t},, Q_{3b},, Q_{4t},, Q_{4b}	International Rectifier IRLML5103, IRLML2803	P-Type: V_{DS}= 30 V, I_D = −0.76 A, $R_{DS(on)}$ = 0.60 Ω, Q_G = 3.4 nC N-Type: V_{DS} = 30 V, I_D = 1.2 A, $R_{DS(on)}$ = 0.25 Ω, Q_G = 3.3 nC	0.16 (Conduction) 0.08 (CV^2)
Total	-	-	0.59

transistors and $V_{\rm DD}$ is the supply voltage in the gate drive circuit for the control transistors.

If the duty ratio $D_{\rm boost}$ is not significantly larger than 50% and the zero inductor voltage period in Fig. 11 can be neglected, the current terms in (25) can be, respectively, found as

$$I_{LG,rms} = \sqrt{\frac{1+8\rho}{3}} I_{LGp} \tag{26}$$

$$I_{Q3t,rms} = \sqrt{\frac{1+8\rho}{6}} I_{LGp} \tag{27}$$

$$I_{Q3b,rms} = \sqrt{\frac{1-4\rho}{6}} I_{LGp} \tag{28}$$

$$I_{G3,rms} = \sqrt{2\rho} I_{LGp}. \tag{29}$$

Equations (25)–(29) confirm that the power loss in the gate drive circuit is very small if the dead time ratio and the parasitic component values are small. A component list of the hardware implementation and the calculated individual power losses is given in Table II. Under the selected optimized operating point, the switch duty ratio in the two-inductor boost cell is $D_{\rm boost} = 0.615$ and the calculated inductance value from (23) is 5.6 μH if $V_{\rm DD} = 12$ V and $\rho = 0.1$. The gate inductor is experimentally adjusted to 6.7 μH and a total drive power loss of 0.83 W can be measured, which agrees reasonably well with the theoretical calculation.

V. EXPERIMENTAL RESULTS

In order to prove the theoretical analysis, a prototype converter of 12.5 cm × 22.5 cm (5 in × 9 in) has been built in the laboratory as shown in Fig. 12. As the device switching frequency in the buck stage is 250 kHz, a current ripple frequency of 500 kHz exists after the IPT. In the converter, a Linear Technology two-phase synchronous step-down switching regulator LTC1929CG is used to simplify the design of the synchronous buck converter. The gate signals in the buck converter are synchronized with the output signal of a frequency divider, whose input is the gate signal in the two-inductor boost cell. The IPT is implemented by an Epcos EFD15 core with 14 turns on both primary and secondary sides.

The boost stage operates with a converter frequency of 1 MHz, which corresponds to the device switching frequency of 500 kHz. In the ZVS boost cell, the transformer and the two inductors are wound on Ferroxube ETD29 cores. The inductor core has 0.5-mm air gaps on both outer legs. SiC diodes with 600-V ratings are used in the voltage-doubler rectifier. In the unfolder, the photovoltaic MOSFET drivers are used to drive the MOSFETs in the full bridge inverter. Figs. 13–17 show the experimental waveforms.

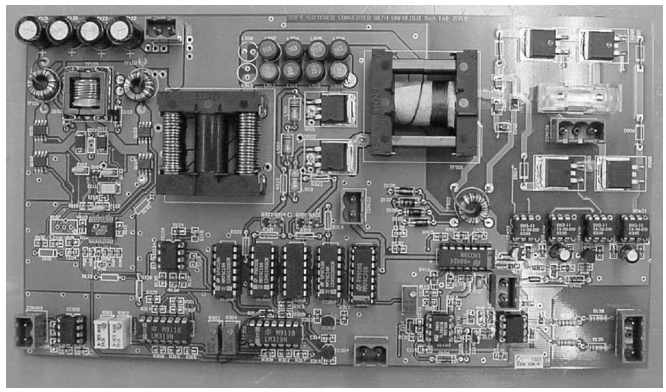

Fig. 12. Prototype converter.

Fig. 13 shows the buck converter waveforms under static tests. From top to bottom, Fig. 13(a) and (b), respectively, shows the waveforms of v_1, v_2, and $v_{\rm H}$ with the duty ratio smaller or greater than 50%. The voltage after the IPT swings between zero and the half input voltage when the duty ratio of the buck stage MOSFETs $D_{\rm buck}$ <50% and swings between the half and the full input voltages when $D_{\rm buck}$ >50%. In both cases, the frequency of the voltage after the IPT $v_{\rm H}$ is twice those of the two voltages v_1 and v_2.

Fig. 14 shows the two-inductor boost converter output voltage $v_{\rm C}$ and the input voltage $v_{\rm H}$ from top to bottom during the sinusoidal modulation. A three-level modulation can be obviously observed in the $v_{\rm H}$ waveform although the waveform captured by the oscilloscope is heavily aliased.

Fig. 15 shows the waveforms in the low frequency unfolder. From top to bottom, they are respectively the waveforms of the switch gate voltages, the output voltage $v_{\rm O}$ and the output current $i_{\rm O}$ at 50 Hz. In this case, a resistive load is supplied and this is adjusted to give the rated average power, 100 W, at 240 V ac, which is equivalent to the nominal mains voltage.

From top to bottom, Fig. 16 shows the gate and drain source voltage waveforms of the MOSFETs in the ZVS two-inductor

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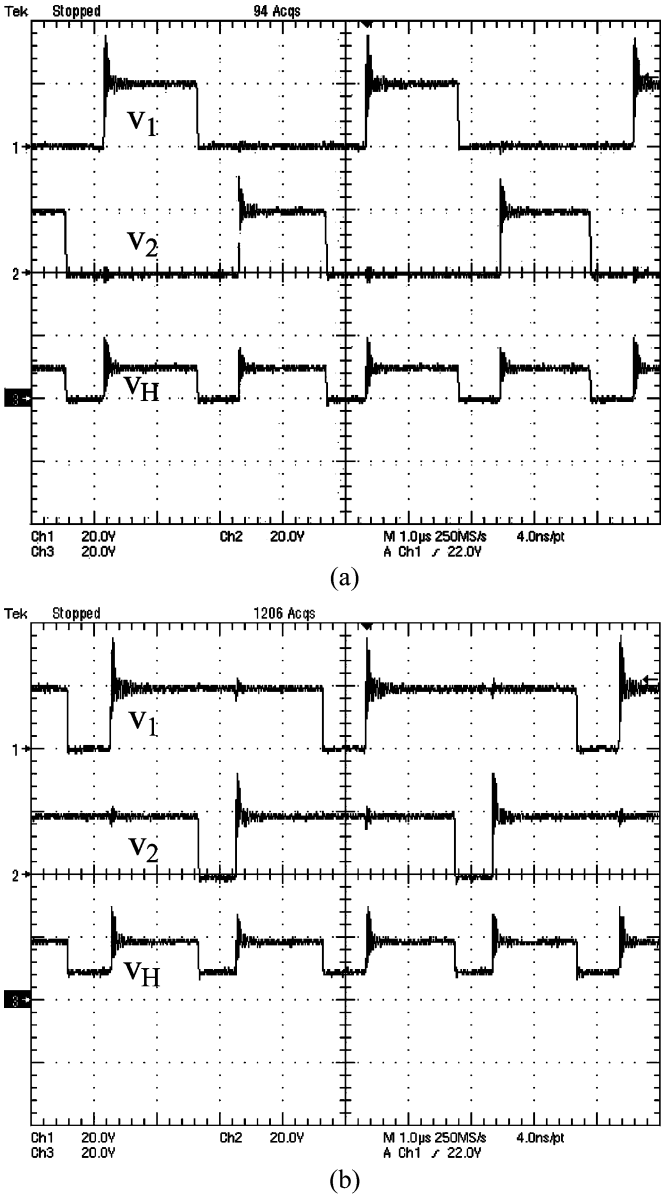

Fig. 13. Voltage waveforms in the two-phase buck converter: (a) $D_{\rm buck}$ <50% and (b) $D_{\rm buck}$ >50%.

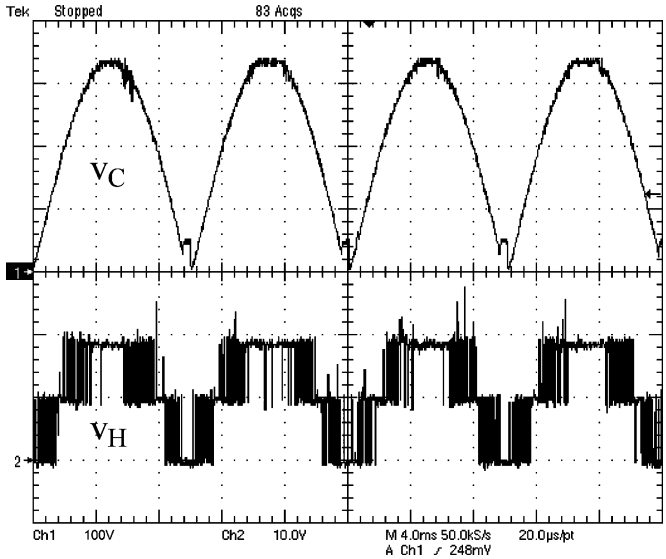

Fig. 14. Input and output voltage waveforms in the ZVS two-inductor boost cell.

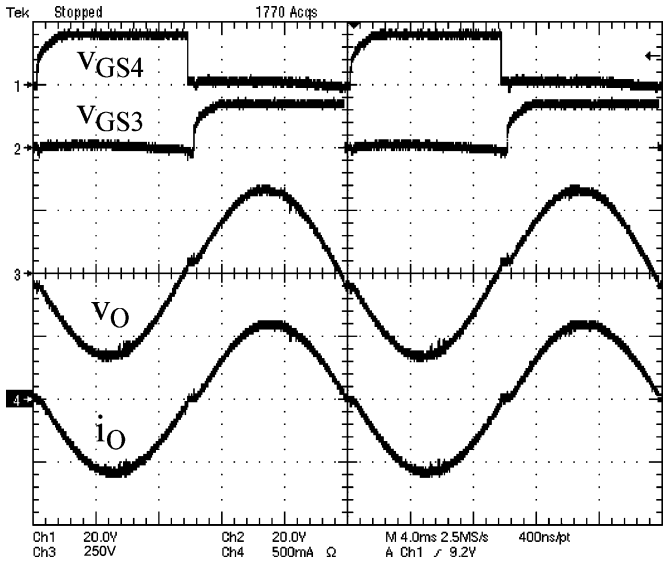

Fig. 15. MOSFET gate voltage, output voltage, and current waveforms in the unfolder.

boost cell when the output voltage is close to the peak. The MOSFET gate waveforms agree with the theoretical waveforms shown in Fig. 11 except that the overlap of the on intervals of the two MOSFETs is smaller in the experimental waveforms. The MOSFET drain source voltage waveforms confirm that the MOSFETs turn on at zero voltage.

Fig. 17 shows the voltage across the diode in the voltage-doubler rectifier when the output voltage is close to the peak. The waveform is relatively clean. No reverse recovery can be seen in the silicon carbide Schottky rectifiers although some lower frequency oscillations with an approximately 200-ns period can be seen. These are driven by the resonance between the diode junction capacitance and the inductance in series with the transformer T_2 secondary winding including the leakage inductance and the additional resonant inductance referred to the secondary.

A conversion efficiency of 91% has been obtained for the module integrated PV converter power train. The power loss includes the losses in the buck stage, the ZVS cell and the unfolding stage. Input and output powers of the individual stages were measured using the mathematical functions of a Tektronix TDS5034 four-channel oscilloscope equipped with converter input and output voltage and current probes. The current probes are Tektronix TCP202. Table III shows the breakdown of the 9.3-W total power loss observed in the 100-W converter. The power losses of the individual components in the ZVS cell were indirectly obtained from the corresponding stabilized temperature rises [22]. The estimated total power loss in the MOSFETs, the resonant inductor and capacitors in the ZVS cell is 2.5 W and this agrees well with that in the theoretical analysis.

VI. Conclusion

In this paper, a current fed ZVS two-inductor boost converter with an unfolder is proposed for the MIC applications in the grid

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TABLE III
POWER LOSS BREAKDOWN

STAGE	POWER LOSS (W)	COMPONENT	POWER LOSS (W)
Two-Phase Buck Converter	2.3	-	-
ZVS Two-Inductor Boost Cell	6.4	L_1, L_2	0.7
		T_2	1.6
		D_3, D_4	1.6
		L_r, C_1, C_2, Q_3, Q_4	2.5
Unfolder	0.6	-	-

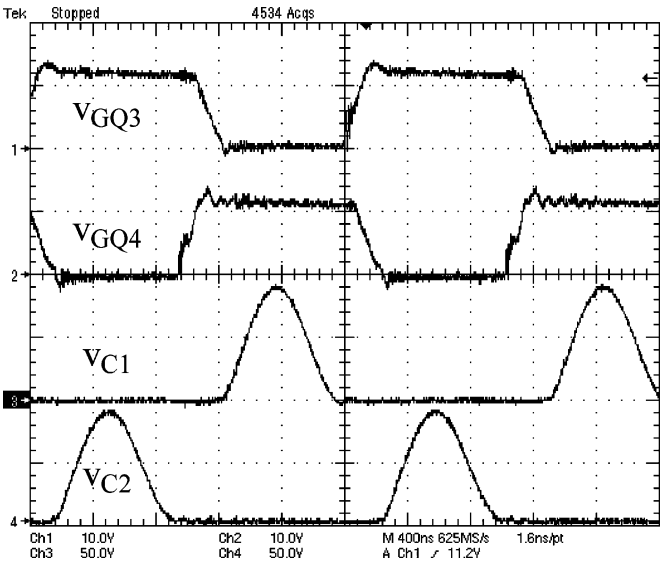

Fig. 16. MOSFET gate and drain source voltage waveforms in the ZVS two-inductor boost cell.

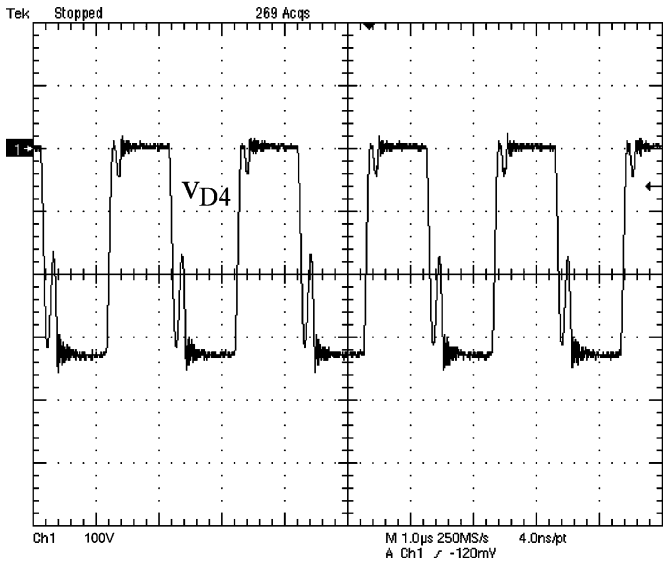

Fig. 17. Diode voltage waveform in the ZVS two-inductor boost cell.

interactive PV system. The ZVS boost cell is fed from a sinusoidally modulated two-phase synchronous buck converter, allowing itself to operate under a power loss optimized point with a fixed switching frequency. The rectified sinusoidal voltage waveform is produced at the output of the current fed two-inductor boost converter and converted to the mains compatible sinusoidal current by a low frequency unfolder.

A power loss optimization method is proposed for the two-inductor boost cell to achieve the minimized total power loss. Three power loss components that vary with different circuit parameters are identified and the numerical analysis of the average power loss is conducted with MATLAB, which generates the visual surface plots to show the average power losses in the two operating regions and assist in determining the optimized operating point.

This paper also proposes an ideally lossless resonant transition gate drive to reduce the drive power loss under high switching frequency operations. Only one small inductor is introduced compared with the conventional MOSFET gate drive circuit and the new gate drive circuit is ready for semiconductor integration. Experimental results show that the drive power loss is controlled within 1% of the power rating of the converter under 500-kHz switching frequency.

The theoretical analysis is validated by a current fed ZVS two-inductor boost converter with a converter switching frequency of 1-MHz and an average power of 100 W. The prototype converter has achieved an efficiency of 91% for a power train that includes the two-phase buck converter stage, the ZVS boost cell and the output unfolder stage.

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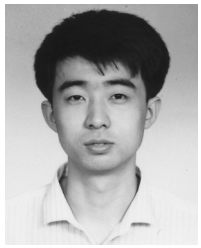

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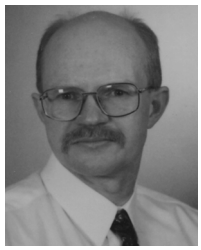

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