A UPFC with Reduced DC Bus Capacitance for LV Distribution Networks with High PV Penetrations

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***Abstract* — A low voltage (LV) distribution level unified power flow controller (UPFC) is shown capable of regulating the positive sequence voltage with a network while simultaneously correcting phase unbalance voltages that can be produced by high levels of distributed photovoltaic (PV) generation. Instantaneous reactive power theory shows that DC-bus capacitor power will fluctuate at twice mains frequency during any unbalanced operation. Instantaneous power balance can be maintained by allowing the input converter to draw a small negative sequence current. This allows a hundred-fold reduction in the value of the DC bus capacitance allowing long life ceramic or polypropylene capacitors to replace electrolytic capacitors in this application.**

Keywords - UPFC; power quality, photovoltaic, distributed generation; instantaneous power theory, reduced bus capacitance.

I. INTRODUCTION

Distributed photovoltaic generation, in the form of roof-top domestic systems, is being installed at an increasing scale. Significant power quality issues, especially voltage rise and voltage unbalance have been widely studied, [1-4]. The penetration of renewable energy supplies in distribution networks is materially restricted by the voltage management philosophies that were applied at construction. The majority of distribution networks are radial and the power flow direction is from a point of bulk supply outwards to loads. The prevailing flow direction allows voltage regulators to be set to compensate for the largest voltage drops at the highest loads. Distributed generation can cause the power flow to reverse when the loads are light. In conjunction with the pre-set voltage profile, which is purposefully placed at the upper edge of the acceptable voltage band, distribution over-voltages quickly result. Over-voltages have been observed with high penetrations of residential roof-top solar systems. The midday loads during the working week can be very low while the solar generation is high. The resulting over-voltages cause inverter tripping and the loss of the solar generation.

II. A UPFC SOLUTION TO VOLTAGE MANAGEMENT FOR DISTRIBUTED RENEWABLE ENERGY SYSTEMS

Higher penetrations of renewable generation within the distribution network can be achieved by the addition of intelligent control, storage or regulatory devices, [5,6]. Figure 1 shows a voltage regulation device based on the Unified Power Flow Controller, (UPFC), concept, [7]. In this case the DC bus capacitor has a reduced size to allow the application of ceramic capacitors in place of conventional electrolytic capacitors. Electrolytic capacitors often determine the limitations on working temperature for converters and can contribute significantly to cost and failure rate, [8-9]. This paper explores how a UPFC can be controlled if the DC bus capacitor size is reduced by two orders of magnitude – a one hundred fold reduction. Murata and others now provide high temperature high-current multi-layer ceramic capacitors, (MLCC), for electric vehicle inverter applications, [10]. As electrolytic capacitors with thousands of microfarads are replaced by ceramic capacitors of tens of microfarads the major research challenge is to manage the DC capacitor voltage by ensuring instantaneous power balance for the input and output converters, [11].

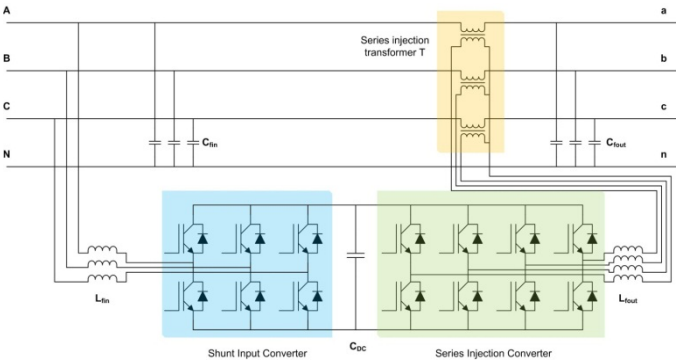

Figure 1. Compensator with Reduced DC Bus Capacitor

III. DC CAPACITOR VOLTAGE VARIATION AND INSTANTANEOUS POWER FLOW

The proposed UPFC system regulates the voltages at the output terminals a, b and c by injecting a series voltage component. In general low-voltage four-wire distribution networks unbalanced loading or unbalanced solar generation will produce unbalanced variations in voltage. The injected correcting voltage will have positive, negative and zero sequence components and the series injection converter must have four phase legs to produce the necessary degrees of freedom. Figure 2 shows the regulator system modeled with continuous time voltage and current sources. The instantaneous power developed by the series injection elements is:

$$p_s(t) = i_a(t) \times v_{Aa}(t) + i_b(t) \times v_{Bb}(t) + i_c(t) \times v_{Cc}(t) = \overline{p_s} + \widetilde{p_s} \quad (1)$$

The instantaneous power can be expressed as an average value, $\overline{p}$, and an oscillatory component $\tilde{p}$. The injected voltage is expressed as a sum of positive, negative and zero sequence components:

$$v_{Aa}(t) = \sqrt{2}V_{s+}sin(\omega t + \varphi_{vs+}) + \sqrt{2}V_{s-}sin(\omega t + \varphi_{vs-}) + \sqrt{2}V_{s0}sin(\omega t + \varphi_{vs0}) \quad (2)$$

$$v_{Bb}(t) = \sqrt{2}V_{s+}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{vs+}\right) + \sqrt{2}V_{s-}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{vs-}\right) + \sqrt{2}V_{s0}sin(\omega t + \varphi_{vs0}) \quad (3)$$

$$v_{Cc}(t) = \sqrt{2}V_{s+}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{vs+}\right) + \sqrt{2}V_{s-}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{vs-}\right) + \sqrt{2}V_{s0}sin(\omega t + \varphi_{vs0}) \quad (4)$$

Similarly the line currents can be expressed as:

$$i_a(t) = \sqrt{2}I_{s+}sin(\omega t + \varphi_{is+}) + \sqrt{2}I_{s-}sin(\omega t + \varphi_{is-}) + \sqrt{2}I_{s0}sin(\omega t + \varphi_{is0}) \quad (5)$$

$$i_b(t) = \sqrt{2}I_{s+}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{is+}\right) + \sqrt{2}I_{s-}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{is-}\right) + \sqrt{2}I_{s0}sin(\omega t + \varphi_{is0}) \quad (6)$$

$$i_c(t) = \sqrt{2}I_{s+}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{is+}\right) + \sqrt{2}I_{s-}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{is-}\right) + \sqrt{2}I_{s0}sin(\omega t + \varphi_{is0}) \quad (7)$$

The resulting average and oscillatory powers are, [12]:

$$\overline{p_s} = 3\,V_{s+}\,I_{s+}\cos(\varphi_{vs+} - \varphi_{is+}) + 3\,V_{s-}\,I_{s-}\cos(\varphi_{vs-} - \varphi_{is-}) + 3\,V_{s0}\,I_{s0}\cos(\varphi_{vs0} - \varphi_{is0}) \quad (8)$$

$$\widetilde{p_s} = 3\,V_{s+}\,I_{s-}\cos(2\omega t + \varphi_{vs+} + \varphi_{is-}) + 3\,V_{s-}\,I_{s+}\cos(2\omega t + \varphi_{vs-} + \varphi_{is+}) + 3\,V_{s0}\,I_{s0}\cos(2\omega t + \varphi_{vs0} + \varphi_{is0}) \quad (9)$$

Assume the input voltages to the parallel converter are:

$$v_{AN}(t) = \sqrt{2}V_{p+}sin\left(\omega t + \varphi_{vp+}\right) + \sqrt{2}V_{p-}sin\left(\omega t + \varphi_{vp-}\right) + \sqrt{2}V_{p0}sin\left(\omega t + \varphi_{vp0}\right) \quad (10)$$

$$v_{BN}(t) = \sqrt{2}V_{p+}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{vp+}\right) + \sqrt{2}V_{p-}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{vp-}\right) + \sqrt{2}V_{p0}sin\left(\omega t + \varphi_{vp0}\right) \quad (11)$$

$$v_{CN}(t) = \sqrt{2}V_{p+}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{vp+}\right) + \sqrt{2}V_{p-}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{vp-}\right) + \sqrt{2}V_{p0}sin\left(\omega t + \varphi_{vp0}\right) \quad (12)$$

In a voltage regulator with negligible energy storage the series injected power must be balanced by power delivered by the shunt converter. It will be shown this can be achieved using positive and negative sequence currents only. The input currents are arbitrarily controlled in terms of the positive and negative sequence currents as follows:

$$i_{Ap}(t) = \sqrt{2}I_{p+}sin\left(\omega t + \varphi_{ip+}\right) + \sqrt{2}I_{p-}sin\left(\omega t + \varphi_{ip-}\right) \quad (13)$$

$$i_{Bp}(t) = \sqrt{2}I_{p+}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{ip+}\right) + \sqrt{2}I_{p-}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{ip-}\right) \quad (14)$$

$$i_{Cp}(t) = \sqrt{2}I_{p+}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{ip+}\right) + \sqrt{2}I_{p-}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{ip-}\right) \quad (15)$$

The parallel input converter instantaneous power is

$$p_p(t) = i_{Ap}(t) \times v_{AN}(t) + i_{Bp}(t) \times v_{BN}(t) + i_{Cp}(t) \times v_{CN}(t) = \overline{p_p} + \widetilde{p_p} \quad (16)$$

The average and oscillatory powers for the parallel converter are:

$$\overline{p_p} = 3\,V_{p+}\,I_{p+}\cos\left(\varphi_{vp+} - \varphi_{ip+}\right) + 3\,V_{p-}\,I_{p-}\cos\left(\varphi_{vp-} - \varphi_{ip-}\right) \quad (17)$$

$$\widetilde{p_p} = 3\,V_{p+}\,I_{p-}\cos\left(2\omega t + \varphi_{vp+} + \varphi_{ip-}\right) + 3\,V_{p-}\,I_{p+}\cos\left(2\omega t + \varphi_{vp-} + \varphi_{ip+}\right) \quad (18)$$

In practical applications the shunt converter input voltage has a dominant positive sequence component, $V_{p+} \angle \varphi_{vp+}$, but is not necessarily completely balanced. If:

$$V_{p+} \gg V_{p-} \quad (19)$$

Then

$$\overline{p_p} = 3\,V_{p+}\,I_{p+}\cos\left(\varphi_{vp+} - \varphi_{ip+}\right) \quad (20)$$

$$\widetilde{p_p} = 3\,V_{p+}\,I_{p-}\cos\left(2\omega t + \varphi_{vp+} + \varphi_{ip-}\right) \quad (21)$$

Equation 20 shows that the average power, $\overline{p}$, could be satisfied with the lowest current if the shunt converter draws positive sequence current in phase with the local positive sequence voltage. Equation 21 shows the oscillatory power can be balanced by the input converter by drawing a negative sequence current with an appropriate magnitude and phase. These relationships can form the basis of control systems to manage the voltage on a DC bus capacitor with reduced size.

IV. CONTINUOUS DOMAN MODEL

Modern switching converters, especially below 100kVA where the switching frequencies often exceed 10 kHz, can be usefully modeled for control purposes using continuous domain models as shown in Figure 2. The series converter is controlled to produce the injected voltages and the parallel converter is current controlled to satisfy the instantaneous power requirements for the series elements. The DC bus capacitor power is the difference between the input parallel converter power and output series injection powers and the voltage is the integral of the resulting charging current.

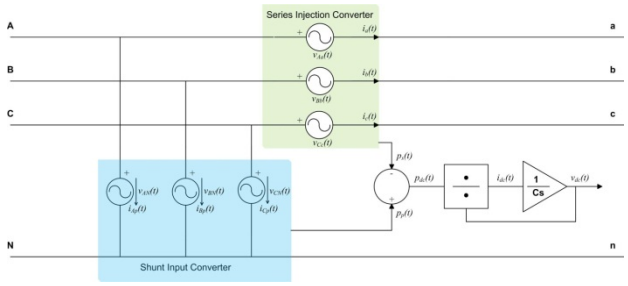

Figure 2. Continuous Domain Model

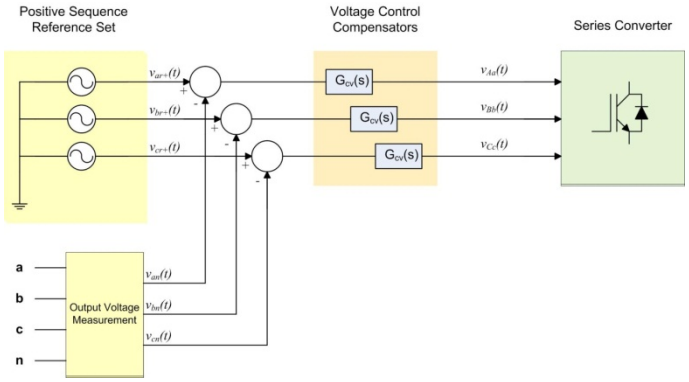

Figure 3. Voltage Control For the Series Element

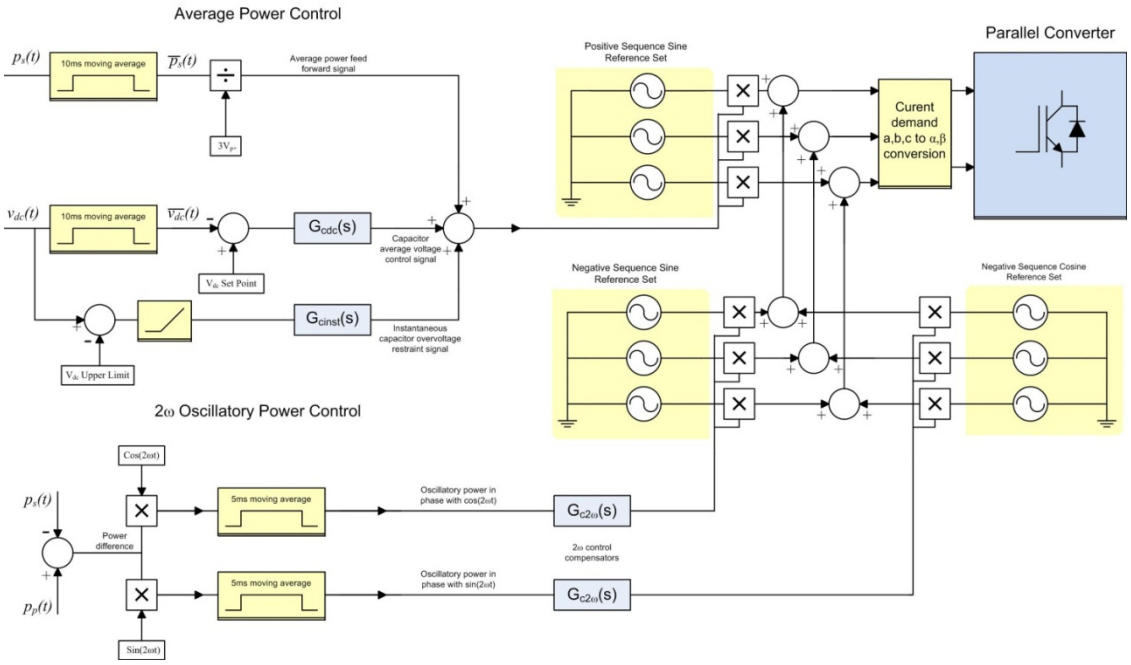

Figure 4. Power Control for the Parallel Element

In the most simplified models it is assumed both converters utilize switching frequencies, filter designs and control methodologies that provide rapid responses that introduce negligible phase delays over the control bandwidths of interest. An improved continuous time model can include the modulation transport delay and the inverter filter state variables. Figure 3 and figure 4 show possible control arrangements for the management of the series and parallel converters. In figure 3 the series converter is voltage controlled to force the output voltages to follow a positive sequence reference set. In practice the three controlled voltage sources will need to inject positive, negative and zero sequence components.

As three degrees of freedom are required either a four leg converter or three independent single phase inverters can be applied. The parallel converter must be controlled to provide the instantaneous power demands of the series injection element. Figure 4 shows a possible power control solution which requires the parallel converter to be equipped with a responsive current control system. An instantaneous power control system could be constructed in the α,β frame but this paper proposes a positive and negative sequence framework approach. Direct control of the 2ω oscillatory powers in the α,β frame will produce fundamental and third harmonic line currents. This is avoided in the positive/negative sequence based approach. As seen in equation 20 the average power is best satisfied through the control of an in phase positive sequence current. In figure 4 the average power control system has three parts:

- A feed forward control which calculates the required positive sequence current from the 10ms average power demand of the series converter and the magnitude of the input positive sequence voltage;
- A DC capacitor average voltage control loop that responds to errors in the average DC bus voltage. The controller $G_{cdc}(s)$ has a PI response;
- An instantaneous DC bus voltage limit function. The controller $G_{cinst}(s)$ could have a proportional or hysteresis response. During transients this controller may demand short bursts of positive sequence current that persist for a few milliseconds.

These three systems produce a total positive sequence magnitude demand signal that is multiplied by a three phase positive sequence sinusoidal reference set to produce phase demand signals. The reference set is generated from the converter input voltages using a PLL. The oscillatory 2ω power control loop balances the oscillatory powers introduced by unbalanced loading of the series converter. In Figure 4 the instantaneous power difference between the series and parallel converters is determined by subtraction. A sine and cosine synchronous detector and the associated 5ms moving average filters determine the oscillatory powers at 2ω. These components are forced to zero by the actions of the control amplifiers $G_{c2\omega}(s)$. A residual oscillatory power in phase with $\cos(2\omega t)$ is cancelled by injecting a sinusoidal negative sequence current into the phase current demand signals driving the parallel converter.

V. Continuous Time Model Simulation Results

Figure 5 shows a voltage compensator placed at the centre point of a 300m low voltage four-wire three-phase aerial feeder constructed with a 7/3.75mm all aluminium conductor. This conductor, commonly designated as "mars" is widely used within Australian distribution networks. The conductor impedance is $(0.452+0.270j)\Omega$/km. The supply transformer is rated at 200kVA, 415/240V, 50Hz and has a per-unit series impedance of $0.01+0.03j\Omega$. Three $100A_{rms}$ 0.95pf lagging loads are applied to the far end of the feeder. A switchable $50A_{rms}$ unity power factor single-phase solar generator is also placed at the far end and is connected to phase "b".

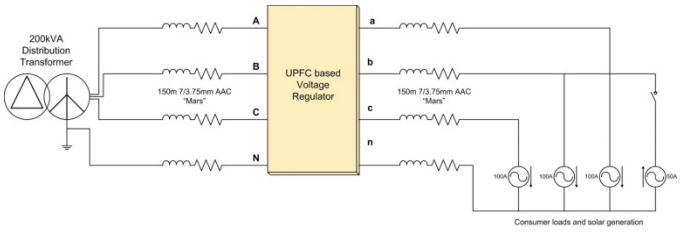

Figure 5. Regulator Application in a LV Feeder

The key simulation parameters are as follows:

- DC bus capacitor 10μF; V_{dc} Set Point 700V; V_{dc} Upper Limit 800Vdc;
- Output voltage regulators - $G_{ccv}(s)=2+10{,}000/s$; The three phase reference set has a 240Vrms magnitude; the series injection controlled voltage sources have unity gain;
- DC bus regulator $G_{cdc}(s)=0.0004+0.004/s$;
- DC bus instantaneous voltage limit regulator, proportional gain only above 800Vdc - $G_{cinst}(s)=0.1$; Current limit 10A peak.
- 2ω oscillatory power compensators - $G_{c2\omega}(s)=2+200/s$. The $\sin(2\omega t)$ and $\cos(2\omega t)$ sources have unit magnitude.
- The positive sequence sine and negative sequence sine and cosine sets have unit peak magnitude.
- The parallel converter current sources have a transconductance of 1S.
- To improve the stability of the simulation 10μF capacitors are connected at the regulator input from terminals A,B,C to N and at the load terminals, phase to neutral.

Table 1 outlines the steady state regulatory performance with the solar generation in service. It is noteworthy that this style of loading produces significant zero sequence voltages. These are four times higher than the negative sequence voltages and this outcome is expected from the network sequence diagrams.

As expected the regulator, when in the active state, corrects the voltages at the a,b,c,n output terminals and forces the negative and zero sequence voltages nearly to zero. The attenuation is determined by the voltage loop gain. The input positive sequence current increases, as with any regulator, to provide the real power requirement to correct the positive sequence voltage drop. There is a slight increase in negative sequence current to provide the oscillatory power necessary to eliminate the negative and zero sequence voltages at the regulator output terminals. This has a minor effect on the negative sequence voltage upstream of the regulator. The oscillatory power could be compensated by the parallel converter with a negative or zero sequence current but a negative sequence choice is preferable from a voltage disturbance perspective. The dynamic response of the regulator is explored in Figures 6 to 11. The regulator is allowed to settle into steady state operation with a balanced 100A 0.95 power factor load. At t=0.5067s, the voltage zero crossing in "b" phase, a 50A solar generator commences operation. The solar current ramps up over one 20ms cycle and reaches its full current at t=0.5267s.

TABLE I. INPUT AND OUTPUT VOLTAGES AND CURRENTS

Regulator State	Terminals A,B,C,N	Terminals a,b,c,n	Consumer Terminals
Inactive and Solar Generation Enabled	$V_+ = 229.1V_{rms}$ $\varphi_+ = 0.9°$ $V_- = 2.3V_{rms}$ $\varphi_- = 124.2°$ $V_0 = 9.1V_{rms}$ $\varphi_0 = -116.0°$ $I_+ = 83.9A_{rms}$ $\varphi_+ = -21.0°$ $I_- = 16.7A_{rms}$ $\varphi_- = -59.2°$ $I_0 = 16.7A_{rms}$ $\varphi_0 = 60.6°$	$V_+ = 229.1V_{rms}$ $\varphi_+ = 0.9°$ $V_- = 2.3V_{rms}$ $\varphi_- = 124.2°$ $V_0 = 9.1V_{rms}$ $\varphi_0 = -116.0°$ $I_+ = 84.1A_{rms}$ $\varphi_+ = -21.4°$ $I_- = 16.7A_{rms}$ $\varphi_- = -59.2°$ $I_0 = 16.7A_{rms}$ $\varphi_0 = 60.6°$	$V_+ = 218.3V_{rms}$ $\varphi_+ = 1.8°$ $V_- = 4.5V_{rms}$ $\varphi_- = 124.2°$ $V_0 = 18.2V_{rms}$ $\varphi_0 = -116.0°$ $I_+ = 84.1A_{rms}$ $\varphi_+ = -21.4°$ $I_- = 16.7A_{rms}$ $\varphi_- = -59.2°$ $I_0 = 16.7A_{rms}$ $\varphi_0 = 60.6°$
Active and Solar Generation Enabled	$V_+ = 228.4V_{rms}$ $\varphi_+ = 0.9°$ $V_- = 2.4V_{rms}$ $\varphi_- = 123.0°$ $V_0 = 9.1V_{rms}$ $\varphi_0 = -115.9°$ $I_+ = 88.5A_{rms}$ $\varphi_+ = -19.8°$ $I_- = 17.7A_{rms}$ $\varphi_- = -60.4°$ $I_0 = 16.7A_{rms}$ $\varphi_0 = 60.7°$	$V_+ = 240.3V_{rms}$ $\varphi_+ = 0.8°$ $V_- = 0.1V_{rms}$ $\varphi_- = 0°$ $V_0 = 0.4V_{rms}$ $\varphi_0 = 0°$ $I_+ = 84.1A_{rms}$ $\varphi_+ = -21.4°$ $I_- = 16.7A_{rms}$ $\varphi_- = -59.2°$ $I_0 = 16.7A_{rms}$ $\varphi_0 = 60.7°$	$V_+ = 229.5V_{rms}$ $\varphi_+ = 1.7°$ $V_- = 2.3V_{rms}$ $\varphi_- = 126.0°$ $V_0 = 9.1V_{rms}$ $\varphi_0 = -114.1°$ $I_+ = 84.1A_{rms}$ $\varphi_+ = -21.4°$ $I_- = 16.7A_{rms}$ $\varphi_- = -59.2°$ $I_0 = 16.7A_{rms}$ $\varphi_0 = 60.7°$

Figure 6 shows the three phase voltages at the input terminals A,B,C and the output terminals a,b,c. The output voltages are constant, well regulated and show no variation as the solar generation enters the network. The input voltages prior to t=0.5067s are balanced but low. After the solar generation commences phase "b" (cyan) rises as the phase current reduces.

Figure 7 shows the response of the series injection converter. After t=0.5067s the voltage injected in phase "b" (cyan) reduces over one cycle in response to the reduction in phase "b" (cyan) current, seen in the lower trace.

Figure 8 shows the response of the parallel converter. Prior to t=0.5067s the input current is balanced and the regulator adds a balanced positive sequence voltage to control the voltages at terminals a,b,c. The real power requirement is slightly above 4kW. Once the solar generation starts the real power requirement drops and an oscillatory power requirement develops. The parallel converter draws a combination of positive and negative sequence currents to satisfy the average and oscillatory power requirement.

Figure 9 focuses on the positive sequence current control system and the management of the DC bus voltage. As the solar generation commences the line currents become unbalanced and the series converter demands a lower average power and an oscillatory current, shown as the upper blue trace. The parallel converter, the upper red trace, should rapidly follow the power demand to control the DC bus capacitor voltage shown as the second trace.

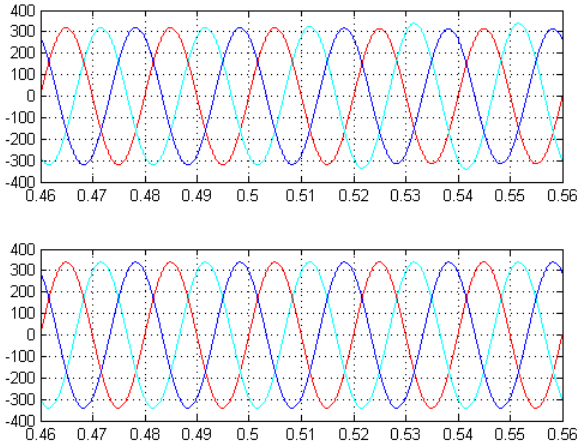

Figure 6. Top Traces Voltages to N at Terminals A,B,C; Lower Traces Voltages to n at Terminals a,b,c.

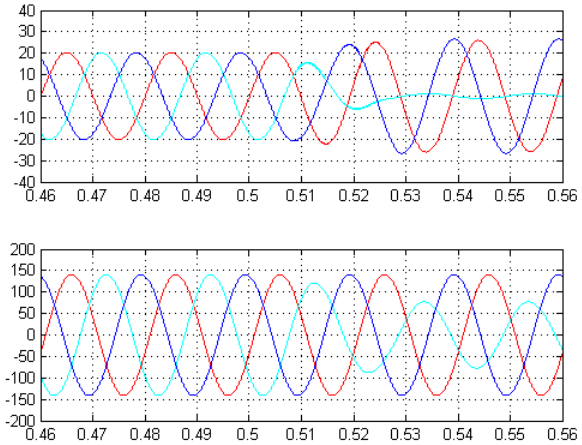

Figure 7. Top Traces Series Injection Voltages; Lower Traces Currents from Terminals a,b,c,n

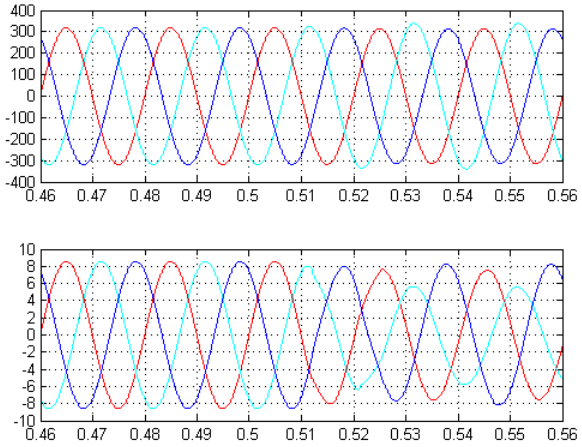

Figure 8. Top Traces Shunt Converter Input Voltages; Lower Traces Shunt Converter Input Line Currents.

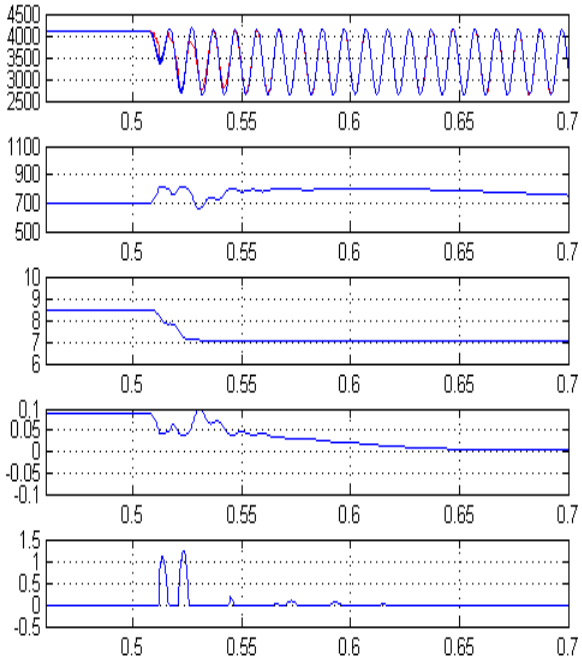

Figure 9. Top Traces Series Converter Power (Blue) and Shunt Converter Power (Red). Other Traces Top to Bottom: DC Bus Voltage; Positive Sequence Current Demand Feed Forward Signal; DC Bus Voltage Regulator Current Demand; Instantaneous Bus Voltage Current Demand

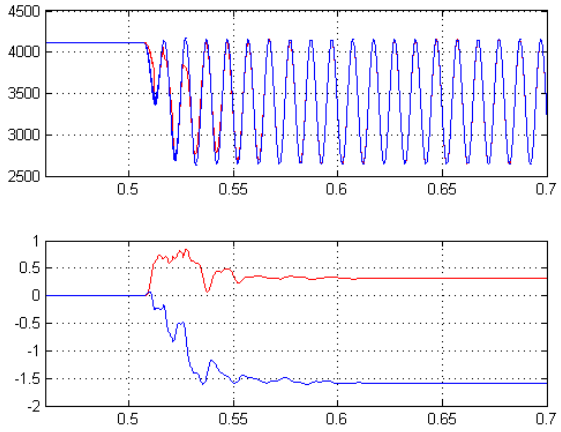

Figure 10. Top Traces Series Converter Power (Blue) and Shunt Converter Power (Red). Lower Traces Current Demand Signals for Negative Sequence Cosine (Blue) and Sine (Red) Terms

The positive sequence current forward system has a minimum 10mS response time and the demand signal is shown as the third trace. The capacitor voltage regulation loop, the demand signal of which is shown as the fourth trace, is slow responding and only corrects any minor tracking errors in the feed forward system. The instantaneous power balance causes the capacitor voltage to rise rapidly. Once the capacitor voltage reaches 800Vdc the instantaneous voltage limit system becomes active as shown in the lower trace. This instantaneously reduces the positive sequence current drawn by the parallel converter limiting the voltage rise.

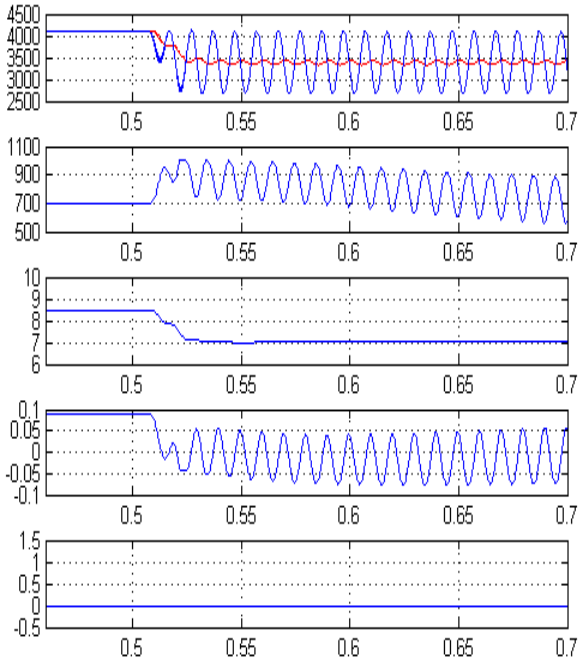

Figure 11. Top Traces Series Converter Power (Blue) and Shunt Converter Power (Red). Other Traces Top to Bottom: DC Bus Voltage; Positive Sequence Current Demand Feed Forward Signal; DC Bus Voltage Regulator Current Demand; Instantaneous Bus Voltage Current Demand

The positive sequence current forward system has a minimum 10mS response time and the demand signal is shown as the third trace. The capacitor voltage regulation loop, the demand signal of which is shown as the fourth trace, is slow responding and only corrects any minor tracking errors in the feed forward system. The instantaneous power balance causes the capacitor voltage to rise rapidly. Once the capacitor voltage reaches 800Vdc the instantaneous voltage limit system becomes active as shown in the lower trace. This instantaneously reduces the positive sequence current drawn by the parallel converter limiting the voltage rise.

From t=0.55s the instantaneous loop is inactive and the normal voltage control loop can rebalance the capacitor power and voltage. Figure 10 shows the actions of the 2ω control loops. At t=0.5067s the oscillatory power requirement emerges and the 2ω control amplifiers begin to demand negative sequence sine and cosine currents as shown in the lower traces.

Figure 11 illustrates the effectiveness of the control systems in managing the DC capacitor voltage. In this case the instantaneous voltage limit control system and the 2ω control loops are turned off. From t=0.5067s the parallel converter cannot track the 2ω power oscillations and the DC bus voltage regulators and feed forward systems cannot respond rapidly to the capacitor voltage rise. The DC bus voltage rises sharply and exceeds 1100Vdc, as seen in the second trace. The DC bus average voltage does slowly reduce but the capacitor voltage has a sustained 2ω voltage ripple as the small capacitor is forced to absorb the oscillatory power.

VI. CONCLUSIONS

This paper has established a new method for the management of the DC bus voltage in a distribution level UPFC to allow a hundred-fold reduction in the value of the DC bus capacitance. Instantaneous reactive power theory has been applied to show how the 2ω power fluctuations that are inherent in the compensation of unbalanced systems can be compensated by allowing the input converter to draw a negative sequence current. The practicality of this approach has been confirmed by a detailed simulation study. The device regulates the positive sequence voltage while eliminating the zero and positive sequence voltages at the output terminals. In the steady state 2ω voltage fluctuations are absent in the DC capacitor voltage as these are activity suppressed by controlling the shunt converter negative sequence current. During transients the DC bus voltage can be successfully limited by the high speed control of the shunt converter real power through its instantaneous positive sequence current.

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