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New Techniques for Measurement and Tracking of Phase and Frequency

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Abstract

This thesis presents and analyses new techniques to measure and track the phase and frequency of high frequency narrow bandwidth signals. In particular, these techniques are all digital in nature or can be implemented in digital integrated circuit technology.

Presented first is a frequency measurement technique which involves sampling at regular intervals a binary quantized narrow band signal. The binary quantized samples are digitally processed to obtain the instantaneous frequency of the signal.

It is shown that small phase movements in the signal can be detected even though the sampling occurs at a rate much lower than the signal frequency; that there are no frequency offsets in the frequency measurement technique; that the phase error in the technique is small and bounded provided the signal frequency is maintained within derived limits. Other properties of the technique are also derived.

The frequency measurement technique is experimentally demonstrated in a number of typical applications.

Secondly, a new phase tracking system is presented, which has similarities to conventional phase locked loops. However, unlike phase locked loops, the new system incorporates a local reference source which effectively stabilizes the phase estimate of the signal input being tracked.

It is shown that the new system has the following advantages: Precise centre frequency, controllable lock range, and elimination or reduction of the effects of imperfections like voltage controlled oscillator phase noise. General behaviour in noise of the new phase tracking system is derived.

An implementation of the new system is presented which employs the frequency measurement technique described above. This implementation is characterized by very precise centre frequency, high phase noise suppression, and can be built almost entirely in digital integrated circuit technology. The new system is experimentally demonstrated in some typical applications.

The techniques presented in this thesis provide improvements of several orders of magnitude in the ability of systems implemented in digital integrated circuit technology to: Measure and control phase and frequency of narrow band signals; Implement high performance phase tracking systems.

Contents

1

Introduction

1.1. INTRODUCTION

High frequency signals in electronic systems often require some type of signal processing. Current signal processing techniques typically rely on either down conversion using heterodyning followed by high speed analog to digital conversion and digital processing. Or the use of analog systems to perform the signal processing.

Considerable effort has gone into developing sophisticated digital signal processing techniques [1],[2]. However, less attention has been paid to developing techniques to digitally perform even simple signal processing, without down conversion and analog to digital conversion [3].

In some applications the use of high speed analog to digital conversion and digital processing may not be possible due to: The nature of the signal is not suitable for down conversion. Or the cost and complexity of the converters and digital processing is considered excessive.

This thesis presents and analyses new techniques to measure and track the phase and frequency of high frequency narrow bandwidth signals. In particular these techniques are all digital in nature or can be implemented in digital integrated circuit technology. The techniques do not employ down conversion via heterodyning, or analog to digital converters.

The techniques presented in this thesis are applicable to a number of common, simple signal processing tasks. For example, modulation and demodulation of narrow bandwidth signals, frequency synthesis, and filtering [5],[4].

The techniques presented are also experimentally demonstrated in typical applications to:

- Verify the theoretical results.
- Demonstrate the simplicity and elegance of the implementations of the new techniques, and the ease of application to common problems.
- Highlight the high performance that can be achieved.

Two related techniques for measuring and tracking phase and frequency are described: a frequency measurement technique, and a phase tracking system.

The frequency measurement technique involves sampling at regular intervals a narrow band signal which has been binary quantized. That is, the narrow band signal can be represented by a square wave. The binary quantized samples are digitally processed to obtain the instantaneous frequency of the signal.

The frequency measurement technique has the advantages that: It is constructed from simple digital components such as logic gates and flip flops. Small phase changes in the signal square wave can be detected even when the frequency measurement system is clocked at a low rate.

Properties of the new frequency measurement technique are derived. It is shown that there are no frequency offsets, also that the phase error in the technique is small and bounded provided the signal frequency is maintained within derived limits. It is highlighted that the frequency measurement technique is most suited for very narrow bandwidth signals. The spectral characteristics of the frequency estimator are also derived.

The frequency measurement technique is demonstrated in typical applications, specifically frequency synthesis and demodulation of a high frequency signal.

The new phase tracking system presented has similarities to conventional phase locked loops. However, unlike phase locked loops [6], the new system incorporates a stable and accurate local reference signal source.

The local reference source effectively stabilizes the phase estimate of the signal input being tracked. The stabilization is achieved via a frequency difference measurement between the local reference and the phase tracking system output.

A small signal model of the new phase tracking system is presented and some properties derived. The general non-linear behaviour is also derived for some important classes of the new phase tracking system, specifically when the input signal is corrupted with noise. Further properties are derived, including the effects of component imperfections like voltage controlled oscillator phase noise.

The analysis results show that the new phase tracking system has significant advantages such as: Very precise and controllable centre frequency. The range of frequencies to which the phase tracking system can lock, can be confined to a small and controllable region around the local reference. The effects of voltage controlled oscillator phase noise can be reduced to an insignificant level.

The centre frequency and phase noise advantages are particularly important when the phase tracking system employs voltage controlled oscillators made in digital integrated circuit technology. The phase noise reduction advantage is dramatically illustrated in the experimental results of one of the example applications.

Many frequency measurement techniques can be used in an implementation of the new phase tracking system. However, an implementation employing the new frequency measurement technique presented first in this thesis, is described. This particular implementation is characterized by very precise centre frequency, high phase noise suppression, and can be built almost entirely in digital integrated circuit technology.

As mentioned previously the new frequency measurement technique is restricted to signal inputs of narrow bandwidth. In contrast, the new phase tracking system can have broadband signal inputs. Hence, the new phase tracking system can also be thought of as providing a broadband interface for the new frequency measurement technique.

The new phase tracking system is experimentally demonstrated in the application of demodulation of a frequency modulated signal. Furthermore, it is demonstrated in the application of a very narrow bandwidth phase locking system. The narrow bandwidth

system is used to synthesize a high rate clock from a low rate reference [7], and also provide filtering for the jitter and noise on the low rate reference.

Aspects of this thesis have been reported in [8], [9], [10] and are the subject of two patent applications [11], [12].

Furthermore, a clock recovery system in a digital application specific integrated circuit employed the new phase tracking system. The digital integrated circuit, integrated functions ranging from clock recovery, physical layer framing, to asynchronous transfer mode cell switching.

1.2. CONTRIBUTIONS OF THESIS

The contributions of this thesis are as follows:

- The proposal of a new frequency measurement technique which involves sampling at regular intervals a binary quantized narrow band signal.
- The analysis of the frequency measurement technique, deriving its operating limits and errors that arise.
- The proposal of a new phase tracking system, which diminishes or overcomes many problems associated with phase locked loops.
- The development of models to quantitatively describe the behaviour of the new phase tracking system. Furthermore the verification of these models and analysis results through simulations and experiments.
- The proposal of a digital implementation of the new phase tracking system, which provides a high precision low cost realization.

1.3. STRUCTURE OF THESIS

In the introduction of the chapters describing the frequency measurement technique and phase tracking system, the relevant existing techniques are referenced and described.

This thesis is organized as follows:

In Chapter 2 the new frequency measurement technique is described. Various properties and operating limits of the frequency measurement method are derived.

In Chapter 3 the new phase tracking system is described. Models are proposed to describe the behaviour of the new phase tracking system, and key properties are derived from these models. A digital implementation of the new phase tracking system is proposed. Experimental verification of the properties derived from the models confirms the accuracy of the models and analysis.

In Chapter 4 the new frequency measurement technique is experimentally demonstrated in typical applications. Experimental results verify the operation of the new frequency measurement technique.

The new phase tracking system is demonstrated in typical applications in Chapter 5.

An implementation of the new phase tracking system employing another frequency measurement technique is presented in Chapter 6. The frequency measurement technique is very simple, but some benefits such as phase noise reduction cannot be obtained when it is employed. However, this particular implementation is useful for applications with undemanding phase noise requirements, such as clock recovery.

Finally, Chapter 7 gives suggestions for further work and concludes the thesis.

2

Digital Frequency Measurement of a Square Wave

2.1. INTRODUCTION

This chapter describes a new digital method to measure the frequency difference between two square waves. For convenience the new method is called the *precise digital frequency detector* (PDFD) (patent pending).

Figure 2-1 illustrates the task that is addressed by the PDFD. At time t_1 the reference square wave leads the signal square wave by θ, at time t_2 the relative phase lead has increased a small amount to $\theta+\delta$, because of a difference in frequency. The PDFD must be able to detect these small relative phase movements and indicate the appropriate difference in frequency.

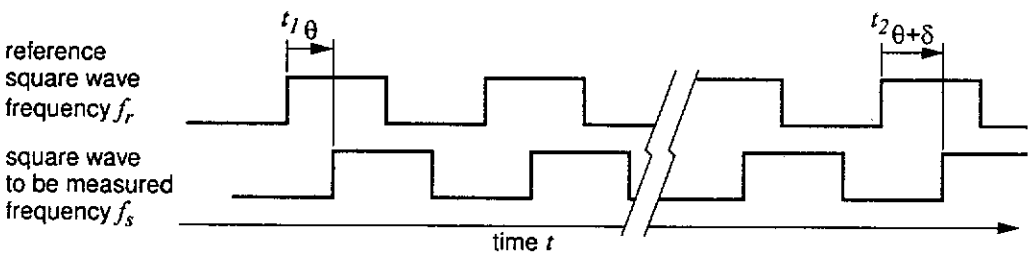

Figure 2-1. Frequency Measurement of a Square Wave. The frequency measurement needs to detect small phase movements between the two square waves, possibly occurring over many cycles.

It is assumed that the phase slipping of the signal square wave of frequency f_s relative to a reference square wave of frequency f_r occurs over several reference cycles, that is

$$|f_r - f_s| \ll f_r \tag{2-1}$$

We assume that the frequency f_r is constant and is the 'nominal' or 'expected' frequency of the signal to be measured of frequency f_s. f_s may be constant or time varying. In many PDFD applications the reference square wave signal of frequency f_r need not exist. However, as will be shown later, to design the PDFD the value f_r needs to be known.

Previous Work. Many methods have been described to measure the frequency of a square wave signal, the methods are divided here into three classes:

- Digital methods.
- Analog methods
- Mixed methods employing analog to digital converters with some analog processing of the square wave.

The existing digital methods can only detect large phase movements between the signal and reference (typically a complete cycle)[13]. Or, they require clock rates much higher than the signal frequency to measure small phase movements. These need to measure accurately the period or difference in phase of every signal clock cycle, thus limiting their application to moderately low frequencies [14],[15]. Some methods employ delay line time digitizers to accurately measure the period of every signal clock cycle without resorting to high clock rates [16]. Unfortunately these methods require delay elements with very small and accurate delays which require full custom integrated circuit design. Furthermore application to high signal frequencies is again limited.

The analog methods are able to detect small phase changes between the signal and reference. Some examples are the quadricorrelator [17], and classic FM discriminators involving the differentiation of the signal by use of tuned filters or time delays [18]. Some examples of mixed analog digital methods are, heterodyning the signal to a much lower frequency whose period can be accurately measured digitally [15],[19]. Converting the square wave to a sine wave by low pass filtering and / or down conversion, then digitizing the waveform using analog to digital converters. There is a

significant amount of literature on using the samples to determine the frequency of the signal [14],[1],[2]. A mixed analog digital method employing analog integration and delta-sigma modulation techniques is presented in [3].

In contrast to the current techniques described above, the PDFD involves sampling the square wave at discrete times. Typically employing a flip flop as the sampler. The binary quantized samples are then digitally processed to obtain the phase movement between the signal and reference square waves.

The PDFD has the following important advantages over the current techniques just described. It can be constructed from simple digital components such as logic gates and flip flops. Small phase movements between the signal and reference square waves can be detected, even when the PDFD is clocked at low rates. Finally, as will be shown, the PDFD has no frequency offsets.

2.1.1. Outline of Chapter 2

This chapter is organized as follows:

Section 2.2 provides an overview of the PDFD operation to aid in the understanding of the more detailed descriptions which follow.

In Section 2.3 equations which describe the operation of the simple frequency detector are derived.

Section 2.4 further details how PDFDs can be implemented using an array of simple frequency detectors and how the output of the array is processed.

Section 2.5 details how to design a PDFD with uniform starting phases and derives operating limits for the PDFD. The operating limits of the PDFD are also discussed.

Section 2.6 generalizes the sampling rate of the PDFD.

Section 2.7 details how to design a PDFD and derives operating limits when the generalized simple frequency detectors described in Section 2.6 are used in the PDFD.

Section 2.8 derives some further limits on the PDFD operating range.

In Section 2.9 the spectral characteristics of the frequency estimator output by the PDFD are determined.

Section 2.10 states that the results on PDFD operating limits are valid when the frequency of the signal square wave is time varying.

Finally, Section 2.11 summarizes the chapter.

Also in Appendix A some derivations concerning aspects of the PDFD are given.

2.1.2. Contributions of Chapter 2

The all digital measurement of small phase movements in a square wave without resorting to high clock speeds has not been described in the literature.

The contributions of this chapter are as follows:

- The proposal of the PDFD method to measure the frequency of a square wave. The advantages the PDFD has over current techniques are given above.
- The analysis of the PDFD, deriving its operating limits and errors that arise in the PDFD.

2.2. OVERVIEW OF PDFD OPERATION

2.2.1. Basic Terms and Definitions

Some terms and definitions important for the understanding of the operation of the PDFD will now be introduced.

The concept of phase for a square wave will be defined at this point. The square wave waveform $v(t)$ is related to the square wave phase $\theta(t)$ as follows:

$$v(t) = \begin{cases} 1, & m \le \theta(t) < m + 1/2 \\ 0, & m + 1/2 \le \theta(t) < m + 1 \end{cases} \qquad m \in Z \tag{2-2}$$

Where Z denotes the set of integers. As can be seen from (2-2), $\theta(t)$ going from 0 to 1 delineates one cycle of the square wave. The time between rising edges of the square wave is $\frac{1}{f}$ seconds, where f is considered the constant frequency of the square wave. f is related to the square wave phase $\theta(t)$ as follows:

$$\theta(t) = ft + \theta_o \tag{2-3}$$

Other frequencies besides f_s and f_r which will appear in text and equations throughout this chapter will now be described. The PDFD samples the signal square wave at regular intervals. The time between sample instants is $\frac{1}{f_c}$ seconds, that is, the PDFD samples at a constant frequency f_c, referred to as the sampling rate of the PDFD.

The ultimate task of the PDFD is to measure the phase movements of the signal square wave with respect to the reference square wave of frequency f_r. However, to achieve this ultimate objective the PDFD utilizes an intermediate measurement which is the phase movements of the signal square wave with respect to another square wave of constant frequency f_{cmp}. The origin of and precise definition of this signal is described later in Section 2.3.

2.2.2. PDFD Operation

The operation of a simple PDFD will now be qualitatively described to aid understanding of the mathematical description which follows.

The signal square wave of frequency f_s is divided by two to produce a square wave of 50/50 mark space ratio and frequency $\frac{f_s}{2}$. This divided down square wave is then sampled at a rate of f_c samples per second. Figure 2-2 illustrates the sampling of the square wave.

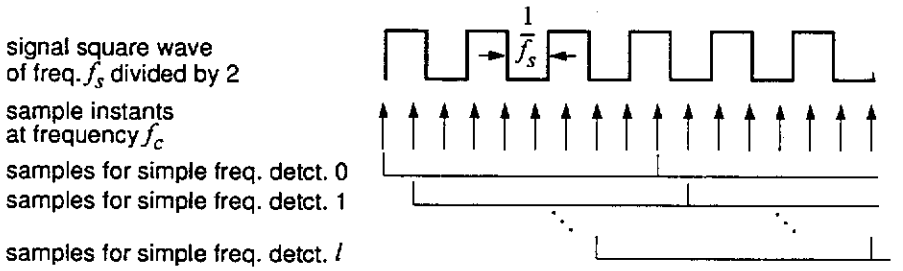

Figure 2-2. Sampling of the signal and pairing the samples to create simple frequency detectors.

To simplify the explanation of the operation of the PDFD and also to simplify its subsequent analysis it is assumed that the signal square wave has a constant frequency f_s. The restriction of constant frequency f_s is later relaxed in Section 2.10.

A first step in the processing is to divide the stream of binary samples into k lower sample rate streams. Each stream consists of samples spaced $\frac{k}{f_c}$ seconds apart. Furthermore, l out of the possible k streams are used (see Figure 2-2). Consecutive samples in each stream (that is samples spaced $\frac{k}{f_c}$ seconds apart) are processed by a mechanism referred to here as a 'simple frequency detector'. Figure 2-3 shows a section of Figure 2-2 in detail. As shown in Figure 2-3 each simple frequency detector has an initial starting phase, for the i^{th} simple frequency detector the starting phase is denoted by θ^i_{init}, ($i \in [0, 1, 2, \ldots, l-1]$). θ^i_{init} is the phase relationship between the instant of the first sample in one of the k streams and the next edge of the signal square wave. θ^i_{init} is a dimensionless quantity defined such that θ^i_{init}/f_s is the actual time delay between the relevant epochs.

Each simple frequency detector indicates when the signal square wave phase moves a complete cycle with respect to a square wave of frequency f_{cmp}. More precisely, the simple frequency detector will indicate a phase movement corresponding to a complete cycle when $(\theta^i_{init} + \theta_{slip})$ equals an integer, and where θ_{slip} is the phase movement of the signal square wave with respect to a square wave of frequency f_{cmp}, that is,

$$\theta_{slip} = (f_{cmp} - f_s)t \tag{2-4}$$

The simple frequency detector is assumed to emit one when a phase movement corresponding to a full cycle is detected and a zero otherwise. The simple frequency detector produces this one output immediately after receiving its sample of the signal square wave. Recall that the simple frequency detector operates on samples spaced $\frac{k}{f_c}$ seconds apart.

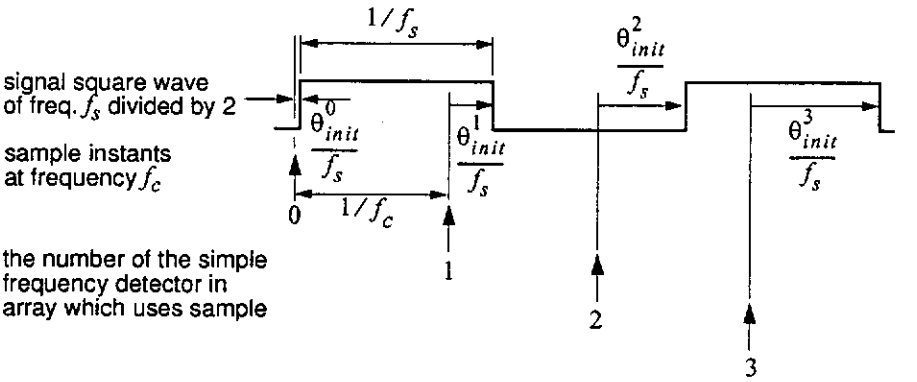

Figure 2-3. The sampling process creates diverse starting phases.

As shown in Figure 2-3, the θ^i_{init} for each of the simple frequency detectors will be different, due to the different starting times of the simple frequency detectors. Out of the k possible simple frequency detectors the l used in the PDFD can be chosen (see Section 2.5) so that the θ^i_{init} will be uniformly distributed across a signal square wave cycle.

The l simple frequency detectors are considered to form an array of l phased simple frequency detectors. In a period of $\frac{k}{f_c}$ seconds each of the l simple frequency detectors will have an opportunity to report its decision on a phase movement of a complete cycle. Let the integers N_j represent the total number of complete cycle phase movements reported by all simple frequency detectors in the j^{th} interval. N_j will have a value between 0 and l. The value of a particular N_j in the sequence represents the phase movement of the signal square wave with respect to a square wave of frequency f_{cmp} that occurred in the j^{th} interval.

By accumulating the successive N_j generated by the PDFD, the phase movement of the signal square wave with respect to a square wave of frequency f_{cmp} can be found. This phase movement is quantized to $1/l^{th}$ of the signal square wave cycle. Thus the PDFD acts as a phase movement quantizer. Dividing the phase movement measured by the PDFD by the time taken for the PDFD to measure the phase movement yields an estimate of relative frequency. Since the error in the phase measurement is bounded, the frequency measurement has no long term offset from the true value.

2.3. THE SIMPLE FREQUENCY DETECTOR

In this section we develop equations which describe the operation of a simple frequency detector. As noted previously, the square wave signal to be measured is divided down by two using a flip flop to ensure a good mark space ratio in the resulting square wave. The resulting square wave is sampled at rate f_c such that

$$f_s < f_c < 2f_s \tag{2-5}$$

As a first step, consider a simple frequency detector which uses every sample as illustrated in Figure 2-4. The simple frequency detector starting phase θ^i_{init} (see Figure 2-4) is a dimensionless quantity defined such that θ^i_{init}/f_s is the actual time delay between the relevant epochs. Thus θ^i_{init} will take on a value in the range 0 to 1.

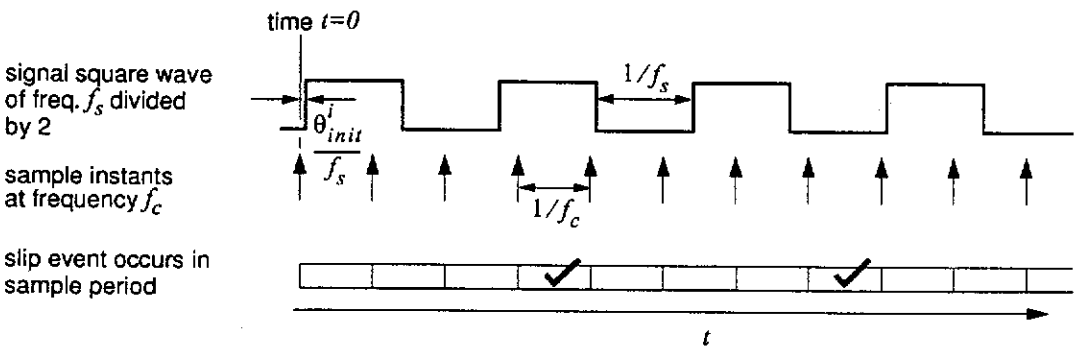

Figure 2-4. The sampling process. Simple frequency detectors are formed by comparing consecutive samples, or by comparing samples spaced k samples apart.

For the simple frequency detector which uses every sample, θ_{slip} is given by

$$\theta_{slip} = (f_c - f_s)t \tag{2-6}$$

The key element of the simple frequency detector is a mechanism that identifies when two sampling instants of the sampling process fall within a single period of the signal square wave. As shown in Figure 2-4, this event can be identified by simply checking the last two successive samples to see if they have the same value. Identification of the event can logically be accomplished using the exclusive OR of successive samples followed by an inversion. A logical 1 is output to report when the event occurs. The event will be referred to as a 'slip event'. It is shown in Appendix A.2 that a slip event will be reported on the sampling instants following the time instants given by (2-7). Where Z^+ denotes the positive integers.

$$t_m = \frac{m - \theta^i_{init}}{f_c - f_s}, \qquad m \in Z^+ \tag{2-7}$$

The system comprised of the signal sampler and a mechanism for reporting slip events behaves as a simple frequency detector in the sense that the average frequency of slip event reports is given by

$$f_p = f_c - f_s \tag{2-8}$$

From inspection of (2-7) and (2-8) it can be seen that a slip event occurs when $\theta^i_{init} + \theta_{slip}$ equals an integer. That is, a slip event indicates a phase movement of a complete cycle between the signal square wave of frequency f_s and a square wave of frequency f_c.

In the PDFD described in Section 2.2, the simple frequency detectors used only every k^{th} sample of the signal to be measured. Thus consider a system where only every k^{th} sample of the signal is used. For k odd, the slip event that is to be identified corresponds to an occurrence of two consecutive samples having the same value. Again, a pulse is output by the system to report when one of these slip events occurs.

Define p as

$$p \equiv \left\lfloor \frac{k(f_c - f_s)}{f_c} \right\rfloor, \tag{2-9}$$

where $\lfloor x \rfloor$ denote the floor function, that is the greatest integer less than or equal to x [20]. It is shown in Appendix A.2 that if p is even then a slip event will be reported on the sampling instants following the time instants given by (2-10),

$$t_m = \frac{m - \theta_{init}^i}{f_{cmp} - f_s} \tag{2-10}$$

where

$$f_{cmp} \equiv f_c\left(1 - \frac{p}{k}\right) \tag{2-11}$$

From (2-10) it can be seen again that a slip event occurs when $\theta_{init}^i + \theta_{slip}$ equals an integer. Where θ_{slip} is now given by (2-4). Note that no signal with frequency f_{cmp} actually exists. f_{cmp} is simply the frequency of a square wave relative to which the signal square wave f_s is effectively measured.

If p is odd, then a slip event will be reported on all sampling instants other than those sampling instants immediately following the instants defined by (2-10).

The simple frequency detector is linear in the range defined by (2-12), and has negative slope if p is even, and a positive slope if p is odd.

$$f_c\left(1 - \frac{p+1}{k}\right) < f_s < f_c\left(1 - \frac{p}{k}\right) \tag{2-12}$$

Up to now it has been assumed that k is odd. When k is even, an identical result is obtained. However, the slip event that is to be identified corresponds to occurrence of two consecutive samples with a different value, instead of the same value.

The simple frequency detector just described, in which every k^{th} sample is used, can be modified to ensure that the detector has only a negative slope. If p is odd the action of

not reporting a slip event and reporting a slip event are swapped. In this way, the frequency detector characteristic always has a negative slope, as shown in Figure 2-5.

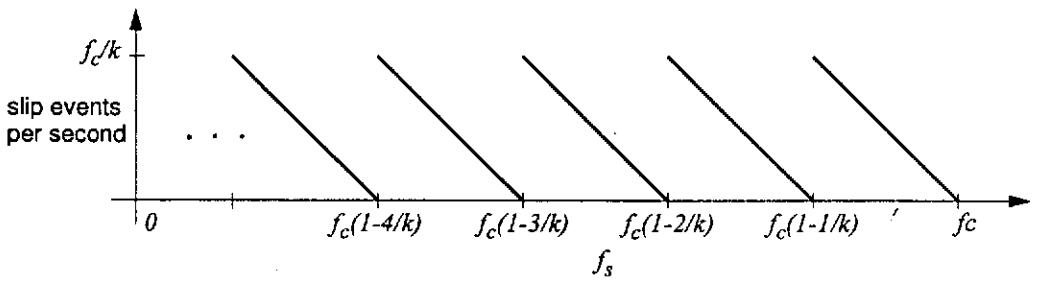

Figure 2-5. Modified frequency detector characteristics

2.4. THE PDFD, AN ARRAY OF SIMPLE FREQUENCY DETECTORS

In this section we derive equations relating the PDFD array output N_j to the phase movement θ_{slip} (2-4). Furthermore, in this section we show that the PDFD acts as a quantizer of phase movement.

As described in Section 2.2, in the PDFD l streams are processed by an array of the simple frequency detectors. These l simple frequency detectors can be constructed to have staggered starting phases θ^i_{init} as illustrated in Figure 2-3. Note that the l simple frequency detectors will have correspondingly staggered outputs. The start time of each simple frequency detector in the array will be separated by at least $\frac{1}{f_c}$ seconds.

Each of the simple frequency detectors reports whether or not it has detected a slip event every k clock periods, this period of $\frac{k}{f_c}$ seconds is referred to as the "reporting period" of the PDFD.

The starting phases θ^i_{init} of the l simple frequency detectors, will be distributed in some manner in the interval [0,1). By a judicious choice of l, k, f_s, f_c and the actual l streams utilized, the distribution of the θ^i_{init} can be made close enough to uniform for practical purposes. With uniformly distributed θ^i_{init}, the slip event instant for each of the l frequency detectors, given by (2-10), will be uniformly distributed in time.

As described in Section 2.2, a sequence of integers N_j is generated as follows: Once every $\frac{k}{f_c}$ seconds, the decisions on phase movements corresponding to a complete

cycle (or slip events) output by the l simple frequency detectors are added up to form N_j. In each reporting period, the average number of the l frequency detectors that will report a slip event can be found from (2-10). This average value of N_j which is denoted by N_{ave}, is given by:

$$N_{ave} = \frac{lk}{f_c}(f_{cmp}-f_s) = l\left(k-p-\frac{kf_s}{f_c}\right) \tag{2-13}$$

Since the l starting phases θ_{init}^{i} are assumed to be uniformly distributed in the interval [0,1), their values will be in the set given by (2-14)

$$[\phi_0, \phi_0+\frac{1}{l}, \phi_0+\frac{2}{l}, \ldots, \phi_0+\frac{l-1}{l}] \tag{2-14}$$

where ϕ_0 is the smallest of the θ_{init}^{i}.

Consider now the addition of all the N_j generated since the initialization of the PDFD up to the end of the n^{th} reporting period and multiplying this sum by $\frac{1}{l}$. This sum, denoted by θ_{out}, is given by (2-15)

$$\theta_{out} = \frac{1}{l}\sum_{i=0}^{l-1}\left\lfloor \theta_{slip}+\theta_{init}^{i}\right\rfloor \tag{2-15}$$

where

$$\theta_{slip} = \frac{nk}{f_c}(f_{cmp}-f_s), \qquad n \in Z^{+} \tag{2-16}$$

It can be shown (Appendix A.3) that for θ_{init}^{i} given by (2-14), θ_{out} can be expressed as

$$\theta_{out} = \frac{\lfloor l(\theta_{slip}+\phi_0)\rfloor}{l} \tag{2-17}$$

From (2-17) it can be seen that the PDFD acts a quantizer of phase movement. As illustrated in Figure 2-6, the quantization level is $1/l$ $^{\text{th}}$ of a signal square wave cycle,

and there is an offset of $-\phi_0$. The relationship between θ_{out} and θ_{slip} given in (2-15) is referred to here as the PDFD characteristic.

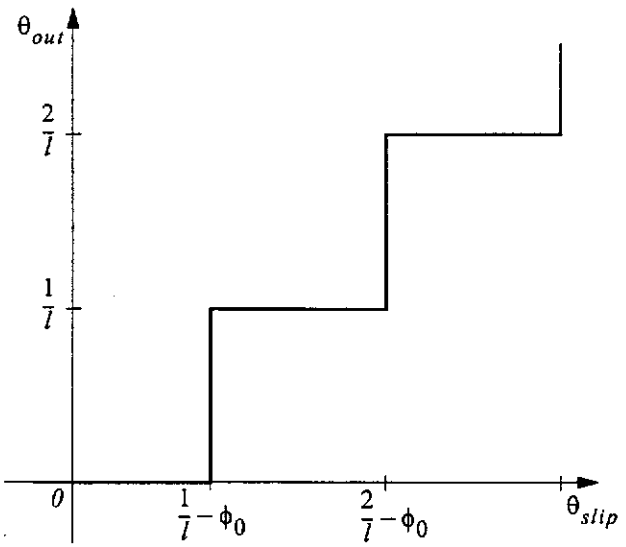

Figure 2-6. PDFD Characteristic for uniformly distributed starting phases. The PDFD acts as a quantizer of phase movement.

In many applications, the phase movement of the signal square wave with respect to a reference square wave of the nominal frequency f_r (Figure 2-1) will be required. The phase movement of the signal square wave with respect to a reference square wave of frequency f_r is obtained as follows: The average number of frequency detectors which report a slip each reporting period N_{ave}, (2-13) is found for $f_s=f_r$. This specific value of N_{ave} is denoted N_{nom}. N_{nom} is then subtracted from the actual PDFD output (N_j) each reporting period, to obtain the phase movements with respect to a reference square wave of frequency f_r.

Alternatively, two arrays of simple frequency detectors can be used, one measuring the phase movement of the signal square wave with frequency f_s with respect to f_{cmp}. The other measuring phase movement of the reference square wave with frequency f_r with

respect to f_{cmp}. The phase movement of the signal square wave with respect to the reference square wave can be obtained by subtracting the f_r measurement from the f_s measurement.

2.5. OPERATING LIMITS

In this section we determine the range of values of the signal square wave frequency f_s for which the PDFD correctly reports phase movements. A key factor to be considered is the distribution of the starting phases θ^i_{init}. Therefore we initially show how k, l and f_c can be chosen to obtain the θ^i_{init} evenly distributed (Figure 2-3) for the case when the frequency of the signal square wave is exactly f_r, that is when $f_s=f_r$.

The specific, but important case, where the l simple frequency detectors use l successive samples of the signal waveform is considered. The θ^i_{init} values generated by this process are illustrated in Figure 2-3. The value θ^i_{init} for the i^{th} frequency detector can be determined given the value θ^j_{init} for one other frequency detector, say j=0, and the frequencies f_r and f_c (see Figure 2-3):

$$\theta^i_{init} = 1 + \theta^0_{init} - \frac{f_r i}{f_c} + \left\lfloor \frac{f_r i}{f_c} - \theta^0_{init} \right\rfloor, \qquad i \in [0, 1, 2, \ldots, l-1] \tag{2-18}$$

For a given f_r and l, the θ^i_{init} will be evenly distributed (Figure 2-3) if f_c satisfies

$$f_c = \left(\frac{l}{l-p}\right) f_r \tag{2-19}$$

and l and $(l-p)$ have no common factors.

k is chosen so that the individual frequency detectors are maintained in their linear region (2-12) for the expected values of f_s.

Note that it will not be possible to use successive samples of the signal square wave in applications were the sampling rate f_c is not freely chosen. In these cases, which samples are observed to obtain even starting phases will be specific to f_r and f_c.

However, many of the results obtained here are applicable to this more complex situation.

Although l, k, and f_c may be chosen to obtain uniformly distributed starting phases when the signal square wave frequency is exactly the nominal frequency f_r, this will in general not result in perfectly uniformly distributed starting phases for sampling the signal square since its frequency f_s is not known. However, it is shown in Appendix A.3 that for f_s close to the nominal frequency f_r, the θ_{init}^{i} generated by sampling the signal square wave will not be significantly perturbed from those generated by sampling a square wave of frequency f_r. Below we quantify how close f_s needs to be to the nominal frequency f_r.

It is shown in Appendix A.3 that for f_s close to f_r the PDFD characteristic (2-15) is bounded by two quantizer functions (2-20), that is,

$$\frac{\lfloor l(\theta_{slip} + \phi_0 - |\Delta_{max}|) \rfloor}{l} \le \theta_{out} \le \frac{\lfloor l(\theta_{slip} + \phi_0 + |\Delta_{max}|) \rfloor}{l} \tag{2-20}$$

The two bounding quantizer functions are shown in Figure 2-7. The Δ_{max} in (2-20) is the maximum perturbation of the starting phases from their nominal uniform distribution.

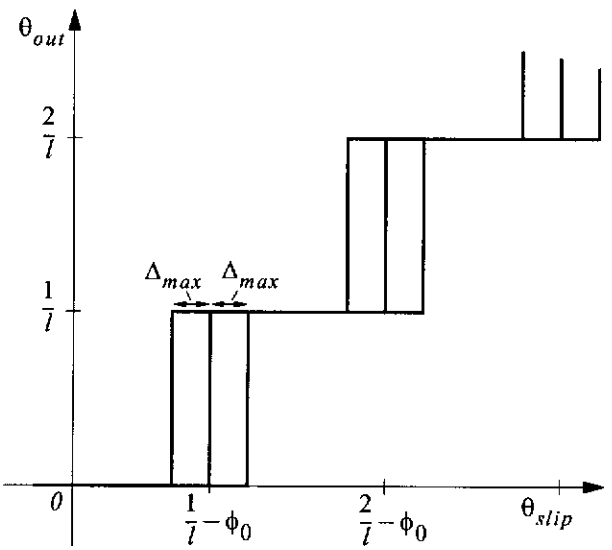

Figure 2-7. PDFD Characteristic for non-uniformly distributed starting phases as will occur in practice. The PDFD Characteristic is bounded by two quantizer functions.

Based on (2-20), it is shown in Appendix A.3 that the operating range for f_s is given by (2-21)

$$f_{smin} \leq f_s \leq f_{smax} \tag{2-21}$$

Where

$$f_{smin} = f_r\left(1 - \frac{\gamma}{(l-p)(l-1)}\right) \tag{2-22}$$

$$f_{smax} = f_r\left(1 + \frac{\gamma}{(l-p)(l-1)}\right) \tag{2-23}$$

$$|\Delta_{max}| = \frac{\gamma}{l} \tag{2-24}$$

γ is chosen to be less than one, so that Δ_{max} is some fraction of $\frac{1}{l}$ (2-24) which is the PDFD quantization interval.

Clearly it is desirable to have the distance between the two bounding quantizers (2 Δ_{max}) as small as possible (Figure 2-7). However, the results of this section and Appendix A.3 demonstrate that when the PDFD is required to measure phase movements much less than one cycle (i.e. large l), and the sampling rate f_c is not high, the operating range of f_s (2-21) is narrow. For example, for a PDFD with l equal to one hundred, and a sampling rate approximately equal to the signal frequency (p equal to one, γ equal to 0.5), f_s must be within ±51 parts per million (ppm) of f_r (2-22), (2-23), (2-21). Nevertheless, in many systems the signals will be in a narrow range of frequencies as they are of low data rate and modulated onto a high carrier frequency [21]. Or the signals may not contain data themselves, but rather timing information to facilitate the synchronization of transmitting and receiving components in a communication system.

To increase the range of f_s the following methods can be employed: The sampling rate f_c can be increased (p greater than one) to increase the operating range. Choosing a smaller l dramatically increases the operating range as $f_{smax} - f_{smin}$ (2-21) is approximately proportional to $1/l^2$.

The different starting phases θ_{init}^{i} may be obtained in a 'parallel' fashion. The different θ_{init}^{i} is obtained by delaying the signal by different amounts before it is sampled. The delayed versions of the signal are sampled simultaneously. This 'parallel' method is in contrast to the 'serial' like method used up to this point, where the different θ_{init}^{i} arises from the sampling process itself (see Figure 2-3). It can be shown that the obtaining of many samples in parallel increases the operating range of f_s (2-21). However, the hardware complexity is increased when using parallel methods. Furthermore, the accuracy with which the delay elements can be made may limit the smallest phase movement that can be measured.

Finally, a combination of the 'serial' and 'parallel' methods described above is possible with parallel groups of serial simple frequency detectors. In this situation hardware complexity can be traded off against the operating range of f_s.

2.6. GENERALIZED SAMPLING RATE

In Section 2.3 the sampling rate of the PDFD, f_c, was required to be in the restricted range given by (2-5). However, in this section the simple frequency detector is generalized so that PDFD sampling rate can be outside the restricted range of (2-5).

Consider that the signal square wave is now sampled at the rate ηf_c, where f_c is in the range given by (2-5), and η is in the set

$$\eta \in \left(\ldots, \frac{1}{3}, \frac{1}{2}, 1, 2, 3, \ldots \right) \tag{2-25}$$

Firstly consider the cases where η is an integer. If only every η^{th} sample is used. Then the generalized simple frequency detector is equivalent to the simple frequency detector described in Section 2.3 that uses every sample at rate f_c.

Consider now the cases where η is a fraction. If only every ηk^{th} sample is used. Then the generalized simple frequency detector is equivalent to the simple frequency detector described in Section 2.3 that uses every k^{th} sample of a sampler running at rate f_c.

2.7. OPERATING LIMITS FOR GENERALIZED FREQUENCY DETECTORS

In this section the range of values of the signal square frequency f_s for which a PDFD employing generalized simple frequency detectors (Section 2.6) correctly reports phase movements, is found.

Note that the generalized simple frequency detector described in Section 2.6 uses only one in ηk samples. Thus, using a single sampler running at rate ηf_c an array of l simple frequency detectors can be constructed for

$$1 \le l \le \eta k \tag{2-26}$$

Note that slip events for the PDFD using the generalized simple frequency detector are reported every ηk clock periods which have period $\frac{1}{\eta f_c}$ seconds. Hence the PDFD has the reporting period of $\frac{k}{f_c}$ seconds.

As in Section 2.5, we initially show how η, k, l and f_c can be chosen to obtain the θ^i_{init} evenly distributed for the case when the frequency of the signal square wave is exactly f_r, that is when $f_s=f_r$. Note that initially only η less than or equal to one is considered.

Again, the specific but important case, where the l simple frequency detectors use l successive samples of the signal waveform is considered. The θ^i_{init} values generated by this process are illustrated in Figure 2-8. The value θ^i_{init} for the i^{th} frequency detector can be determined given the value θ^j_{init} for one other frequency detector, say $j=0$, and the frequencies f_r and f_c (see Figure 2-8):

$$\theta^i_{init} = 1 + \theta^0_{init} - \frac{f_r}{\eta f_c} i + \left\lfloor \frac{f_r}{\eta f_c} i - \theta^0_{init} \right\rfloor, \qquad i \in [0, 1, 2, \ldots, l-1] \tag{2-27}$$

For a given f_r and l, the θ^i_{init} will be evenly distributed across 0,1 if f_c satisfies

$$f_c = \frac{l}{l - p\eta} f_r \tag{2-28}$$

and l and $(l-p\eta)$ have no common factors.

Furthermore, the value of N_{ave} when the signal frequency f_s is equal to f_r, N_{nom} will be

$$N_{nom} = p(k\eta - l) \tag{2-29}$$

k is chosen so that the individual frequency detectors are maintained in their linear region (2-12) for the expected values of f_s.

The operation of the PDFD using the generalized simple frequency detectors is similar to PDFD operation described in Section 2.4 and Section 2.5. Again the PDFD characteristic (2-15) when f_s is close to f_r can be shown to be bounded by two quantizer functions (2-20). Where again Δ_{max} in (2-20) is the maximum perturbation of the starting phases from their nominal uniform distribution.

As in Section 2.5 with Δ_{max} set to some fraction γ of $\frac{1}{l}$ (2-24) limits f_{smin}, f_{smax} for f_s (2-22) can be found

$$f_{smin} = f_r\left(1 - \frac{\gamma\eta}{(l-p\eta)(l-1)}\right) \tag{2-30}$$

$$f_{smax} = f_r\left(1 + \frac{\gamma\eta}{(l-p\eta)(l-1)}\right) \tag{2-31}$$

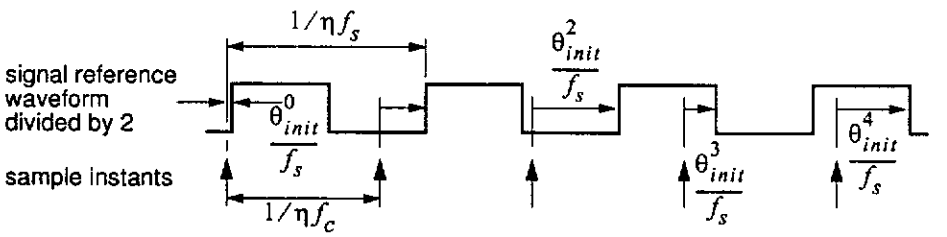

Figure 2-8. Frequency detector start phases for generalized sampling rate. In this section the sampling frequency is chosen so that using successive samples yields evenly distributed starting phases. Using successive samples simplifies the analysis and yields simplified hardware.

The limits f_{smin}, f_{smax} can be found for more general situations when η is greater than one or when successive samples are not used. Suppose the time between the sample instant for the first simple frequency detector (0^{th}) and the sample instant for the last (l-1^{th}) simple frequency detector is T_{max}. T_{max} can be expressed as a fraction χ of $\frac{1}{f_r}$

$$T_{max} = \frac{\chi}{f_r} \tag{2-32}$$

Then Δ_{max} can be found to be

$$\Delta_{max} = \chi\left(1 - \frac{f_s}{f_r}\right) \tag{2-33}$$

and with Δ_{max} set to some fraction γ of $\frac{1}{l}$ (2-24) limits f_{smin}, f_{smax} are found

$$f_{smin} = f_r\left(1 - \frac{\gamma}{\chi l}\right) \tag{2-34}$$

$$f_{smax} = f_r\left(1 + \frac{\gamma}{\chi l}\right) \tag{2-35}$$

From (2-34), (2-35) a useful bound can be found on the minimum sampling rate required to achieve $\Delta_{max} < \frac{1}{2l}$:

$$\eta f_c > l^2(f_{smax} - f_{smin}) \tag{2-36}$$

2.8. INSTANTANEOUS ERROR

Thus far we have considered the error between the accumulated reported phase movements, θ_{out} (2-15), and the actual phase movement since the PDFD start θ_{slip}.

However, the PDFD may also incorrectly report the phase movement between the square waves of frequency f_s and f_{cmp} that has occurred in the last reporting period as follows: With f_s not equal to f_r the array of frequency detectors should report a phase movement of $\lfloor N_{ave} \rfloor$ or $\lfloor N_{ave} \rfloor$+1 $1/l^{\text{th}}$ cycles between f_s and f_{cmp}. However for a particular detector the θ_{init} may be sufficiently perturbed from its nominal value such that $\lfloor N_{ave} \rfloor$-1 or $\lfloor N_{ave} \rfloor$+2 is reported. Hence the instantaneous phase movement measurement is in error by more than $1/l^{\text{th}}$ of a cycle. The limits between which f_s may range before this instantaneous measurement error occurs will now be given.

Case p=1, η ≤1. Consider the case of f_s slightly greater than f_r, and p equal to one. A frequency f_{smax1} (2-37) can be found (Appendix A.4), such that: For f_s greater than f_{smax1} $\lfloor N_{ave} \rfloor$-1 may be reported and for f_s less than f_{smax1} $\lfloor N_{ave} \rfloor$-1 will never be reported. $\lfloor N_{ave} \rfloor$-1 is the first error to occur for f_s greater than f_r.

$$f_{smax1} = f_r\left(1 + \frac{\eta}{(l-\eta)(2l+1)}\right) \tag{2-37}$$

For the case of f_s slightly less than f_r, and p equal to one a frequency f_{smin1} (2-38) can be found (Appendix A.4), such that: For f_s less than f_{smin1} $\lfloor N_{ave} \rfloor$+2 may be reported and for f_s greater than f_{smin1} $\lfloor N_{ave} \rfloor$+2 will never be reported. $\lfloor N_{ave} \rfloor$+2 is the first error to occur for f_s less than f_r.

$$f_{smin1} = f_r\left(1 - \frac{\eta}{(l-\eta)(2l-1)}\right) \tag{2-38}$$

Case p>1, η ≤1. Now considering the cases were p is greater than one. To make the problem more tractable only the cases were l is chosen as follows are considered.

$$l = pr + 1 \qquad r \in Z, r \geq 2 \tag{2-39}$$

As for the p equal to one cases, the frequencies f_{smaxp}, f_{sminp} can be found (Appendix A.4), such that when f_s is greater than f_{sminp} and less than f_{smaxp} the $\lfloor N_{ave} \rfloor$-1 and $\lfloor N_{ave} \rfloor$+2 errors discussed above do not occur.

$$f_{smaxp} = f_r\left(1 + \frac{\eta p}{(l-p\eta)(l(2p-1)+1)}\right) \tag{2-40}$$

$$f_{sminp} = f_r\left(1 - \frac{\eta p}{(l-p\eta)(l(p+1)-1)}\right) \tag{2-41}$$

2.9. SPECTRAL CHARACTERISTICS

Denote the difference between the accumulated PDFD output θ_{out} (2-15) and θ_{slip} at the end of the n^{th} reporting period by the sequence ϕ_n, that is

$$\phi_n = \theta_{slip} - \theta_{out} \tag{2-42}$$

In this section the spectral characteristics of the sequence ϕ_n are derived. For certain applications of the PDFD, it may be necessary to low pass filter the output of the PDFD. For example filtering may be used to reduce the high frequency variation or jitter of ϕ_n. So the spectrum of ϕ_n will be required to ascertain the effects of filtering. The spectral characteristics of ϕ_n are similar to the spectral characteristics of waiting time jitter described in [22], [23].

Define the sequences υ_n^i as follows

$$\upsilon_n^i = \xi n + \theta_{init}^i - \lfloor \xi n + \theta_{init}^i \rfloor \tag{2-43}$$

$$\xi = \frac{k}{f_c}(f_{cmp} - f_s) \tag{2-44}$$

ϕ_n (2-42) can be given as a linear combination of the υ_n^i and a constant

$$\phi_n = \frac{1}{l}\left(\sum_{i=0}^{l-1} \upsilon_n^i - \sum_{i=0}^{l-1} \theta_{init}^i \right) \tag{2-45}$$

The periodic function $\upsilon(t)$ (2-46) has the Fourier series representation (2-47)

$$\upsilon(t) = \xi t - \lfloor \xi t \rfloor \tag{2-46}$$

$$\upsilon(t) = \sum_{w=-\infty}^{\infty} F_w e^{j2\pi w \xi t} \qquad F_w = \begin{cases} \frac{1}{2} & w = 0 \\ \frac{-1}{j2\pi w} & w \neq 0 \end{cases} \tag{2-47}$$

The periodic functions $\upsilon^i(t)$ (2-48) are time shifted versions of $\upsilon(t)$ and hence have the same Fourier series representation as $\upsilon(t)$ but with coefficients F_w^i.

$$\upsilon^i(t) = \xi t + \theta_{init}^i - \left\lfloor \xi t + \theta_{init}^i \right\rfloor \tag{2-48}$$

$$F_w^i = F_w e^{j2\pi w\theta_{init}^i} \tag{2-49}$$

When the $\upsilon^i(t)$ are sampled at the equispaced times (2-50) the sequences υ_n^i are obtained.

A periodic function $\phi(t)$ can be constructed from the functions $\upsilon^i(t)$, which when sampled at the equispaced times (2-50) the sequence ϕ_n is obtained.

$$t = 1, 2, 3\ldots \tag{2-50}$$

From (2-45), (2-47), and (2-49) the Fourier series representation of $\phi(t)$ is the same as $\upsilon(t)$ but with coefficients F_w^T.

$$F_w^T = \begin{cases} \dfrac{1}{2} - \dfrac{1}{l}\displaystyle\sum_{i=0}^{l-1} \theta_{init}^i & w = 0 \\ F_w \dfrac{1}{l}\displaystyle\sum_{i=0}^{l-1} e^{j2\pi w\theta_{init}^i} & w \neq 0 \end{cases} \tag{2-51}$$

The Fourier transform of $\phi(t)$ is found to be

$$\Phi(j2\pi f) = 2\pi \sum_{w=-\infty}^{\infty} F_w^T \delta(f - \xi w) \tag{2-52}$$

Furthermore, the Fourier transform of the sampled $\phi(t)$, ϕ_n is found to be

$$\Phi_s(j2\pi f) = 2\pi \sum_{w=-\infty}^{\infty} F_w^T \sum_{m=-\infty}^{\infty} \delta(f - \xi w - m) \tag{2-53}$$

Confining ourselves to the frequency interval [0,1), the spectrum of the ϕ_n sequence can be written as

$$\Phi_s(j2\pi f) = 2\pi \sum_{w=-\infty}^{\infty} F_w^T \delta(f-(\xi w - \lfloor \xi w \rfloor)) \tag{2-54}$$

The frequency interval [0,1) physically corresponds to the frequency interval [0, $\frac{f_c}{k}$) as the physical reporting rate of the PDFD is $\frac{f_c}{k}$.

Thus the spectrum of ϕ_n consists of a number of spectral lines (infinitely many if ξ irrational) who amplitudes are given by the F_w^T.

To verify the prediction of the spectral characteristics of ϕ_n, a ϕ_n sequence of length one thousand was generated for a PDFD with l=10 and ξ=0.5301. A discrete Fourier transform was performed on the sequence. The resulting spectrum is shown in Figure 2-11. Also shown in Figure 2-9 and Figure 2-10 are spectrum for the υ_n^i sequence and the ϕ_n sequence if the θ_{init}^i were uniformly distributed.

The spectrum for ϕ_n was also generated using (2-54) for one thousand terms. The result is shown in Figure 2-12 and as can be seen, is in good agreement with the spectrum obtained from the sequence. In Figure 2-9 to Figure 2-12 the spectral line at $f = 0$ has been removed, and the scales in the figures are linear. Furthermore the figures are intended only to show similarities or differences in the shape of the spectrum and not provide detailed results for the specific example.

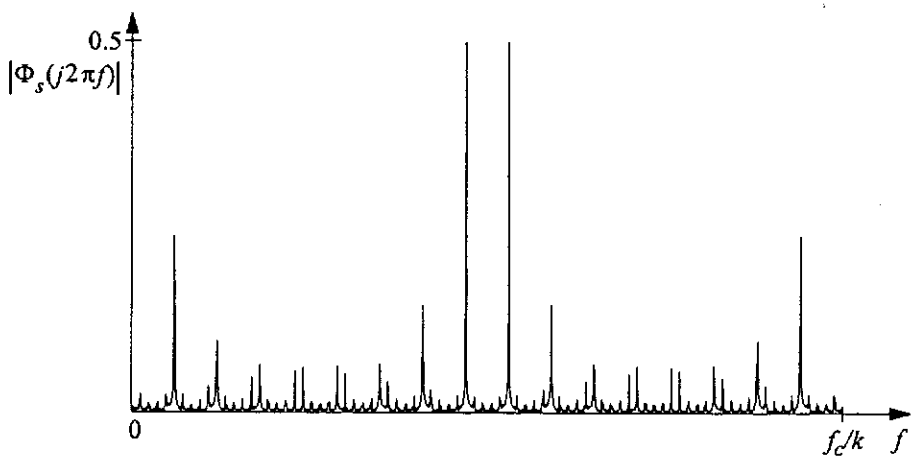

Figure 2-9. Spectrum for sequence υ_n^i

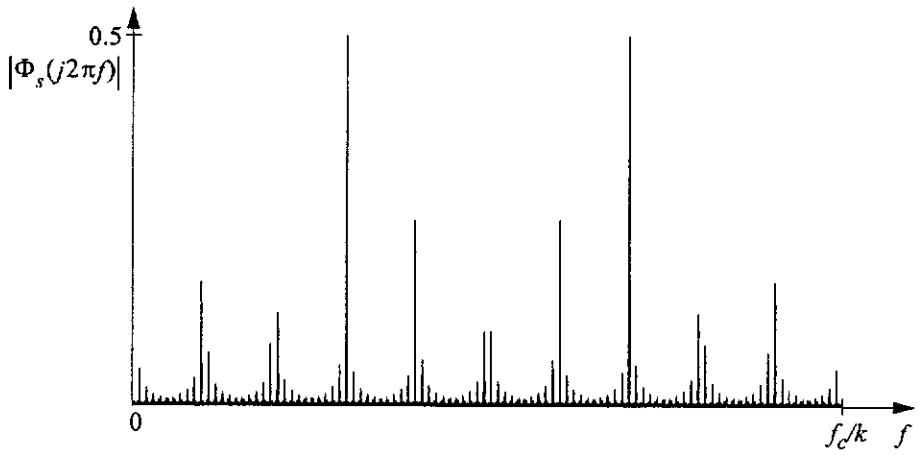

Figure 2-10. Spectrum for sequence ϕ_n with uniformly distributed θ^i_{init}. Note the difference between this spectrum and the spectrum for each individual frequency detector Figure 2-9.

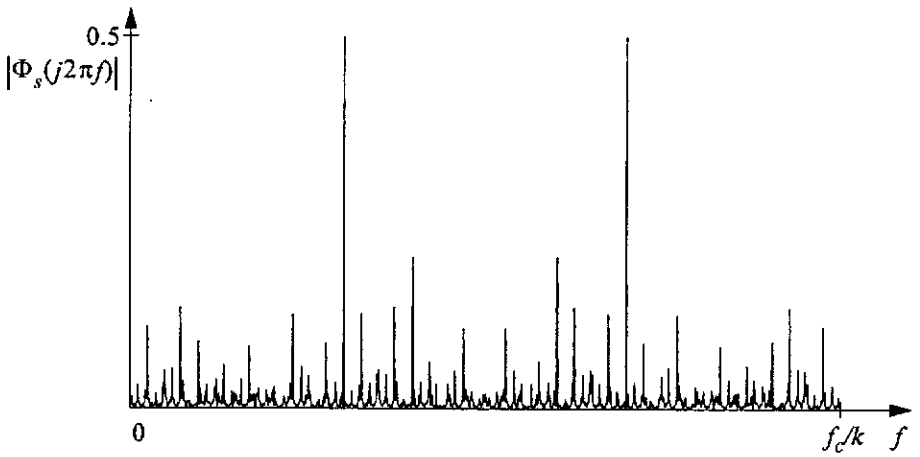

Figure 2-11. Spectrum for sequence ϕ_n. Note how this spectrum contains the dominate features of the uniformly distributed θ^i_{init} spectrum above.

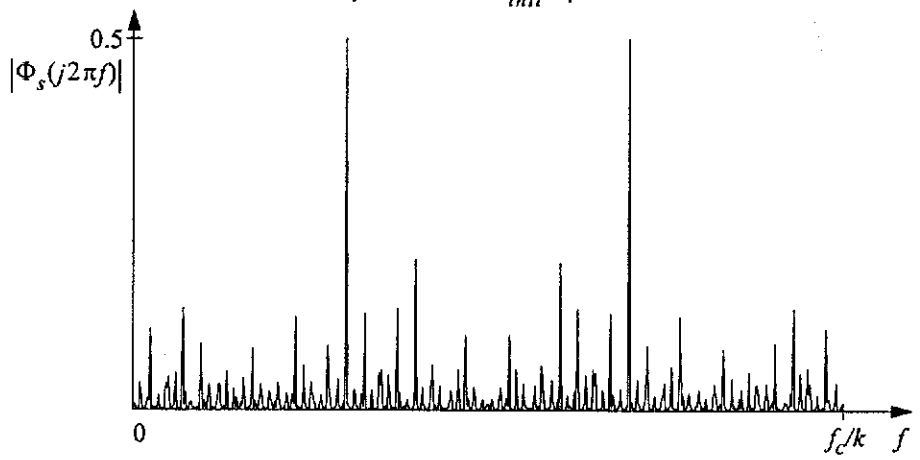

Figure 2-12. Predicted Spectrum for sequence ϕ_n. Agrees well with the actual spectrum Figure 2-11.

2.10. PDFD OPERATION FOR TIME VARYING FREQUENCY

Thus far it has been assumed that the signal square wave frequency f_s is constant. Assuming f_s was constant permitted a succinct derivation of the PDFD properties. Furthermore some of the more specific properties such as spectral characteristics and instantaneous error can likely only be derived with the assumption of constant f_s.

However in many applications the signal square wave frequency f_s is a function of time $f_s(t)$. It is shown in Appendix A.5 that if the function $f_s(t)$ is bounded as follows

$$f_{smin} \leq f_s(t) \leq f_{smax} \tag{2-55}$$

with f_{smin} and f_{smax} as given by (2-22)(2-23), (2-30)(2-31), or (2-34)(2-35). Then the PDFD characteristic (2-15) relating θ_{out} to θ_{slip} will be bounded by the two quantizer functions given in (2-20).

2.11. SUMMARY

A new method has been presented to measure small frequency differences between two square waves. The method called the PDFD involves the use of a large number of simple frequency detectors each with different start phases. Importantly, arbitrarily small phase movements between the signal and reference square waves can be detected, even when the PDFD is clocked at a low rate. The PDFD is totally digital and has no frequency offsets. For many applications it will permit the removal of analog subsystems, or high speed analog to digital converters used for frequency detection.

The operating limits of the PDFD were derived. It was found that the allowable deviation from the nominal frequency of the signal being measured was approximately proportional to $1/l^2$. That is, approximately proportional to the square of the smallest measurable phase change.

The PDFD offers significant advantages for applications wherever small frequency differences have to be measured. For example in the demodulation or modulation of angle modulated signals, measurement and reconstruction of frequency in baseband digital transmission systems, and frequency synthesis.

3

A Frequency Steered Phase Locked Loop

3.1. INTRODUCTION

Phase locked loops (PLL) are one of the most frequently used communications circuits. PLLs have been used for filtering, frequency synthesis, frequency and phase modulation, demodulation, signal detection and a variety of other applications. The PLL commonly has a number of defects when constructed from typical components. Some of the defects of the PLL that are relevant to this chapter include:

- Rapid, reliable locking to the desired signal of narrow bandwidth PLLs. Particularly when there is significant frequency difference between the PLL's voltage controlled oscillator (VCO) and the input signal. This problem is especially serious when the VCO has a poorly specified centre frequency and can operate over a wide frequency range. Additionally, the PLL may false lock to a sideband of the input signal. Or even to an unwanted signal if the signal is buried in noise and other signals.

- The effects of VCO phase noise can cause significant errors in the tracking of the input signal. This problem is especially serious when a very narrow bandwidth PLL is required and/or low quality VCOs are employed.

Previous Work - Acquisition. Much work has been done in developing techniques to aid acquisition and prevent false lock in PLLs. Some of the techniques employed to aid acquisition include:

- Sweeping of the VCO [6].

- Switching of loop filter in tracking and acquisition modes [24].
- Injection of the input signal into the VCO [25].
- Addition of a non-linearity in the loop filter [26].
- Use of combined phase and frequency detectors, either as separate devices [27] or as a single device with both phase and frequency discrimination characteristics [28], [29], [30].
- Use of multiple phase detectors [31].
- Accurate initial VCO frequency and limited tuning range by use of a voltage controlled crystal oscillator.

In many applications it is difficult to apply the above techniques due to one or more of the following reasons: Input signal deeply buried in noise and other signals. Missing signal transitions for example in clock recovery. High cost, and low level of integration.

In the field of clock recovery for baseband digital data transmission, a number of techniques have been reported to obtain accurate initial VCO tuning to aid acquisition, without having to resort to expensive voltage controlled crystal oscillators. These techniques include:

- The use of high speed digital PLLs using novel methods to generate the very high speed clocks and to process the phase information [32].
- A Master/Slave dual loop architecture employing highly matched VCOs [33].
- Switching the VCO between a crystal controlled "training" loop and the input signal at start-up and when false locking is detected [34], [35].

All the above techniques employ a fixed frequency crystal oscillator to either obtain a very high speed clock for use in a digital PLL. Or to influence the tuning of the VCO. These techniques may suffice for clock recovery, but for more demanding applications

where the signal is deeply buried in noise they may not be adequate. Furthermore, detailed mathematical models of their operation have not been developed.

Previous Work - Phase Noise. The problem of VCO phase noise in PLLs has not received much attention. The compromise between increasing the PLL bandwidth to reduce the effects of VCO phase noise, and reducing the PLL bandwidth to obtain the required filtering of the signal has been studied [36]. For the application of frequency synthesis a type of frequency feedback employing delay line frequency discriminators [18] has been used to reduce VCO phase noise. However only VCO phase noise outside the main PLL bandwidth [37]. But, no general solutions to the problem of VCO phase noise appear to have been proposed.

Hence very narrow bandwidth PLLs can be difficult and costly to realise as they require very low phase noise VCOs. Certainly, VCOs with poor phase noise (such as integrated circuit relaxation oscillators) can not be used in narrow bandwidth applications.

In many communications systems the frequencies at which data is transmitted are specified with tight tolerances. Typically, in the order of several or several tens of parts per million (ppm) [38], [39]. Some communication systems have even tighter tolerances [21]. In the application of clock recovery, the bandwidth of the PLL used would typically be in the order of a thousand ppm of the transmission frequency [38].

The Steered Frequency Phase Locked Loop. A new phase tracking system is presented, the Steered Frequency Phase Locked Loop (SFPLL) (patent pending). The SFPLL presented in this chapter is a system that will phase lock to an input signal as in a conventional PLL. But the SFPLL overcomes many of the problems associated with PLLs. The SFPLL technique allows the PLL used in the receiver component of the communication system to be centred at the appropriate frequency, with the same accuracy and stability associated with the transmission component. Exploiting the fact that the transmission frequency is often very accurately specified, the PLL can be centred very close and within the PLL bandwidth, to the transmission frequency. This close initial tuning of the PLL avoids sideband lock and achieves fast frequency acquisition.

Like conventional PLLs the SFPLL takes an input signal which it is required to phase lock to. In addition to this input signal, the SFPLL has an accurate reference frequency input of frequency ω_r. The reference frequency ω_r is chosen to be close to (though not necessarily the same as) the frequency of the input signal which the SFPLL is required to phase lock to. The SFPLL does not require any monitoring nor any switching of the frequency reference signal which is always acting.

The key advantages of the SFPLL are:

- the output frequency is ω_r (or is close to ω_r) when no input signal is present.
- The range of frequencies to which the SFPLL can lock can be confined to a small and controllable region around ω_r.
- For a particular class of SFPLLs, the effects of VCO phase noise can be reduced to an insignificant amount. And the SFPLL bandwidth made less dependent on component parameters.
- The SFPLL can be realized in simple digital integrated circuit technology. Allowing low cost miniaturized realizations, and also extremely precise and controllable positioning of the frequency the SFPLL is centred on.

3.1.1. Outline of Chapter 3

This chapter is organised as follows:

In Section 3.2 the structure of the SFPLL is described and a small signal linear model for the SFPLL is analyzed. Some general properties of SFPLLs are obtained, and some extensions to the basic SFPLL are mentioned.

In Section 3.3 further properties of an important class of SFPLL are obtained. In particular, the performance of the SFPLL when the input signal is corrupted with additive white Gaussian noise. It is shown that the SFPLL has a mathematical model which is equivalent to certain types of PLLs. This model equivalence allows the non-linear noise theory developed for PLLs to be applied to SFPLLs.

In Section 3.4 the frequency and step response characteristics of an important type of SFPLL are investigated. It is shown that undesirable peaking and overshoot in the frequency and step responses can be eliminated.

The effects of VCO phase noise in the SFPLL are then studied in Section 3.5. It is shown that in theory the SFPLL can reduce the effects of VCO phase noise to an insignificant amount.

In Section 3.6 simulations are performed to verify that the SFPLL and PLL models are equivalent. Furthermore, that the SFPLL performance with the input signal corrupted by noise is predicted well using established techniques.

A digital implementation of the SFPLL is outlined in Section 3.7. Then in Section 3.8 experimental results from a prototype of the SFPLL implementation are presented.

Finally Section 3.9 summarizes the chapter.

Note that some details relating to the non-linear behaviour of the SFPLL in noise, are given in Appendix B.

3.1.2. Contributions of Chapter 3

The introduction of the third signal source ω_r, independent from the input signal and the VCO signal, into a phase locking system has not been dealt with in the literature. The use of frequency feedback in PLLs using delay line discriminators has been considered in [37]. It was used to reduce VCO phase noise outside the main PLL bandwidth and noise generated by digital phase detectors, for frequency synthesis applications. In contrast, in the SFPLL frequency feedback is not employed merely as an addition to alleviate some problems, but instead dominates the SFPLL behaviour.

The contributions of this chapter are as follows:

- The proposal of the SFPLL which diminishes or overcomes the following problems inherent in PLLs: Reliable frequency acquisition, accurate free run frequency, locking to unwanted signals or sidebands, bandwidth change due to component variations, and VCO phase noise.

- The development of models to quantitatively describe the behaviour of the SFPLL and the verification of these models through simulations and experiments.
- The proposal of a digital implementation of the SFPLL which provides a high precision low cost realization of the SFPLL.

3.2. THE SFPLL AND ITS LINEAR MODEL

3.2.1. Analysis of SFPLL

The structure of the SFPLL is shown in Figure 3-1. In Figure 3-1 the Phase Detector, Frequency Detector, and VCO have the gains K_{pd}, K_{fd} and K_o respectively. K_p and K_f is additional gain. $F_p(s)$, $F_f(s)$ are filters which do not have poles at the origin. $F_c(s)$ is a filter which may have one pole at the origin or may have no poles at the origin. Note that the phase detector detects only phase difference and doesn't perform any frequency discrimination.

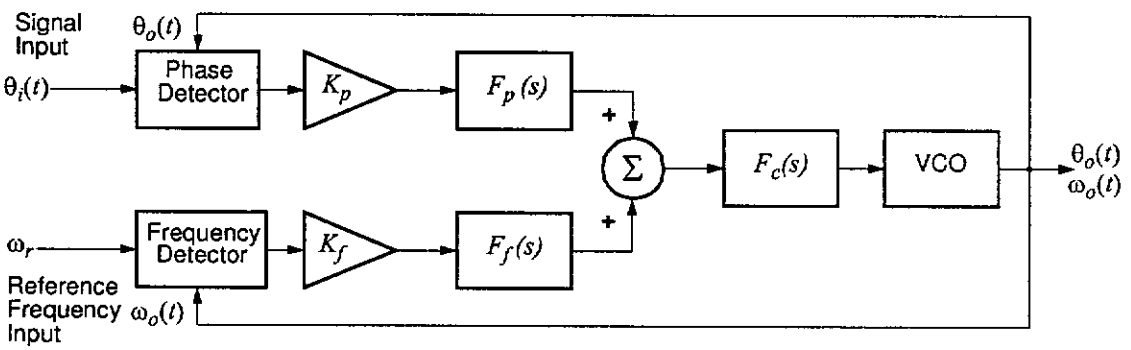

Figure 3-1. The Steered Frequency Phase Locked Loop (SFPLL). The SFPLL can be thought of as two parts in competition against each other: a phase loop and a frequency loop. Each loop fights for control of the VCO.

The SFPLL can be thought of as two parts in competition against each other: a phase loop and a frequency loop. The frequency loop acts to force the VCO to be equal to the reference frequency. The phase loop acts to force the VCO to be equal to the frequency of the signal input. For a controllable range of input signal frequencies the phase loop is

able to phase lock to the input signal. The phase loop uses a static phase error to counteract the effects of the frequency loop.

Note that the phase variables $\theta_i(t)$, $\theta_o(t)$ describe the instantaneous angle of the signal. For example if the input signal is of constant frequency ω and initial phase θ_{i0}:

$$\theta_i(t) = \omega t + \theta_{i0} \tag{3-1}$$

When the SFPLL is in the steady state and is locked to the signal input it can be represented by the small signal linear model shown in Figure 3-2.

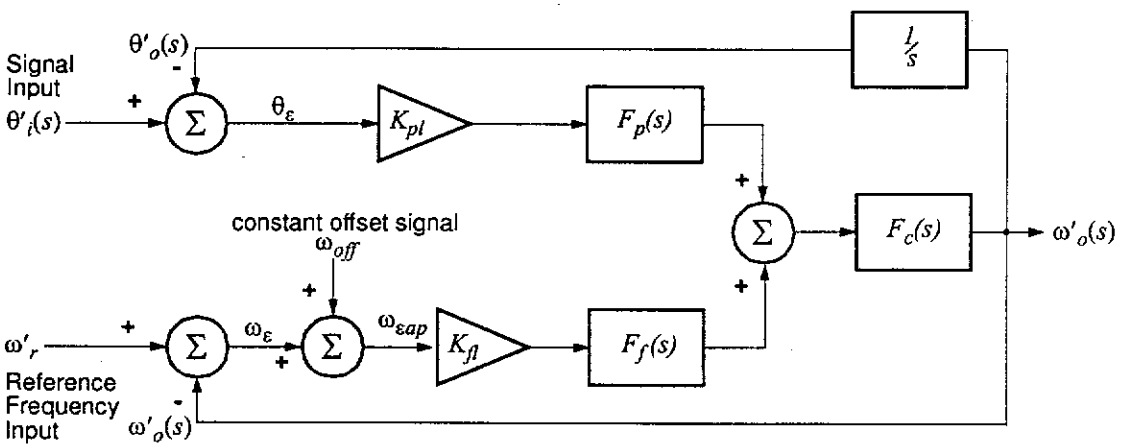

Figure 3-2. Small signal linear model for the SFPLL with reference frequency offset

With reference to Figure 3-2, the new variables ω'_r, and $\theta'_i(t)$ are defined as offsets from the free running frequency of the VCO ω_f:

$$\theta'_i(t) = \theta_i(t) - \omega_f t \tag{3-2}$$

$$\omega'_r = \omega_r - \omega_f \tag{3-3}$$

$\omega'_o(t)$ and $\theta'_o(t)$ are similarly defined as offsets from ω_f. K_{pl} accounts for all the gains in the phase loop, and K_{fl} for all the gains in the frequency loop.

$$K_{pl} = K_{pd} K_p K_o \tag{3-4}$$

$$K_{fl} = K_{fd}K_fK_o \tag{3-5}$$

The output of the SFPLL can be determined for the case when the phase detector output $\theta_\varepsilon(s)$ equals 0. For certain phase detectors, particularly in the field of clock recovery [28], the output $\theta_\varepsilon(s)$ equals 0 when there is no input signal present. The SFPLL output when $\theta_\varepsilon(s)$ equals 0 can be written as

$$\omega'_o(s) = \frac{K_{fl}F_f(s)F_c(s)}{1 + K_{fl}F_f(s)F_c(s)}(\omega'_r(s) + \omega_{off}(s)) \tag{3-6}$$

A constant offset signal ω_{off} has been added into the frequency loop of the SFPLL. The introduction of an offset in the frequency loop may be intentional or it may be due to undesirable offsets occurring in the frequency loop components. In the initial discussion of the small signal linear model the signal ω_{off} should be assumed to be zero.

When ω'_r is a constant reference frequency, the steady state value of $\omega'_o(t)$ can be found using the final value theorem. For the case where $F_c(s)$ does not contain a pole at the origin

$$\lim_{t\to\infty} \omega'_o(t) = \frac{K_{fl}}{1 + K_{fl}}(\omega'_r + \omega_{off}) \tag{3-7}$$

For the case where $F_c(s)$ does contain a pole at the origin

$$\lim_{t\to\infty} \omega'_o(t) = \omega'_r + \omega_{off} \tag{3-8}$$

Hence when the phase detector output $\theta_\varepsilon(s)$ equals 0 the SFPLL tracks the reference frequency, as shown by (3-7) and (3-8).

Now consider when the input signal is present and the phase detector output $\theta_\varepsilon(s)$ does not equal 0. The phase error $\theta_\varepsilon(s)$ as a function of $\theta'_i(s)$ is

$$\theta_\varepsilon(s) = \frac{s(1 + K_{fl}F_f(s)F_c(s))\theta'_i(s) - K_{fl}F_f(s)F_c(s)\dfrac{(\omega'_r + \omega_{off})}{s}}{s(1 + K_{fl}F_f(s)F_c(s)) + K_{pl}F_p(s)F_c(s)} \tag{3-9}$$

If the input signal is a signal of constant frequency ω'. Then for the case where $F_c(s)$ doesn't contain a pole at the origin, the steady state phase error θ_ε is

$$\lim_{t\to\infty}\theta_\varepsilon(t) = \frac{(1+K_{fl})\omega' - K_{fl}(\omega'_r + \omega_{off})}{K_{pl}} \tag{3-10}$$

If the assumption is made that

$$K_{fl} \gg 1 \tag{3-11}$$

then

$$\lim_{t\to\infty}\theta_\varepsilon(t) \approx \frac{K_{fl}}{K_{pl}}(\omega' - (\omega'_r + \omega_{off})) \tag{3-12}$$

For the case where $F_c(s)$ does contain a pole at the origin assumption (3-11) is not required and, the steady state phase error θ_ε is

$$\lim_{t\to\infty}\theta_\varepsilon(t) = \frac{K_{fl}}{K_{pl}}(\omega' - (\omega'_r + \omega_{off})) \tag{3-13}$$

Equations (3-12) and (3-13) can be interpreted as follows. For the SFPLL to lock to an incoming frequency of ω' the phase loop has to provide the appropriate phase lag/lead (θ_ε) to overcome the ω'_r 'pulling'.

Note that the maximum absolute value of $\theta_\varepsilon(t)$ is finite, with maximum value $\theta_{\varepsilon max}$

$$|\theta_\varepsilon(t)| \le \theta_{\varepsilon max} \tag{3-14}$$

Normally $\theta_{\varepsilon max}$ is at most 2π and depending on the particular phase detector $\theta_{\varepsilon max}$ may be less. From (3-13) and (3-14)

$$|\omega' - (\omega'_r + \omega_{off})| \le \theta_{\varepsilon max}\frac{K_{pl}}{K_{fl}} \tag{3-15}$$

From (3-15) it can be seen that due to the finite phase error, the allowable input frequencies to which the SFPLL will lock is restricted to a range of frequencies near ω'_r. The extent of the range is determined by the ratio of K_{pl} and K_{fl}.

The frequency loop components of the SFPLL ensure that the output frequency is always confined to a small and controllable range close the reference frequency ω'_r. The reference frequency would normally be chosen to be equal to the nominal frequency of the signal input, ω'_i. Furthermore the range of frequencies to which the SFPLL is confined would normally be less than the bandwidth of the phase loop. To avoid sideband locking, the SFPLL may also be confined to a range of frequencies which doesn't contain sidebands. Since the pull-out frequency [6] of a type I or II PLL is approximately equal to the bandwidth of the PLL, the SFPLL will achieve phase and frequency lock without cycle slipping.

When the SFPLL has locked to the signal, the phase error due to the frequency difference between the signal and reference will be insignificant in many cases. As the frequencies in many communications systems are very accurately specified. An example: with the maximum difference between transmitter and receiver reference frequencies of 9.2 ppm [38]. The receiver clock recovery SFPLL confined to frequencies inside the bandwidth of the SFPLL (836 ppm), and a $\theta_{\varepsilon max}$ of $\pi/2$. The phase error will be only 0.017 radians. It is possible to use two SFPLLs to correct the induced phase error θ_ε, and obtain an output that is in phase with the input. Further work needs to be done on the interaction between the two SFPLLs in this configuration.

The effect of the offset ω_{off} is now discussed. From inspection of equations (3-6) and (3-9) it is clear that the effect of the constant offset signal is to offset the real reference frequency (ω'_r) to an apparent reference frequency (ω'_{rap})

$$\omega'_{rap} = \omega'_r + \omega_{off} \tag{3-16}$$

The apparent reference frequency ω'_{rap} can be arbitrarily offset from the real reference frequency. But, the precision of the offsetting depends on the precision and linearity of the frequency detector and the summer. And also any inherent offsets in the frequency loop components. This offsetting of the reference frequency is useful, as the SFPLL can

be centred on any number of arbitrary frequencies by changing the offset value ω_{off}. This offsetting technique can be successfully employed in the SFPLL implementation described in Section 3.7. The offsetting technique is successful here because digital techniques are used in the construction of the frequency loop components, thus allowing an almost arbitrary level of precision. There is some inherent offset in the frequency loop due to leakage currents in some of the analog components, which degrades the precision.

3.2.2. Phase Tracking System with VCO stabilized by Phase Locking

It is worthwhile to compare the SFPLL to a standard PLL which employs a VCO stabilized [6] by phase locking it to the reference input. For convenience call this system the Stabilized PLL (Figure 3-3).

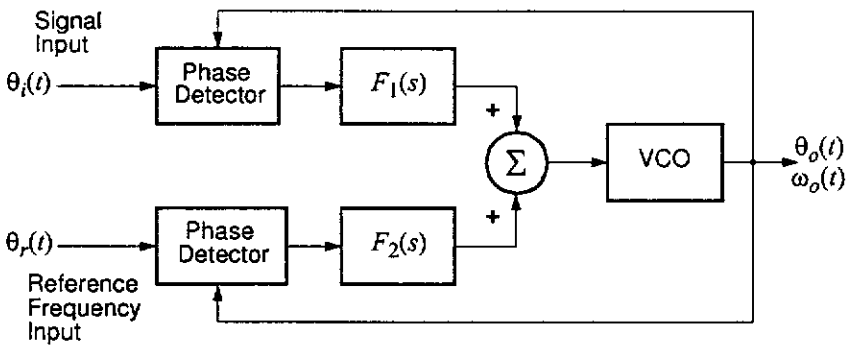

Figure 3-3. Phase Tracking System using VCO stabilized by Phase Locking. This system does not provide a useful phase tracking system, as the phase detector between the reference input and the output cannot be linearized. Whereas the SFPLL provides a useful phase tracking system.

Assuming the phase detectors can be modelled by a linear characteristic, a linear model can be found for the Stabilized PLL. With the filters $F_1(s)$, $F_2(s)$ chosen appropriately, it can be shown that the linear models of the Stabilized PLL and SFPLL can be equivalent. However, typical phase detectors have highly non-linear, periodic characteristics which can only be considered linear for a small phase error.

The phase error between the reference and output is unbounded and time varying. As there will be a frequency difference between the reference and output, when the output is locked to the signal input. It is not at all obvious that the linearization of the phase

detector between the output and the reference is valid. As there is not a fixed, bounded phase difference between the reference and output. The actual behaviour of the Stabilized PLL will most likely be complex as it is a highly non-linear system. An explanation of its behaviour is beyond the scope of this thesis.

However, the linearization of the frequency detector in the SFPLL is valid, for the following reasons:

1) There are several mechanisms which measure the frequency difference between two signals (that is, the phase slipping between the signals) and have an approximately linear characteristic over a certain range [13],[17].

2) It is safe to assume that the SFPLL frequency detector will always be operating in its linear region because:

- The linear region of the frequency detector may be greater than the signal or VCO frequency ranges.
- The action of the SFPLL maintains the VCO frequency close to the reference and hence in the linear region of the frequency detector. Irrespective of the signal input, as the frequency loop dominates the phase loop.

If at start-up the VCO frequency is outside the linear range, external systems may bring the VCO frequency into the linear range. From then on normal SFPLL operation can commence.

Hence, via frequency measurement it is possible to stabilize the VCO with the local reference, and this is what has been done in the SFPLL.

3.3. NOISE PERFORMANCE OF A CLASS OF SFPLLS

In the previous section some properties of general SFPLLs were derived. In this section further properties of an important class of SFPLLs are derived. This class of SFPLLs have the filters $F_p(s)$, $F_f(s)$ removed. Furthermore, filter $F_c(s)$ is either removed, phase loop equivalent to type I PLL, called type I SFPLL. Or $F_c(s)$ contains a pole at the origin (a perfect integrator) and a zero, phase loop equivalent to type II PLL, called type II SFPLL. That is:

$$F_p(s) = F_f(s) = 1 \tag{3-17}$$

$$F_c(s) = 1, \text{ or } \frac{s/\omega_z + 1}{s} \tag{3-18}$$

It will be shown that for these SFPLLs there is in theory a PLL whose properties are identical to the SFPLL. But, as will be seen, the physical realization of this equivalent PLL may be very costly or impossible due to the limitations of practical VCOs. Whereas, the SFPLL can achieve high performance, almost independent of the qualities of its VCO.

The type I SFPLL can be characterized by the set of four parameters ω_r, ω_f, ω_c and λ. Where ω_c is the open loop cross over frequency of the phase loop of the type I SFPLL with the frequency loop removed. The important parameter λ, which describes how small the range of frequencies to which the SFPLL can lock is compared to ω_c, is defined

$$\lambda \equiv \omega_c \frac{K_{fl}}{K_{pl}} \tag{3-19}$$

The type II SFPLL is also characterized by a set of four parameters namely, ω_r, ζ_p, ω_n and λ. Where the damping factor ζ_p and natural frequency ω_n characterize the phase loop only [6] of the SFPLL. The open loop cross over frequency of the phase loop when it is separated from the frequency loop is approximately given by [36]

$$\omega_c = 2\zeta_p\omega_n \tag{3-20}$$

By employing equation (3-20), λ for the type II SFPLL is also defined by equation (3-19). Note that when ζ_p is very small (3-20) may not be a valid approximation. Nevertheless, as used subsequently and in the definition of λ for the type II SFPLL, ω_c is defined by (3-20).

3.3.1. SFPLL with Additive Noise

The signal input is assumed to be corrupted with additive narrow-band Gaussian noise $n(t)$. In [40] it is shown that $g'(\theta_\varepsilon)$, the effective phase detector characteristic, and K_{pd} the effective phase detector gain are both dependent on the signal to noise ratio (SNR_i) at the input. As well as the noise free phase detector characteristics. $n'(t)$ is the baseband equivalent of the additive band pass noise.

Type I SFPLL. The behaviour of the type I SFPLL can be described by a non-linear stochastic differential equation, with phase error θ_ε being chosen as the state variable.

With time t normalised as follows

$$\tau = \omega_{ceff} t \tag{3-21}$$

the non-linear stochastic differential equation describing the type I SFPLL is

$$\frac{d}{d\tau}\theta_\varepsilon(\tau) = -g'(\theta_\varepsilon(\tau)) - n'(\tau) + \frac{\omega_i - \omega_{feff}}{\omega_{ceff}} \tag{3-22}$$

Where

$$\omega_{ceff} \equiv \frac{\omega_c}{1+\lambda} \tag{3-23}$$

$$\omega_{feff} \equiv \frac{\lambda}{1+\lambda}\omega_r + \frac{1}{1+\lambda}\omega_f \tag{3-24}$$

Equation (3-22) represents a first order type I PLL [41]. The first order type I PLL is characterized with an open loop cross over frequency ω_{ceff}, and an (VCO) free running frequency ω_{feff}. Hence the behaviour of a type I SFPLL is identical to that of a first

order type I PLL. Thus theory developed for the first order type I PLL can be used to predict the performance of the type I SFPLL [41],[36],[42].

Type II SFPLL. The behaviour of the type II SFPLL can be described by a set of two non-linear stochastic differential equations. With the two state variables being θ_ε, x. The state variable x is related to the state of the integrator in the filter $F_c(s)$.

Define ω_{neff}

$$\omega_{neff} \equiv \frac{\omega_n}{\sqrt{1+\lambda}} \tag{3-25}$$

The frequency represented by the state of the integrator in the filter $F_c(s)$ is given by the function $y(t)$. The dimensionless function $x(t)$ is defined as

$$x(t) \equiv \frac{y(t) + \omega_f - \omega_r}{(1+\lambda)\omega_{neff}} \tag{3-26}$$

Time t is normalised as follows

$$\tau = \omega_{neff} t \tag{3-27}$$

The non-linear stochastic differential equations describing the state variables (θ_ε, x) of the type II SFPLL are

$$\frac{d}{d\tau}\theta_\varepsilon(\tau) = \frac{-2\zeta_p g'(\theta_\varepsilon(\tau))}{\sqrt{1+\lambda}} - x(\tau) - \frac{2\zeta_p n'(\tau)}{\sqrt{1+\lambda}} + \frac{(\omega_i - \omega_r)}{\omega_{neff}} \tag{3-28}$$

$$\frac{d}{d\tau}x(\tau) = \frac{g'(\theta_\varepsilon(\tau))}{1+\lambda} + \frac{n'(\tau)}{1+\lambda} - \frac{\lambda}{2\zeta_p\sqrt{1+\lambda}}x(\tau) \tag{3-29}$$

Equations (3-28) and (3-29) represent a second order type I PLL which has an imperfect or lossy integrator in its loop filter. It is still classed as a type I PLL as there is only one pole at the origin. For the imperfect integrator PLL the transfer function of the filter has the form (from [36])

$$F_c(s) = \frac{1+sT_2}{1+sT_1} \tag{3-30}$$

The following loop parameters for the imperfect integrator PLL (from [36]) are

$$\omega_{nl} = \sqrt{\frac{KA}{T_1}} \tag{3-31}$$

$$\zeta_l = \frac{T_2}{2}\sqrt{\frac{KA}{T_1}}\left(1+\frac{1}{KAT_2}\right) \tag{3-32}$$

$$\beta = \frac{1}{\omega_{nl}T_1} \tag{3-33}$$

Where KA is the product of all the gains in the PLL and the input signal amplitude. With the time and state variable $y_l(t)$ normalized as follows

$$\tau_l = \omega_{nl}t \tag{3-34}$$

$$x_l(t) = \frac{y_l(t)}{\omega_{nl}} \tag{3-35}$$

The imperfect integrator PLL is described by the following non-linear stochastic differential equations (adapted from [36]).

$$\frac{d}{d\tau_l}\theta_\varepsilon(\tau_l) = -(2\zeta_l-\beta)g'(\theta_\varepsilon(\tau_l)) - x_l(\tau_l) - (2\zeta_l-\beta)n'(\tau_l) + \frac{(\omega_i-\omega_{fl})}{\omega_{nl}} \tag{3-36}$$

$$\frac{d}{d\tau_l}x_l(\tau_l) = (1-2\zeta_l\beta+\beta^2)g'(\theta_\varepsilon(\tau_l)) + (1-2\zeta_l\beta+\beta^2)n'(\tau_l) - \beta x_l(\tau_l) \tag{3-37}$$

Where ω_{fl} is the imperfect integrator PLL VCO free run frequency. From a comparison of (3-28) and (3-29) to (3-36) and (3-37) it can be seen that they are of the same form with,

$$\tau = \tau_l \tag{3-38}$$

$$x = x_l \tag{3-39}$$

$$\zeta_l = \frac{4\zeta_p^2 + \lambda}{4\zeta_p\sqrt{1+\lambda}} \tag{3-40}$$

$$\beta = \frac{\lambda}{2\zeta_p\sqrt{1+\lambda}} \tag{3-41}$$

$$\frac{(\omega_i - \omega_r)}{\omega_{neff}} = \frac{(\omega_i - \omega_{fl})}{\omega_{nl}} \tag{3-42}$$

Hence for any type II SFPLL, an imperfect integrator PLL described by identical non-linear differential equations can be constructed. Note that due to state variable $y(t)$ scaling differences (3-26), (3-35), the frequency of signals in the PLL (such as input, VCO free run, output) have to be scaled down by a factor $1+\lambda$. Alternatively, the state variable (θ_ε, x_l) response of the PLL has to be observed with a time scale slowed down by the factor $1+\lambda$, to match the SFPLL. Thus theory developed for the imperfect integrator PLL can be used to predict the performance of the type II SFPLL [36],[43].

Note that if only the phase error state variable response is of importance, then there exists an imperfect integrator PLL whose phase error corresponds to that of the SFPLL. Where the response of the PLL does not have to be observed in a scaled time system. For this imperfect integrator PLL β and ζ_l are as in (3-40) and (3-41), but ω_{nl} and ω_{fl} are as follows

$$\omega_{nl} = \omega_{neff} \tag{3-43}$$

$$\omega_{fl} = \omega_r \tag{3-44}$$

3.4. TYPE II SFPLL TRANSFER AND STEP RESPONSE CHARACTERISTICS

The type II SFPLL is the SFPLL of greatest practical importance. It was just shown that the phase response of the type II SFPLL is identical to the phase response of an imperfect integrator PLL. The type II SFPLL was described by four parameters ζ_p, λ, ω_n, and ω_r. The imperfect integrator PLL was also described by four parameters ζ_l, β, ω_{nl}, and ω_{fl}.

When the SFPLL is used to perform some function in a system, some design parameters will have to be met. For PLLs the design parameters normally specify characteristics of the PLL frequency response. The design parameters may also specify characteristics of the PLL transient response. Most common is the transient response to a phase step, with rise time and overshoot being specified.

The frequency and transient response of the linear model of the imperfect integrator PLL has been studied [36],[4]. However, only for imperfect integrator PLLs with the parameter β small (i.e. small imperfection/loss in the integrator). The imperfect integrator PLL with a phase response identical to the SFPLL can have the parameter β large.

It is worthwhile to study the frequency (Section 3.4.1) and transient (Section 3.4.2) response of the imperfect integrator PLL with a phase response identical to the SFPLL. That is imperfect integrator PLLs with ζ_l and β described by equations (3-40), (3-41). It will be shown that the type II SFPLL has some remarkable and useful properties. In particular peaking and overshoot can be eliminated when ζ_p is sufficiently small.

The key characteristics of the frequency and transient response such as peaking and overshoot are solely determined by the parameters ζ_l and β. Typically, to meet design requirements a range of values for ζ_l and β will be found. This range of values will then in turn specify via (3-40) (3-41) a range of values for ζ_p and λ.

The use of the imperfect integrator PLL as an intermediate step in determining the SFPLL parameters has the following benefits: The important characteristics are concisely expressed in terms of ζ_l and β. Furthermore when β is small there is considerable similarity between the imperfect integrator PLL and the familiar type II PLL behaviour. However, many of the conditions derived are also given in terms of ζ_p,

λ, and graphs illustrating the behaviour of key characteristics are labelled in terms of ζ_p, λ.

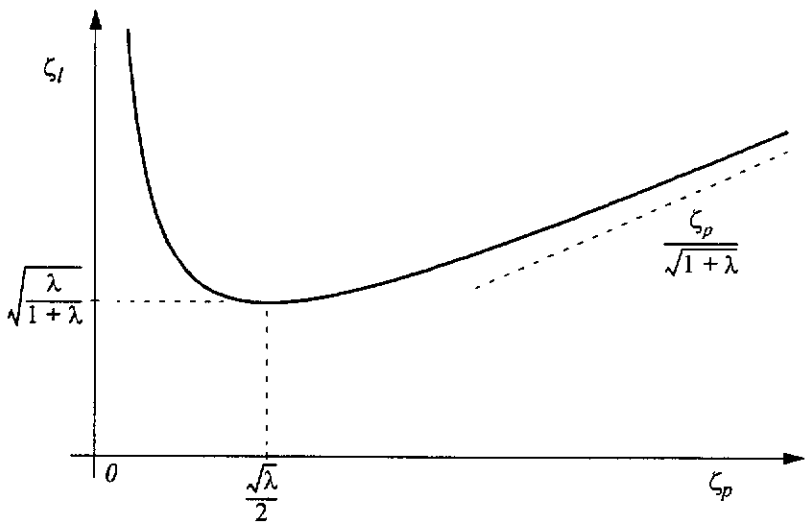

Figure 3-4. Behaviour of ζ_l as a function of ζ_p with λ as a parameter. Notice that small phase loop damping ζ_p actually results in a high system damping ζ_l.

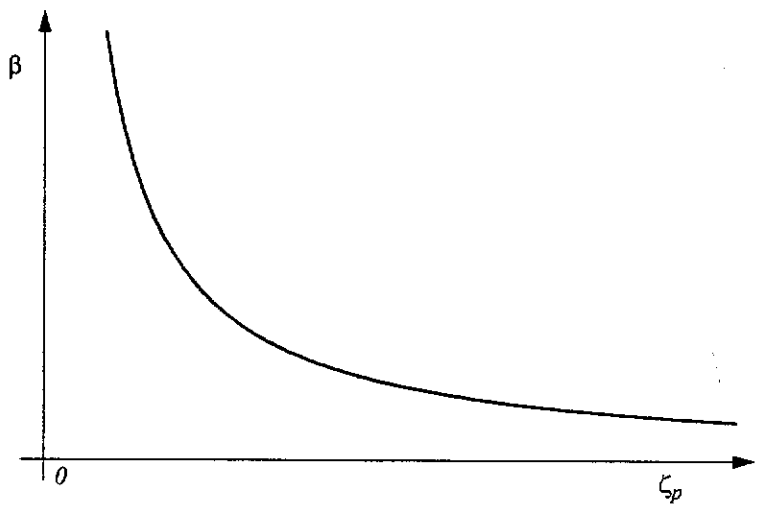

Figure 3-5. Behaviour of β as a function of ζ_p with λ as a parameter.

Firstly, the behaviour of ζ_l and β as functions of ζ_p with λ as a parameter is examined. A graph of ζ_l (3-40) is shown in Figure 3-4. Note that the graph has a minimum and equals β, for ζ_p equal to $\sqrt{\lambda}/2$. Also, for large ζ_p, the graph is asymptotic with the line $\zeta_p/\sqrt{1+\lambda}$.

From Figure 3-4 it can be seen that a small phase loop damping ζ_p actually results in a high system damping ζ_l. For completeness the graph of β (3-41) is shown in Figure 3-5.

3.4.1. Transfer Function Characteristics

Open and Closed Loop Response. From (3-30), (3-31), (3-32), (3-33), the open loop transfer function $G(s)$ of the imperfect integrator PLL can be found to be

$$G(s) = \frac{(2\zeta_l - \beta)\frac{s}{\omega_{nl}} + 1}{\frac{s}{\omega_{nl}}\left(\frac{s}{\omega_{nl}} + \beta\right)} \tag{3-45}$$

The magnitude of $G(s)$ is found to be

$$|G(j\omega)| = \frac{1}{\omega/\omega_{nl}}\sqrt{\frac{1 + (\omega/\omega_{nl})^2(2\zeta_l - \beta)^2}{\beta^2 + (\omega/\omega_{nl})^2}} \tag{3-46}$$

The asymptotic approximation to the Bode diagram of the open loop transfer function is depicted in Figure 3-6. From (3-45) and Figure 3-6 it can be seen that there is a pole at $\omega_{nl}\beta$ and a zero at $\omega_{nl}/(2\zeta_l - \beta)$. The ratio of the pole and zero frequencies can be found using (3-40) and (3-41)

$$\frac{\beta}{\frac{1}{2\zeta_l - \beta}} = \frac{\lambda}{1 + \lambda} \tag{3-47}$$

From (3-47) it can be seen that the ratio of the pole and zero frequencies will always be less than one. Hence the pole will always occur before the zero. Furthermore, as λ becomes large, the pole and zero frequencies converge, and the open loop transfer function $G(s)$ approaches that of a first order type I PLL (3-48).

$$\lim_{\lambda \to \infty} G(s) \propto \frac{1}{s} \tag{3-48}$$

Hence as λ tends to infinity, the characteristics of the imperfect integrator PLL become increasingly like the characteristics of a first order type I PLL.

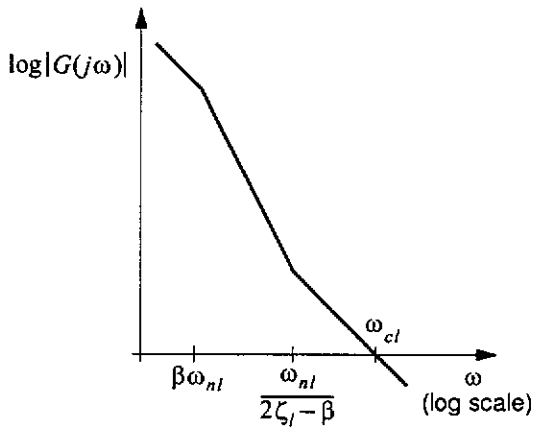

Figure 3-6. Bode diagram of open loop transfer function for imperfect integrator PLL. Note with β and ζ_l determined by (3-40), (3-41) the open loop cross over ω_{cl} may also occur in the region to the left of the pole $\omega_{nl}\,\beta$. Or in the region between the pole and zero.

The closed loop transfer function $H(s)$ of the imperfect integrator PLL can be found to be

$$H(s) = \frac{G(s)}{1+G(s)} = \frac{(2\zeta_l-\beta)\frac{s}{\omega_{nl}}+1}{\left(\frac{s}{\omega_{nl}}\right)^2+2\zeta_l\frac{s}{\omega_{nl}}+1} \tag{3-49}$$

The magnitude of $H(s)$ is

$$|H(j\omega)| = \sqrt{\frac{1+(\omega/\omega_{nl})^2(2\zeta_l-\beta)^2}{(1-(\omega/\omega_{nl})^2)^2+4\zeta_l^2(\omega/\omega_{nl})^2}} \tag{3-50}$$

In Figure 3-7 the frequency response of $H(s)$ is plotted for various λ and a fixed ζ_p. As can be seen, a key effect of increasing λ is to reduce the peaking in the closed loop frequency response.

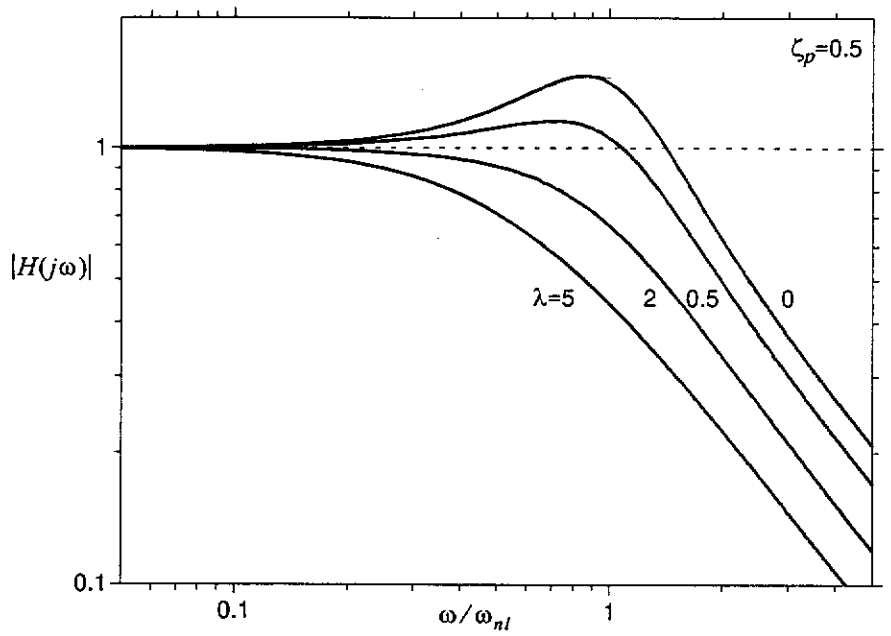

Figure 3-7. Closed loop frequency response for various λ and fixed ζ_p. A key effect of increasing λ is to reduce the peaking in the closed loop frequency response.

Bandwidth Measures. Typically, the most important design parameters concerned with the transfer function of the lossy integrator PLL will be; The peak value of the closed loop frequency response, and some form of bandwidth measure. The appropriate bandwidth measurement may be the 3dB bandwidth of the closed loop frequency response ω_{3db}. Or the actual ω_{ca} or asymptotic approximation ω_{cl} of the unity gain (cross over) frequency of the open loop transfer function. For example, when designing a PLL system for clock recovery, the appropriate jitter transfer mask must be taken into consideration [38]. In this case, the critical parameters are the peak value M_p of the closed loop frequency response and ω_{cl}.

The asymptotic approximation to the open loop cross over frequency is given by [36]

$$\omega_{cl} = (2\zeta_l - \beta)\omega_{nl} \tag{3-51}$$

The above approximation is valid when the open loop cross over occurs to the right of the zero $\omega_{nl}/(2\zeta_l - \beta)$ as shown in Figure 3-6. Cross over to the right of the zero occurs provided condition (3-52) is met. Condition (3-52) can be expressed in terms of ζ_p and λ (3-53)

$$1 < 2\zeta_l - \beta \tag{3-52}$$

$$\frac{\sqrt{1+\lambda}}{2} < \zeta_p \tag{3-53}$$

However, with β and ζ_l determined by (3-40), (3-41) the open loop cross over may also occur in the region to the left of the pole $\omega_{nl}\beta$. Or in the region between the pole and zero.

For cross over to occur between the pole and zero requires that the condition (3-54) is satisfied. Condition (3-54) can be expressed in terms of ζ_p and λ (3-55), and ω_{cl} is given by (3-56).

$$2\zeta_l - 1 < \beta < 1 \tag{3-54}$$

$$\frac{\lambda}{2\sqrt{1+\lambda}} < \zeta_p < \frac{\sqrt{1+\lambda}}{2} \tag{3-55}$$

$$\omega_{cl} = \omega_{nl} \tag{3-56}$$

For cross over to occur to the left of the pole requires that the condition (3-57) is satisfied. Condition (3-57) can be expressed in terms of ζ_p and λ (3-58), and ω_{cl} is given by (3-59).

$$\beta > 1 \tag{3-57}$$

$$\zeta_p < \frac{\lambda}{2\sqrt{1+\lambda}} \tag{3-58}$$

$$\omega_{cl} = \frac{\omega_{nl}}{\beta} = \frac{\lambda}{1+\lambda}(2\zeta_l - \beta)\omega_{nl} \tag{3-59}$$

From (3-46) the actual open loop cross over frequency is found to be

$$\omega_{ca} = \omega_{nl}\sqrt{2\zeta_l(\zeta_l - \beta) + \sqrt{1 + (2\zeta_l(\zeta_l - \beta))^2}} \tag{3-60}$$

From (3-50) the 3dB bandwidth is found to be

$$\omega_{3db} = \omega_{nl}\sqrt{1+2\zeta_l^2+\beta^2-4\zeta_l\beta+\sqrt{1+(1+2\zeta_l^2+\beta^2-4\zeta_l\beta)^2}} \tag{3-61}$$

Peaking. The peak value of the closed loop frequency response M_p will now be examined. From examination of the first and second derivatives of $|H(j\omega)|$ (3-50) it can be shown that if the condition (3-62) is satisfied. Then $|H(j\omega)|$ will be greater than one for some ω and hence 'peaking' will occur. If condition (3-62) is not satisfied then $|H(j\omega)|$ will be a monotonically decreasing function of ω. Furthermore $|H(j\omega)|$ will be less than one for all ω greater than zero, that is no 'peaking' will occur.

$$\zeta_l < \frac{\beta}{4}+\frac{1}{2\beta} \tag{3-62}$$

Employing (3-40) and (3-41) the condition (3-62) can be expressed in terms of ζ_p and λ.

$$\zeta_p > \frac{\lambda}{2\sqrt{2}} \tag{3-63}$$

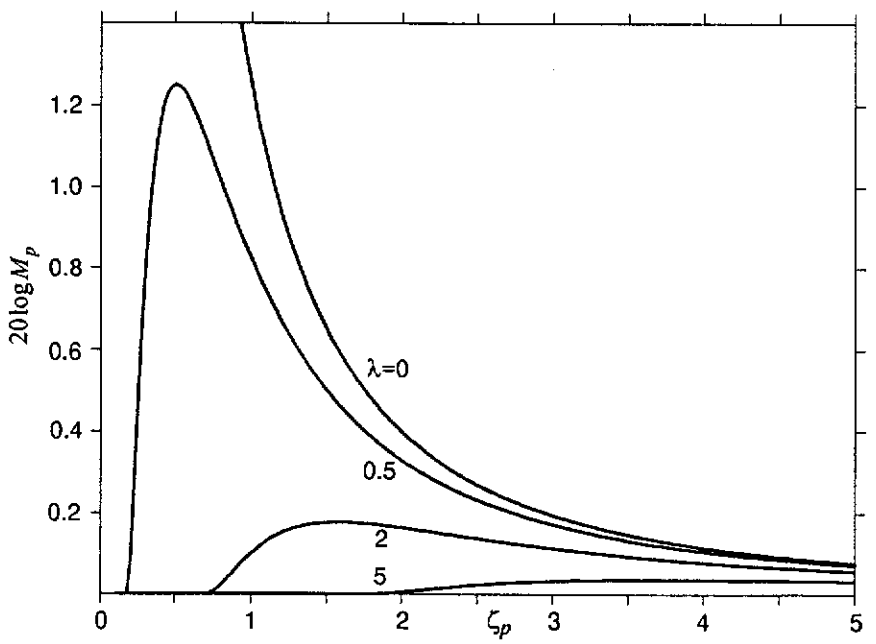

Figure 3-8. Peaking as a function of ζ_p for various λ. This figure shows that peaking is eliminated when ζ_p is below a critical value dependent on λ (3-63).

Hence for peaking to occur ζ_p and λ must satisfy (3-63). The peak value M_p as a function of ζ_p is plotted in Figure 3-8 for various λ.

Note that bandwidth (ω_{3db}, ω_{ca} or ω_{cl}) can be set independently of the peaking or overshoot characteristics by adjusting the SFPLL parameter ω_n , which affects ω_{nl} (3-25), (3-43).

3.4.2. Step Response Characteristics

The PLL system may also be specified in terms of the transient response characteristics, instead of the frequency response. A common practice is to specify the peak value of the time response to a unit step input. This peak value (called overshoot) will be determined for the imperfect integrator PLL in this section.

The phase error θ_ε transfer function for the imperfect integrator PLL can be found to be

$$\frac{\theta_\varepsilon(s)}{\theta_i'(s)} = \frac{s^2 + \omega_{nl}\beta s}{s^2 + 2\zeta_l s + \omega_{nl}^2} \tag{3-64}$$

and the response to a unit step input is

$$\theta_\varepsilon(s) = \frac{s + \omega_{nl}\beta}{s^2 + 2\zeta_l s + \omega_{nl}^2} \tag{3-65}$$

The corresponding time domain response is

$$\theta_\varepsilon(t) = e^{-\zeta_l \omega_{nl} t}\left[\cos\omega_{nl}t\sqrt{1-\zeta_l^2} - \frac{\zeta_l - \beta}{\sqrt{1-\zeta_l^2}}\sin\omega_{nl}t\sqrt{1-\zeta_l^2}\right] \tag{3-66}$$

The peak output signal is found by first finding the time at which the error signal is at a minimum t_p. t_p is determined by setting the first derivative of (3-66) equal to zero.

$$t_p = \frac{1}{\omega_{nl}\sqrt{1-\zeta_l^2}}\operatorname{atan}\left(\frac{(2\zeta_l - \beta)\sqrt{1-\zeta_l^2}}{2\zeta_l^2 - 1 - \zeta_l\beta}\right) \tag{3-67}$$

The corresponding peak value P_o in the output $\theta'_o(t)$ is

$$P_o = 1 - \exp\left(\frac{-\zeta_l}{\sqrt{1-\zeta_l^2}} t_p'\right)\left[\cos t_p' - \frac{\zeta_l - \beta}{\sqrt{1-\zeta_l^2}} \sin t_p'\right] \tag{3-68}$$

With t_p' defined

$$t_p' = t_p \omega_{nl} \sqrt{1-\zeta_l^2} = \operatorname{atan}\left(\frac{(2\zeta_l - \beta)\sqrt{1-\zeta_l^2}}{2\zeta_l^2 - 1 - \zeta_l \beta}\right) \tag{3-69}$$

It can be shown that if the either of the two conditions (3-70), (3-71), are satisfied then overshoot will occur. That is $\theta'_o(t)$ attains a maximum P_o greater than one. If (3-70) and (3-71) are not satisfied, then overshoot will not occur, that is $\theta'_o(t)$ never exceeds one.

$$\zeta_l < 1 \tag{3-70}$$

$$\beta < \zeta_l - \sqrt{\zeta_l^2 - 1} \tag{3-71}$$

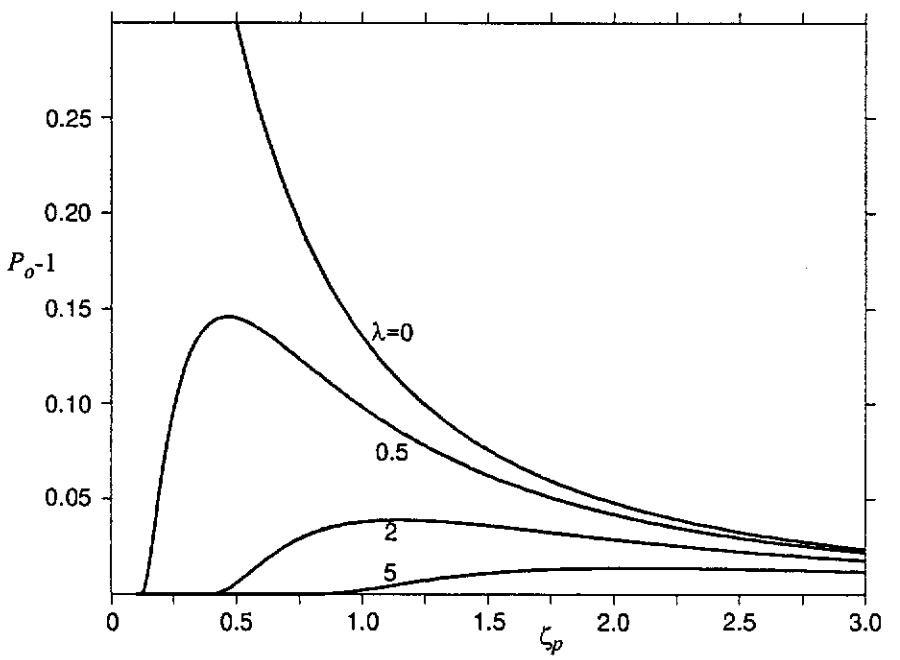

Figure 3-9. Overshoot of step response as a function of ζ_p for various λ. This figure shows that overshoot is eliminated when ζ_p is below a critical value dependent on λ (3-72).

Employing (3-40), (3-41), (3-70) and (3-71) it can be shown that if the condition (3-72) is satisfied then overshoot will not occur.

$$\zeta_p < \frac{\sqrt{1+\lambda}-1}{2} \tag{3-72}$$

The peak overshoot (P_o-1) as a function ζ_p is plotted in Figure 3-9 for various λ.

3.5. EFFECTS OF VCO PHASE NOISE AND PARAMETER VARIATIONS

3.5.1. Effects of Parameter Variations on Bandwidth

The bandwidth of the type I SFPLL was shown to be ω_{ceff}(3-23).

The approximate open loop cross over frequency of the imperfect integrator PLL with phase response equivalent to type II SFPLL was found in Section 3.4. Several expressions for the cross over frequency were found (3-51), (3-56), (3-59). However, the three expression are approximately equal when the condition (3-73) is satisfied.

$$\lambda \gg 1 \tag{3-73}$$

Thus it can be shown that when (3-73) is satisfied the bandwidth of the type II SFPLL is also approximately ω_{ceff}(3-23). As for the type I SFPLL, the bandwidth of the type II SFPLL is reduced compared to the bandwidth of the phase loop with the frequency loop removed.

With (3-73) satisfied ω_{ceff} can be made insensitive to variations in parameters such as the VCO gain K_o. Since ω_{ceff} only depends on the ratio of the phase and frequency loop gains.

$$\omega_{ceff} \approx \frac{\omega_c}{\lambda} \approx \frac{K_{pl}}{K_{fl}} \tag{3-74}$$

3.5.2. Effects of VCO Phase Noise on SFPLL Performance

The effects of VCO phase noise on the SFPLL are now considered. The VCO is modeled by a perfect VCO plus an internal disturbance source $\Psi(s)$, [36], Figure 3-10.

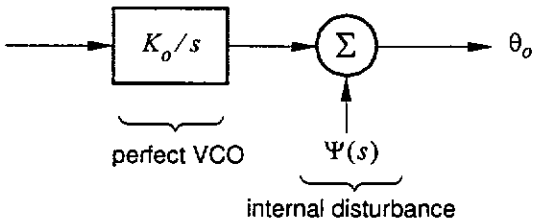

Figure 3-10. Model of VCO with phase noise

Employing a small signal linear model, the contribution of the VCO instabilities to phase error can be shown to be

$$\theta_{\varepsilon\Psi}^{SFPLL}(s) = \frac{-\Psi(s)}{1 + K_{fl}F_c(s) + \dfrac{K_{pl}F_c(s)}{s}} = \theta_{\varepsilon\Psi'}^{PLL}(s) \tag{3-75}$$

The use of a linear model is justified because the frequency loop of the SFPLL is free of non-linearities. The frequency loop acts to reduce the VCO phase noise to a small level.

For the type I SFPLL it can be shown that (3-75) represents the phase error response to VCO phase noise in a type I PLL. With the PLL bandwidth equal to ω_{ceff} and, importantly, the VCO phase noise equal to $\Psi'(s)$ (3-77). For the type II SFPLL (3-75) represents the response to phase noise in a type II PLL (note not an imperfect integrator PLL). With the PLL bandwidth equal to ω_{cfil} (3-76) and VCO phase noise equal to $\Psi'(s)$.

$$\omega_{cfil} = \omega_{ceff} + \frac{\lambda}{(1+\lambda)}\frac{\omega_n}{2\zeta_p} = \omega_{ceff}\left(1 + \frac{\lambda}{4\zeta_p^2}\right) = 2\zeta_l\omega_{neff} \tag{3-76}$$

$$\Psi'(s) = \frac{1}{1+\lambda}\Psi(s) \tag{3-77}$$

Hence the phase noise is reduced by the factor 1+λ (3-77). For the type II SFPLL, the low frequency phase noise will be further reduced due to the increased bandwidth (3-76) seen by the phase noise. Note the type II PLL with closed loop bandwidth ω_{cfil} (3-76) has a damping factor equal to ζ_l and a natural frequency equal to ω_{neff}.

Strategies for reducing VCO phase noise. VCO phase noise can be reduced by either increasing λ. Or for the type II SFPLL, by increasing ω_{cfil} through reducing ζ_p, or increasing both λ and ω_{cfil}.

The static phase for an input of constant frequency ω_i, as a function of λ can be found from (3-13), (3-19), (3-23) and (3-20)

$$\lim_{t\to\infty}\theta_\varepsilon(t) = \lambda\frac{\omega_i-\omega_r}{\omega_c} = \frac{\lambda}{1+\lambda}\frac{\omega_i-\omega_r}{\omega_{ceff}} \tag{3-78}$$

A large λ does not significantly increase the static phase error. However, a large λ may be inconvenient due to implementation issues, as discussed in Section 3.7.

As was shown in Section 3.4, a small ζ_p provides other benefits than just reducing phase noise.

In theory, provided the reference source is free of phase noise, a λ and ω_{ceff} can be independently chosen so as to achieve the desired loop bandwidth. And also reduce the phase error due to VCO phase noise to an insignificant level. For the type II SFPLL ζ_p may also be chosen to reduce the phase noise significantly.

In summary, the performance of an important class of SFPLLs has been shown to be identical to certain types of PLL. But importantly, while the VCO of the PLL needs to have an extremely accurate free run frequency and have very low phase noise. The SFPLL can achieve the same performance independent of the qualities of its VCO. It can be argued that if there is a reference signal with better accuracy and stability than any VCO. Then a SFPLL can be realised which more closely approximates an ideal imperfect integrator PLL than any physically realisable imperfect integrator PLL.

3.6. SIMULATION OF SFPLL WITH ADDITIVE NOISE

A number of simulations were performed for an SFPLL and its equivalent PLL, where the input signal was corrupted with additive white Gaussian noise. The purpose of these simulations was to verify that the SFPLL and PLL models are equivalent. Furthermore to verify that the SFPLL performance with the input signal corrupted by noise is predicted well using established techniques.

The parameters of the type II SFPLL and the equivalent imperfect integrator PLL are given in Table 3-1.

Table 3-1. SFPLL and PLL Parameters for Simulation

SFPLL & PLL Parameter	Value
ζ_p	$1/\sqrt{2}$
λ	1
ω_n	$2\pi\sqrt{50}$ 100 r/s
ω_r	$2\pi \times 10^5$ r/s
ω_i	$2\pi \times 10^5$ r/s
ζ_l	3/4
β	1/2

The SFPLL and PLL were run simultaneously, with the input signal frequencies being equal. Due to state variable $y(t)$ scaling differences (3-26), (3-35), the actual bandwidth of the PLL was twice (scaling of $1+\lambda$) that of the SFPLL. Thus the noise on the input to the SFPLL was increased to ensure the same signal to noise ratio for the PLL and SFPLL.

Table 3-2. Simulated and Predicted Phase Error Variance. Results show good agreement between simulated and predicted phase error variance.

Signal to Noise Ratio ρ		10	4	2	1
Theoretical	Linear	0.10	0.25	0.50	1.00
$\sigma^2_{\theta\varepsilon}$	Fokker-Planck	0.11	0.31	0.81	1.61
Simulated	SFPLL	0.11	0.33	0.86	1.74
$\sigma^2_{\theta\varepsilon}$	PLL	0.11	0.33	0.88	1.66

Simulations were performed for various signal to noise (ρ) ratios. Note the signal to noise ratio refers to the signal to noise ratio inside the loop, see [36] for an explanation. The phase error variance ($\sigma^2_{\theta\varepsilon}$) for each simulation run was recorded and compared to the phase error variance predicted by linear and non-linear methods, Table 3-2.

A non-linear method was employed to find the exact stationary probability density function (PDF) for θ_ε. The method involved numerically finding the eigenfunctions of the Fokker-Planck operator of the imperfect integrator PLL. For a description of the method [36] and Appendix B should be consulted. As can be seen in Table 3-2 the simulation results agree well with the predicted phase error variance. A plot of the simulated and theoretical θ_ε probability density function for the ρ=2 case is shown in Figure 3-11.

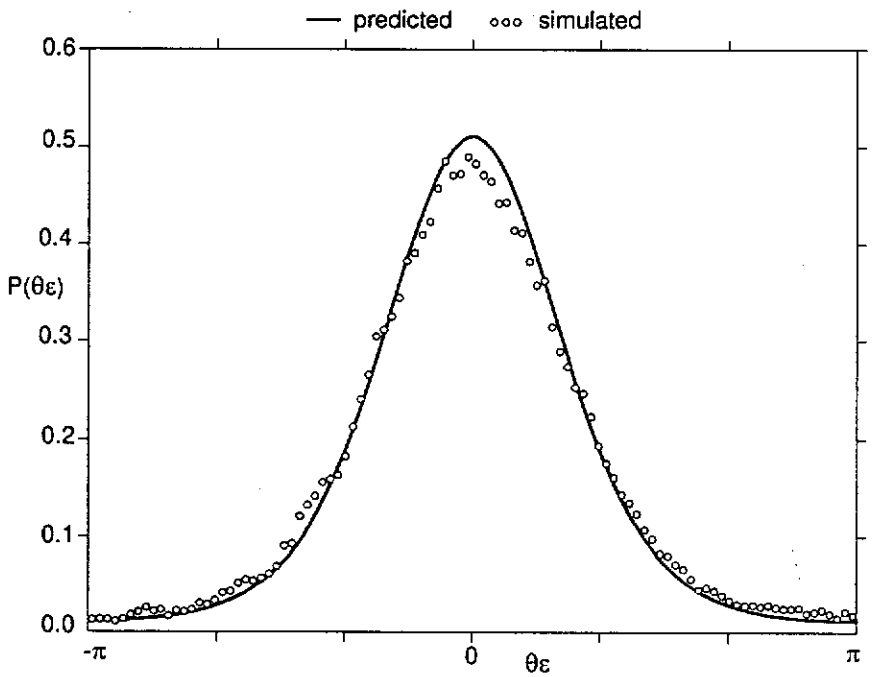

Figure 3-11. Simulated and Theoretical Probability Density Function for Phase Error (ρ=2). The good agreement between PDFs shown here, and results in Table 3-2, Table 3-3 demonstrate current PLL theory can predict SFPLL performance. Also the results verify that the SFPLL has an equivalent PLL.

The non-linear method also predicted the cycle slip rates for the imperfect integrator PLL. The theoretical slip rates and the slip rates obtained from the simulations are given in Table 3-3. Slip rates are given as normalized slip rates. (That is, number of slips per

unit of normalized time $\tau=B_L\, t$, B_L is the loop noise bandwidth[36]). For low signal to noise there is good agreement between the simulation and theoretical slip rates. For high signal to noise ratio the slip rate was so low that no slips occurred during the simulation.

The good agreement between predicted and simulated SFPLL slip rates and phase error variance, demonstrates that the SFPLL performance is predicted well using established techniques. Furthermore, the good agreement of the PLL and SFPLL simulation results verifies the equivalence of the PLL and SFPLL models.

Table 3-3. Simulated and Theoretical Normalized Cycle slip rate (N/B_L). Results show good agreement between simulated and theoretical slip rates.

Signal to Noise Ratio ρ		10	4	2	1
Theoretical N/B_L		5.6×10^{-8}	1.2×10^{-3}	3.3×10^{-2}	2.0×10^{-1}
Simulated N/B_L	PLL	0	1.2×10^{-3}	3.3×10^{-2}	1.8×10^{-1}
	SFPLL	0	0	3.2×10^{-2}	2.0×10^{-1}

3.7. DIGITAL IMPLEMENTATION

In this section an implementation of the SFPLL system is presented. The implementation demonstrates that SFPLL systems can be realized almost entirely with simple low cost digital integrated circuit technology. Realization in digital integrated circuit technology allows integration of the SFPLL with higher layer functions found in the systems in which it would be employed. Furthermore, advantage can be taken of the rapid advances in digital integrated circuit technology to improve performance.

The use of digital techniques in the frequency loop of the SFPLL allows precise and controllable positioning of the frequency the SFPLL is centred on. Especially when employing a digital frequency detector which has no frequency offsets. In particular the precise digital frequency detector (PDFD) developed in Chapter 2 will be used as the frequency detector.

A block diagram of the digital implementation is shown in Figure 3-12.

3.7.1. Filter Realization

The digital implementation is a type II SFPLL with a filter $F_c(s)$ that has a pole at the origin, that is it contains a perfect integrator. This particular SFPLL has the desirable property that the output frequency is exactly ω_r when the phase error θ_ε is zero. Depending on the particular phase detector, zero phase error occurs when no signal input is present. Also, the range of frequencies to which it can lock is centred on the reference frequency ω_r. An almost perfect integrator is realized with a capacitor in the filter and charge pumps on the outputs of the phase and frequency detectors. Charge-pump PLLs [44][45] realize an almost perfect integrator in the same way.

Imperfections in the integrator are due to leakage currents, which are very small, and the SFPLL is centred very close to the reference frequency (typically within 1 part per million). Charge-pumps are used to connect the digital circuits to the analog components: resistor R and capacitor C. The charge-pumps produce ternary current pulses of possible values +I, 0, -I amps.

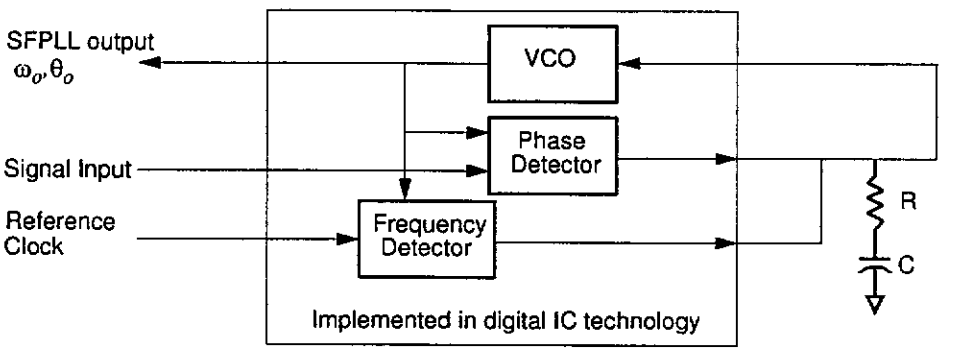

Figure 3-12. Digital Implementation of SFPLL. It is a type II SFPLL. The analog filter component which contains an almost perfect integrator is implemented with resistor R, capacitor C and charge pumps on the digital outputs.

3.7.2. Frequency Detector and Frequency Loop

Ideal Frequency Detector. The analysis is this chapter assumes an ideal frequency detector and frequency loop that have infinite bandwidth. In practice, the frequency detector and frequency loop can only approach this ideal. A practical digital frequency detector and frequency loop will depart from the ideal in the following key ways:

- *Frequency Detector Bandwidth.* In the particular digital implementation described, the signals are square waves rather than sinusoids. The phase and frequency information is contained in the zero crossings of the signal. Hence, frequency information can only be obtained at most once every cycle of the square wave, and typically many cycles are required (Chapter 2).

- *Phase Quantization.* The output of the frequency detector is quantized in some manner. For the frequency detector used in the particular digital implementation described, phase is the fundamental quantity which is quantized (Chapter 2).

- *Frequency Loop Bandwidth.* There may be some delay between the measurement of a frequency difference and the application of the response to the filter $F_c(s)$.

These departures from the ideal are dealt with in the following ways:

Phase Quantization. Phase quantization in the frequency detector leads to limit cycles in the phase of the output signal. With the limit cycle amplitude of the order of one quantization level. The phenomenon of limit cycles due to quantization in closed loop systems has been covered in the literature [46]. A recent study of this phenomenon has been presented in [47].

In the experimental SFPLLs presented in Section 3.8 and Chapter 5, the effects due to phase quantization are insignificant as the phase quantization level is very small. Typically the phase quantization is of the order of one hundreth of a cycle. However, useful free run frequency and lock range properties (Section 3.2), can still be obtained when using a simpler frequency detector, such as the rotational frequency detector [13]. The rotational frequency detector provides a very coarse measurement of frequency as the phase quantization is large. An SFPLL employing the rotational frequency detector is developed in Chapter 6.

Frequency Detector and Loop Bandwidth. Only SFPLLs with very narrow bandwidth phase loops will be considered. The narrow bandwidth allows the frequency loop components sufficient time to obtain a frequency measurement and apply the

response to the filter $F_c(s)$. Before the phase loop has moved θ_o more than one phase quantization level. Furthermore, the narrow bandwidth allows the phase loop to be treated as a continuous time system [44], as is assumed by the analysis of this chapter.

The bandwidth of the phase loop ω_c is approximately λ times the SFPLL bandwidth ω_{ceff} (3-23). Employing a large λ to reduce phase noise may result in a phase loop bandwidth which can no longer be considered very narrow. In these cases it may be more appropriate to reduce phase noise by reducing ζ_p.

3.7.3. VCO and Phase Detector

Phase Detectors and VCOs which can be realized with digital technology have been reported extensively in the literature [29],[48],[49],[50],[51].

3.8. EXPERIMENTAL SFPLL

3.8.1. SFPLL System

A SFPLL was constructed as described and shown in Section 3.7 and Figure 3-12. The SFPLL and PDFD parameters are given in Table 3-4 and Table 3-5. The phase quantization of the PDFD was 1/96 th (1/l th) of a cycle (67 picoseconds).

Table 3-4. Experimental SFPLL Parameters

SFPLL Parameter	Value
ζ_p	1.83
λ	0.1 to 8
ω_n	17191 r/s
ω_r	2π 155.52 × 10^6 r/s

Table 3-5. Parameters for PDFD used in SFPLL

PDFD Parameter	Value
f_r	155.52 MHz
f_c	(288/235) * 155.52MHz
l	96
η	1/3
k	291

The VCO used was a commercial integrated circuit (Motorola MC12148) inductor capacitor (LC) type oscillator, with varactor diodes for tuning. The majority of the digital logic was implemented in a Field Programmable Gate Array.

3.8.2. Results

For a λ of one the free running frequency of the SFPLL was 0.002 parts per million from ω_r. This illustrates the high precision with which the SFPLL can be centred.

The frequency response of the SFPLL was measured for various λ and the results are shown in Figure 3-13. The decrease in bandwidth with increasing λ can be clearly seen. The measured and predicted bandwidths (ω_{ceff}) are given in Table 3-6. As can be seen there is close agreement between predicted and experimental values.

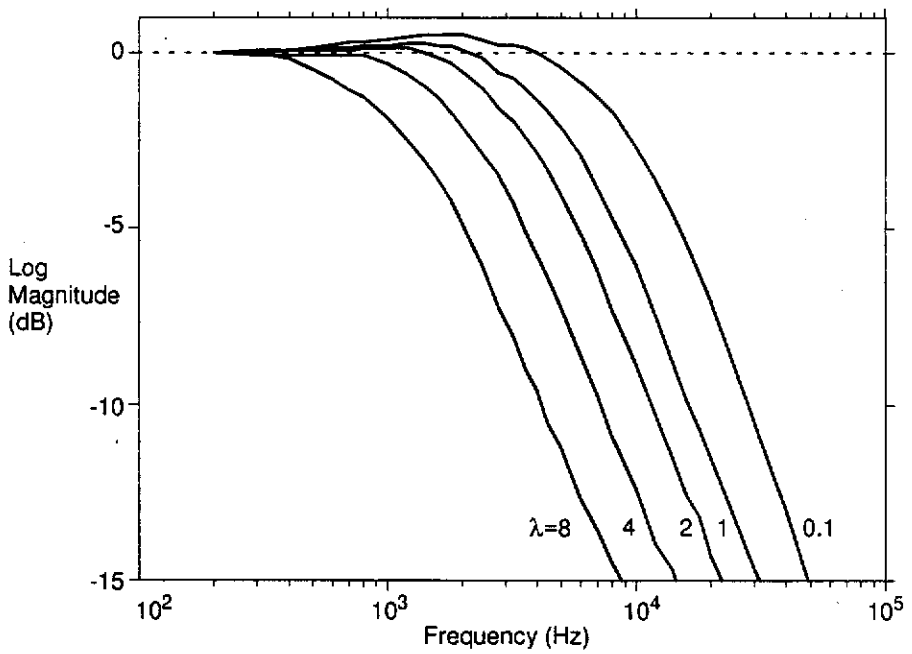

Figure 3-13. Frequency response of SFPLL for various λ. Note the reduction in bandwidth with increased λ. Also note the elimination of peaking in the frequency response with increased λ.

Table 3-6. Predicted and Experimental ω_{ceff}. Note there is good agreement between experimental and predicted bandwidth.

λ	0.1	1	2	4	8
Experimental ω_{ceff}(kHz)	9.0	4.6	3.1	1.8	1.0
Predicted ω_{ceff}(kHz)	9.1	5.0	3.3	2.0	1.1

The spectrum of the free running SFPLL was measured for various λ and the results are shown in Figure 3-14. Note the reduction of close in phase noise (the spectrum span is only 100 Hz) with increased λ.

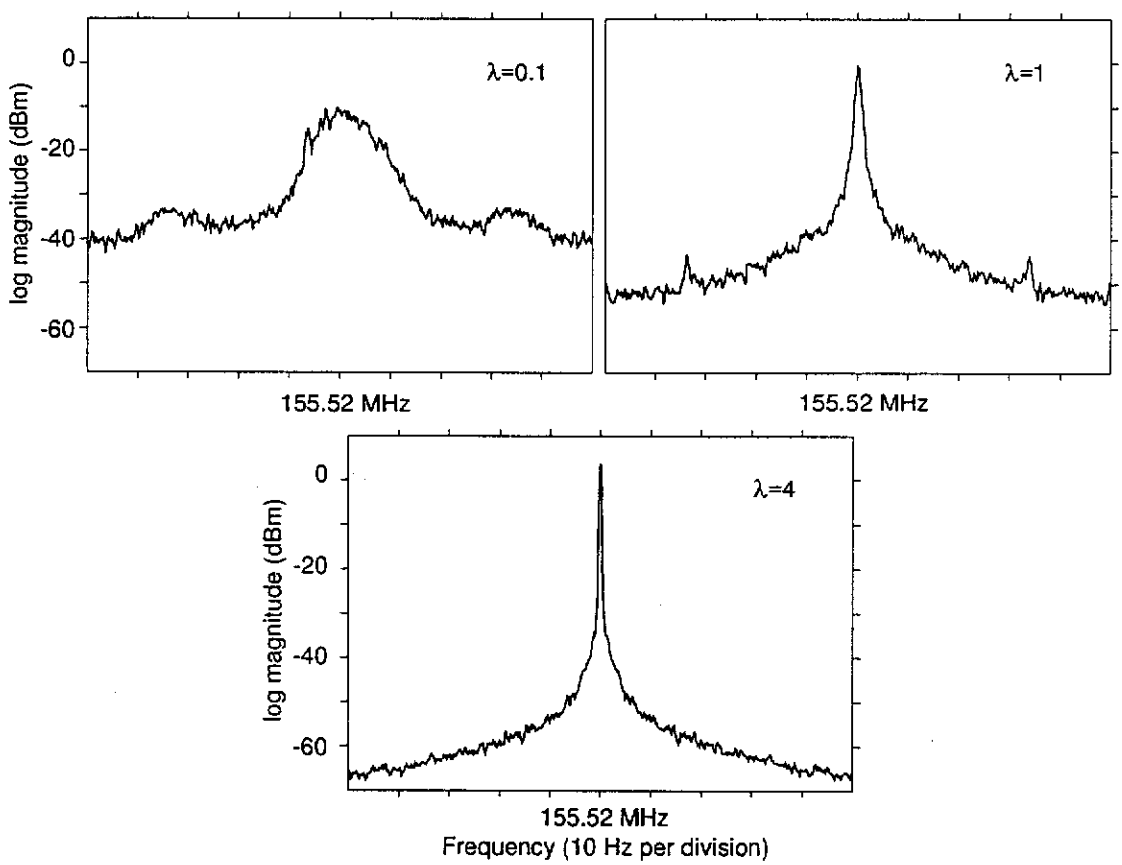

Figure 3-14. Spectrum of output of free running SFPLL showing phase noise effects for various λ. Note how VCO phase noise effects are reduced by increasing λ.

3.9. SUMMARY

A new phase tracking system, the SFPLL, has been described, which introduces a dominate reference frequency and frequency loop into a PLL. The SFPLL diminishes or overcomes the following problems inherent in PLLs: Reliable frequency acquisition, accurate free run frequency, locking to unwanted signals or sidebands, bandwidth change due to component variations, and VCO phase noise.

A small signal linear model for the SFPLL was presented and some general properties of SFPLLs derived. In particular it was shown that the locking range of the SFPLL

could be restricted to a range of frequencies close to the reference frequency. The extent of the range can be controlled and is determined by the ratio of phase loop gain to frequency loop gain.

The general non-linear behaviour of an important class of SFPLL was examined in detail and shown to be identical to types of PLLs. The equivalent PLL requires a high quality VCO to obtain good performance. Whereas the SFPLL can obtain very high performance independent of the qualities of its VCO. It was found that the most important SFPLL, the type II SFPLL is characterized by four parameters ζ_p, λ, ω_n, and ω_r. Its equivalent PLL, an imperfect integrator PLL, is also characterized by four parameters ζ_l, β, ω_{nl}, and ω_{fl}.

The frequency and step responses of the type II SFPLL were also investigated. It was shown that peaking and overshoot in the frequency and step responses could be eliminated with small phase loop damping ζ_p.

Simulations were performed to demonstrate that the SFPLL performance with the input signal corrupted by noise is predicted well using established techniques.

It was shown that the SFPLL can reduce the effect of VCO phase noise to an insignificant level. Also the SFPLL can reduce the dependence of the bandwidth on component parameters.

A digital implementation of the SFPLL was presented. The implementation consisted almost entirely of components made with digital integrated circuit technology, allowing high integration, high speed and low cost. Furthermore the digital implementation provides high accuracy in the frequency loop components of the SFPLL.

A prototype SFPLL was constructed and the experimental results obtained supported the analysis results.

4

Applications of the PDFD

4.1. INTRODUCTION

The precise measurement of frequency offered by the precise digital frequency detector (PDFD) described in Chapter 2, can play a useful role in many systems. Also, through the use of feedback, the PDFD can be used to control or synthesize signals.

In baseband digital communication systems the precise measurement of the frequency of a square wave is required in the following areas: The measurement of the frequency of data sources at the input of networks, and the reconstruction of the data source frequency at the output of the network.

In wireless communication systems employing angle modulation, the information bearing signal often does or can exist as a square wave at some point in the system. Hence the measurement of the frequency of a square wave may find application in both demodulation and modulation components of the wireless system.

Finally, the Steered Frequency Phase Locked Loop described in Chapter 3 employs frequency measurement to eliminate many problems inherent in Phase Locked Loops.

The all digital PDFD method provides a very elegant and integrable solution to the frequency measurement of a square wave. In addition high frequencies can be measured even when the PDFD is clocked at low rates, and the PDFD has no frequency offsets.

This chapter describes two applications of the PDFD. These applications demonstrate that the PDFD can be used to provide solutions to some common problems in electronic

systems. Also, the experimental results obtained from the prototypes constructed verify the principles and operation of the PDFD.

In the first application, Section 4.2, the PDFD is employed to perform demodulation of a continuous phase frequency shift keyed FM signal. The modulation format for the frequency modulated (FM) signal was from a current radio paging system standard [21]. Also, a signal with a very high carrier frequency was demodulated, to demonstrate the fine time resolution of the PDFD.

In the second application, Section 4.3, the PDFD is used to synthesize frequencies. The particular application required a large number of very precise, closely related frequencies to be generated. The PDFD was used to provide an economical and highly integrated solution.

4.2. DEMODULATION OF A FREQUENCY MODULATED SIGNAL

4.2.1. Modulation Format and PDFD Parameters

The FM signal was modulated using a 4 level pulse amplitude modulated FM modulation format [21]. The carrier frequency was 169.425MHz. The symbol rate was 3125Hz and the symbol alphabet was 169.425MHz ±4687Hz, ±1562Hz.

The PDFD parameters are given in Table 4-1. Phase movements down to 1/96 of a reference square wave period (that is, 61 pico seconds) could be detected.

Table 4-1. PDFD Parameters for Demodulator

PDFD Parameter	Value
f_r	169.425 MHz
f_c	(288/235) * 169.425 MHz
l	96
η	1/3
k	291

Another FM signal was demodulated to demonstrate the ability of the PDFD to measure the frequency of high frequency signals. The modulation format of the signal was

identical to the previous format [21], except that the carrier frequency was increased from 169 MHz to 520.833 MHz. The demodulation system and PDFD realization were identical to the 169 MHz case.

The PDFD parameters are given in Table 4-2. Phase movements down to 1/96 of a reference square wave period (that is, 20 pico seconds) could be detected. Note that the PDFD was clocked at the rate of ηf_c, which was only about 62 MHz. This is a much lower rate than the carrier frequency of 520 MHz. Furthermore, it is a much lower rate than the inverse of the phase quantization, that is 1/(20 pico seconds), or 50 gigaHertz.

Table 4-2. PDFD Parameters for High Frequency Demodulator

PDFD Parameter	Value
f_r	520.833 MHz
f_c	(864/811) * 520.833 MHz
l	96
η	1/9
k	873

4.2.2. PDFD Realization and Demodulation System

The demodulation system and details on the realization of the PDFD are shown in Figure 4-1. The simple flip flop which samples the divided down signal, was replaced by a system of flip flops to reduce failure due to metastability to an insignificant amount [52]. The memory elements for the l simple frequency detectors were implemented in a shift register. An exclusive OR gate was time shared between the frequency detectors. The slip events output from the exclusive OR gate were observed for 96 out of 97 clock periods and accumulated by a counter. At the end of every $\frac{k}{f_c}$ reporting period the accumulated slip events held by the counter had N_{nom} subtracted to obtain the phase movement with respect to f_r. The result of the subtraction, N_j^{out}, was output from the PDFD.

The counter was reset at the start of each reporting period. Another counter was used to sequence the operations in the PDFD, and signal the end of reporting periods to the system using the frequency measurement.

The majority of the components of the PDFD were realized in a field programmable gate array.

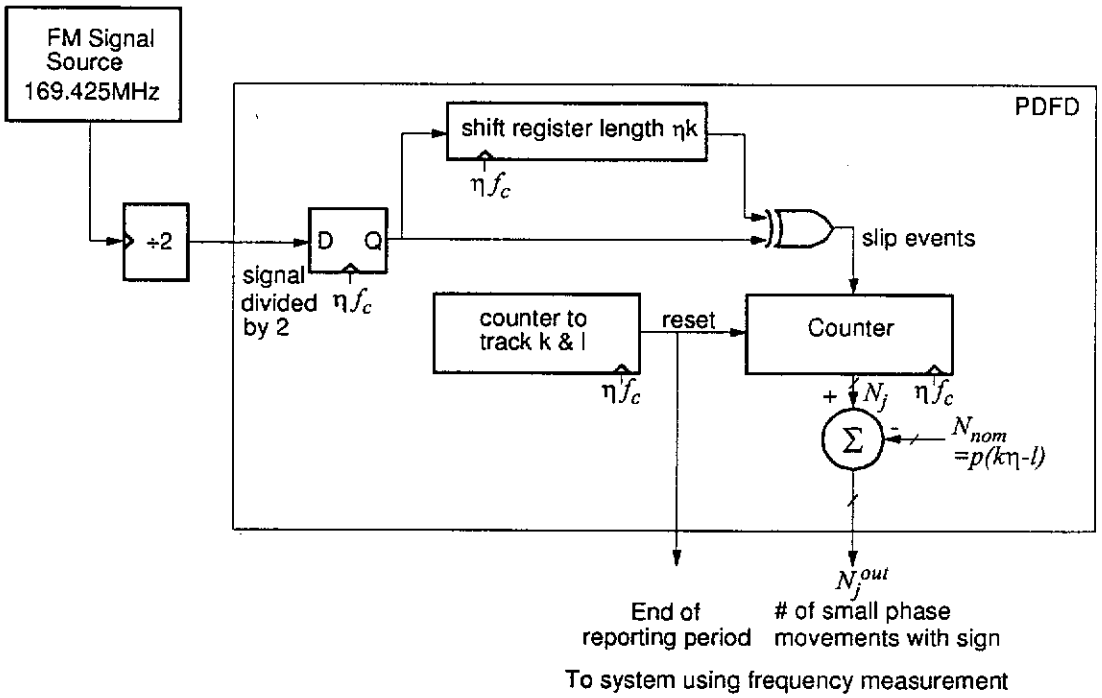

Figure 4-1. PDFD setup used for FM demodulation

4.2.3. Results

For the demodulation of the 169 MHz signal: The number N_j^{out} output from the PDFD was accumulated and reset over twenty five PDFD reporting periods ($\frac{k}{f_c}$). This accumulated value is plotted in Figure 4-2, and shows the successful demodulation of the FM signal.

For the demodulation of the 520 MHz signal: The number N_j^{out} output from the PDFD was accumulated and reset over twenty two PDFD sampling periods ($\frac{k}{f_c}$). This accumulated value is plotted in Figure 4-3, and again shows the successful demodulation of the FM signal.

4.2.4. Demodulation for Signals in Noise

The signals demodulated in the previous section were free of noise and other interfering signals. To demodulate signals buried in noise a classic limiter-discriminator FM

demodulator structure could be used [53]. The PDFD would replace the analog frequency discriminator in the limiter-discriminator demodulator. Note that the bandwidth of the band pass filter proceeding the FM demodulator needs to be very narrow to satisfy the PDFD bandwidth limits (Chapter 2).

It is a subject for future work to further investigate the use of the PDFD in a limiter-discriminator FM demodulator.

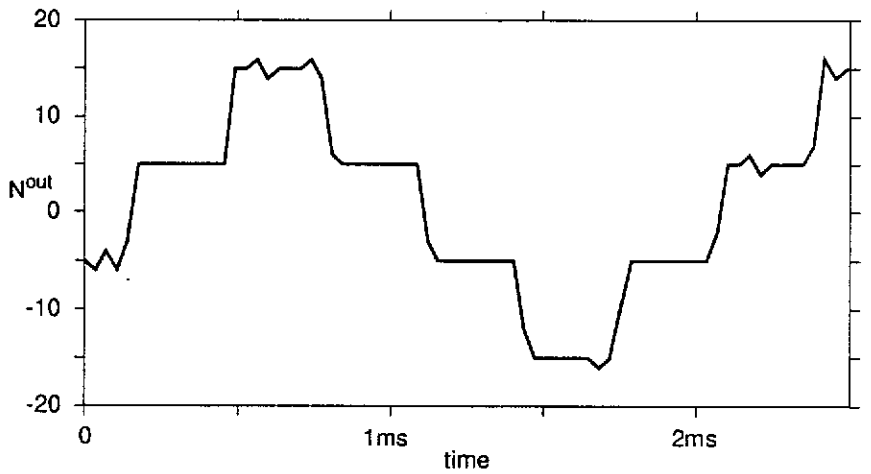

Figure 4-2. Demodulation using PDFD. Shows the successful demodulation of a FM signal of carrier frequency 169 MHz. Phase quantization was $1/96^{th}$ of a cycle, that is 61 pico seconds.

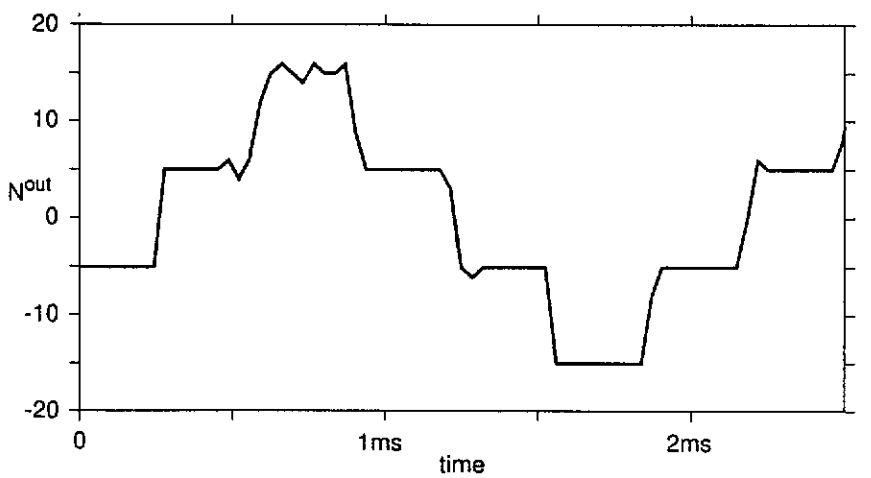

Figure 4-3. Demodulation of high frequency signal using PDFD. Successful demodulation of a FM signal of carrier frequency 520 MHz. Phase quantization was $1/96^{th}$ of a cycle, that is 20 pico seconds. Note that the PDFD was clocked at about 62 MHz, much lower than the carrier frequency, and also much lower than the inverse of the phase quantization, 50 GHz.

4.3. FREQUENCY SYNTHESIS

4.3.1. Requirements and PDFD Parameters

The key requirements of the frequency synthesizer were as follows: frequency range of 139.264MHz ±20ppm, frequency resolution better than 0.2 ppm. It was determined that it would not be economical to use conventional frequency synthesis techniques (PLL, direct digital frequency synthesis) [54]. Due to the digital nature of the PDFD and that it has no long term frequency offsets, it was possible using the PDFD as the key element to construct a frequency synthesizer meeting the requirements. The parameters of the PDFD employed are given in Table 4-3.

Table 4-3. PDFD Parameters for frequency synthesizer

PDFD Parameter	Value
f_r	139.264 MHz
f_c	(288/235) * 139.264 MHz
l	96
η	1/3
k	291

4.3.2. Frequency Synthesis System

The structure of the PDFD based frequency synthesizer is shown in Figure 4-4. The PDFD realization was as shown in Figure 4-1. Most of the components of the frequency synthesizer were realized in a field programmable gate array, the main exceptions were the analog filter and voltage controller oscillator (VCO).

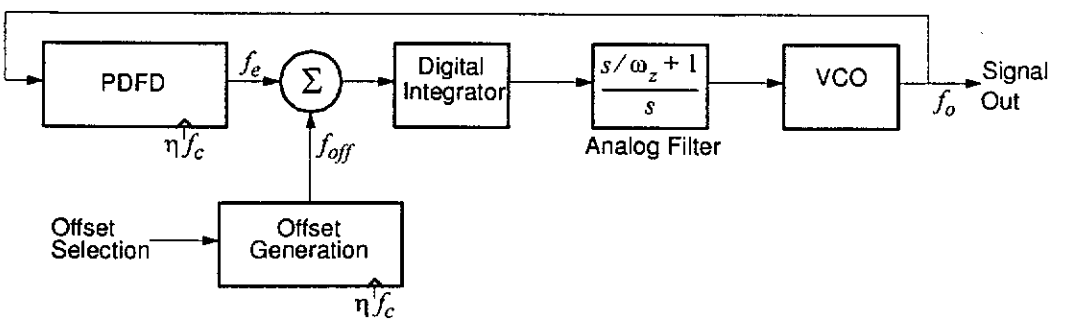

Figure 4-4. PDFD based frequency synthesizer. The synthesizer is possible due to the absence of long term frequency offsets in the PDFD and the ideal nature of digital integration.

Some of the major components of the frequency synthesizer are now described.

- *Digital Integrator.* This digital component outputs the sum of all previous inputs. It samples its inputs at the end of each $\frac{k}{f_c}$ reporting period. Note, being digital, the digital integrator provides 'ideal' integration. That is, there is no leakage or relaxation as there would be for an analog integrator. In Chapter 2 it was shown that the PDFD followed by 'ideal' integration acts a phase movement quantizer, with a quantization level of $1/l^{th}$ of a cycle.

- *Analog Filter.* This filter has a zero and also a pole at the origin. It is identical to the filter discussed in Section 3.7.1, and the filters used in Charge-pump PLLs [44][45]. The filter is realized with a resistor R and capacitor C, and a charge pump on the output of the digital integrator.

- *Offset Generation.* This component outputs 0, or ±1 at the end of each $\frac{k}{f_c}$ reporting period. The offset selection input determines how many reporting periods where 0 is output occur before a ±1 is output. The offset selection input also determines the sign of the output. Each ±1 output will cause a movement of $1/l^{th}$ of a cycle between f_r and f_o. Thus, the rate of 1s output by this component determines the frequency offset f_{off} of the output signal with respect to f_r.

The operating principles of the frequency synthesizer are now described by examining a linear model of the frequency synthesizer. The operation of the PDFD is described by

$$f_e(s) = \frac{f_r}{s} - f_o(s) \tag{4-1}$$

The operation of the VCO is described by

$$f_o(s) = K_o V_{in}(s) \tag{4-2}$$

The digital integrator is modelled by a perfect integrator

$$\frac{1}{s} \tag{4-3}$$

The analog filter transfer function is as follows. Note that ω_l models the small losses in the analog integrator, and typically will be a very small frequency.

$$\frac{s/\omega_z + 1}{s/\omega_l + 1} \tag{4-4}$$

The frequency of the signal out f_o can be found from (4-1), (4-2), (4-3), (4-4)

$$f_o(s) = \frac{(K/\omega_z)s + K}{s^2/\omega_l + (1 + K/\omega_z)s + K}\left(\frac{f_r + f_{off}}{s}\right) \tag{4-5}$$

where K is the product of all the gains in the loop. The steady state value of f_o can be found using the final value theorem

$$\lim_{t \to \infty} f_o(t) = \lim_{s \to 0} s f_o(s) = f_r + f_{off} \tag{4-6}$$

Since the PDFD has no frequency offsets, and the digital integrator is ideal, the linear model describes f_o well. However, as discussed in Chapter 3, Section 3.7.2, the PDFD does depart from the ideal model (4-1) in two key ways, limited bandwidth and phase quantization.

As in Section 3.7.2, the effects due to phase quantization are reduced to an insignificant level by making the phase quantization level very small. In the case considered here the quantization is approximately $1/96^{th}$ of a cycle or 75 pico seconds.

The frequency measurement time $(\frac{k}{f_c})$ of the PDFD was also small enough to counter-act any disturbances in the system (typically from VCO phase noise). Before the output phase had moved more than one phase quantization level.

4.3.3. Results

The component parameters used in the prototype synthesizer are given in Table 4-4. R, C and the charge pump current I are described in Section 3.7.1. The VCO used was a commercial integrated circuit (Motorola MC12148) inductor capacitor (LC) type oscillator, with varactor diodes for tuning, and gain K_o.

Table 4-4. Component parameters for frequency synthesizer

PDFD Parameter	Value
R	5 Ω
C	47 μF
I	1 mA
K_o	10.7 MHz/V

The spectrum of the output of the synthesizer is shown in Figure 4-5. The spectrum compares well with other reported methods of frequency synthesis [5].

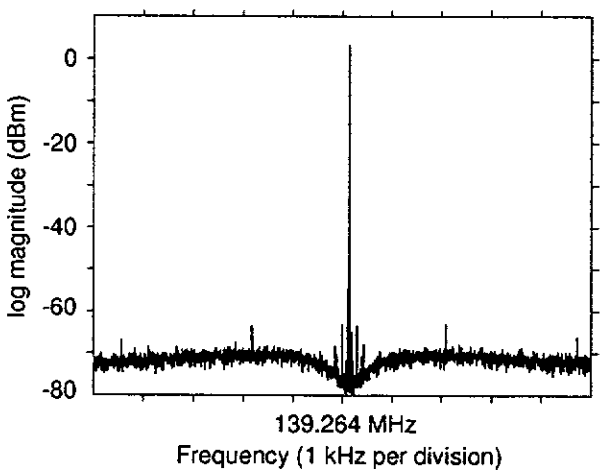

Figure 4-5. Frequency Synthesizer Output Spectrum. Output frequency approximately 139.264 MHz + 1 part per million. Spectrum compares well with other reported frequency synthesis methods.

5

Applications of the SFPLL

5.1. INTRODUCTION

The Steered Frequency Phase Locked Loop (SFPLL) presented in Chapter 3 has several advantages compared to conventional PLLs. The SFPLL may play a useful role in many systems where PLLs are currently used. As it permits higher system integration and lower cost due to the relaxed requirements of the VCO. The SFPLL may also provide solutions to problems which cannot be solved economically with current analog PLL technology, and where high signal frequencies prohibit the use of digital PLL techniques.

This chapter describes two applications of the SFPLL. These applications demonstrate that the SFPLL can be used to provide elegant and integrable solutions to some problems in electronic systems. Also, the experimental results obtained from the prototypes constructed verify the principles and operation of the SFPLL.

In the first application (Section 5.2) the SFPLL is used to construct a phase locking system of very narrow bandwidth. The narrow bandwidth phase locking system is then used to synthesize a high rate clock source (155.52 MHz) from a low rate reference (8 KHz). Furthermore the phase locking system provides filtering for the jitter and noise on the low rate reference.

In the second application, Section 5.3, the PDFD is employed to perform demodulation of a continuous phase frequency shift keying FM signal.

5.2. SYNTHESIS OF HIGH RATE CLOCK FROM LOW RATE REFERENCE IN THE PRESENCE OF JITTER

5.2.1. Introduction

An application which requires very narrow bandwidth PLL systems is the synthesis of a high rate clock source from a jittered low rate reference. This application occurs frequently in broadband digital transmission networks. At the network boundary, a stable high rate clock must often be constructed for the data leaving the network. Typically the high rate clock is synthesized from an 8 KHz frame marker. The 8 KHz frame marker is usually jittered due to the stuffing mechanisms used in the network. The bandwidth of the PLL may need to be very narrow to filter out this jitter [22],[23].

In some contemporary digital transmission networks (SDH/SONET [38]) the jitter may be of very low frequency. To filter out this jitter would require a PLL bandwidth so narrow that it is virtually impossible to attain using analog circuitry [7]. Furthermore, the high signal frequencies (155.52 MHz) prohibit the use of digital PLL techniques.

In this section a SFPLL system is demonstrated which has a centre frequency of 155.52 MHz and a bandwidth of less than one hertz. Furthermore, the SFPLL VCO is a digital application specific integrated circuit relaxation oscillator, and hence the SFPLL system can achieve a high degree of integration.

5.2.2. SFPLL Realization

The SFPLL realization was similar to that shown in Figure 3-12. A description of the realization is given Section 3.7.

The VCO used had a gain K_o of 106 MHz/Volt and a poorly specified centre frequency.

The SFPLL parameters are given in Table 5-1.

The frequency detector used in the SFPLL was a PDFD. The PDFD realization is shown in Figure 4-1 and described in Section 4.2.2. The PDFD parameters are given in Table 5-2.

Table 5-1. SFPLL Parameters for Synthesis

SFPLL Parameter	Value
ζ_p	0.019
λ	64
ω_n	2π 858 r/s
ω_r	2π 155.52 $\times$ 10^6 r/s
ω_{cfil}	2π 22161 r/s
ω_{ceff}	2π 0.5 r/s

Table 5-2. PDFD Parameters for Synthesis

PDFD Parameter	Value
f_r	155.52 MHz
f_c	(288/235) * 155.52MHz
l	96
η	1/3
k	291

5.2.3. Results

To give an indication of the phase noise of the VCO Figure 5-1 shows the spectrum of a free running SFPLL with reduced λ and increased ζ_p. Spectrum are shown with 10 KHz and 100 Hz spans. The free running spectrum of the SFPLL with the correct λ and ζ_p (Table 5-1) is shown in Figure 5-2. The massive reduction of many orders of magnitude in the phase noise effects is clear.

Figure 5-3 is an oscilloscope trace showing the 8 KHz frame marker pulse and the synthesized 155.52 MHz clock. As can be seen the 155.52 MHz clock maintains a stable phase relationship with respect to the frame marker.

The determine the bandwidth of the SFPLL, a phase step was applied to the SFPLL. From the step response the bandwidth was determined approximately to be 0.46 Hz. This is in good agreement with the predicted 0.5 Hz (Table 5-1).

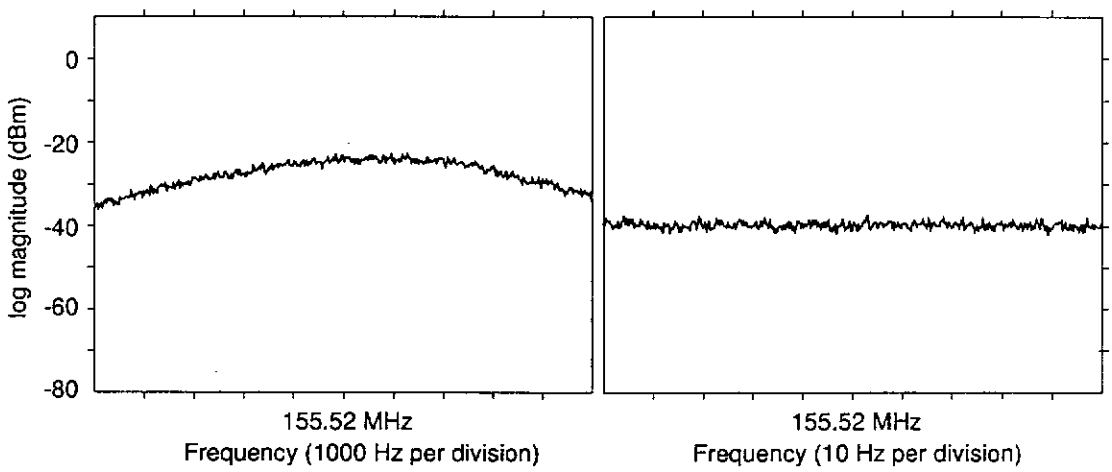

Figure 5-1. Spectrum of output of free running SFPLL with small λ and increased ζ_ρ, to provide an indication of VCO phase noise. (λ=0.25, ζ_ρ=0.14)

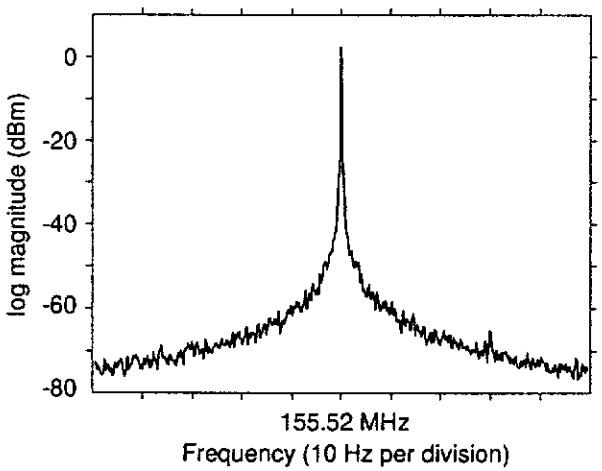

Figure 5-2. Spectrum of output of free running SFPLL with large λ and small ζ_ρ (λ=64, ζ_ρ=0.019). Note the reduction of the effects of VCO phase noise by many orders of magnitude.

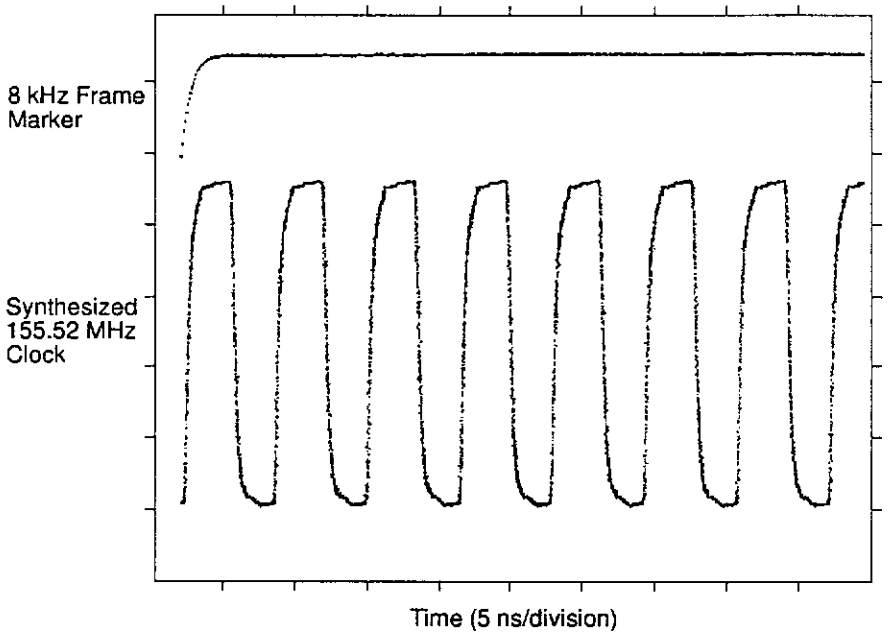

Figure 5-3. Frame Marker and Synthesized 155.52 MHz clock. Shows successful synthesis of the 155.52 MHz clock from the 8 KHz frame marker. The bandwidth of the SFPLL employed was very narrow (0.5 Hz) to provide filtering of jitter and noise on the frame marker.

5.3. DEMODULATION OF A FREQUENCY MODULATED SIGNAL

5.3.1. Introduction

The coherent demodulation of signals by PLLs has been well documented [4]. The use of PLLs to demodulate signals deeply buried in noise has also received attention [4], [43]. A mapping of the SFPLL model to an equivalent ideal PLL was performed in Chapter 3. This mapping enables the literature dealing with PLL demodulators to be applied to SFPLL based demodulators.

It is a subject for future work to investigate in detail the use of the SFPLL to demodulate a signal buried in noise and other signals. However, the demodulation of a noise free signal is given here to: Firstly, demonstrate the possibility of an SFPLL based demodulator. Secondly, to highlight some of the SFPLLs advantages, especially when it is used with the PDFD.

It is worthwhile to compare the SFPLL based demodulator to the PDFD only demodulator presented in Chapter 4. The PDFD demodulator requires a very narrow bandwidth input signal, which may limit its application. Whereas the SFPLL demodulator can cope with wide bandwidth inputs. When the PDFD is used in a SFPLL, the SFPLL can be thought of as providing a broadband interface for the PDFD.

The SFPLL may offer the following advantages over conventional PLLs when used in coherent receivers:

- Controlled and accurate lock range, to enable the de-modulation of a specific channel when the received signal contains a number of channels at different frequencies.
- Reduced VCO phase noise allowing low quality VCOs to be used.
- For SFPLLs employing the PDFD and demodulating angle modulated signals, the modulation information can be obtained in digital form at the output of the PDFD.

In this section a SFPLL system is demonstrated which demodulates a continuous phase frequency shift keyed FM signal. The modulation format for the FM signal is described in Section 4.2.1 and [21].

5.3.2. SFPLL Realization

The SFPLL realization was the same as that shown in Figure 3-12. A description of the realization is given Section 3.7.

The VCO used was a commercial integrated circuit (Motorola MC12148) inductor capacitor (LC) type oscillator, with varactor diodes for tuning. The VCO had a gain K_o of 13.6 MHz/Volt.

The SFPLL parameters are given in Table 5-3.

The frequency detector used in the SFPLL was a PDFD. The PDFD realization is shown in Figure 4-1 and described in Section 4.2.2. The PDFD parameters are given in Table 5-4.

Table 5-3. SFPLL Parameters for Demodulator

SFPLL Parameter	Value
ζ_p	1.11
λ	0.5
ω_n	2π 5.45 × 10^3 r/s
ω_r	2π 169.425 × 10^6 r/s
ω_{ceff}	2π 8 × 10^3 r/s
ω_{ca}	2π 0.3 r/s

Table 5-4. PDFD Parameters for Demodulator

PDFD Parameter	Value
f_r	169.425 MHz
f_c	(288/235) * 169.425 MHz
l	96
η	1/3
k	291

5.3.3. Results

The demodulated signal was obtained in digital form at the PDFD output. The number N_j^{out} output from the PDFD was accumulated and reset over twenty five PDFD reporting periods ($\frac{k}{f_c}$). This accumulated value is plotted in Figure 5-4, and shows the successful demodulation of the FM signal.

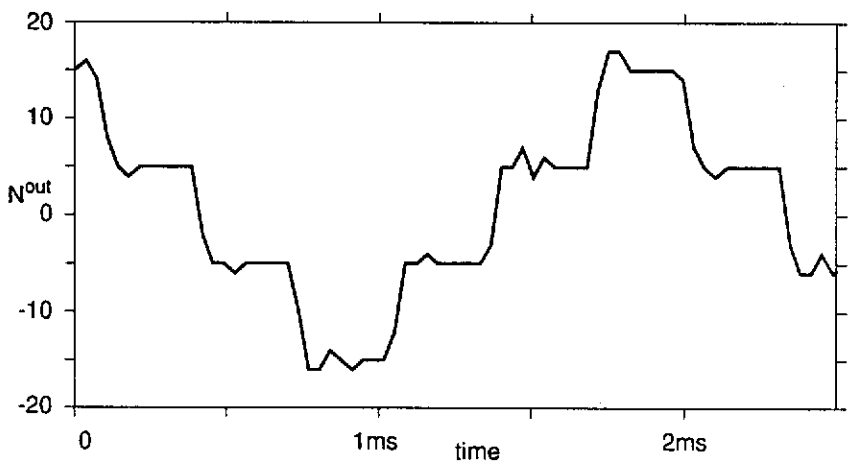

Figure 5-4. Demodulated FM signal. Shows the successful demodulation of a FM signal by the SFPLL. A PDFD was employed as the frequency detector which allowed the demodulated signal to be obtained directly in digital form. The PDFD phase quantization was 1/96th of a cycle, that is 61 ps.

6

SFPLL Implementation with Simple Frequency Measurement

6.1. INTRODUCTION

Much of the analysis of Chapter 3 assumed an ideal frequency detector and frequency loop that have infinite bandwidth. A practical digital frequency detector which approaches this ideal behaviour must have a bandwidth much higher than the phase loop of the SFPLL. Furthermore, the quantization level (normally phase is quantized) of the frequency detector must be small so that the effects due to quantization are insignificant. The PDFD (Chapter 2) is a digital frequency detector which has high bandwidth and small phase quantization, and was used successfully in SFPLLs (Chapter 3).

However, useful accurate free run frequency and restricted lock range properties (Section 3.2), can be obtained when using a simpler frequency detector than the PDFD. In this chapter the use of a simple frequency detector, called the rotational frequency detector [13], in an SFPLL is developed.

The main problem to overcome when using the rotational frequency detector is to mitigate disturbances on the phase loop. These disturbances are due to the quantized nature of the frequency detector. The phase quantization level of the rotational frequency detector is at least one clock cycle. The disturbances on the phase loop are mitigated by employing a low pass filter on the output of the frequency detector ($F_f(s)$, Figure 3-1).

The SFPLL employing a rotational frequency may be useful in applications that do not require the benefits obtained when using the PDFD. Benefits such as VCO phase noise reduction. Typical applications include clock and data recovery circuits. As was mentioned in Chapter 3 a number of techniques have been reported to obtain accurate initial VCO tuning to aid acquisition.

The key advantages of the SFPLL employing the rotational frequency detector over the reported techniques are:

- the output frequency is extremely close to ω_r when no input signal is present.
- The range of frequencies to which the SFPLL can lock can be confined to a small and controllable region around ω_r.
- The SFPLL does not require any monitoring nor any switching of the reference signal which is always acting.

This chapter is organized as follows: In Section 6.2 an overview of the implementation is given. Then in Section 6.3 and Section 6.4 the phase and frequency loops of the SFPLL are examined. In Section 6.5 and Section 6.6 a method to mitigate the disturbances of the frequency loop on the phase loop is described. Experimental results for a clock recovery system operating at 155.52MHz are given in Section 6.7. Finally, Section 6.8 summarizes the chapter.

Note also that in Appendix C the digital filter used in this SFPLL implementation is developed.

6.2. SYSTEM OVERVIEW

The digital implementation of the SFPLL using the rotational frequency detector is shown in Figure 6-1. The components in the digital implementation correspond to the blocks in the SFPLL model presented in Chapter 3 Figure 3-1, as follows:

The phase detector, frequency detector and VCO are the same in both model and implementation. The digital filter in the implementation corresponds to the filter $F_f(s)$. The digital combiner corresponds to the summer in the model.

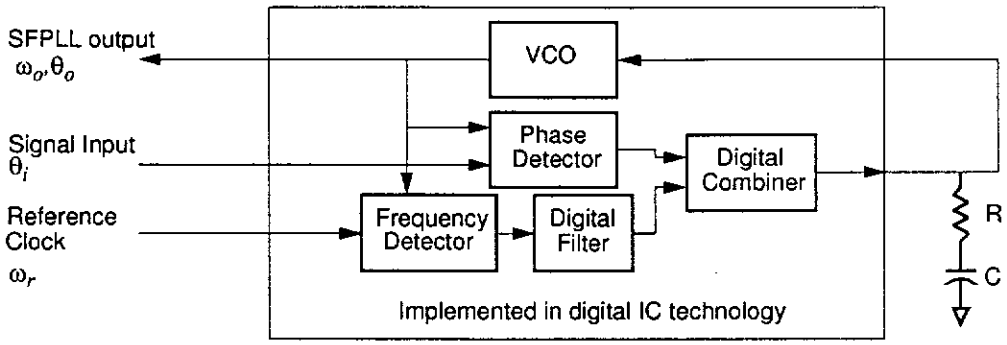

Figure 6-1. Digital Implementation of SFPLL using simple frequency detector. The key difference with the previous SFPLL implementation is the presence of the digital filter block. The digital filter is required to mitigate the disturbances on the phase loop caused by the simple frequency detector.

The resistor and capacitor correspond to the filter $F_c(s)$ in the model. As was discussed in Section 3.7.1, $F_c(s)$ has a pole very close to the origin and a zero. The output from the digital combiner is a current. This current source is achieved with a charge pump on the output of the digital combiner.

The additional gains K_p and K_f in the model are related to the magnitude of the digital combiner charge pump current. The filter $F_p(s)$ is not present in this implementation.

The parameters of the system and how they relate to system performance requirements are now given:

- The small signal characteristics of the SFPLL implementation described here are specified by ζ_p and ω_n. It is assumed that the phase loop dynamics are not affected by the frequency loop, because the output of the frequency detector is low pass filtered, unlike in Section 3.3. The approximate open loop cross-over frequency ω_c (related to ω_n, ζ_p (3-20)) and ζ_p can be deduced from system performance parameters. For example jitter transfer mask in [38], which requires $\omega_c < 2\pi$ 130 kr/s and $\zeta_p > 4.5$.

- The range of frequencies to which the phase loop is confined by the frequency loop (3-19). The steady state phase error θ_ε under worst case frequency offsets, that is, maximum ω-ω_r (3-78).

- The frequency loop of the SFPLL must be stable and hence have a sufficiently high damping factor ζ_f.
- The reference frequency is normally a sub-multiple, m, of the SFPLL output frequency.
- The maximum clock rate at which the various digital components can be run at will typically be a sub-multiple of the SFPLL output frequency, N_w.

6.2.1. Phase and Frequency Detectors

Phase detectors can be constructed using digital logic gates and/or flip flops. The individual designs and characteristics are covered extensively in the literature e.g. [48]. The phase detector characteristics of importance in this chapter are the gain K_{pd}, and the maximum phase error $\theta_{\varepsilon max}$.

The frequency detector used is described by Messerschmitt in [13] and is called a rotational frequency detector. It is implemented using purely digital components such as flip flops and logic gates. The rotational frequency detector outputs a pulse every time the reference clock (ω_r) phase 'slips' past the VCO clock (ω_o) by a cycle. Hence the phase quantization level of the rotational frequency detector is one cycle. The rate at which the detector outputs pulses indicates the magnitude of the frequency difference ω_r-ω_o. The gain of the rotational frequency detector, K_{fd} is

$$K_{fd} = \frac{1}{\omega_r} \tag{6-1}$$

6.3. PHASE LOOP PARAMETERS

Based on the results presented in [44], the values of the filter components R and C can found in terms of ω_c, ζ_p, K_o (VCO gain) and K_{pd}

$$R = \frac{\omega_c}{K_{pd}K_oI_p} \tag{6-2}$$

$$C = \frac{4\zeta_p^2 K_{pd}K_oI_p}{\omega_c^2} \tag{6-3}$$

Consider for the moment that the digital combiner (Figure 6-1) is removed and that the phase and frequency detectors each have a charge pump. The outputs of the two charge pumps are tied together and pump current into the RC filter. The digital combiner will be introduced and a charge pump eliminated in Section 6.5.

I_p is the phase detector charge pump current, and is defined as the additional gain factor K_p. The frequency detector charge pump current I_{ff}, defined as the additional gain factor K_f, can be found

$$I_{ff} = \frac{\lambda I_p K_{pd}}{K_{fd}\omega_c} \tag{6-4}$$

When the frequency detector pumps current into the C it causes phase and frequency disturbances to the phase loop. If these disturbances are too great they will cause the phase loop to loose lock. There are two disturbance mechanisms:

The first disturbance is a phase disturbance θ_d. It is caused when the frequency detector pumps current through R, thus causing a short term shift in the VCO voltage and hence a phase jump. For the phase loop to maintain lock θ_d must be less than 2π. In fact for reliable operation and low phase jitter on the SFPLL output condition (6-5) must be met.

$$\theta_d \ll 2\pi \tag{6-5}$$

With the current pulse from the frequency detector lasting for one VCO clock period, that is $2\pi/\omega_o$ seconds. Then from (6-2), (6-4), and applying the condition of (6-5), the following relating phase disturbance as a fraction of one cycle (that is, 2π) is obtained

$$\frac{\theta_d}{2\pi} = \frac{\lambda}{K_{fd}\omega_o} \ll 1 \tag{6-6}$$

The second disturbance is a frequency disturbance ω_d. It is caused by the voltage on C being shifted as a result of current being pumped into C. Hence the VCO has a shifted voltage applied to it. The phase loop will eventually counter act this through its phase error, θ_ε, providing the phase loop remains locked. For the phase loop to maintain lock ω_d must be less than the pull out frequency of the phase loop [6]. The pull out frequency for a highly damped type II PLL is approximately ω_c. For reliable operation and low jitter on the SFPLL output the condition (6-7) must be met.

$$\omega_d \ll \omega_c \tag{6-7}$$

If the current pulse from the frequency detector lasts for one VCO clock period. Then from (6-3) and (6-4), and applying the condition of (6-7), the following relating ω_d as a fraction of ω_c is obtained

$$\frac{\omega_d}{\omega_c} = \frac{\pi\lambda}{2K_{fd}\zeta_p^2\omega_o} \ll 1 \tag{6-8}$$

Now consider the situation where the reference clock input is not ω_r, but instead is a sub-multiple, ω''_r i.e.

$$\omega''_r = \frac{\omega_r}{m} \tag{6-9}$$

Where m is an integer. This situation will likely be the norm as firstly the frequency detector actually needs to be run at $4\omega''_r$ rate (see [13]). And secondly the range of frequencies at which low cost crystal oscillators (which will most likely provide ω''_r) operate is limited to a few tens of megahertz. To perform a valid comparison with ω''_r

ω_o also has to be similarly scaled down. The rate at which phase slips of one cycle between ω''_r and ω''_o occur is also reduced by m.

The slip rate is also the rate at which the frequency detector emits pulses and the gain of the frequency detector is reduced by a factor of m. Effectively the quantization level of the frequency detector has been increased from one clock cycle to m clock cycles. To maintain the same frequency loop gain the duration of the frequency detector current pulse must be increased m times. Or the current I_{ff} must be increased m times. Either way the disturbance to the phase loop is increased m times, even though it will occur m times less often.

6.4. FREQUENCY LOOP PARAMETERS

Consider for the moment that the R is replaced by a short circuit. The open loop transfer function of the frequency loop is

$$\frac{K_{fl}}{s} \tag{6-10}$$

K_{fl} is related to other system parameters

$$K_{fl} = K_{fd} I_{ff} \frac{1}{C} K_o = \frac{\lambda \omega_c}{4\zeta_p^2} \tag{6-11}$$

If a pole at frequency ω_p is introduced by the digital filter, the frequency loop becomes a second order system. The positioning of the pole ω_p will affect the closed loop stability and damping factor ζ_f. A general requirement is that the frequency loop is stable and hence the damping is sufficient. ω_p can be determined in terms of ζ_f and other system parameters

$$\omega_p = \frac{\lambda \zeta_f^2 \omega_c}{\zeta_p^2} \tag{6-12}$$

Considering now the effect of the R on the frequency loop. The effect of R is to introduce a zero at frequency ω_z in the frequency loop, which enhances frequency loop stability.

6.5. DISTURBANCE REDUCTION

To reduce the sudden phase and frequency disturbance of each pulse from the frequency detector (Section 6.3), the pulse is spread out over a long time. This can be done by breaking the pulse up into a large number of smaller pulses as shown in Figure 6-2.

Each frequency detector pulse is broken up into N_s smaller pulses, each of N_w VCO clock periods wide, and spaced at N_pN_w VCO clock periods. Thus I_{ff} is reduced, effectively decoupling it from K_f. The new frequency loop output current I_f is defined as

$$I_f \equiv I_{ff}\frac{m}{N_wN_s} \tag{6-13}$$

The new phase and frequency disturbances for the smaller pulses of width N_w are reduced from (6-6), (6-8) by a factor N_s

$$\frac{\theta_d}{2\pi} = \frac{m\lambda}{N_sK_{fd}\omega_o} \ll 1 \tag{6-14}$$

$$\frac{\omega_d}{\omega_c} = \frac{m\pi\lambda}{2N_sK_{fd}\zeta_p^2\omega_o} \ll 1 \tag{6-15}$$

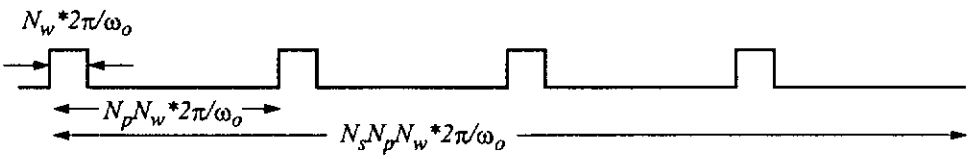

Figure 6-2. Spreading out frequency detector pulses to reduce their disturbance on the phase loop.

Having I_f now decoupled from K_f provides freedom in choosing I_f. The frequency loop only has to nullify the phase loop output to steer and confine the VCO and hence ω_o. As

$F_c(s)$ has a pole at the origin. So I_f must be greater than the maximum average phase detector output

$$I_f > \theta_{\varepsilon max} K_{pd} I_p \tag{6-16}$$

Fast steering of the VCO at system start-up, when C is discharged, is what is sacrificed by making I_f small. This fast steering at start-up would not normally be a critical performance requirement. Providing

$$\theta_{\varepsilon max} K_{pd} < 1 \tag{6-17}$$

it is possible to choose I_f equal to I_p. With I_f equal to I_p the frequency and phase detector outputs can be combined digitally, and only one charge pump is required (digital combiner Figure 6-1).

6.6. FREQUENCY LOOP FILTER

A possible system for implementing the disturbance reduction scheme outlined in the previous section, is to employ Binary Rate Multipliers (BRM) [55]. Also it is advantageous to include a pole ω_p in the pulse spreading system, forming a low pass filter. The digital low pass filter limits the bandwidth of the frequency loop, helping to decouple it from the dynamics of the phase loop.

'Operational digital' techniques [55], can be used to provide an implementation of the pulse spreading system, that also has the characteristics of a low pass filter. The detailed development of a suitable Binary Rate Multiplier based digital filter with one pole is given in Appendix C. The structure of the BRM based digital filter is shown in Figure 6-3. Note that this BRM based digital filter corresponds to the digital filter block in Figure 6-1.

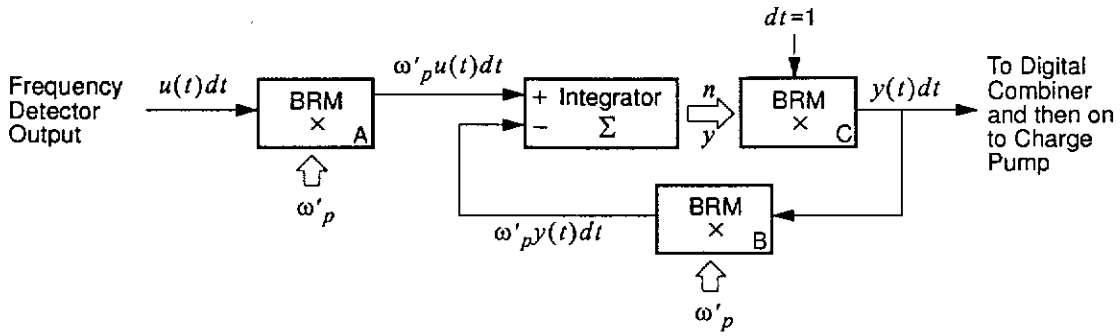

Figure 6-3. Binary Rate Multiplier (BRM) based system to implement pulse spreading with pole. The pulse spreading significantly reduces the frequency detector disturbances on the phase loop. Note that this BRM based system is the digital filter block in Figure 6-1.

6.7. EXPERIMENTAL RESULTS FOR SONET STS-3C CLOCK RECOVERY

The digital implementation of the SFPLL was used as the basis for a clock recovery system that meets SONET STS-3c specifications [38]. The SONET STS-3c clock recovery system was constructed using a field programmable gate array for the digital circuits. The VCO used was an integrated circuit multivibrator with a large gain (K_o) of 106 MHz/V, and a poorly specified free running frequency. A version was also integrated in a digital application specific integrated circuit. The digital integrated circuit, integrated functions ranging from clock recovery, SONET framing, to asynchronous transfer mode cell switching.

Experimental results on the performance of the system are shown in Figure 6-4 and Figure 6-5. Figure 6-4 shows that the SFPLL can be designed to limit the peaking in the transfer function to meet the standards requirement.

A version of the SFPLL which had the frequency loop bypassing R and the output of the digital filter feeding directly into C was built. This version requires two current pumps but the phase disturbance caused by pumping current through R (6-14) is avoided. In Figure 6-5 the reduction of frequency loop induced noise for the version which bypasses R can be clearly seen.

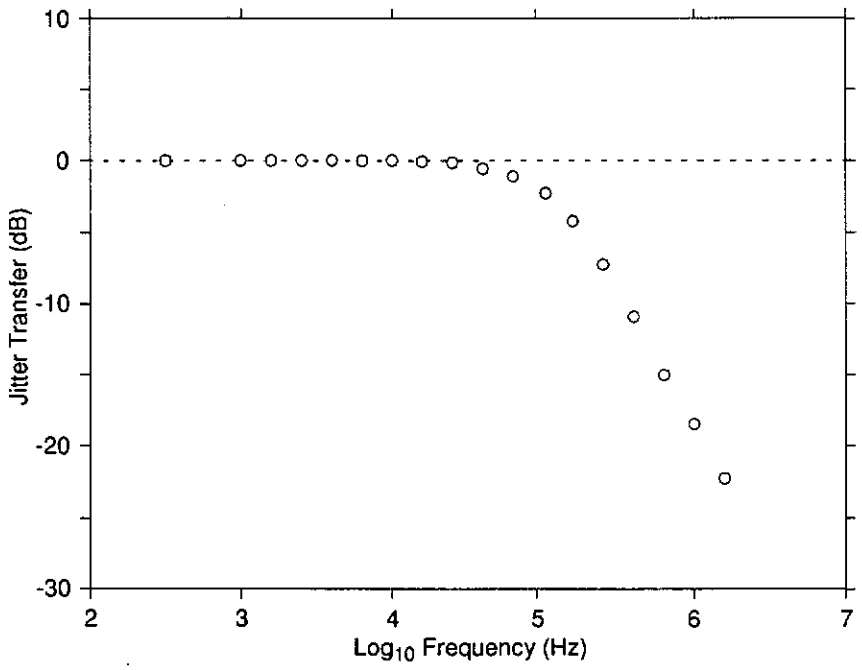

Figure 6-4. Jitter transfer characteristics of SFPLL based clock recovery system (using 7 bit PRBS sequence). The transfer characteristic meets standards requirements of peaking and bandwidth.

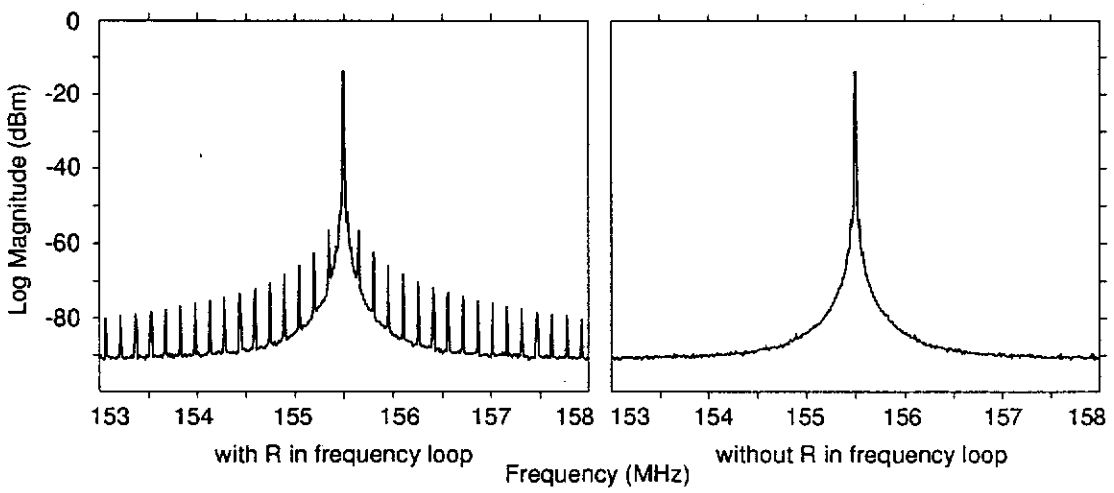

Figure 6-5. Spectrum of recovered clock (11001100 data pattern). Note the difference in frequency loop induced noise when the R is bypassed, and the phase disturbance (6-14) is not present.

6.8. SUMMARY

In this chapter it was identified that the rotational frequency detector has large phase quantization. Also, it was identified that this large phase quantization causes significant disturbances on the SFPLL phase loop.

A digital filter method was proposed to mitigate these disturbances, and also decouple the dynamics of the phase loop from the frequency loop. The parameters of the digital filter were determined from the SFPLL system requirements.

The SFPLL implementation was experimentally demonstrated in a clock recovery system that met SONET STS-3c specifications [38]. The SFPLL based clock recovery system provided accurate free run frequency and a confined locking range at low cost. Additionally, different data rates can be accommodated with the same VCO by simply changing the reference frequency, or by adding an offset in the frequency loop.

A digital frequency loop delivers great precision in control of the SFPLL frequency. However, in this implementation the frequency loop introduced noise into the SFPLL output clock. Other SFPLL applications will typically have greater spectral purity requirements for the SFPLL output clock than clock recovery. Although the noise introduced by the digital frequency loop can be made small for a highly damped, narrow bandwidth loop (Figure 6-5).

7

Conclusion

7.1. FURTHER WORK

In this section some suggestions are given for further research work to answer questions arising from this thesis.

In Chapter 4 the precise digital frequency detector (PDFD) was experimentally demonstrated resolving phase movements down to 20 pico seconds. The time resolution limits of the PDFD have not been determined, given the particular technology and other factors such as signal to noise levels. Knowledge of the time resolution limits of the PDFD and the limiting causes will likely enable the design of PDFD systems with time resolution limits much smaller than 20 pico seconds.

Hence, a suggestion for further work is to determine the time resolution limits of the PDFD when it is implemented in a given technology.

It may be possible to extend the PDFD technique to other quantized repetitive waveforms. The extended PDFD technique may provide a way to obtain finer phase quantization.

How the PDFD fits into contemporary theories of sampling, demodulation and signal processing, should be investigated.

For the steered frequency phase locked loop (SFPLL, Chapter 3) it was assumed that the frequency detector quantization was small and bandwidth large. This allowed the frequency detector to be considered ideal. However, where the SFPLL phase tracking

bandwidth needs to be large it may be difficult to obtain a frequency detector that can be considered ideal.

Hence, a suggestion for further work is to determine the exact behaviour of the SFPLL when the frequency detector can no longer be considered ideal.

7.2. CONCLUSION

A new method has been presented to measure small frequency differences between a reference square wave and a signal square wave. The method called the PDFD involves the use of a large number of simple frequency detectors each with different start phases.

The PDFD has the following important advantages over current techniques of frequency measurement:

- It can be constructed from simple digital components such as logic gates and flip flops.
- Small phase movements between the signal and reference square waves can be detected, even when the PDFD is clocked at low rates.
- Finally, the PDFD has no frequency offsets.

The operating limits of the PDFD were derived. It was found that the allowable deviation from the nominal frequency of the signal being measured was approximately proportional to $1/l^2$. That is, approximately proportional to the square of the smallest measurable phase movement. Hence the PDFD is most suitable for measuring the frequency of narrow-band signals.

The spectral characteristics of the frequency estimator output by the PDFD were also derived.

The PDFD was experimentally demonstrated in two applications: FM demodulation and frequency synthesis. These applications demonstrated that the PDFD can be used to provide elegant and integrable solutions to some common problems in electronic

systems. The PDFD was able to resolve small phase movements in a high frequency signal that corresponded to 20 pico seconds.

The PDFD method was demonstrated to provide an improvement over current all digital frequency measurement techniques for narrow-band signals of several orders of magnitude.

A new phase tracking system, the SFPLL, has been described, which introduces a dominate local reference frequency and frequency loop into a PLL (phase locked loop).

The SFPLL has the following important advantages over PLLs:

- The centre frequency of the SFPLL can be precisely controlled.
- The range of frequencies to which the SFPLL can lock can be confined to a desired small region around the accurate centre frequency of the SFPLL.
- Bandwidth changes due to component variations can be reduced.
- The effects of VCO phase noise can be reduced to insignificant levels.

A small signal linear model for the SFPLL was presented and some general properties of SFPLLs derived. In particular it was shown that the locking range of the SFPLL could be restricted to a range of frequencies close to the reference frequency.

The general non-linear behaviour of an important class of SFPLL was examined in detail and shown to be identical to types of PLLs. Simulations were performed to demonstrate that the SFPLL performance with the input signal corrupted by noise is predicted well using established techniques.

It was shown that the SFPLL can reduce the effect of VCO phase noise to an insignificant level, and also reduce the dependence of the bandwidth on component parameters.

A digital implementation of the SFPLL was presented. The implementation consisted almost entirely of components made with digital integrated circuit technology, allowing

high integration and low cost. Furthermore the digital implementation provides high accuracy in the frequency loop components of the SFPLL.

A prototype SFPLL was constructed and the experimental results obtained supported the analysis predictions of phase noise reduction and bandwidth changes.

The SFPLL was experimentally demonstrated in two applications: Very narrow bandwidth phase locking systems and FM demodulation. In particular the very narrow bandwidth phase locking system demonstrated the ability of the SFPLL to reduce VCO phase noise effects by several orders of magnitude.

In summary, the techniques presented in this thesis provide significant improvements in the ability of systems implemented in digital integrated circuit technology to: Measure and control phase and frequency of narrow band signals; Implement high performance phase tracking systems.

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A

PDFD Derivations

A.1. INTRODUCTION

This appendix details some derivations relating to the PDFD (Chapter 2).

A.2. SIMPLE FREQUENCY DETECTOR OPERATION

The operation of the simple frequency detectors described in Chapter 2, Section 2.3, is characterized by the key equations (2-7) and (2-10). In this section these two equations will be derived.

k=1 case. Considering first the case where every sample is used. The situation is illustrated in Figure A-1. At the a^{th} sample instant T_{diff} is given by

$$T_{diff} = \frac{a}{f_s} - \frac{a}{f_c} + \frac{\theta^i_{init}}{f_s} \qquad \text{(A-1)}$$

Note that here the sample which occurs at time zero is denoted the 0^{th} sample, with subsequent samples being the 1^{st}, 2^{nd}, 3^{rd} etc.

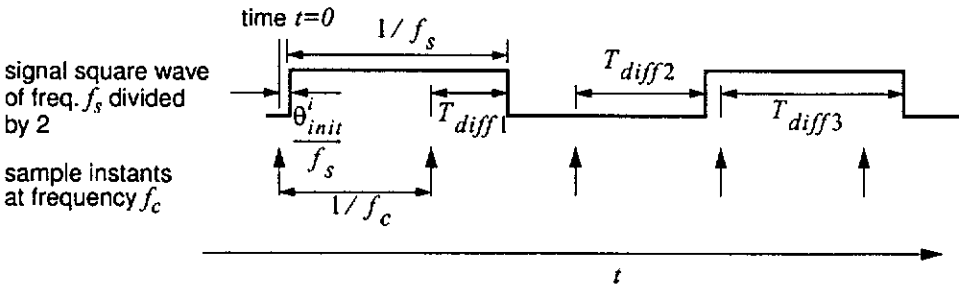

Figure A-1. Slip events for k=1

From Figure A-1 it is clear that the first slip event occurs on the sample instant after the condition (A-2) is satisfied. Let the sample instant where condition (A-2) is satisfied be the $a_1{}^{th}$ sample. a_1 can be determined (A-3)

$$T_{diff} > \frac{1}{f_c} \tag{A-2}$$

$$a_1 = \left\lfloor f_c \left(\frac{1-\theta_{init}^i}{f_c - f_s} \right) \right\rfloor \tag{A-3}$$

From the properties of the floor function ($\lfloor x \rfloor$), the following relation is true

$$\left\lfloor f_c \left(\frac{1-\theta_{init}^i}{f_c - f_s} \right) \right\rfloor \leq f_c \left(\frac{1-\theta_{init}^i}{f_c - f_s} \right) < \left\lfloor f_c \left(\frac{1-\theta_{init}^i}{f_c - f_s} \right) \right\rfloor + 1 \tag{A-4}$$

From which follows

$$\frac{a_1}{f_c} \leq t_m\big|_{m=1} < \frac{a_1 + 1}{f_c} \tag{A-5}$$

With t_m being given by (2-7). Hence the first slip event will be reported on the sampling instant following t_1 (2-7), that is, the $(a_1+1)^{th}$ sample.

Now considering the m^{th} slip event. The condition which must be satisfied by the $a_m{}^{th}$ sample is

$$T_{diff} > \frac{1}{f_c} + \frac{m-1}{f_s} \tag{A-6}$$

a_m can be found to be

$$a_m = \left\lfloor f_c \left(\frac{m-\theta_{init}^i}{f_c - f_s} \right) \right\rfloor \tag{A-7}$$

and in a manner similar to a_1 the following relation is found to be true

$$\frac{a_m}{f_c} \le t_m < \frac{a_m + 1}{f_c} \tag{A-8}$$

Hence the m^{th} slip event will be reported on the sampling instant following t_m (2-7), that is, the $(a_m+1)^{th}$ sample.

k >1 case, k odd, p even. Considering now the case where only every k^{th} sample of the signal is used. Initially only k odd and p (2-9) even is considered. The situation is illustrated in Figure A-2. At the a^{th} sample instant T_{diff} is given by

$$T_{diff} = a\left(\frac{k-p}{f_s} - \frac{k}{f_c}\right) + \frac{\theta^i_{init}}{f_s} = ak\left(\frac{f_{cmp} - f_s}{f_s f_c}\right) + \frac{\theta^i_{init}}{f_s} \tag{A-9}$$

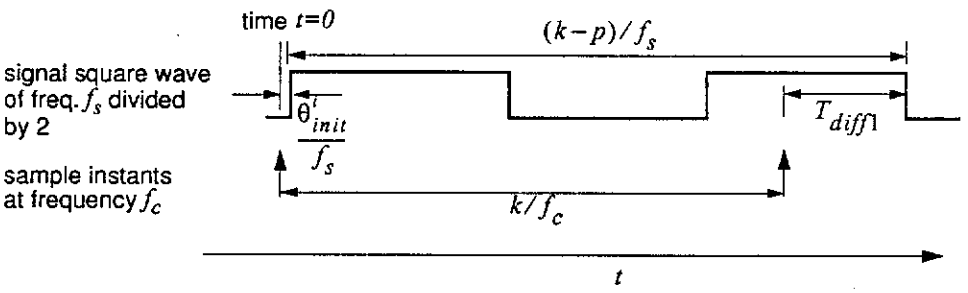

Figure A-2. Slip events for k>1

Now considering the m^{th} slip event. The condition which must be satisfied by the $a_m{}^{th}$ sample is

$$T_{diff} > \frac{m}{f_s} - k\left(\frac{f_{cmp} - f_s}{f_s f_c}\right) \tag{A-10}$$

a_m can be found to be

$$a_m = \left\lfloor \left(\frac{f_c}{k}\right)\left(\frac{m - \theta^i_{init}}{f_{cmp} - f_s}\right) \right\rfloor \tag{A-11}$$

From the properties of the floor function the following relation is true

$$\left\lfloor \left(\frac{f_c}{k}\right)\left(\frac{m-\theta^i_{init}}{f_{cmp}-f_s}\right)\right\rfloor \le \left(\frac{f_c}{k}\right)\left(\frac{m-\theta^i_{init}}{f_{cmp}-f_s}\right) < \left\lfloor \left(\frac{f_c}{k}\right)\left(\frac{m-\theta^i_{init}}{f_{cmp}-f_s}\right)\right\rfloor + 1 \qquad \text{(A-12)}$$

From which follows

$$a_m\left(\frac{k}{f_c}\right) \le t_m < (a_m+1)\left(\frac{k}{f_c}\right) \qquad \text{(A-13)}$$

With t_m being given by (2-10). Hence the m^{th} slip event will be reported on the sampling instant following t_m (2-10), that is, the $(a_m+1)^{th}$ sample.

k >1 case, k odd, p odd. Considering now the case where k is odd and p is odd. The number of signal square wave f_s clock periods between sample instants $(k\text{-}p)$ will be even. Whereas in the previous cases the number of clock periods between sample instants have been odd.

For k odd, a slip event is defined as two consecutive samples having the same value. With k-p even, it is clear that slip events will be reported on all sample instants except those sample instants following t_m (2-10). That is, the $(a_m+1)^{th}$ sample.

k >1 case, k even. For k even, a slip event is defined as two consecutive samples having the different values (Chapter 2). In a manner similar to the k odd case, it can be shown that for k even, p even, the m^{th} slip event will be reported on the sampling instant following t_m. Furthermore for k even, p odd, slip events will be reported on all sample instants except those sample instants following t_m.

A.3. OPERATING LIMITS

It is shown here that the PDFD characteristic (2-15) is bounded by two quantizers. In particular the case of l successive samples being used is dealt with.

In Chapter 2, Section 2.4, with the θ^i_{init} uniformly distributed over [0,1) the PDFD characteristic was said to be a quantizer. However, when f_s is not equal to f_r the θ^i_{init} will not be uniformly distributed. For the case of f_s slightly greater than f_r, the θ^i_{init} will be less than their nominal values. Each θ^i_{init} will be perturbed from its nominal position

by $\Delta(\theta^i_{init})$. The θ^i_{init} of the last simple frequency detector is perturbed most and is denoted Δ_{max}. (Note $\Delta(\theta^i_{init})$ is negative for f_s greater than f_r). $\Delta(\theta^i_{init})$ can be determined from (2-19) and examining Figure 2-3.

$$\Delta(\theta^i_{init}) = i\delta \tag{A-14}$$

where

$$\delta \equiv \frac{l-p}{l}\left(1-\frac{f_s}{f_r}\right) \tag{A-15}$$

$$\Delta_{max} = \max_i \Delta(\theta^i_{init}) = (l-1)\delta \tag{A-16}$$

Using the uniformly distributed θ^i_{init} (2-14), and the perturbations (A-14), equation (2-15) can be expanded to give an equation of the following form

$$\theta_{out} = \frac{1}{l}\left(\lfloor \theta_{slip}+\phi_0 \rfloor + \left\lfloor \theta_{slip}+\phi_0+\frac{1}{l}+\delta \right\rfloor + \ldots \right. \\ \left. \ldots + \left\lfloor \theta_{slip}+\phi_0+\frac{l-1}{l}+(l-1)\delta \right\rfloor\right) \tag{A-17}$$

Employing the following identity (A-18) from [20], bounds on θ_{out} can be found.

$$\lfloor mx \rfloor = \lfloor x \rfloor + \left\lfloor x+\frac{1}{m} \right\rfloor + \ldots + \left\lfloor x+\frac{m-1}{m} \right\rfloor, \qquad m \in Z, x \in R \tag{A-18}$$

Where Z denotes the set of integers and R the set of real numbers. For the case of f_s slightly greater than f_r, the θ_{out} is bounded as follows:

$$\frac{\lfloor l(\theta_{slip}+\phi_0-|\Delta_{max}|) \rfloor}{l} \le \theta_{out} \le \frac{\lfloor l(\theta_{slip}+\phi_0) \rfloor}{l} \tag{A-19}$$

The lower bound (A-19) equals θ_{out} when

$$\theta_{slip}+\phi_0 = w^- + \frac{1}{l} + |\Delta_{max}|, \qquad w \in Z^+ \tag{A-20}$$

The upper bound (A-19) equals θ_{out} when

$$\theta_{slip} + \phi_0 = w^+ \tag{A-21}$$

For the case of f_s slightly less than f_r, similar bounds can be constructed to the f_s slightly greater than f_r case. The result of both sets of bounds is that for f_s close to f_r, θ_{out} is bounded as given in (2-20).

As was mentioned in Section 2.5, f_s needs to remain sufficiently close to f_r so that the magnitude of Δ_{max} is less than $\frac{1}{l}$. Setting Δ_{max} equal to some fraction of $\frac{1}{l}$, γ (2-24) it is possible from (A-16) to obtain f_{smin} (2-22) and f_{smax} (2-23) which identify the operating range for f_s (2-21).

A.4. INSTANTANEOUS ERRORS

Considering the case of f_s slightly greater than f_r, and p equal to one. The spaces between the θ^i_{init} deviate from the ideal $\frac{1}{l}$ and are as follows

$$\theta^i_{init} \text{ to } \theta^{i+1}_{init} = \frac{1}{l} + \delta \qquad i \in [0, 1, \ldots, l-2] \tag{A-22}$$

$$\theta^{l-1}_{init} \text{ to } \theta^0_{init} = \frac{1}{l} - (l-1)\delta \tag{A-23}$$

Where δ in this section is defined for the generalized sampling rate (see Section 2.6):

$$\delta \equiv \frac{l - p\eta}{\eta l}\left(1 - \frac{f_s}{f_r}\right) \tag{A-24}$$

These unevenly spaced θ^i_{init} cause the slip event instants to be unevenly spaced in time. These unevenly spaced slip event instants are illustrated in Figure A-3. The first error to occur for f_s slightly greater than f_r, is the reporting of $\lfloor N_{ave} \rfloor$-1. The frequency f_{smax1} (2-37) at which the reporting of $\lfloor N_{ave} \rfloor$-1 will just start to occur can be found by solving the following equation for f_{smax1}.

$$\frac{(\lfloor N_{ave} \rfloor - 1)\left(\frac{1}{l} + \delta\right) + \frac{1}{l} - (l-1)\delta}{f_{cmp} - f_{smax1}} = \frac{k}{f_c} \tag{A-25}$$

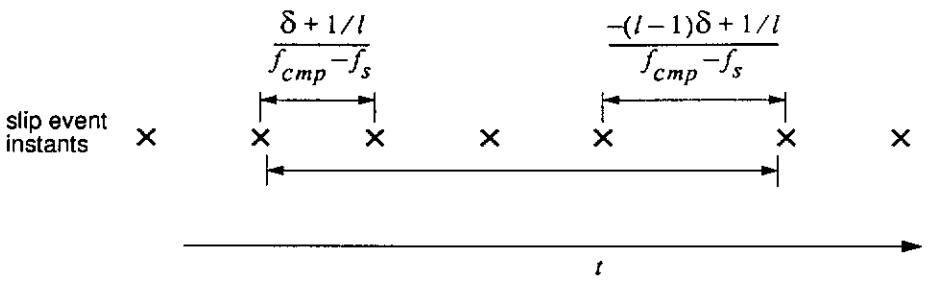

Figure A-3. Unevenly spaced slip events causing instantaneous measurement error

(A-25) is obtained by noting that the reporting of $\lfloor N_{ave} \rfloor$-1 slip events starts to occur when the period $\frac{k}{f_c}$ just falls inside $\lfloor N_{ave} \rfloor$+1 slip event instants. The spaces between these $\lfloor N_{ave} \rfloor$+1 slip events will be as follows: $\lfloor N_{ave} \rfloor$-1 spaces of (A-22) and one space of (A-23).

$$\lfloor N_{ave} \rfloor = N_{nom} - 1 \tag{A-26}$$

Equation (A-25) can be simplified by employing (2-11), (2-28), (2-29), (A-24), (A-22), (A-23) and assuming (A-26)

$$(k\eta - 2l - 1)\frac{f_r - f_{smax1}}{\eta f_c} - \frac{1}{l} = k\frac{f_r - f_{smax1}}{f_c} \tag{A-27}$$

from which f_{smax1} can be found (2-37).

For the case of f_s slightly less than f_r, and p equal to one, the spaces between the θ^i_{init} will be as given in (A-22) and (A-23), note that δ is positive for f_s less than f_r. In a similar manner to the f_s slightly greater than f_r case, the frequency f_{smin1} (2-38) can be found.

For the cases where p is greater than one, the ordering of the θ^i_{init} is somewhat more complex than the p equal one case. But, with p chosen according to (2-39) the spaces between the θ^i_{init} can be readily found. Again they deviate from the ideal $\frac{1}{l}$ and are as follows

$$\theta_{init}^{i} \; to \; \theta_{init}^{\frac{(p-1)l+1}{p}+i} = \frac{1}{l} + \frac{(p-1)l+1}{p}\delta \qquad i \in [0, 1, \ldots, r-1] \qquad \text{(A-28)}$$

$$\theta_{init}^{\frac{(p-i)l+i}{p}+j} \; to \; \theta_{init}^{\frac{(p-i-1)l+i+1}{p}+j} = \frac{1}{l}\frac{(l-1)}{p}\delta \qquad \text{(A-29)}$$

$$i \in [1, 2, \ldots, p-1], \quad j \in [0, 1, \ldots, r-1]$$

$$\theta_{init}^{r} \; to \; \theta_{init}^{0} = \frac{1}{l}\frac{(l-1)}{p}\delta \qquad \text{(A-30)}$$

These unevenly spaced θ_{init}^{i} again cause the slip event instants to be unevenly spaced in time. Employing (2-10), (2-11), (2-13), (2-28), (A-24), (A-28), (A-29) and (A-30) the frequency f_{smaxp} (2-40) can be found.

In a similar manner to the f_s slightly greater than f_r case, the frequency f_{sminp} (2-41) can be found.

A.5. PDFD OPERATION FOR TIME VARYING FREQUENCY

The derivations presented in this section extend the principle finding of Chapter 2 to the case of the signal square wave frequency being a function of time $f_s(t)$. It is shown here that if the function $f_s(t)$ is bounded as follows

$$f_{smin} \le f_s(t) \le f_{smax} \qquad \text{(A-31)}$$

with f_{smin} and f_{smax} as given by (2-22)(2-23), (2-30)(2-31), or (2-34)(2-35). Then the PDFD characteristic (2-15) relating θ_{out} to θ_{slip} will be bounded by the two quantizer functions given in (2-20).

This section is organized as follows: Firstly the operation of the simple frequency detectors is derived in Section A.5.1. Then in Section A.5.2 the entire PDFD, consisting of an array of simple frequency detectors is described.

A.5.1. Simple Frequency Detector Operation

Here key equations equivalent to (2-7), (2-10) of Chapter 2, describing the simple frequency detector operation, are derived. As in the constant $f_s(t)$ case, a simple frequency detector that uses every sample of the signal square wave is presented first. This derivation of the simple frequency detector which uses every sample provides a base for the more complex derivation of the simple frequency detector which uses every k^{th} sample.

Simple Frequency Detector using every Sample. Consider the phasor diagram of Figure A-4. A signal phasor representing the signal square wave is indicated by a solid vector in Figure A-4. A sampling phasor representing the sampling process is shown with a dashed vector. The phasors are shown at time t=0.

In this appendix we adopt the convention that phasors rotate once around the unit circle when their phase increases by one. This convention is consistent with the way the phase of a square wave was defined in Chapter 2 (2-2).

Each time the sampling phasor passes through the origin or zero point a sample instant occurs and a sample is taken.

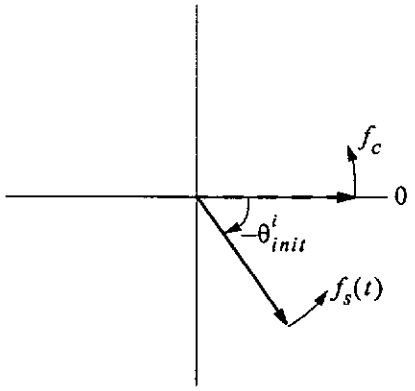

Figure A-4. Phasor diagram for Simple Frequency Detector using every sample

The actual waveform sampled is a divided by two in frequency version of the signal square wave. As the signal phasor passes through the origin or zero point, the waveform which will be sampled is toggled from zero to one or visa versa.

As previously described a slip event occurs when two samples have the same value. Two samples having the same value will occur if the sampling phasor overtakes the signal phasor between the two sample instants.

The time instants t_m at which the sampling phasor overtakes the signal phasor can be found to be:

$$t_m = \frac{m - \theta^i_{init} + \theta_s(t_m)}{f_c}, \qquad m \in Z^+ \tag{A-32}$$

Where

$$\theta_s(t_m) = \int_0^{t_m} f_s(x)dx \tag{A-33}$$

Slip events will be reported on the sampling instants following the time instants t_m given in (A-32).

Simple Frequency Detector using every k^{th} Sample. Consider the phasor diagram of Figure A-5. Again, the signal phasor is indicated by a solid vector in Figure A-5. A phasor representing the sampling process is shown with a dashed vector. The phasors are shown at time t=0.

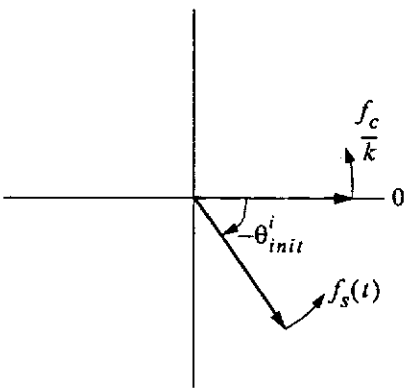

Figure A-5. Phasor diagram for Simple Frequency Detector using every k^{th} sample

Note that the sampling phasor now rotates at frequency $\frac{f_c}{k}$. Each time the sampling phasor passes through the origin a sample instant occurs and a sample is taken.

Again, the actual waveform sampled is a divided by two in frequency version of the signal square wave.

We will assume at this point that $f_s(t)$ is bounded as follows:

$$f_c\left(1-\frac{p+1}{k}\right)<f_s(t)<f_c\left(1-\frac{p}{k}\right) \tag{A-34}$$

With $f_s(t)$ bounded as in (A-34) the signal phasor will do $k-p-1$ full rotations plus a fraction of a rotation, denoted θ_{frac} in $\frac{k}{f_c}$ seconds. This θ_{frac} is found to be

$$\theta_{frac} = \int_0^{\frac{k}{f_c}} f_s(t)-\frac{f_c(k-p-1)}{k}dt \tag{A-35}$$

As far as the sampling process is concerned, the signal phasor can be considered equivalent to a phasor which rotates only θ_{frac} in $\frac{k}{f_c}$ seconds. That is a phasor with instantaneous frequency:

$$f_s(t)-f_c\left(1-\frac{p+1}{k}\right) \tag{A-36}$$

This lower frequency phasor will be called the fractional phasor.

As in the case of the simple frequency detector using every sample; Each time the signal phasor passes through the origin the waveform which will be sampled is toggled from zero to one or visa versa. Between sample instants the waveform to be sampled will toggle at least $k-p-1$ times, as the signal phasor does $k-p-1$ full rotations in $\frac{k}{f_c}$ seconds. If the sampling phasor overtakes the fractional phasor between sampling instants then the waveform to be sampled will toggle only $k-p-1$ times between sampling instants. Otherwise, if the sampling phasor does not overtake the fractional phasor the waveform to be sampled will toggle $k-p$ times between sampling instants.

It should be noted that sampling phasor always rotates faster than the fractional phasor as with $f_s(t)$ bounded as in (A-34), the following is true:

$$0 < f_s(t) - f_c\left(1 - \frac{p+1}{k}\right) < \frac{f_c}{k} \tag{A-37}$$

The time instants t_m at which the sampling phasor overtakes the fractional phasor can be found to be:

$$t_m = \frac{m - \theta^i_{init} + \theta_s(t_m)}{f_{cmp}} \tag{A-38}$$

For the simple frequency detector using every k^{th} sample, a slip event is said to have occurred when:

- Case $k-p$ *even*, when two consecutive samples have *different* values
- Case $k-p$ *odd*, when two consecutive samples have the *same* values

These slip events will be reported on the sample instants following the time instants t_m defined in (A-38).

The definition of slip events given above is consistent with the definition of slip events for the modified simple frequency detector of Chapter 2, Section 2.3.

A.5.2. The Array of Simple Frequency Detectors

As was explained in Chapter 2 the PDFD consists of a phased array of these simple frequency detectors.

Assume simple frequency detector 0 starts operation at time $t = 0$. The other simple frequency detectors will start at progressively later times. Let the start time for simple frequency detector i be denoted t^i_s.

The total number of slip events that will have been reported after the n^{th} reporting period of the PDFD by a particular simple frequency detector can be found from (A-38)

$$\left\lfloor \frac{f_{cmp} nk}{f_c} - \left(\theta_s\left(\frac{nk}{f_c} + t_s^i\right) - \theta_s(t_s^i) \right) + \theta_{init}^i \right\rfloor \tag{A-39}$$

Define an average signal square wave frequency $\bar{f}_s$ as follows:

$$\bar{f}_s = \frac{\theta_s\left(\frac{nk}{f_c}\right)}{\frac{nk}{f_c}} \tag{A-40}$$

For every simple frequency detector i the accumulated reported slip events given in (A-39) can be written as

$$\left\lfloor \frac{nk}{f_c}(f_{cmp} - \bar{f}_s) + \theta_{init}^i - \Delta_f^i \right\rfloor \tag{A-41}$$

Where

$$\Delta_f^i = \theta_s\left(\frac{nk}{f_c} + t_s^i\right) - \theta_s\left(\frac{nk}{f_c}\right) - \theta_s(t_s^i) = \int_{\frac{nk}{f_c}}^{\frac{nk}{f_c} + t_s^i} f_s(x)dx - \int_0^{t_s^i} f_s(x)dx \tag{A-42}$$

Assume the sampling frequency f_c and/or l sampling instants used have been chosen to obtain uniformly distributed θ_{init}^i when $f_s(t)$ equals f_r. (see Chapter 2, Section 2.5). With $f_s(t)$ not equal to f_r the θ_{init}^i will be perturbed from their nominal values. Each θ_{init}^i will be perturbed from its nominal position by $\Delta(\theta_{init}^i)$.

$$\Delta(\theta_{init}^i) = \int_0^{t_s^i} f_r - f_s(x)dx \tag{A-43}$$

Furthermore

$$\Delta(\theta^i_{init}) - \Delta^i_f = \int_{\frac{nk}{f_c}}^{\frac{nk}{f_c}+t^i_s} f_r - f_s(x)dx \tag{A-44}$$

The accumulated reported slip events for simple frequency detector i (A-41) can also be written as

$$\left\lfloor \frac{nk}{f_c}(f_{cmp} - \bar{f}_s) + \theta^i_{fr} + (\Delta(\theta^i_{init}) - \Delta^i_f) \right\rfloor \tag{A-45}$$

Where θ^i_{fr} is the value of θ^i_{init} if $f_s(t)$ were exactly equals to f_r, that is θ^i_{fr} is the appropriate member of the set (2-14).

θ_{out} can now be obtained:

$$\theta_{out} = \frac{1}{l}\sum_{i=0}^{l-1} \left\lfloor \theta_{slip} + \theta^i_{fr} + (\Delta(\theta^i_{init}) - \Delta^i_f) \right\rfloor \tag{A-46}$$

where

$$\theta_{slip} = \frac{nk}{f_c}(f_{cmp} - \bar{f}_s) = \frac{nkf_{cmp}}{f_c} - \theta_s\left(\frac{nk}{f_c}\right) \tag{A-47}$$

In a manner similar to that given in Section A.3 θ_{out} can be shown to be bounded by two quantizers:

$$\frac{\left\lfloor l(\theta_{slip} + \phi_0 - |\Delta_{max}|) \right\rfloor}{l} \le \theta_{out} \le \frac{\left\lfloor l(\theta_{slip} + \phi_0 + |\Delta_{max}|) \right\rfloor}{l} \tag{A-48}$$

Where Δ_{max} is defined here to be the maximum of the right most term in the floor function of (A-46), that is

$$\Delta_{max} = \max_i \left|\Delta(\theta^i_{init}) - \Delta^i_f\right| \tag{A-49}$$

By setting Δ_{max} to some fraction γ of $1/l$, as was done in Chapter 2, the range of frequencies around f_r which $f_s(t)$ can be in can be found (A-31).

From (A-44) it can be seen that the largest $\left|\Delta(\theta^i_{init}) - \Delta^i_f\right|$ occurs when t^i_s is the greatest and $f_s(t)$ equals one of the frequency bounds f_{smin} or f_{smax}. The greatest value for t^i_s occurs for simple frequency detector $l-1$ and in Chapter 2 this particular t^i_s was denoted by T_{max}. So the largest value of $\left|\Delta(\theta^i_{init}) - \Delta^i_f\right|$ and hence Δ_{max} is given by

$$\Delta_{max} = T_{max}(f_r - f_{smin}) = T_{max}(f_{smax} - f_r) \qquad \text{(A-50)}$$

Hence from (A-50) the frequency bounds f_{smin} and f_{smax} can be determined in the same manner as in Chapter 2.

In summary, with $f_s(t)$ bounded as in (A-31), the PDFD characteristic will be bounded by the two quantizer functions given in (A-48) and (2-20) of Chapter 2.

B

Eigenfunctions of Fokker-Planck Operator

B.1. INTRODUCTION

This appendix contains details relating to the non-linear behaviour of the SFPLL in noise (Chapter 3).

A numerical method called the Matrix Eigenvalue Approach [36][56][57][58] is employed to obtain the eigenvalues and eigenfunctions of the Fokker-Planck operator of the imperfect integrator PLL. From the eigenfunctions the stationary probability density functions (PDF) of the state variables (θ_ε , x_l) can be obtained. Importantly, the eigenvalues provide information on the cycle slip rate of the PLL, which is the most important single performance measure.

For a description of the Matrix Eigenvalue Approach [36] should be consulted. Presented in this appendix are some imperfect integrator PLL specific derivations, necessary to employ the Matrix Eigenvalue Approach.

B.2. FOKKER-PLANCK OPERATOR

From (3-36), (3-37) , results presented in [36] and with the assumption

$$g'(\theta_\varepsilon) = \sin(\theta_\varepsilon) \tag{B-1}$$

, the Fokker-Planck operator L for the imperfect integrator PLL can be found to be

$$L = \frac{\partial}{\partial\theta_\varepsilon}\left((2\zeta_l-\beta)\sin\theta_\varepsilon + x_l - \frac{\Delta\omega}{\omega_{nl}}\right) - (1-2\zeta_l\beta+\beta^2)\sin\theta_\varepsilon\frac{\partial}{\partial x_l} + \beta\frac{\partial}{\partial x_l}(x_l) \qquad \text{(B-2)}$$
$$+\gamma\frac{(2\zeta_l-\beta)^2}{2}\frac{\partial^2}{\partial\theta_\varepsilon^2} - \gamma(2\zeta_l-\beta)(1-2\zeta_l\beta+\beta^2)\frac{\partial^2}{\partial\theta_\varepsilon\partial x_l} + \gamma\frac{(1-2\zeta_l\beta+\beta^2)^2}{2}\frac{\partial^2}{\partial x_l^2}$$

Where

$$\Delta\omega = \omega_i - \omega_{fl} \qquad \text{(B-3)}$$

$$\gamma = \frac{1}{\rho\zeta_l\left(1-\frac{\beta}{\zeta_l}+\frac{1+\beta^2}{4\zeta_l^2}\right)} \qquad \text{(B-4)}$$

and ρ is the signal to noise ratio in the loop [36].

Employing the set of base functions recommended in [36]

$$\{z_n(\theta_\varepsilon)\} = \left\{\exp\left(j\frac{n}{M}\theta_\varepsilon\right)\right\} \qquad \text{(B-5)}$$

$$\{h_m(x_l,\alpha)\} = \left\{\frac{1}{\left[(2\alpha)^m m!\sqrt{\frac{\pi}{\alpha}}\right]^{1/2}}\exp\left(-\alpha\frac{x_l^2}{2}\right)H_m(x_l,\alpha)\right\} \qquad \text{(B-6)}$$

With the functions H_m being closely related to the Hermite polynomials [59].

$$H_m(x_l,\alpha) = (-1)^m\exp(\alpha x_l^2)\frac{\partial^m}{\partial x_l^m}\exp(-\alpha x_l^2) \qquad \text{(B-7)}$$

The image $z_n(\theta_\varepsilon)h_m(x_l,\alpha)$ is found to be

$$
\begin{aligned}
L[z_n(\theta_\varepsilon)h_m(x_l,\alpha)] = {} & \frac{E}{2j}\sqrt{\frac{\alpha m}{2}}z_{n-M}(\theta_\varepsilon)h_{m-1}(x_l,\alpha) \\
& -D\frac{n-M}{2M}z_{n-M}(\theta_\varepsilon)h_m(x_l,\alpha) \\
& -\frac{E}{2j}\sqrt{\frac{\alpha(m+1)}{2}}z_{n-M}(\theta_\varepsilon)h_{m+1}(x_l,\alpha) \\
& +\frac{\sqrt{m(m+1)}}{2}\left(\beta+\frac{E^2\alpha\gamma}{2}\right)z_n(\theta_\varepsilon)h_{m-2}(x_l,\alpha) \\
& +j\frac{n}{M}\left(\sqrt{\frac{m}{2\alpha}}-\gamma\frac{DE}{2}\sqrt{2\alpha m}\right)z_n(\theta_\varepsilon)h_{m-1}(x_l,\alpha) \\
& +\left(\frac{\beta}{2}-\gamma\frac{D^2}{2}\left(\frac{n}{M}\right)^2-\alpha\gamma\frac{E^2}{4}(2m+1)-j\frac{\Delta\omega}{\omega_{nl}}\frac{n}{M}\right)z_n(\theta_\varepsilon)h_m(x_l,\alpha) \\
& +j\frac{n}{M}\left(\sqrt{\frac{m+1}{2\alpha}}+\gamma\frac{DE}{2}\sqrt{2\alpha(m+1)}\right)z_n(\theta_\varepsilon)h_{m+1}(x_l,\alpha) \\
& +\frac{\sqrt{(m+1)(m+2)}}{2}\left(-\beta+\frac{E^2\alpha\gamma}{2}\right)z_n(\theta_\varepsilon)h_{m+2}(x_l,\alpha) \\
& -\frac{E}{2j}\sqrt{\frac{\alpha m}{2}}z_{n+M}(\theta_\varepsilon)h_{m-1}(x_l,\alpha) \\
& +D\frac{n+M}{2M}z_{n+M}(\theta_\varepsilon)h_m(x_l,\alpha) \\
& +\frac{E}{2j}\sqrt{\frac{\alpha(m+1)}{2}}z_{n+M}(\theta_\varepsilon)h_{m+1}(x_l,\alpha)
\end{aligned}
\tag{B-8}
$$

Where for convenience

$$D = 2\zeta_l - \beta \tag{B-9}$$

$$E = 1 - 2\zeta_l\beta + \beta^2 \tag{B-10}$$

With (B-8) the eigenvalues and eigenfunctions of the Fokker-Planck operator (B-2) can be found by the Matrix Eigenvalue Approach outlined in [36].

C

Development of a BRM Based Digital Filter

In this appendix a Binary Rate Multiplier (BRM [55]) based digital filter that has one pole is developed. The digital filter is employed in the SFPLL implementation given in Chapter 6.

BRMs take an n bit binary number, B (between 0 and 2^n-1), and produce an output pulse stream which has a ratio of ones to zeros given by

$$\frac{B}{2^n} \tag{C-1}$$

n is related to N_p

$$N_p = 2^n \tag{C-2}$$

A single pole system with input $u(t)$, and output $y(t)$ is described by the following differential equation

$$dy = \omega_p u(t)dt - \omega_p y(t)dt \tag{C-3}$$

A system of integrators and BRMs that implements (C-3) is shown in Figure 6-3. The BRM based system runs off a clock of period $N_w 2\pi/\omega_o$. The integrator block accumulates the n bit value $y(t)$, which is then fed into a BRM to produce the output pulse stream. The integrator block is implemented with an up down counter. The pulse stream from the frequency detector forms the input $u(t)dt$. The fractional multiplier ω'_p is assigned a value (C-6) so that the BRM based system has an identical time response as the system described in (C-3).

ω'_p is determined as follows. For the continuous time system, from (C-3), in time dt seconds $y(t)$ is reduced by

$$\omega_p y(t)dt \tag{C-4}$$

In the BRM system, $y(t)$ is reduced by $\omega'_p y(t)$ when $\omega'_p y(t)$ pulses leave BRM B. For $\omega'_p y(t)$ pulses to leave BRM B requires $y(t)$ pulses to be input to BRM B. To input $y(t)$ pulses requires 2^n clocks (n is the length of BRM C), which is a time of $2^n N_w 2\pi/\omega_o$ seconds.

In the BRM system dt seconds corresponds to $dt/(2^n N_w 2\pi/\omega_o)$ cycles of BRM C and hence in dt seconds $y(t)$ is reduced by

$$\omega'_p y(t)\frac{dt}{2^n N_w \frac{2\pi}{\omega_o}} \tag{C-5}$$

Equating (C-4) and (C-5) and substituting in (C-2) obtain

$$\omega'_p = \omega_p N_p N_w \frac{2\pi}{\omega_o} \tag{C-6}$$

The output of the frequency detector is in pulse rate form and is fed directly into the system as $u(t)dt$. Every increment in $y(t)$ produces $1/\omega'_p$ pulses at the system output, before that increment in $y(t)$ is nullified by a pulse at the negative input of the integrator block. To produce an increment in $y(t)$ requires $1/\omega'_p$ pulses from the frequency detector. The pulse spreading scheme requires that N_s pulses be generated from every frequency detector pulse though. N_s pulses from every frequency detector pulse can be achieved by either multiplying the input pulse rate by N_s. Or simply changing the fractional multiplier of BRM A ω'_p to $\omega'_p N_s$, that is don't divide by so much. The latter is the more preferable method, as no extra hardware is required. Though because the new fractional multiplier must be less than or equal to one, a new constraint is created:

$$\omega'_p N_s \leq 1 \tag{C-7}$$

From (C-6) and (C-7) the following relating N_p to other system parameters is obtained

$$N_p \leq \frac{\omega_o}{2\pi N_s N_w \omega_p} \tag{C-8}$$

If

$$\omega'_p N_s = 1 \tag{C-9}$$

then BRM A is eliminated and the frequency detector output is fed directly into the integrator. In general, as N_p has to be a power of two ω_p will have to be modified to satisfy (C-9)

$$\omega_p = \frac{\omega_o}{2\pi N_s N_w N_p} \tag{C-10}$$