Boost Rectifier Power Factor Correction Circuits with Improved Harmonic and Load Voltage Regulation Responses

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***Abstract* – The time domain step response for rapid load changes can be improved in boost type power factor correction circuits by using a capacitor voltage model. In single phase PFC circuits, the dc bus voltage must have a significant voltage ripple at twice the mains frequency due to energy balance requirements. In traditional implementations, the presence of this ripple voltage causes a trade-off between line current wave shape and speed of the dc output regulatory response. The capacitor voltage model provides a ripple free estimate of the storage capacitor voltage. This allows the bandwidth of the dc bus voltage regulation loop to increase without causing a degradation of line current wave shape. Simulations show that the dc regulatory response is complete within one mains cycle and significant reductions in voltage over and under-shoots are achieved.**

***Keywords* – Power factor correction, boost rectifier, model referenced control.**

I. INTRODUCTION

Boost rectifier power factor correction circuits are intensively applied and have been extensively studied, [1, 2]. The focus of the majority of publications has been upon the control of an inner current loop which determines the line current wave shape. Much less attention has been given to the dynamic response of the converter output voltage. The boost power factor correction circuit commonly uses an electrolytic DC bus capacitor to provide low frequency energy storage and that capacitor must exhibit a significant voltage ripple at twice the mains frequency.

The storage capacitor voltage is regulated by adjusting the magnitude of the line current that is drawn by the boost stage. Resistive emulation, controlling the converter to draw a line current proportional to voltage, is common. Two approaches, the voltage follower approach or the multiplier approach are popular, [3]. The voltage follower approach relies on an inductor peak or average current being proportional to the volt second product applied by the line voltage during a switching period. This method can be current sensor free. The multiplier approach normally uses an explicit current control loop and is used at higher powers. An output capacitor voltage controller responds to the voltage error and drives a multiplier to produce a current demand signal that tracks the supply wave shape. This is in turn is applied to the inner current control loop. Fuzzy mode controllers have also been proposed as the voltage regulation element, [4]. The control loop design must balance two conflicting needs:

- The need to respond rapidly to changes in capacitor voltage on the application of load and especially on the removal of load to avoid unnecessary voltage stress on the storage capacitor;
- The need to provide a power demand signal that is free from ripple frequency components, as that signal is used to generate a current reference signal for an inner control loop and fed back ripple increases harmonic distortion in the converter input current.

This paper proposes the use of a capacitor current balance model to provide a ripple free estimate of the storage capacitor voltage which can be used as an input to a high bandwidth voltage regulation loop. This allows very high speed responses to load changes and tighter control of the capacitor voltage while maintaining high quality line current inputs. Responses are effectively complete within one half cycle of the mains supply and this is a significant improvement on past designs where response times of five to ten cycles occur.

The paper presents a continuous mode, three-way interleaved boost converter with an improved predictive current control method. The target application area is single phase power converters of a few kilowatts rating as may be applied for UPS battery charging or single phase input variable speed drive systems for heat pumps and air conditioners. In these applications a digital signal processor such as the TMS320F2808 or other high end microcontrollers can be readily justified as a control device.

II. PREDICTIVE CURRENT CONTROL

Many current control methods can be applied based on current mode control, average current control, [6], sliding controls [7], one cycle control [8] or variations on these, [9]. Each of the three boost cells uses an inner most loop with a digital predictive current controller, [10], which has been applied in PWM bridge rectifier applications. The basic principles are:

- The boost inductor current, the DC bus voltage and input diode rectifier voltage are sampled at the beginning of each control period, in this case the control period is 12.5μS;
- At the beginning of the control period the actual inductor current is subtracted from a current reference to give a current error;
- The current error signal is multiplied by the inductor value to give a volt-second product to be applied during the control period to force the inductor current error to zero;
- The volt-second product is used with a knowledge of the diode rectifier voltage and the DC bus voltage to determine the duty cycle during the control period.

III. Interleaved Boost Converter

Figure 1 shows a three way interleaved boost rectifier. The cells switch at 80kHz and the converters are phase displaced to achieve ripple cancellation. Each stage has a dedicated predictive current controller as an inner loop. An average mode controller is overlaid as a second current control mechanism. As with peak current mode controls the predictive method will produce a small amount of harmonic distortion as the end point current rather than the average current is controlled, [6].

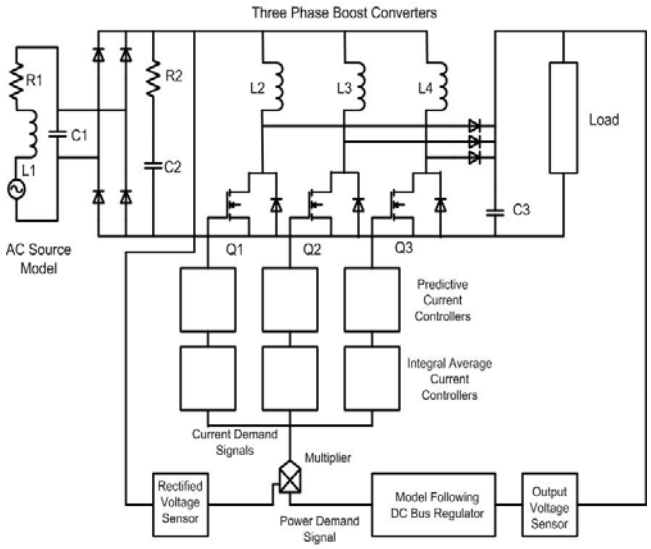

Fig 1. Boost Rectifier.

Resistive load emulation is applied by a common DC bus voltage regulator. This generates a power demand signal which is multiplied by the absolute value of the mains voltage to provide a shared current demand signals for each of the boost cells. Precise current sharing is forced by the individual current loops which act to maintain equivalent averaged currents in each of the boost converter phases.

IV. Sinusoidal Operation of the Boost Converter Stage

Initially, to illustrate the ripple cancellation effects of interleaving, the operation of the inner current loops is examined using simulation of a 3500W, 240Vrms, 50Hz input 400Vdc output rectifier. A reference signal equivalent to the full rating of the converter is applied. This is derived from the rectified mains voltage in the converter power circuit. The boost converter currents are seen in Figure 2. The boost inductors, L2 to L4, are each 200μH and the 80kHz ripple currents in each group, shown as the top three traces, are relatively high with a maximum value of 6.25App.

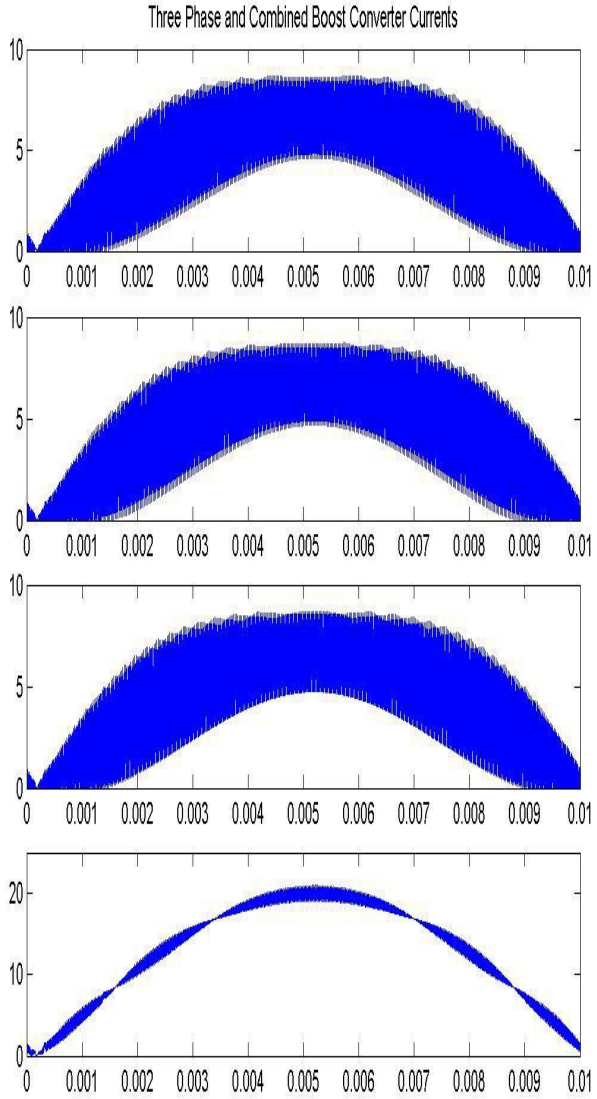

Fig 2. Boost Converter and Total Converter Group Current

Significant cancellation occurs in the group currents shown in the lower trace. Current ripple zeroes occur at one third and two thirds duty ratio. It is note worthy that the boost converters do operate in a discontinuous mode for a significant part of the mains cycle. This will cause a prediction error with the current control method but this is compensated for by the integral control of average inductor current.

In order to absorb the ripple frequency components RFI filters will be required. In combination with the mains impedance these pose a stability risk for the rectifier controls. The simulation model includes a series inductor resistor representation of the mains source impedance with 1Ω and 3.18mH, or 1 Ω inductive used in this case. This results in a 6% voltage drop at full load and would be at the upper end of what would be expected in terms of voltage regulation. Capacitor C1 is 4μF and represents the lumped sum of class X capacitors in any RFI suppression networks. Components R2 and C2, 50 Ω and 1 μF respectively, provide some small signal damping at the natural frequency of the mains impedance and the RFI capacitors. Additionally they provide an alternative ripple current path that avoids the rectifier diodes.

The selected control gains give a inner current control bandwidth of 100krad/s or approximately 15kHz. The inner loop removes the inductor from the small signal models and the loop dynamics are dominated by the controller integral response. This results in a first order system with good phase margins.

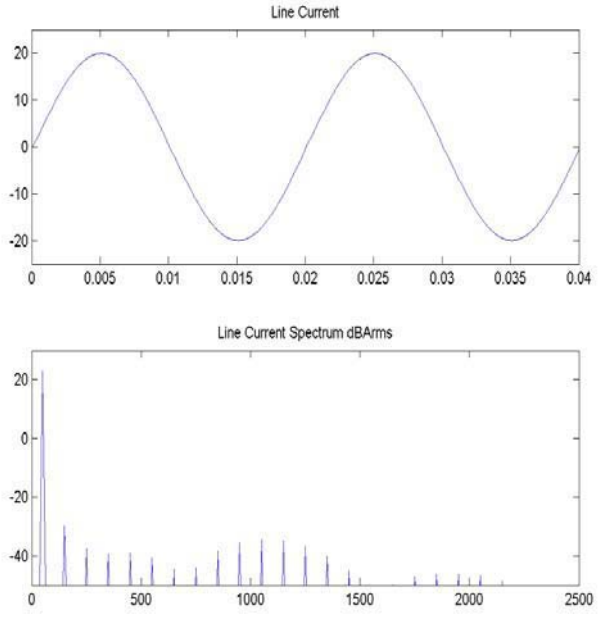

Fig 3. Line Currents under Sinusoidal Demand Signal Operation

Figure 3 shows the resulting line current wave shape for a current demand equivalent to full load or 20Ap. The third harmonic is 53dB down or 0.23%. This converter will mimic a resistive load and will draw harmonic current if the supply voltage waveform is distorted. This simulation does not include the effects of a DC bus voltage regulator which will significantly contribute to the overall line current distortion. As the voltage loop responds on a much slower time scale it is simulated separately using a continuous signal rather than a switching model for the internal current loops.

V. A Model Reference Approach to DC Bus Regulation

Systems using the multiplier approach adjust the peak value of the sinusoidal demand current applied to the line current regulator to adjust the rectifier input power. If the bandwidth of the voltage loop is increased the ripple voltage distorts the current reference giving rise to harmonic distortion. A slow voltage loop results in a good wave shape but has a poor dynamic response. Specifically, a step reduction of load will cause DC bus overshoots that can be damaging, especially when the DC bus uses electrolytic capacitors that have limited over-voltage margins.

Figure 4 shows a DC bus voltage regulator based on a capacitor voltage reference model. A similar approach has been proposed for PWM single phase boost rectifiers in railway applications, [10]. A current integration model generates an estimate of the capacitor voltage which has a greatly reduced ripple component.

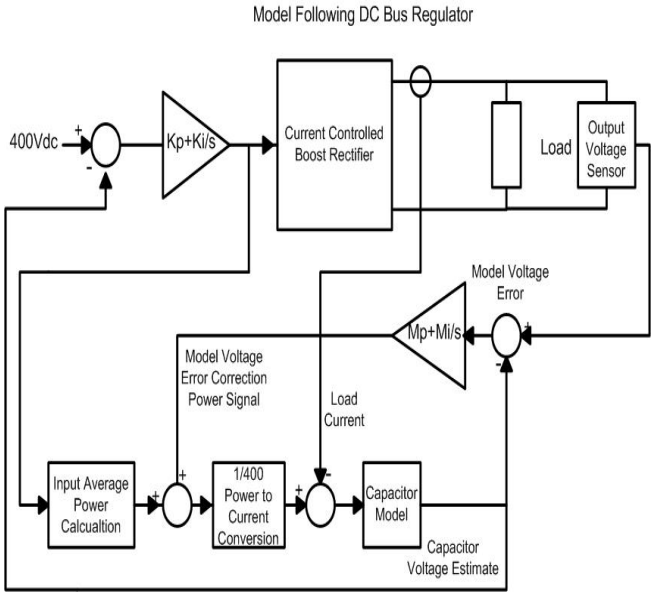

Fig 4. A Reduced Ripple Capacitor Voltage Model

The capacitor is modelled by an integrator that has the following inputs:

- A current term reflecting the average input power from the rectifier – in this case power is estimated using the RMS values of the mains voltage and current;
- The DC load current which may be measured directly or inferred from DC bus power;
- The model voltage and the actual capacitor voltage are held in alignment using a PI control that responds to the voltage tracking error.

Figure 5 shows the simulated step response of a system based on a capacitor voltage model. As the inner current loops have been shown to have a very high bandwidth the boost converter stages can be modelled by a controllable current source. This source delivers current to the capacitor equivalent to the average currents injected by the boost converters. From a zero load condition full load is applied at 0.1s and then removed at 0.3s.

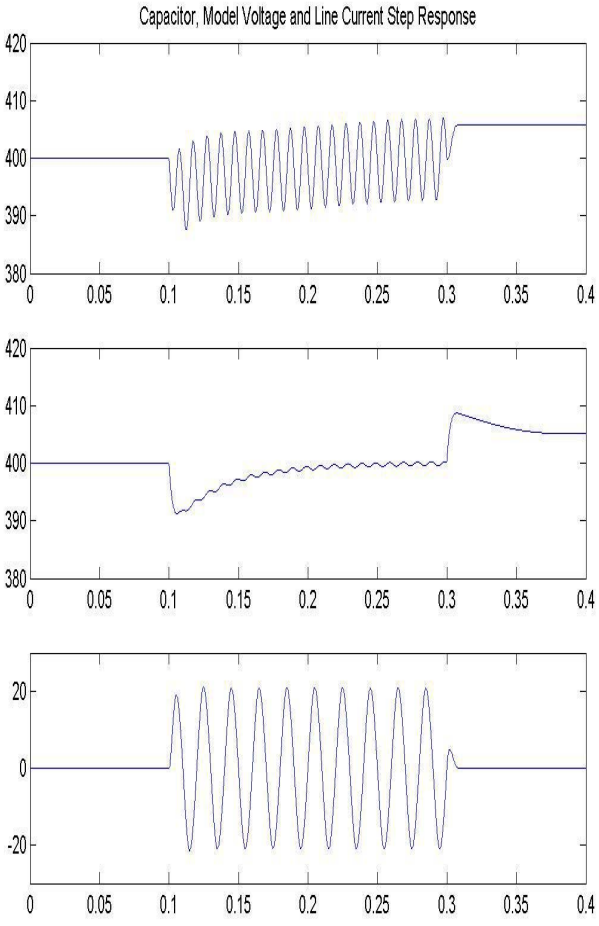

Fig 5. Response for a 100% Step Load Changes

The traces are:

- The actual capacitor voltage;
- The "reduced ripple" capacitor model voltage;
- Line current.

The voltage reduces on the application of the load current which occurs at a line current zero. It is not possible to extract real power from the incoming supply at this point in the cycle so a bus voltage fall is unavoidable. However the correct level of line current is nearly fully achieved by the next mains peak and the voltage drop of 10V is comparable to the normal ripple. On the removal of load the line current is extinguished in a fraction of a cycle and the DC bus overshoots by less than 10V. A Fourier analysis of the full load line current shows a THD of 1.7%. The parameters for the SIMULINK model are:

- Bus capacitor 2 000μF;
- Nominal voltage – 400Vdc;
- Load step 8.75 Adc or 3 500W;
- Kp=2; Ki=50; Mp=30; Mi=1000.

Figure 6 shows the same load step response in the absence of a capacitor voltage reference model. The storage capacitor voltage ripple will now adversely affect the line current regulators. Ripple voltages appear in the voltage error signals and this in turn forces ripples in the power demand signals. Ripple in the power demand signal generates harmonic distortion of the current demand waveforms. The speed of response has been approximately maintained but the voltage undershoot and overshoot have increased somewhat. The line current is visibly and unacceptably distorted with a THD of 25% and it is not possible to maintain the control loop gains due to this effect. By comparison, an earlier work using a standard PI regulation approach, [8], on a 120Vac 60Hz rectifier reported a response time of more than 10 cycles for a load step from 50% to 100% which resulted in a 60V drop on a nominal 240Vdc bus.

VI. Discussion

There are variations on this method that are potentially capable achieving comparable results. In regard to Figure 4, the estimation of the rectifier average power was made in this case using the input RMS current and voltages. An alternative may be to calculate instantaneous power by direct multiplication and then to extract a ripple moving average. Averaging over a period equivalent to a half mains cycle suppresses components at even multiples of the mains frequency. In this case the averaging period must track any mains frequency variations. This approach is unlikely to affect the overall stability of the system response as the filtering impacts are external to the current and voltage regulation loops.

VII. CONCLUSIONS

Single phase boost power factor correction circuits always operate with a degree of output voltage ripple due to the energy storage requirements of a single phase system. Many PFCs use a resistive emulation control approach where a sinusoidal template is multiplied by a power demand signal to develop a reference for current control loops. DC bus ripple voltages feed through the control system to corrupt the current demand signals directly causing unnecessary line current distortion. The use of a capacitor reference model that produces a ripple free indication of the dc bus voltage allows the trade off regulatory response time and line current wave shape to be avoided. Very rapid responses in current control and corresponding reductions in DC bus over shoots and undershoots have been demonstrated.

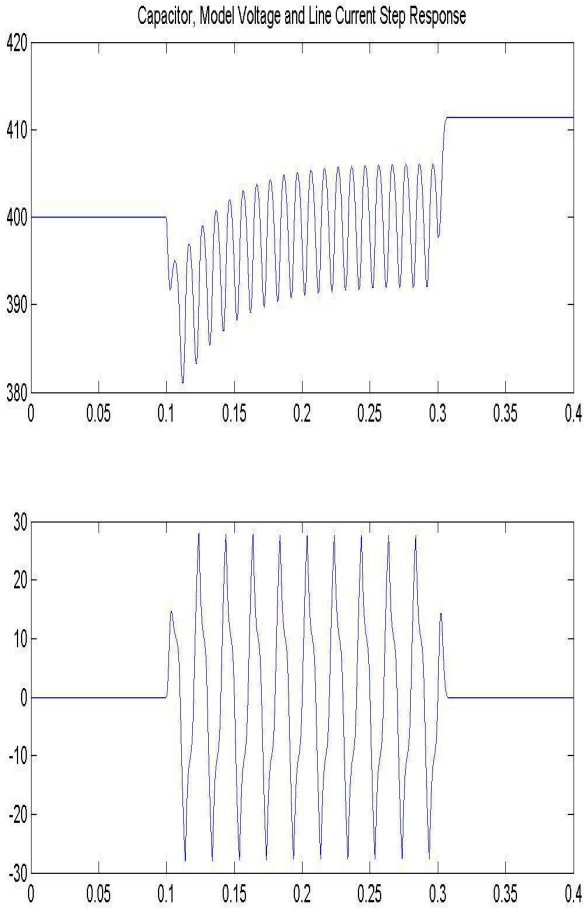

Fig 6. Load Step Response in the Absence of a Capacitor Voltage Model

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