DISTRIBUTED MAXIMUM POWER TRACKING FOR HIGH PERFORMANCE VEHICLE SOLAR ARRAYS

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Abstract

Recent advances in low voltage electronics make possible the development of maximum power tracking converters for single high performance solar cells. Application areas include vehicle arrays where curvature of the array may be significant or where dappled lighting by roadside vegetation or structures produces highly irregular and rapidly changing illumination. This paper will present a design for a high efficiency 600mW maximum power tracking converter for a single dual junction germanium gallium arsenide cell. Switching frequency and synchronisation guidelines for arrays of tens to hundreds of cells with individual cell power tracking are presented.

1. INTRODUCTION

Hybrid vehicle technologies, where an electrical drive is integrated into a petrol-powered vehicle to achieve fuel savings, are being widely embraced by many vehicle manufacturers, [1]. As hybrid vehicles include a significant electrical energy storage, most commonly batteries, it is relatively easy to extend the vehicle range by electric charging either from a road side source of power while parked. Hybrid and electric vehicles can significantly benefit from the inclusion of photovoltaics, [2], as an additional source of energy input. As the area available on vehicles is small, in comparison to the potential energy need, high efficiency cells are preferred. Dual and triple junction cells, while being expensive, achieve conversion efficiencies beyond 28%, [3, 4].

Vehicles must achieve a reasonable aerodynamic performance for reasonable energy efficiency and this drives a preference for curved surfaces. Array curvature combines with rapid illumination changes due to shading by road-side vegetation and structures to present significant challenges for the power management of solar arrays. The maximum power conditions of cells can vary rapidly. Individual cells can transition from full sun to full shade in 50mS. Little has been done to address maximum power tracking at these rates, [5,6]. Maximum power point tracking devices that are distributed at the single cell level can provide the best possible solution for array power optimisation, but only if MPPTs can be developed that offer high efficiency and moderate cost. Proposals exist for power tracking at a module level, [7, 8], but only one proposal exists to offer maximum power tracking at the cell level, [9]. This approach however requires an isolated converter to provide a current bypass around each cell.

This paper demonstrates that recent advances in low voltage electronics, combined with an array arrangement that allows multiple power trackers to share filter inductors makes, single cell maximum power tracking feasible.

2. POWER CONVERTER TOPOLOGY

Dual and triple junction cells have maximum power voltages of approximately 2.0V and 2.5V, [3,4]. A dual junction cell with a nominal current of 300mA yielding a maximum power of 600mW was selected as a target against which a design could be developed. A range of DC-DC converter topologies could be applied. Choices include:

- A direct converter, either buck or boost, that processes the entire cell output power to produce either a voltage or current compliant output allowing many cells and converters to be series or parallel connected.
- A direct converter, with voltage inversion, that allows series connected strings of cells to transfer energy from adjacent cells to achieve a maximum power point, [8].

A buck topology was selected allowing multiple cells, and their individual converters to be series connected as shown in Figure 1. A significant advantage of this arrangement is shown in Figure 2. The buck converter inductors are all effectively series connected and can be replaced by a single device yielding an inductorless converter package at the cell level.

The other approaches do not yield this advantage. A consequence is that the converter does process the entire cell power and this imposes an efficiency challenge, [8].

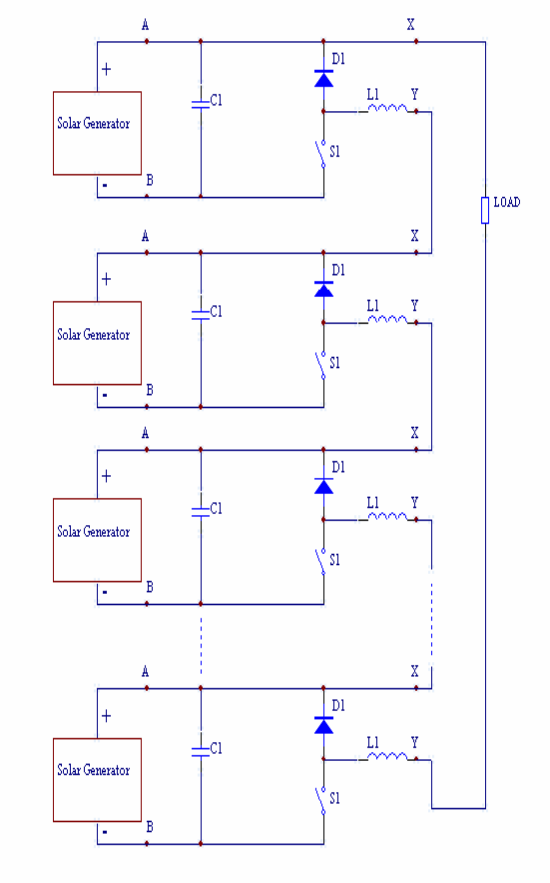

Figure 1. Series Connected Buck MPPTs

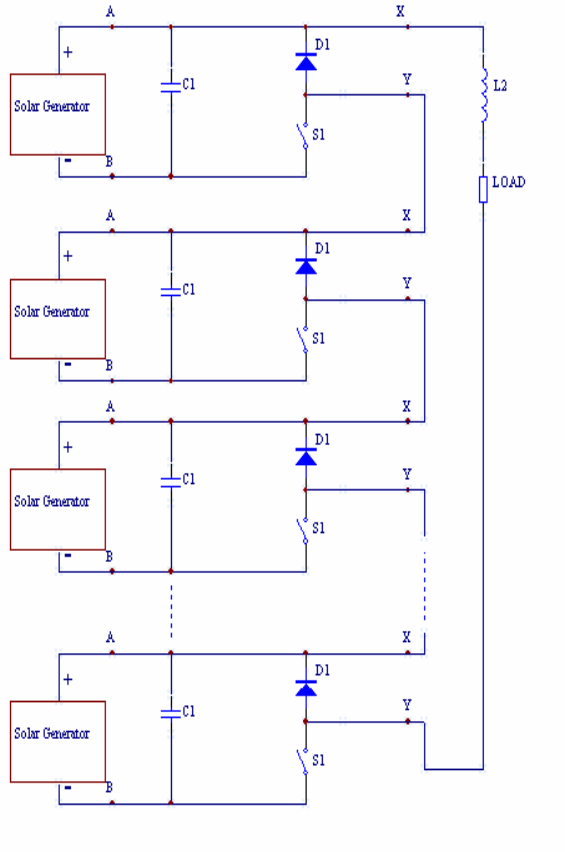

Figure 2. Inductorless Buck MPPTs.

3. MULTIPLE CELL OPERATION

A vehicle array will consist of several hundred cells arranged in series strings of 20 to (potentially) in excess of 200 cells. While it may be possible to synchronise the switching operations in many cells to achieve switching frequency elimination, this paper focuses on asynchronously switching cells. In order to secure high efficiency in the cell converters switching frequencies below 20kHz are desired. Gate charge losses are as significant as switching loss. Some asynchronous strategies can maximise efficiency by tailoring the switching strategy to optimise total converter losses.

The output voltage of large number of asynchronously switching series connected buck converters will follow a binomial distribution. The average output voltage of the group of n cells, with an input voltage V_{in} and a duty cycle d, increases linearly with n while the switching ripple or the distortion voltage, V_{dist}, rises as √n.

$$V_{dist} = V_{in}\sqrt{n(d-d^2)} \qquad (1)$$

Likewise the average volt second area, A, for a shared filter inductor follows a √n relationship.

$$A = \sqrt{n}\,\frac{V_{in}}{f}(d-d^2) \qquad (2)$$

Simulation studies were conducted with groups of n=10, n=25 and n=50 asynchronous cells with normally distributed switching periods with a mean of 100μS and with a standard deviation of 5μS. The input voltage to each converter was 2V and the duty ratio was set at 50%, the maximum distortion voltage case. Table 1 compares expected distortion voltages against those predicted by Equation 1.

For 50 converters, the typical output waveform of the group, without an inductor, is shown as Figure 2. A non-distributed approach produces a square wave of 50V average and 100V peak magnitude so substantial cancellation has been achieved. Figure 3 shows the combined voltage spectrum, individual lines can be related to individual converters, some evidence of reinforcement by random near synchronisation of a few converters is also seen.

N	DC Output (V)	Expected Distortion (V)	Measured Distortion (V)
1	1	1.00 (100%)	1.00
10	10	3.16 (31%)	3.16
25	25	5.00 (20%)	4.82
50	50	7.07 (14%)	6.99

Table 1. Distortion Voltages

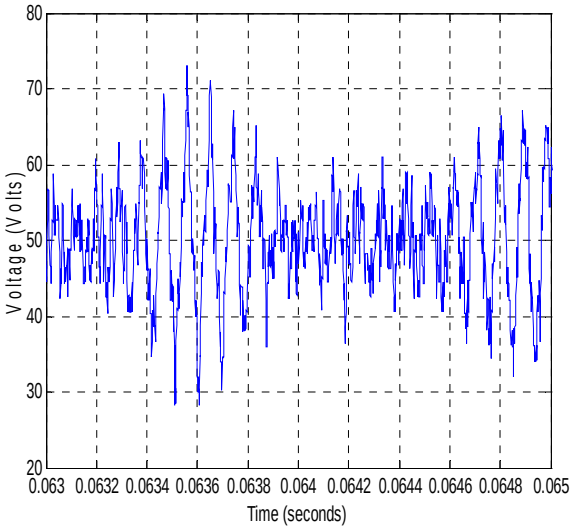

Figure 3. Typical output voltage waveform of group of 50 cells.

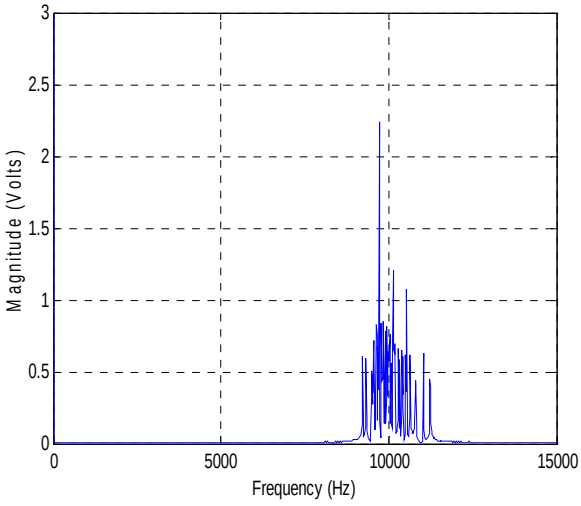

Figure 4. Output voltage spectrum of first switching band, 50 cells 10kHz.

4. CONVERTER DESIGN

The major control element is an ultra-low power Texas Instruments MSP430 microprocessor which is capable of operation from a 1.8V supply at currents of 250μA. This device performs duty cycle modulation and the maximum power tracking function using the cell voltage and the converter duty cycle to infer cell power. The converter schematic is shown as Figure 5.

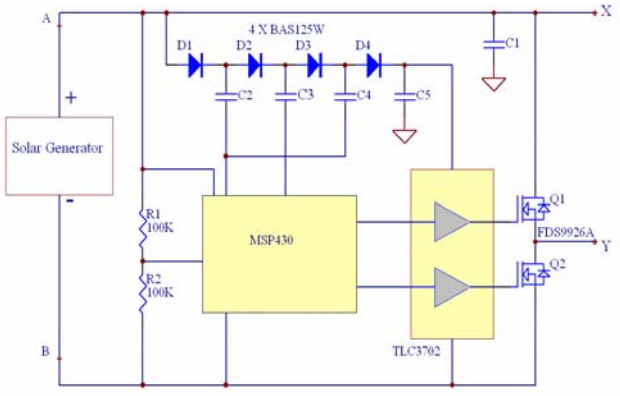

Figure 5. Single Cell MPT Converter

The buck converter MOSFET and synchronous rectifier are FDS9926A 20V, 6.5A, 30mΩ devices and are driven by a TLC 3702 comparator. These have V_{gs} specified at 2.5V and can achieve a solid turn on at low gate voltages and total gate charge of 5nC. The comparator has a 5.5V power supply from a charge pump circuit formed by diodes D_1 to D_4 and their associated capacitors. TLC 3702 has a CMOS output stage that allows it to reach the supply rails. The output stage will have an output characteristic that is resistive and controlled by the channel resistance of the output devices.

During experimentation it was discovered that the dead time, supply current trade off of the comparator is important, for this device delay time is 1μS and the no load current is 50μA. Capacitor C1 is five 22μF, 6.3 V ceramic chip capacitors by Murata, each has an ESR of 4mΩ.

Extreme care has held the projected total loss to around 15mW at 50% duty cycle, placing the conversion efficiency above 97% at 600mW input power. At 50% duty cycle the output current at 600mA is double the input current. Consequently the conduction losses are very high. In many situations the efficiency will be higher if the duty cycle is above 50% at Table 2 lists the estimated loss components at 20kHz. It may be possible to trade reduced conduction loss against increased gate charge loss.

Component	Loss
Microprocessor	0.4
Gate Drive	2
Switching Loss	2
MSOFET Conduction Loss	11
Total	15.4mW

Table 2. Converter Loss Estimates at 20kHz, 50% duty.

5. EXPERIMENTAL RESULTS

A prototype converter was developed to first examine the conversion efficiency of the DC to DC converter stage. For these tests the MSP340 was programmed to drive the charge pump circuitry and to operate the buck converter stage at a fixed 50% duty ratio. The experimental setup can be seen in Figure 6. A header board of MSP 430 is used as the controller. A fixed 2V input source voltage was applied and a load consisting of a 2 500µH inductor and a 1.6 Ω resistor was applied. A dead-time of 0.8µS is inserted in each turn-on and turn-off transient to prevent MOSFETs shoot through conduction events.

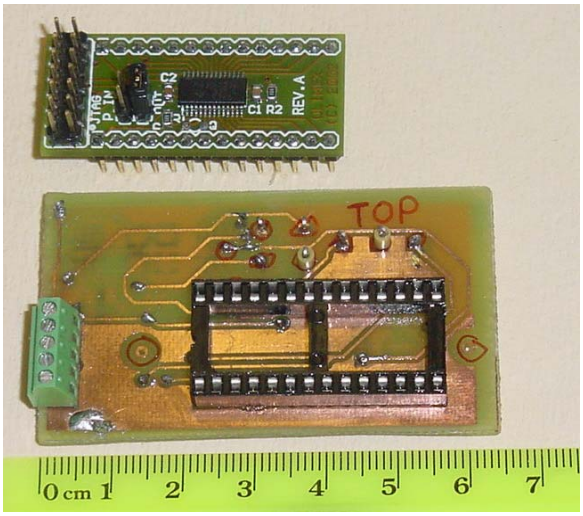

Figure 6. PCBs of the converter and controller.

5.1 Converter Waveforms

As gate loss was a significant loss contributor, a range of operating frequencies was trialled. Figure 7 shows the control waveforms at 20kHz. The waveforms show the dead times between the top and bottom signals at turn-on and turn-off. All waveforms in this figure are ground referred. The measured no load loss in this condition was 6mW which is approximately twice the expected figure. The gate drive loss is fully developed at no load and we may have additional loss in the charge pump circuitry. Figure 8 shows gate waveforms at 2kHz but a differential measurement is made of V_{gs1} to show the lowering of the gate source voltage to approximately 4V due to elevation of the source at the device turn-on.

The waveforms at 20 kHz without load are shown in Figure 9. Note that the load connection is across terminals X and Y. The lower MOSFET has the higher gate drive voltage and a lower R_{dson}. Figure 10 shows the loaded waveforms. Note the conduction of the MOSFET inverse diodes in the dead time as seen by the 2 µS wide peaks on the leading and trailing pulse top edges on the top trace. The transfer of current to these diodes generates an additional conduction loss of 24mW which reduces efficiency at higher frequencies.

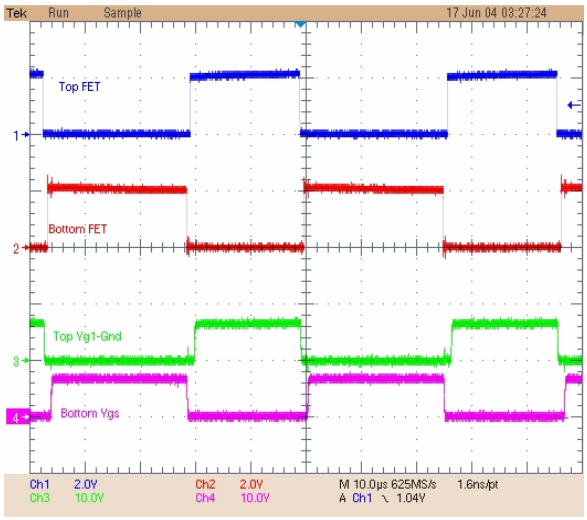

Figure 7. Control signals and gate signals for MOSFETs.

5.2 Efficiency measurement

Given circuit losses are around a few percentage points of rating, precise voltage and current measurements are needed if power measurements are used to determine efficiency. A complication is that the output is inductorless and both the output voltage and current contain significant switching frequency components. It is likely that a significant amount of power is transferred to the combined R-L load at frequencies other than DC. Calorimetry is a method of measuring power loss directly, and can be used for efficiency determination. However, the total power loss of this specific converter is too low to make a temperature change that is easy to measure. We are still working towards this approach.

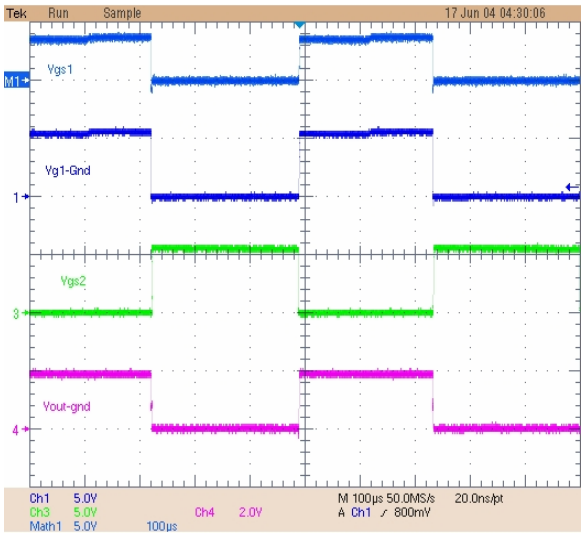

Figure 8. No load 2kHz waveforms, top MOSFET gate waveform; top MOSFET gate drive referred to ground, bottom MOSFET gate waveform to ground, output terminal to ground (from top to bottom).

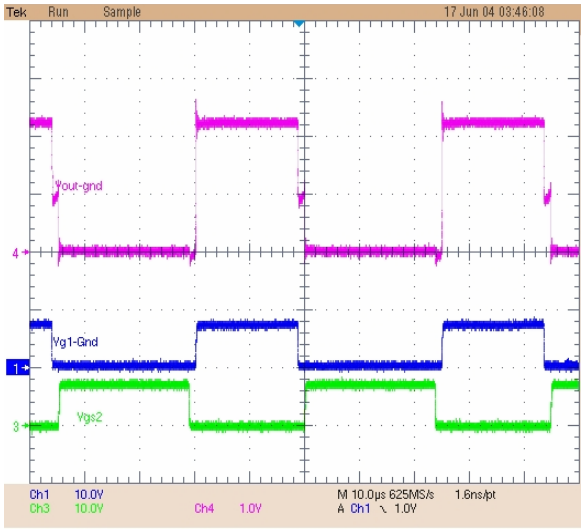

Figure 9. Unloaded 20kHz waveforms, Traces top to bottom, output terminal, bottom MOSFET gate, top MOSFET gate, all referred to ground.

In order to determine the efficiency of this converter, a new high end oscilloscope was used to measure the input and output power. The internal math function was employed to obtain the instantaneous power from the current and voltage, the mean value of which indicates the average power. The current probe was carefully calibrated before each current measurement, to minimumise measurement errors. Table 3 shows the details of the equipment used. Figures 11 and 12 show the input and output voltages, current and power.

The mean value of measured power is displayed at the right column of the figures.

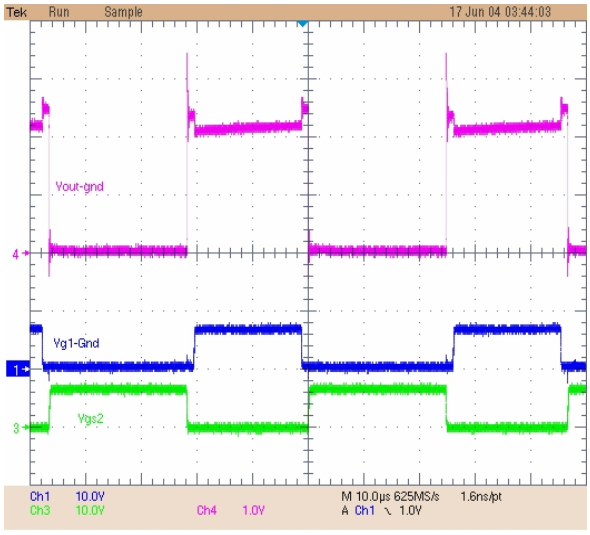

Figure 10. Loaded 20kHz Waveforms, Traces top to bottom, output terminal, bottom MOSFET gate, top MOSFET gate, all referred to ground.

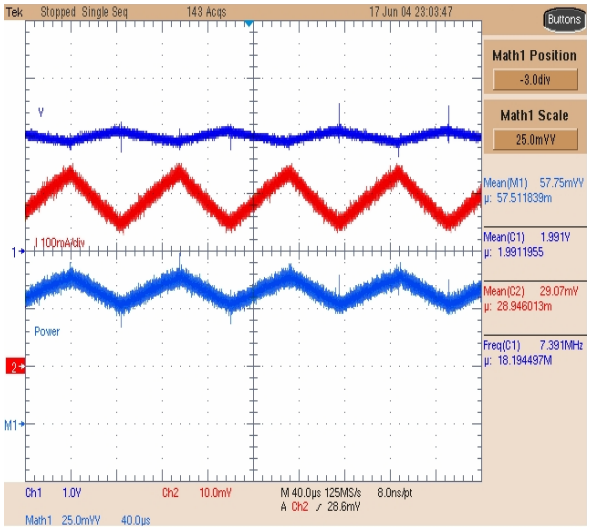

Figure 11. Input voltage, current and power at 10kHz (from top to bottom).

The efficiencies of the converter obtained are shown in Table 4, due to length limit of this paper, the waveforms at 2kHz and 20kHz are not included due to page length limits.

It is seen that the measured efficiency is slightly lower than estimated especially at higher frequencies. One reason is the loss during the dead-time. The on-state voltage drop of the diode is much higher than the MOSFET, and therefore reduces the efficiency of the converter. At 10kHz the dead time loss accounts for 12mW of the observed 30mW. A further 13mW is accounted for losses in Table 2, note switching and

gate losses are halved. Losses of 5mW remain. Some of which are additional no-load losses. The results do confirm that the circuit is capable of achieving high efficiencies especially if the switching frequency is low.

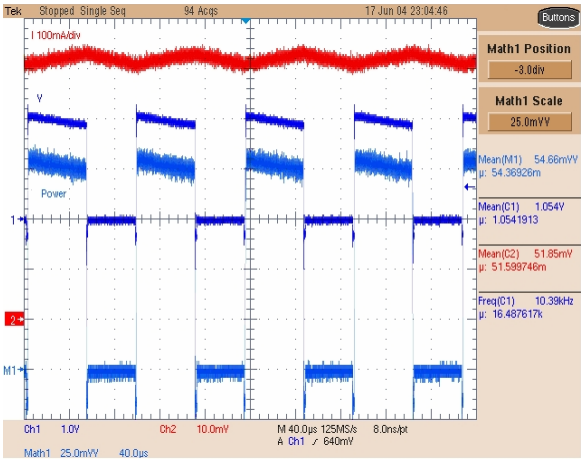

Figure 12. Output current, voltage and power at 10kHz (from top to bottom).

Name of equipment	Model	Quantity
Current probe	Tektronix AM503B+TM502A	1
Voltage probe	Tektronix P5050	1
Oscilloscope	Tektronics DPO5034	1

Table 3. Equipment for efficiency measurement.

Frequency (kHz)	Input Power (mW)	Output Power (mW)	Efficiency
2	520	510	98%
10	577	547	95%
20	506	471	93%

Table 4. Converter efficiency at different frequencies

6. CONCLUSIONS

In this paper, a new maximum power point tracking scheme was proposed and investigated experimentally, the results show a high efficiency converter with simpler structure is possible. The efficiency of the converter can be measured by using oscilloscope and its math functions. Further work will be performed to:

- Further quantify the converter loss mechanisms and optimise the dead time loss, switching loss and conduction loss choices
- Demonstrate a multiple converter application on a solar array
- Develop maximum power tracking algorithms.

7. ACKNOWLEDGEMENTS

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8. REFERENCES

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