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Application of DSTATCOM for Surplus Power Circulation in MV and LV Distribution Networks with Single-phase Distributed Energy Resources

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Abstract—Presence of large number of single-phase distributed energy resources (DER) in a particular phase can cause reverse power flow in that phase making the upstream network unbalanced. In this paper, the possibility of using a Distribution Static Compensator (DSTATCOM) is explored to circulate the excess generation in one phase to the phases with higher load demand. Two different topologies are proposed for DSTATCOM to be installed in low and medium voltage feeders. Similarly, two different power circulation strategies are proposed for power circulation through the DSTATCOM. A suitable switching feedback control scheme is developed and utilized for each topology. In addition to power circulation, the DSTATCOM facilitates a set of balanced phase power flow from the upstream side. The proposals are validated via PSCAD/EMTDC simulation studies.

Index Terms—DSTATCOM, DER, Power circulation

I. INTRODUCTION

RENEWABLE energy based generation is gaining substantial attention these days due to depletion of the traditional energy resource and the negative impact of fossil fuels on environment [1]. Solar photovoltaic (PV), micro wind turbines, fuel cells, etc. are different forms of Distributed Energy Resources (DER). Additionally, electric vehicles are expected to be integrated to the grid in V2G mode as the battery technology improves in the future [2].

Despite the well-known advantages of distributed generation, the integration of DERs in Low Voltage (LV) feeders also has some drawbacks [3]. The main power quality problems are voltage/current unbalance and voltage rise. Unequal distribution of single-phase DERs creates unbalance on LV feeders. Therefore the net effect of these installations will ultimately affect the Medium Voltage (MV) feeders.

Custom power devices are already proven to be an efficient method for alleviating the power quality problems in a distribution feeder [4]. Among them, distribution static compensator (DSTATCOM) is effective in balancing the supply currents, improving power factor, controlling the voltage at a bus and suppressing harmonic currents [4]. A DSTATCOM is used in [5–6] to improve voltage profile and reduce voltage unbalance in LV networks.

Since the DERs will be placed randomly, the generation in a particular phase can exceed the load demand in that phase.

Under such conditions, the surplus phase power will be fed back to the upstream MV feeder creating severe current unbalances. In [7], application of an MV-connected DSTATCOM was considered for circulating this surplus phase power from one phase to another.

In this paper, utilization of a DSTATCOM with different topologies and control algorithms are proposed for both LV and MV feeders to enable the power circulation. The DSTATCOM current and voltage output references are generated such that a set of balanced currents are drawn from the upstream. The proposals are validated through PSCAD simulation studies.

II. DSTATCOM TOPOLOGIES

The proposed DSTATCOM is composed of a Voltage Source Converter (VSC), with the structure as shown in Fig. 1(a). It contains three single-phase H-bridges, supplied from a common DC bus. The output of each H-bridge is connected to an LC filter, consisting of an inductor (L_f) and a capacitor (C_f). To provide galvanic isolation, a single-phase transformer, with a turns ratio of 1: a , is utilized between the output of each VSC and the LC filter. These transformers are connected in star configuration in their secondary and can also provide voltage boosting, if required. In Fig. 1(a), the resistance R_f represents the switching and transformer losses. The filter capacitor C_f is directly connected to the feeder. This is a suitable topology when DSTATCOM is installed in LV feeders.

When DSTATCOM is installed in MV feeder, the VSC and filter are desired in low voltage and connected to the MV feeder through a boosting transformer. Hence, the transformers are installed between filter capacitor and MV feeder as shown in Fig. 1(b). Different control algorithms are proposed for each DSTATCOM topology as discussed in Section III.

III. POWER CIRCULATION STRATEGIES

Two different power circulating strategies are proposed for each topology of the DSTATCOM, introduced in Section II.

A. Power Circulation Strategy for DSTATCOM in LV Feeder

First, let us assume the DSTATCOM is connected to the LV feeder and needs to circulate surplus power generated in a phase to the remaining phases. It is desired that after power circulation, a set of balanced currents are observed in DSTATCOM upstream side. The MV feeder, drawn from the power substation, is connected to an infinite bus in the up-

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stream; hence its voltage is assumed to be balanced. For having a balanced set of current flowing in the MV feeder, originated from the balanced infinite bus, the DSTATCOM PCC voltage must be balanced. This can be achieved by controlling the DSTATCOM such that it generates and holds a balanced set of voltage at its PCC. As the DSTATCOM has an LC filter in its output, a voltage control technique can be utilized to hold a balanced set of voltage across the three filter capacitors (C_f) in PCC. The reference voltage will be as [5]

$$[\mathbf{V}_{cf}]_{ABC}^{ref} = E_{DSTAT} \angle \delta_{cf,A}^{ref} \times [1 \quad \lambda^2 \quad \lambda]^T \quad (1)$$

where E_{DSTAT} is the desired phase voltage RMS for the DSTATCOM PCC (i.e. 240 V in this study), $\delta_{cf,A}$ is the angle of v_{TA} and $\lambda = 1 \angle 120^\circ$. This voltage is used as the reference for the output voltage of the DSTATCOM in next section. The DSTATCOM exchanges reactive power with the LV feeder to hold the desired voltage at its PCC.

The successful operation of the DSTATCOM highly depends on the voltage variations across its DC capacitor (V_{dc}). V_{dc} can be kept constant and equal to its reference value, if the DC capacitor does not exchange power with the VSCs [4]. This can be reassured if the AC system replenishes the DSTATCOM losses. For this, the angle of the voltage across the AC filter capacitor (δ_{cf}) must be varied with respect to the DC capacitor voltage variations as

$$\delta_{cf}^{ref} = \left(k_p + \frac{k_I}{s} \right) (V_{dc}^{ref} - V_{dc}) \quad (2)$$

B. Power Circulation Strategy for DSTATCOM in MV Feeder

Now, let us assume the DSTATCOM is connected to the MV feeder and needs to circulate surplus power generated in a phase to the remaining phases. Through simulation study, it has been revealed that aforementioned voltage control strategy fails to perfectly balance the PCC voltage due to the effect of the leakage inductance of the coupling transformers, although the DSTATCOM will have an acceptable level of voltage tracking over C_f . Hence, a balanced set of currents are not achieved in the upstream side of the DSTATCOM.

Hence, a current control strategy is utilized where proper current output references for each phase of the DSTATCOM are calculated and the DSTATCOM is controlled to reassure the desired current flow to its PCC. The main aims of calculating the reference output currents of the DSTATCOM are ensuring the power circulation from one phase to the other phases and balancing the current in DSTATCOM upstream. In this regard, the theory of instantaneous symmetrical component is utilized [8]. To apply the theory, first the fundamental positive sequence of the PCC voltage is obtained [9]. Let the instantaneous positive sequence voltages be denoted by v_{A1} , v_{B1} and v_{C1} . The reference currents can then be calculated as [10]

$$[\mathbf{i}_T]_{ABC}^{ref} = [\mathbf{i}_L]_{ABC} - \frac{v_{A1}i_{LA} + v_{B1}i_{LB} + v_{C1}i_{LC}}{v_{A1}^2 + v_{B1}^2 + v_{C1}^2} [\mathbf{v}_1]_{ABC} \quad (3)$$

where i_L is the current in the downstream of DSTATCOM. This current is used as the reference current output of DSTATCOM in next section.

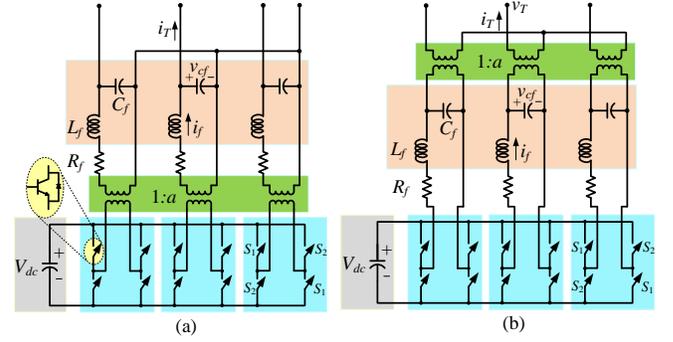


Fig. 1. DSTATCOM topology with power circulation capability to be installed in: (a) LV feeders, (b) MV feeders.

IV. CONVERTER SWITCHING CONTROL

A voltage control technique is required when DSTATCOM is connected to LV feeder while a current control technique is required when connected to MV feeder. Proper reference tracking technique for each mode is described below:

A. Voltage Control Technique

Let us consider only one phase of the DSTATCOM circuit in Fig. 1(a), in which the state vector is defined as [11]

$$\mathbf{x}(t) = [v_{cf}(t) \quad i_f(t)]^T \quad (4)$$

where $v_{cf}(t)$ represent the instantaneous voltage across AC filter capacitor, $i_f(t)$ is the current passing through filter inductor L_f and T is the transpose operator. Then, the equivalent circuit of the system can be represented as

$$\dot{\mathbf{x}}(t) = \mathbf{A} \mathbf{x}(t) + \mathbf{B}_1 u_c(t) + \mathbf{B}_2 i_T(t)$$

$$\text{where } \mathbf{A} = \begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & -\frac{R_f}{L_f} \end{bmatrix}, \quad \mathbf{B}_1 = \begin{bmatrix} 0 & \frac{aV_{dc}}{L_f} \end{bmatrix}^T, \quad \mathbf{B}_2 = \begin{bmatrix} -\frac{1}{C_f} & 0 \end{bmatrix}^T \quad (5)$$

are system matrices, $u_c(t)$ is the continuous-time version of switching function u and $i_T(t)$ represents effect of the network loads on the converter control and hence is assumed as a disturbance and neglected in designing the controller.

In the control systems, the desired values for each control parameter in steady state condition must be known. However, it is rather difficult to determine the reference for i_f in (4). Nevertheless, it is desired that i_f has only low frequencies. Therefore, instead of using i_f as a control parameter, its high frequency components (\tilde{i}_f) can be used in the control system. Based on this assumption, in [11], the higher frequency components of \tilde{i}_f can be obtained utilizing a High Pass Filter whereas its desired reference is equal to zero.

Eq. (2) can be represented in discrete-time domain as

$$\mathbf{x}(k+1) = \mathbf{F} \mathbf{x}(k) + \mathbf{G}_1 u_c(k) + \mathbf{G}_2 i_T(k)$$

$$y(k) = \mathbf{C} \mathbf{x}(k)$$

$$\text{where } \mathbf{F} = e^{\mathbf{A}T_s}, \quad \mathbf{G}_1 = \int_0^{T_s} e^{\mathbf{A}t} \mathbf{B}_1 dt, \quad \mathbf{G}_2 = \int_0^{T_s} e^{\mathbf{A}t} \mathbf{B}_2 dt \quad (6)$$

and T_s is the sampling time. Using a suitable state feedback control law, $u_c(k)$ can be computed as

$$u_c(k) = -\mathbf{K}[\mathbf{x}(k) - \mathbf{x}_{ref}(k)] \quad (7)$$

where \mathbf{K} is a gain matrix and $\mathbf{x}_{ref}(k)$ is the desired state vector in discrete-time mode, expressed as

$$\mathbf{x}_{ref} = [v_{cf}^{ref} \quad \tilde{i}_{f,ref}^T]^T = [v_{cf}^{ref} \quad 0]^T \quad (8)$$

It is to be noted that the desired reference value for $v_{cf}(t)$ is determined by (1).

As the system behavior in steady-state is interested and assuming a full control over $u_c(k)$, an infinite time LQR [12] can be designed for this problem to define \mathbf{K} . This controller is more stable than PID based controls. In addition, PID based controllers are not very effective when utilized in per-phase based controls.

In discrete LQR, objective function J is chosen as [12]

$$J(k) = \sum_{k=0}^{\infty} \left[\begin{array}{l} (x(k) - x_{ref}(k))^T Q(k) (x(k) - x_{ref}(k)) \\ + u_c(k)^T R(k) u_c(k) \end{array} \right] \quad (9)$$

where R is the control cost matrix, Q is the state weighting matrix which reflects the importance of each controlling parameter in x and $J(\infty)$ represents the objective function at infinite time (steady-state condition) for the system. Eq. (9) is then minimized to obtain the optimal control law $u_c(k)$ through solution of steady state Riccati equations [12] while satisfying system constraints in (6). The LQR method ensures the desired results for the system while the variations of system parameters are within acceptable limits of reality.

Eq. (7) shows the total tracking error of DSTATCOM converter. The tracking error can be minimized by limiting this error within a very small bandwidth (e.g. $h = 10^{-4}$). Now, from (7), switching function u is generated using a hysteresis control based on the error level as

$$\begin{array}{ll} \text{If } u_c(k) > +h & \text{then } u = +1 \\ \text{If } -h \leq u_c(k) \leq +h & \text{then } u = \text{previous } u \\ \text{If } u_c(k) < -h & \text{then } u = -1 \end{array} \quad (10)$$

If $u = 1$, then S_1 pair of IGBTs turn ON and if $u = -1$, then S_2 pair of IGBTs turn ON. This switching control was considering only one phase. Similar switching action is employed for the other two phases, separately.

Note that, the switching frequency of IGBTs depends on the value of h . On the other hand, the power loss in the IGBTs depends on their switching frequency. Although reducing h to smaller values improves the reference tracking in the converter output, it might lead to very high impractical switching frequencies in the converter resulting higher power losses in VSCs. Therefore, h is to be defined such that a proper reference tracking is achieved while the switching frequency and power losses remain acceptable [4].

System closed-loop block diagram is shown in Fig. 2(a).

B. Current Control Technique

Let us consider only one phase of the DSTATCOM circuit in Fig. 1(b), in which the state vector is defined as [5]

$$\mathbf{x}(t) = [i_T(t) \quad i_f(t) \quad v_{cf}(t)]^T \quad (11)$$

where i_T is the output current of the DSTATCOM. Then, the

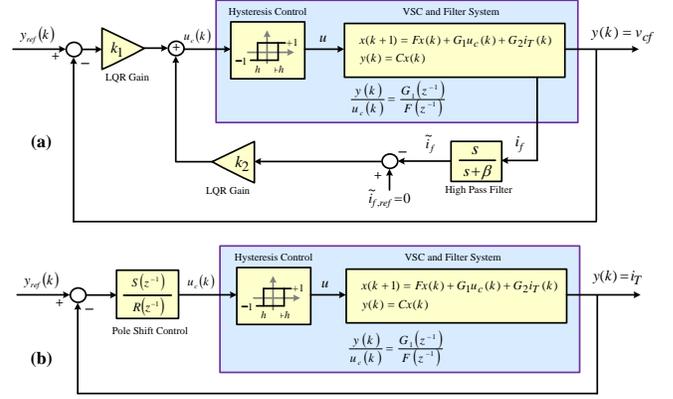


Fig. 2. Closed-loop switching control block diagram for (a) voltage control strategy based on LQR, (b) current control strategy based on pole-shift.

state space equation of the system can be written as

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}_1 u_c(t) + \mathbf{B}_2 v_T(t)$$

$$y(t) = \mathbf{C}\mathbf{x}(t)$$

$$\text{where } \mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{a}{L_f} \\ 0 & -\frac{R_f}{L_f} & -\frac{1}{aL_f} \\ -\frac{a}{C_f} & \frac{a}{C_f} & 0 \end{bmatrix}, \quad \mathbf{B}_1 = \begin{bmatrix} 0 & \frac{V_{dc}}{aL_f} & 0 \end{bmatrix}^T, \quad \mathbf{B}_2 = \begin{bmatrix} -\frac{1}{L_T} & 0 & 0 \end{bmatrix}^T, \quad \mathbf{C} = [1 \quad 0 \quad 0] \quad (12)$$

$v_T(t)$ represents the effects of the network loads on the converter control and hence is assumed as a disturbance and is neglected in designing the controller.

As the system behavior is governed by the poles of its transfer function (i.e. the eigenvalues of matrix \mathbf{A}), it is often desirable to modify the poles of the system in order to obtain improved control performance. In this paper, the system consists of converter and filter control by a state feedback control based on pole-shift technique where the open-loop poles are shifted radially towards the origin (i.e. more stable locations) to form the closed-loop poles [4].

Similar to (6), Eq. (12) is represented in discrete-time domain. Assuming the feedback control shown in Fig. 2(b), the system of converter and filter is represented as

$$\frac{y(k)}{u_c(k)} = \frac{G_1(z^{-1})}{F(z^{-1})} = \frac{g_1 z^{-1} + g_2 z^{-2} + g_3 z^{-3} + \dots}{1 + f_1 z^{-1} + f_2 z^{-2} + f_3 z^{-3} + \dots} \quad (13)$$

where z^{-1} is the delay operator. Let the control law given by

$$u_c(k) = \frac{S(z^{-1})}{R(z^{-1})} \{y_{ref}(k) - y(k)\} \quad (14)$$

where y_{ref} is the desired (reference) output current. From Fig. 2(b), the system closed-loop characteristic equation, $\Delta(z^{-1})$ is $\Delta(z^{-1}) = F(z^{-1})R(z^{-1}) + G(z^{-1})S(z^{-1})$ (15)

Unlike the pole-placement technique where $\Delta(z^{-1})$ is pre-defined by the user, pole-shift technique takes the form of

$$\Delta(z^{-1}) = F(\lambda z^{-1}) = 1 + \lambda f_1 z^{-1} + \lambda^2 f_2 z^{-2} + \lambda^3 f_3 z^{-3} + \dots \quad (16)$$

where the poles are shifted by λ towards origin. In this technique, the closed-loop poles are obtained by multiplying the open-loop eigenvalues by $0 < \lambda < 1$ where λ is a scalar close

to one (e.g. $\lambda = 0.8$), which is called the pole–shift factor. The pole–shift factor is the only parameter to be defined in the controller and its value determines the control gain. It is adjusted such that the controller is limited only for the first few swings following a large impact on the system. Given β is the absolute of the largest characteristic root of $F(z^{-1})$, for guaranteeing the closed–loop system stability, λ is limited as [13]

$$-\beta^{-1} < \lambda < \beta^{-1} \quad (17)$$

Since the penalty on control action can be easily adjusted by λ as in (17), the closed–loop system is unlikely to be instable. This is an advantage of the pole–shift technique compared to other techniques such as deadbeat control which forces all the closed–loop poles to origin and requires high control effort.

Replacing (16) in (15) and equating the coefficients of z^{-1} , z^{-2} , ..., the controller coefficients in $R(z^{-1})$ and $S(z^{-1})$ can be retrieved as discussed in [14]. For the system of converter and filter under consideration in this paper, based on the system order in (12)–(13), $S(z^{-1})$ and $R(z^{-1})$ in (14) are simplified as

$$\frac{u_c(k)}{y_{ref}(k) - y(k)} = \frac{S(z^{-1})}{R(z^{-1})} = \frac{s_0 + s_1 z^{-1} + s_2 z^{-2}}{1 + r_1 z^{-1} + r_2 z^{-2}} \quad (18)$$

and the final objective of the controller design is to calculate proper values for s_0 , s_1 and r_1 . Based on these values, the switching function $u_c(k)$ obtained from (18) is used in (10) to achieve a reference tracking with minimum possible error.

V. SIMULATION RESULTS

For studying the efficacy of the proposed topology and power circulation strategies of the DSTATCOM, when connected in LV and MV feeder, several case studies are carried out through PSCAD/EMTDC, with the technical data given in Table 1 in the appendix. These cases are discussed below:

A. Case–1

Let us consider a LV feeder with unbalanced loads where a DSTATCOM, with the topology of Fig. 1(a), is installed and controlled based on the voltage control strategy described in Section III(A). A reverse power flow in phase A is observed due to the connection of excessive single–phase generation to this phase. The steady–state three–phase instantaneous current waveform in the upstream, downstream and output of the DSTATCOM are shown in Fig. 3. The phase active power flow in the same locations is also shown in this figure. The results are shown separately for the cases before and after connection of DSTATCOM. As seen, due to proper power circulation through DSTATCOM, upstream phase currents are balanced effectively after DSTATCOM is connected.

B. Case–2

Let us consider a MV feeder with unbalanced loads where a DSTATCOM, with the topology of Fig. 1(a), is installed and controlled based on voltage control strategy. Under such conditions, the DSTATCOM successfully balances the upstream current by appropriately circulating the unbalanced load phase power (Fig. 4). Note that, in this topology, the filter capacitor should have a MV rating and this is the main drawback of this configuration.

Now, let us consider utilizing a DSTATCOM, with the topology of Fig. 1(b), in the MV network. As discussed in Section III(B), voltage control strategy fails for this configuration.

C. Case–3

Let us now consider the network and DSTATCOM of case–2, where a current control strategy, as discussed in Section III(B) is utilized. The simulation results are shown in Fig. 5. As seen from this figure, the DSTATCOM successfully balances the upstream current by circulating the unbalanced load phase power (current) through the DSTATCOM.

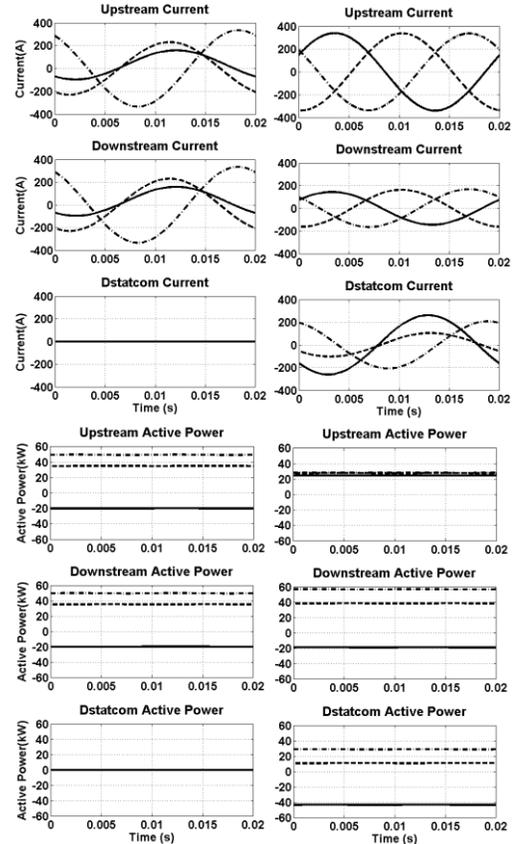


Fig. 3. Case–1 simulations before (left column) and after DSTATCOM connection (right column)

VI. CONCLUSIONS

Large number of single–phase DERs, installed in one phase, can result in reverse power (current) flow in that phase if the generation capacity is higher than the phase load demand. In this paper, two different topologies were proposed for the DSTATCOM in order to provide power circulation capability to prevent the reverse flowing power (current) to the upstream network. The proposed DSTATCOM is composed of a VSC with LC filter, connected directly to the LV feeder while it is connected via a boosting transformer to MV feeders. Simulation results show that a voltage control strategy is a successful strategy for circulating the phase surplus power (current) through the DSTATCOM in LV network while it fails for MV applications due to the leakage inductance of the boosting transformers; hence, a proper current control strategy was developed for such topologies.

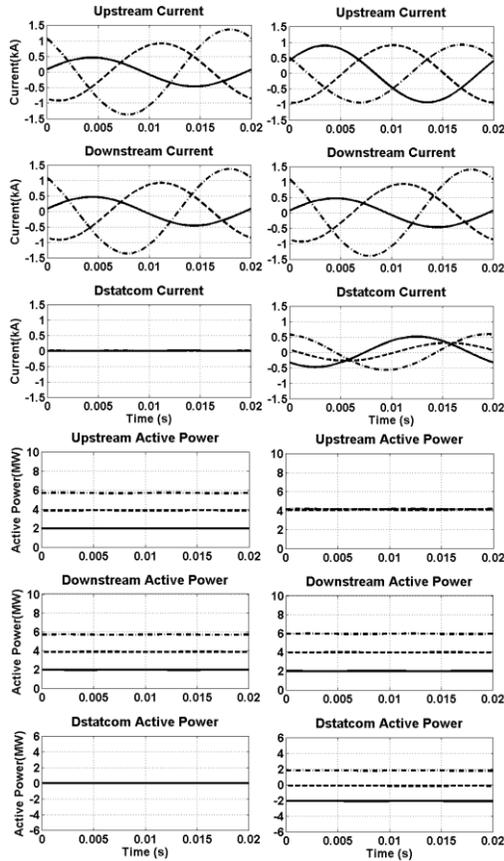


Fig. 4. Case-2 simulation results before (left column) & after DSTATCOM connection (right column)

APPENDIX

Table 1. Technical data of the network in simulation cases.

HV Feeder	132 kV L-L, 50 Hz, $R = 0.25 \Omega$, $L = 10$ mH
MV Feeder	11 kV L-L, 50 Hz, $R = 0.5 \Omega$, $L = 5$ mH
LV Feeder	410 V L-L, 50 Hz, $R = 0.02 \Omega$, $L = 0.1$ mH
HV/MV Transformer	15 MVA, 132 / 11 kV, 50 Hz, $Z_l = 5\%$
MV/LV Transformer	100 kVA, 11 kV / 410 V, 50 Hz, $Z_l = 10\%$
MV load	$Z_A = 18.2004 + j 5.969$, $Z_B = 9.1002 + j 2.9845$, $Z_C = 6.0668 + j 1.9792 \Omega$
LV load	$Z_A = 2.5992 + j 0.8482$, $Z_B = 1.2996 + j 0.4398$, $Z_C = 0.8664 + j 0.2848 \Omega$
DER for Case-1	one single-phase DER with $P = 40$ kW, PF = 1, connected to phase-A
DER for Case-3	Single-phase DER with $P = 0.45$ MW, PF = 1, in phase-A
DSTATCOM for case-1 and 2	$R_f = 0.1 \Omega$, $L_f = 4$ mH, $C_f = 25 \mu\text{F}$, $a = 1$, $h = 10^{-4}$, $\mathbf{K} = [1.5463 \ -0.7092]$, $V_{dc} = 1$ kV (for case-1) and 13 kV (for case-2)
DSTATCOM for case-3	$R_f = 0.1 \Omega$, $L_f = 4$ mH, $C_f = 25 \mu\text{F}$, $V_{dc} = 1$ kV, $a = 11$, $h = 10^{-4}$, $S(z^{-1}) = 43.8019 - 85.4746 z^{-1} + 41.7269 z^{-2}$, $R(z^{-1}) = 1 - 0.1237 z^{-1} - 0.025 z^{-2}$

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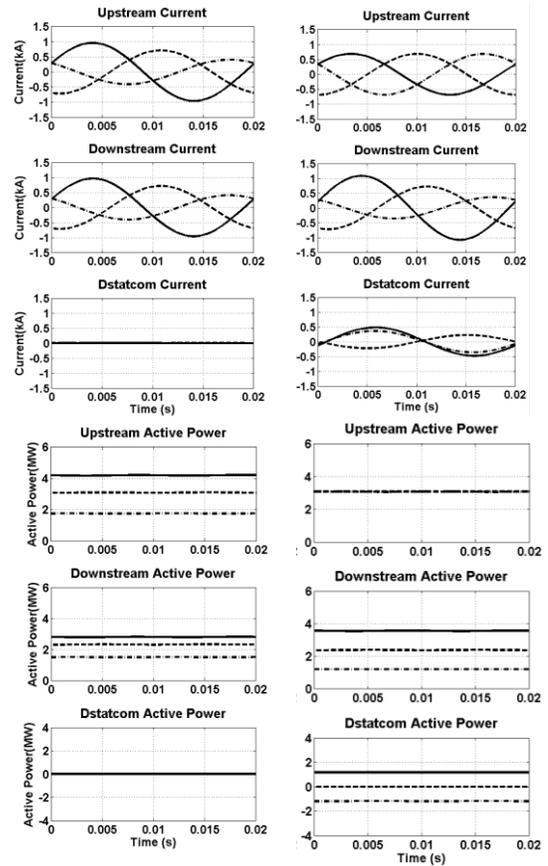


Fig. 5. Case-3 simulation results before (left column) & after DSTATCOM connection (right column)

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