Performance Study of Solder Bond on Thermal Mismatch Stresses in Electronic Packaging Assembly

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Abstract: Thermo-mechanical stresses have been considered as one of the major concern in electronic Packaging assembly structural failure. The interfacial stresses are often caused by the thermal mismatch stresses induced by the coefficient of thermal expansion (CTE) difference between materials, typically during the high temperature change in the bonding process. This research work examined the effect of bond layer on thermal mismatch interfacial stresses in a bi-layered assembly. The paper verified the existing thermal mismatch solder bonded bi-layered analytical model using finite element method (FEM) simulation. The parametric studies on the effect of change of the bond layer properties were carried out in order to provide useful reference for interfacial stress evaluation and the electronic packaging assembly design. These parameters included CTE, temperature, thickness, and stiffness (compliant and stiff bond) of the bond layer. The recent development on the lead free bonding material was being reviewed and found to have enormous potential and key role to address the future electronic packaging assembly reliability.

Keywords: Solder bond layer, interfacial shear stress, bi-layered assembly, thermal mismatch, lead free bond, electronic packaging assembly

1. INTRODUCTION

Thermo-mechanical stresses are a major concern in electronic packaging assembly structural failure. These structural failures often caused by the extreme and prolonged interfacial stresses resulted from the thermal load to the assembly, called thermal mismatch. Generally, typical electronic packaging assembly often stacked and bonded using at least two types of construction materials with different coefficient of thermal expansion (CTE) [1]. The temperature change experienced by the assembly during bonding process is typically as high as 250°C [2]. The CTE difference would cause unsynchronized geometrical shrinkage and expansion upon thermal loading, resulting in bending of the assembly. Consequently, the thermal mismatch resulted from temperature change generates interfacial stresses in the assembly [3]. These interfacial stresses would lead to structural failure in electronic packaging, mainly delamination and crack. Delamination often occurs upon the bond weakening resulted from the long term exposure to residual strains within the interfacial surfaces [4]. The effect of change of bond layer properties and geometry would be an important concern in developing an optimized solution in electronic packaging. Suhir [5-6] proposed a bi-layered interfacial thermal mismatch model by using integro-differential equation. Sujan [7-8] had developed another simpler solution using a second order differential equation approach.

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The effect of bond layer properties and geometry would be an important concern in developing an optimized solution in electronic packaging. In recent years, there were novel efforts in new development on lead free bonding materials. The conventional leaded bonding material was found to have poor thermal mismatch resistance [9]. Particulate reinforced light Metal Matrix Composites (MMC) have shown great promise due to their outstanding tailor-made mechanical and physical properties. The goal is to develop novel bonding material which is compatible to the parent materials (layers) in term of thermal properties in order to eliminate thermal mismatch stresses.

This paper briefly introduced the bi-layered thermal mismatch shearing stress analytical model with the consideration of solder bond layer. The analytical model was then compared with FEM simulation using ANSYS. Subsequently number of parametric studies was conducted to examine the influence of bond layer properties on interfacial thermal mismatch stresses. The properties that were included for investigation are CTE, temperature, thickness, and stiffness (compliant and stiff bond) of the bond layer. Finally the recent development on the lead free bonding material was being reviewed.

2. ANALYTICAL MODEL

The interfacial shear stress model is developed using the beam theory approach [10]. Fig. 1 shows the full length ($2L$) of the model where AA represents the centre line. In the 2D presentation, the model is considered to be of unit width in a direction perpendicular to the plane of the paper and the forces (F_1 and F_2) and moments (M_1 and M_2) are defined with respect to the unit width. The top (Layer 1), bottom (Layer 2), and bond layer (Layer 0) thickness are h_1, h_2 and h_0 respectively.

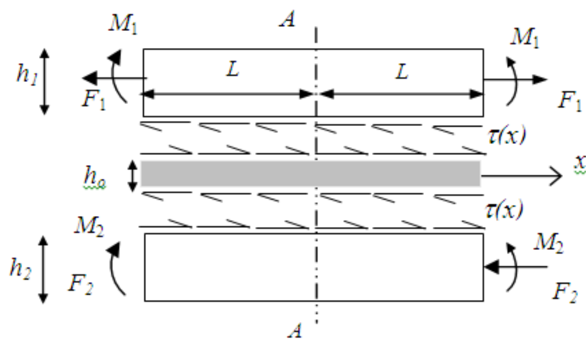

Fig. 1: Free body diagram of bi-layered model

The compatibility condition at the interface is expressed in terms of strain instead of displacement in this model (eq. 1). As such, the model is developed by solving a simple 2nd order differential equation instead of solving a complex integro-differential equation as was seen earlier in Suhir's method [5-6]. The solution is based on the key assumptions as follows: (1) thickness of the layered assembly is relatively small, (2) each layer can be regarded as Bernoulli beam, (3) spherically bending thin plate is acted in each layer, (4) no external force is acting on the assembly, and (5) axial force due to thermal loading varies along the length and full shear length in the interface bonded layers. The key steps of the model developed had been adopted from [10-11] and represented as below:

Including the solder bond layer effect, the strain compatibility condition at the interface can be expressed as

$$\in_{x(1)} - \in_{x(2)} = K_0 \frac{\partial \tau}{\partial x} \tag{1}$$

Replacing the strain components of $\in_{x(1)}$ and $\in_{x(2)}$, eq. (1) takes the form as,

$$(\alpha_1 \Delta T_1 - \alpha_2 \Delta T_2) + \lambda F - (K_1 + K_2)\frac{\partial \tau}{\partial x} = K_0 \frac{\partial \tau}{\partial x} \tag{2}$$

Where, i = 1, 2, material /layer number; α_i = coefficient of thermal expansion (1/°C); h_i = layer thickness (mm); E_i = Young's modulus (GPa); ν_i = Poisson's ratio; ΔT = temperature change (°C); λ_i = axial compliance; $F_1 = F_2 = F$

$$K_1 = \frac{h_1}{3G_1},\ K_2 = \frac{h_2}{3G_2},\ K_0 = \frac{h_0}{G_0},\ \lambda_i = \frac{(1+\nu_i^2)}{E_i h_i}$$

$\alpha_i \Delta T$ =Strain due to change in Temperature

$\lambda_i F_i$ = Strain due to thermal mismatch axial force, F_i

$\frac{h_i}{2R}$ = Strain due to bending

$K_i \frac{\partial \tau}{\partial x}$ = Strain due to shearing force

Differentiating eq. (2), results in a 2nd order differential equation as,

$$\frac{\partial^2 \tau}{\partial x^2} - \mu^2 \tau = 0 \tag{3}$$

Where $\mu^2 = \frac{\lambda}{K}$, $K = K_1 + K_2 + K_0$,

$$\lambda = \lambda_1 + \lambda_2 + \frac{h(h_1+h_2)}{4D}, \; h = h_1 + h_2 + 2h_0 \text{ and}$$

$$D_i = \frac{E_i h_i^3}{12(1-\nu_i^2)}$$

With reference to [11], the solution of eq. (3) can be written as,

$$\tau = C_1 sinh(\mu x) + C_2 sinh(\mu x) \quad (4)$$

Applying the appropriate boundary conditions, the shear stress $\tau(x)$ expression can be derived as,

$$\tau = \frac{\Delta T(\alpha_1 - \alpha_2)}{K\mu\, cosh(\mu L)} sinh(\mu x) \quad (5)$$

3. BI-LAYERED ASSEMBLY WITH BOND LAYER CASE STUDY

The assembly to be examined consists of parameters listed in Table 1. The interfacial shear stress of the assembly was being obtained from both analytical and finite element method (FEM) approaches.

Table I. Material properties and thickness of the assembly

Material	Young's Modulus, E_i (GPa)	CTE, α_i (°C), 10^{-6}	Poisson's Ratio	Thick-ness h_i, mm
Die	188	3	0.3	0.35
Die attach	49.7	25	0.29	0.15
Bond (Compliant)	70.5	16.8	0.41	0.05
Bond (stiff)	18800	16.8	0.35	0.05

3.1 ANALYTICAL AND FEM RESULTS

Fig. 2 showed the shear stress comparison between the analytical and FEM results. The shear stress surges occurred at $x/L > 0.70$ and grown continuously reaching the maximum shear stress magnitude at $x/L = 1$. Therefore, the range of $0.70 < x/L < 1$ would be the main focus to examine. Graphical representation in Figure 4 had shown that FEM results had good agreement with the analytical results, which had proven the validity of the analytical model. Upon x/L=0.95, the edge effect can be observed as the FEM results disagreed with the analytical results.

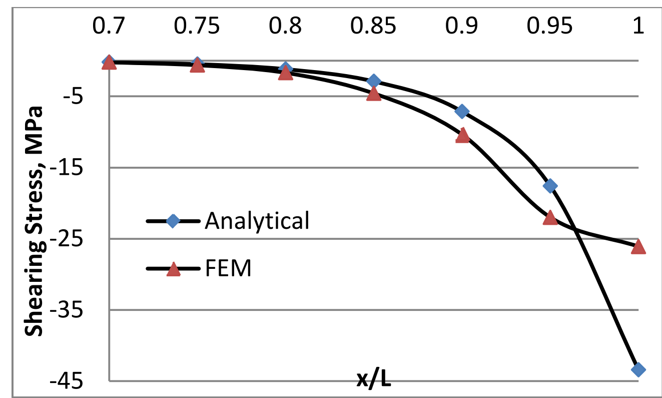

Fig. 2 Shear stress comparison between analytical and FEM

4. PARAMETRIC STUDIES ON EFFECT OF CHANGE OF BOND LAYER PROPERTIES TO THE ASSEMBLY

The effect of change of the significant bond layer properties to the interfacial stress performance would be studied and compared. Based on the verification of the model in Section 3.1, it has been proven the agreement of analytical model and the finite element method (FEM) results. Hence, the effect of change of parameters to the interfacial stress performance would be simulated and discussed using the FEM approach in this Section.

4.1 COEFFICIENT OF THERMAL EXPANSION (CTE) OF THE BOND LAYER

The shear stress analysis was conducted using FEM approach with four different coefficients of thermal expansion ratios of α_0/α_2. The α_0/α_2 ratio would be useful and significant in comparing the CTE difference of the bond layer with respect to the bottom Layer. The ratios being used include 0.032, 1.472, 3.072 and 8, where α_2 is kept constant at 25 e-6 1/C and the α_0 is increased in four stages, i.e. 0.8 e-6 1/C, 36.8 e-6 1/C, 76.8 e-6 1/C, and 200 e-6 1/C. Since there were two interfaces, that is upper interface at between top and bond layer, and lower interface at between bond layer and bottom layer, the analysis will be focused on the shear stress difference between upper and lower interfaces, denoted as $d\tau$. The results were plotted Fig. 3.

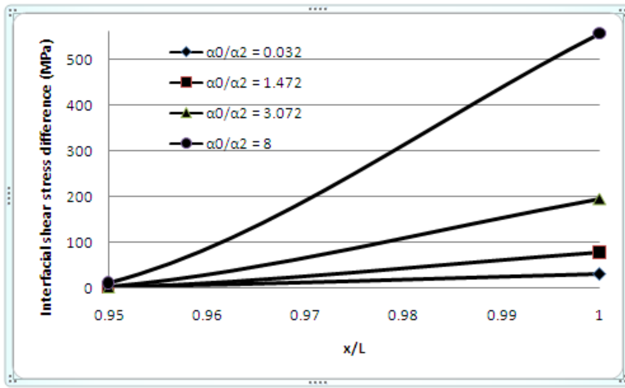

Fig. 3 Shear stress comparison for CTE parameter

The graphical comparison plotted in Fig. 3 had zoomed and focused into the finite range of $0.95 < x/L < 1$ for better and obvious data display. It was observed that the interfacial shear stresses increased drastically at the edge with the increase of the coefficient of thermal expansion (CTE) ratio. It can be explained that the great CTE difference between the two layers would have generated unsynchronized deformation between the upper and lower interfaces. Consequently, the greater interfacial shear stress difference, $d\tau$ which created at higher ratio would increase the failure rate of the assembly. Referring to [4], the greater interfacial shear stress difference would have further increased the severity of the thermal mismatch and finally reduced the life cycle of the assembly. Thus, the lower CTE ratio configuration would be suggested in the electronic packaging assembly design.

4.2 TEMPERATURE CHANGE APPLIED TO THE ASSEMBLY

The shear stress analysis was conducted using FEM approach with four different temperature change values, which would in increasing order of 60°C, 120°C, 180°C, 240°C, and 300°C. The temperature change would be simulating temperature fluctuation subjected by the whole assembly, which experienced during the thermal mismatch process. Based on the graphical comparison plotted in Fig. 4, the shear stress resulted from different temperature change would be focused on the $0.75 < x/L < 1$, whereby the shear stress comparison can be made at a magnified view. It was observed that the shear stress curves pattern was identical, and the shear stress magnitudes increased in identical steps. It can be explained that the total deformation was proportional to the applied thermal loading. Furthermore, the wrapage would be greater at the higher temperature change, which would have increased the failure rate. On the other hand, the bonding temperature commonly applied in the industry would be as high as 250°C and accelerated the failure due to thermal mismatch. Thus, bonding material with lower bonding temperature must be used for shear stress minimization. New bonding material with lower melting temperature would be suggested for the electronic packaging assembly

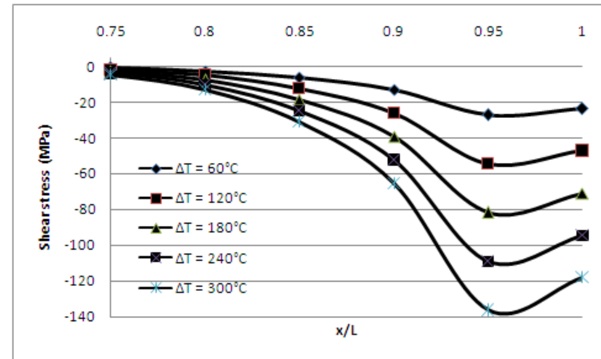

Fig. 4 Shear stress comparison for temperature change parameter

4.3 BOND LAYER THICKNESS

The shear stress analysis was conducted using FEM approach with four different thickness values, which include negligible bond thickness, 0 m, and increasing bond thickness of 0.01 mm, 0.02 mm, and 0.04 mm. Fig. 5 had specifically highlighted the significant variation in the shear stress at $0.94 < x/L < 1$. The shear stress was observed to be reduced along the length whenever the bond layer thickness was being increased. The increased bond layer thickness would have created a surrogate layer acted for shear stress absorption along the interface. Therefore, the higher value of bond layer thickness would be suggested in the electronic packaging design. However, the increased bond thickness was seemed to be another concern for the increased weight, material required and cost. The current trend in the industry prioritized miniaturization, weight and cost reduction.

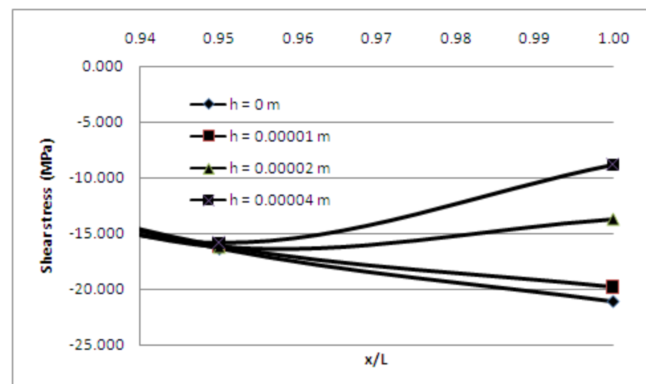

Fig. 5 Shear stress comparison for bond thickness parameter

4.4 COMPLIANT AND RIGID BOND

It is evident from Fig. 6 that shearing stresses decreased due to the compliant bond layer effect at any identical location at the interface. Particularly, near the vicinity of the free end,

the differences were quite significant. For instance, at location x/L =1 (free end) from Fig. 6, the compliant bond layer consideration had reduced the shearing stress value as much as 17.9 MPa or 21% compared to the case of a perfectly bonded layers. However, for the case of a stiff bond layer, no significant changes of the shearing stress was observed at any identical location compared to the case of a perfectly bonded layers. Thus, it indicates that a more compliant bond likely to result in smaller interfacial stress compared to a stiffer bond. It is worth mentioning here that a compliant bond is likely to generate smaller interfacial stress but it is easier to deform. On the other hand, a stiffer bond is likely to results in higher stresses but it is more difficult to deform [12].

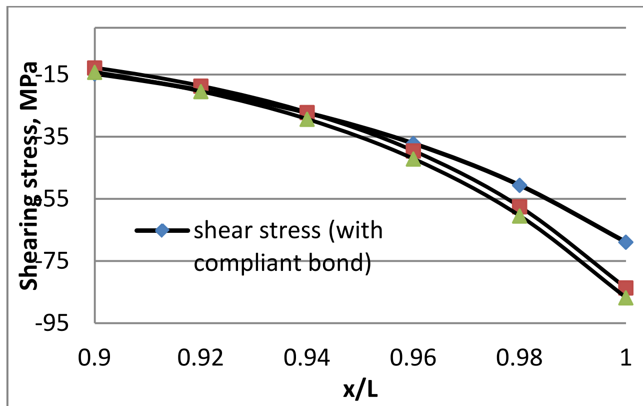

Fig. 6 Shear stress comparison for compliant and rigid bond

5.0 NEW DEVELOPMENT ON LEAD FREE BONDING MATERIAL

Disadvantages of the conventional lead based solder bond:

Apparently, the tin-lead solder is being widely used in the industry as electronic packaging bonding material. Tin-lead (Sn-Pb) has good properties of high sensitivity rate and temperature dependent[13]. However, the large temperature fluctuation within the electronic packaging had induced the thermo-mechanical loading to the assembly which would lead to failure.

Improved reliability in Flip Chip in Package (FCIP) technology

Nowadays, flip chip in package (FCIP) is being the most popular and widely used technology in electronic device assembly. Flip chip packaging has the advantage of reducing the wire bond pad pitch limitations, versatility in power and ground distribution of electronic device designs, as well as the improvement in reliable high speed and high frequency signal transmission. As of today, the flip chip packaging technology development had sophisticatedly evolved in the key area, such as bumping technologies, substrate technologies and thermal management technologies [14].

Advanced ceramic based solder material

Currently, the choices for substrate materials include both organic and ceramic based. Organic based substrates appear popular for flip chip packaging assembly, yet it has high value of coefficient of thermal expansion (CTE) properties, which creates large thermal mismatch between the die and substrate. Many of them have lower durability in the environmental reliability test compared to the ceramic packaging, such as Alumina, mainly because of the moisture absorption. As solution, manufacturers are keen in developing novel materials that incorporate the best features from both organic and ceramic based materials. Kyocera Corporation had developed the new Low Temperature Co-Fired Ceramic (LTCC) technology known as Hi-TCE2, which had improved electrical and mechanical properties [15].

Low cost and improved performance of Tin based solder material

It was reported that Fujitsu has done the research on the new and sophisticated substitutes for the tin-lead solder, which featuring lead free solder. These lead free solder include high temperature Sn-Ag-Cu solder, medium temperature Sn-Zn-Al solder and the low temperature Sn-Bi-Ag solder. All of these new types of solder materials offer better properties over the conventional tin-lead solder, which include more reliable solder joints, lower cost, distortion reduction and greater capability in sustaining heat stress, shock and vibrations [15].

Improved bonding quality using Thermosonic Flip Chip bonding technology

Thermosonic flip chip bonding technology involved thermal energy and ultrasonic power to create the chip-substrate bonding. According to research done by Chuang, the main challenge of this technology would be the generation of copper oxides during the process. Copper oxide residues remained in the bond layer and most importantly, it cannot be removed and as a result reduces the bonding quality. As solution, the copper electrodes were being deposited with silver and titanium as bonding layer and diffusion barrier layer respectively. The deposition resulted in bonding quality improvement. Results from conducted tests also indicated good reliability of the package at prolonged and elevated temperature storage [16].

High quality solder joints with fluxless bonding process

In recent years, new fluxless bonding process was being developed using Au-Sn eutectic solder. Technically, the process was being done by electroplating the multi-layered Au/Sn/Au structure on a ceramic packaging. Firstly, the

assembly was being reflowed at 430 °C for 10 minutes in order to obtain the uniform eutectic Au-Sn solder bond of 80%-20% composition. Next, the ceramic packaging was being bonded to a silicon chip using Cr/Au material, reflowed at 320 °C for 3 minutes. This new soldering technique had shown that high quality joints can be produced even without using flux [17].

Temperature fluction reduction using low melting solder material

Solid-liquid inter-diffusion bonding method is commonly being used to join multi-layered assembly that consists of high-melting and low-melting material properties. The process is being conducted at temperature above the melting point of the low-melting material, which the material being liquefied and create bonding between layers upon solidification. Hence, the indium, In-based solder would be the potential material, which has relatively low melting temperature. In addition, it was found to have good consumption into the silver, Ag [18].

On the other hand, the giant microprocessor manufacturer, AMD found out that pure indium solder would have the best combination thermo-mechanical and electro-mechanical properties for high power electronics, after undergone several severe tests on the indium soldered electronic packaging assembly [19].

Recently, it was published that the pure silver joint between silicon chips and copper substrates were being bonded at temperature relatively lower than the melting point, which would have reduced the large temperature fluctuation. Importantly, the silver layer served as the surrogate bonding layer, purposely to deform for compensation for the interfacial shear stresses across the silicon and copper layers[20]. Thus, it had achieved better advantages of thermo-mechanical and mechanical properties.

6.0 CONCLUSION

The effect of thermal mismatch to the interfacial shear stress in electronic packaging assembly had been analyzed and simulated. The validity of the developed model had been verified by comparing analytical results with finite element method (FEM) solutions. The parametric studies on the effect of change of the bond layer properties had been carried out and analyzed. The new development on the lead free bonding material was being discussed and found to be the potential new technology in the future electronic packaging industry.

The results and suggestions provided on the optimized bond layer parameters in this paper would be the useful reference for the electronic packaging designer to develop new sophisticated electronic device with improved performance. However, it might be limited due to the current technology, practicality, cost and size concerns. Importantly, the useful reference can be extended to other similar case and scenario, such as the wall painting and adhesives. These scenarios would have sharing similar theory, principles, problems and solutions.

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