Department of Electrical and Computer Engineering

Online Control of Modular Active Power Line Conditioner to Improve Performance of Smart Grid

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Declaration

To the best of my knowledge and belief, this thesis contains no material previously published by any other person except where due acknowledgment has been made.

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university.

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SYNOPSIS

Power electronic devices are growing in distribution networks, and their applications are gaining wide attention among different users. These devices which are considered as nonlinear loads inject harmonics to the distribution networks and thus may lead to detrimental effects on network operation. To reduce these harmful effects, in general, harmonic filters are introduced. Harmonic filters are designed with passive and active configurations. Passive filters such as capacitors and inductors are simple and easy to implement but have some disadvantages such as fixed compensation, resonance and large sizes. On the other hand, active power filters (APFs) have smaller sizes and are able to eliminate selected harmonics but require additional control systems for injecting non-sinusoidal harmonic currents to eliminate the current harmonics of the nonlinear load. However, APFs are only able to eliminate the current harmonics of nonlinear loads at their point of common coupling (PCC) and their implementation does not guarantee the elimination of harmonics through the entire network. Therefore, active power line conditioners (APLCs) are introduced which are able to compensate the voltage harmonics of the entire connected network.

Moreover, voltage instability is another issue that utilities and networks are facing. Voltage sag or swell is a common form of voltage instability which occurs due to different reasons such as insufficient power generation or an increase in power demand. This phenomenon causes the network to operate very close to its minimum voltage requirements and thus by switching large industrial loads the network voltages may go below the limited values. A possible solution is to install a static synchronous

compensator (StatCom) which is a shunt connected flexible AC transmission systems (FACTS) device to inject or absorb reactive power to improve the network voltage profile.

ABSTRACT

In the recent years, along with the growing integrations of renewable power generations and power electronic devices into the distribution networks, some serious problems such as voltage fluctuation and harmonic distortions have ascended. These problems have detrimental effects on power systems such as overloading, overheating and failure of power system components and devices such as power electronic components, electric motors, power transformers and conductors.

By controlling the reactive power and reducing harmonic distortions within transmission and distribution networks, maximum active power flow and voltage regulation with high power quality can be achieved. This type of compensation can be achieved by using various topologies. Flexible AC transmission systems (FACTS) devices are used to implement these topologies to improve the power quality.

Static synchronous compensator (StatCom) is one of the shunt FACTS devices which is able to generate or absorb reactive current in order to control the reactive power of the network. The ability of StatCom to improve voltage profile of the entire network is explored in this thesis.

Active power filter (APF) is the most commonly used devices to compensate harmonic distortions at the terminals of the nonlinear loads. APFs are designed to compensate 100% of the nonlinear load's harmonics and improve the power quality of power systems. However, this approach requires one APF for each nonlinear load which is may not be a practical solution for networks with many nonlinear devices. Therefore, active power line conditioners (APLCs) have been proposed to reduce the harmonic current contamination of the entire network according to the power quality standards such as the IEEE 519-1992.

APLC is an advanced shunt active filter which can limit the voltage total harmonic distortion (THDv) of the entire network or a designated area below 5% as recommended by most power quality standards.

Most of the researches are based on compensating of either reactive power flow or harmonic distortions of the network. Furthermore, there is a research gap in design and implementation of APLCs with the consideration of harmonic couplings, which is an inherent characteristic of most realistic nonlinear loads and distorted networks.

The main aims of this thesis are:

1) Optimal siting and sizing of multiple APLCs in distorted smart grid (SG) networks to control the network THDv without and with the consideration of harmonic couplings. This is done by implementing two particle swarm optimization (PSO) algorithms that rely on the transmitted online smart meter data including the bus voltage profiles.

2) Simultaneous compensation of the network fundamental voltage fluctuations (reactive power compensation) and network voltage harmonic distortions by optimal siting and sizing of advanced APLC units with both StatCom and APF functions. This is done by modifying the two PSO algorithms to also include reactive power compensation at the fundamental frequency.

Detailed simulations are performed in Matlab/Simulink to first find the optimal locations and sizes of the APLCs in a 15-bus network with six nonlinear loads (without and with consideration of harmonic couplings) and then investigate their performance and effectiveness in online compensation of both fundamental reactive power and harmonic distortions (Chapter 4).

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I also offer my regards and blessings to my beloved family who gave me their inseparable moral support, encouragement and prayers to the end of my education.

ABBREVIATIONS

AC: Alternating-current

AHCC: Adaptive hysteresis current control

APF: Active power filter

APLC: Active power line conditioner

CMC: Cascaded multilevel converter

CSC: Current source converter

DC: Direct-current

DCMC: Diode-clamped multilevel converter

DG: Distributed generation

D-StatCom: Distribution StatCom

DVR: Dynamic voltage regulator

FACTS: Flexible AC transmission systems

FC: Fixed shunt capacitor

FCMC: Flying capacitor multilevel converter

FL-NPC: Five level neutral-point clamped

FR: Fixed shunt reactor

GTO: Gate turned-off thyristor

HCC: Hysteresis current control

HYS-PWM: Hysteresis control PWM

IEC: International electrotechnical commission

IEEE: Institute of electrical and electronics engineers

IGBT: Insulated gate bipolar transistor

IGCT: Integrated gate-commutated thyristor

IPFC: Interline power flow controller

LCC: Line commutated converter compensator

MSC: Mechanical switched shunt capacitor

MSR: Mechanical switched shunt reactor

PCC: Point of common coupling

PLL: Phase-locked loop

PSO: Particle swarm optimization

SCC: Self-commutated compensator

SG: Smart grid

SGCC: Smart grid central control

SH-PWM: Selective harmonic elimination PWM

SPWM: Sinusoidal PWM

SSSC: Synchronous series compensator

StatCom: Static synchronous compensator

SVC: Static VAR compensator

SVC: Static VAR compensator

SV-PWM: Space vector PWM

TCBR: Thyristor controlled braking resistors

TCPR: Thyristor controlled phase angle regulator

TCPST: Thyristor controlled phase shifting transformers

TCR: Thyristor controlled reactor

TCSC: Thyristor controlled series compensator capacitor

TCSR: Thyristor controlled series compensator reactor

THDv: Voltage total harmonic distortion

TSC: Thyristor switched capacitor

TSR: Thyristor switched reactor

TSSC: Thyristor switched series compensator capacitor

TSSR: Thyristor switched series compensator reactors

UPFC: Unified power flow controller

UPQC: Universal power quality conditioner

UPS: Uninterrupted power supply

VSC: Voltage source converter

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CHAPTER 1: INTRODUCTION

At the beginning of using electrical power networks, the power generation was in direct-current (DC) forms and hence there were no changes in voltage levels due to lack of using transformers. Therefore, the loads were located very close to generation to prevent voltage drops. Due to disadvantages of using DC power generations and also a lack of power electronic device technologies, alternating-current (AC) power systems relying on power transformers were firstly introduced by Nikola Tesla by the end of the 1800s. Therefore, the different voltage levels were introduced by implementing AC power systems combined with power transformers.

Later smart grids were introduced as a new paradigm to change fundamentally the way electrical energy is delivered and consumed. Although the details, configurations and standards of smart grids are yet to be finalized, it is clear that a high-speed bi-directional communication networks will be included as the backbone of the infrastructure. This will provide opportunities for online and real-time monitoring and control of transmission, distribution and end-user consumer assets for more effective coordination and usage of the available energy resources.

Recently, there has been substantial interest in reactive power as one of several supplementary services required for the reliability of the power systems due to its vital effect on power system security. Power electronic devices are becoming more popular and their applications are growing in power systems and specially in distribution networks and gaining wide attention among different users. They are extensively engaged to control a wide range of electrical active and passive loads such as variable speed drives,

uninterrupted power supply (UPS) and electric furnaces. These nonlinear loads draw harmonic currents and reactive power as well as active power from the main AC sources. The harmonic distortions were noticed in 1920s due to the telephone line interferences. Since then various standards are introduced to set the limits on magnitudes of harmonic currents and voltages. Some institutes such as International Electrotechnical Commission (IEC) and Institute of Electrical and Electronics Engineers (IEEE) specify the limits for harmonic voltages [1] while others including IEEE-Industry Applications Society and IEEE-Power Engineering Society aim to detect the effects of harmonics on power systems and introduce standards for harmonics [2]. Three classes of residential, commercial and distribution networks are investigated in the American Electric Power Distribution System [3] and their harmonic levels are reported. IEEE 519-1981 includes the IEEE standard for harmonic control and reactive compensation of static power converters [4]. There are many other activities reported regarding finding standards for harmonics in power systems [5-12].

Reactive power is relative to bus voltage levels and deficiency of enough reactive power supply leading to poor voltage profile with the possibility of voltage collapse within power systems. Moreover, reactive power and harmonic components of load current reduce the system power factor leading to an increase in transmission network losses, overheating of devices, malfunctioning and failure of electronic components (especially protection devices and relays), overloading, overheating and failure of power factor correction capacitors, overheating and failure of electric motors, overloading and overheating of distribution transformers and conductors and measurement errors in metering equipment [3-5]. Furthermore, quick variations in reactive power consumption of large loads can

lead to voltage oscillations which might cause power fluctuations within the network [13-14]. Voltage sag is a significant issue for the utilities, contributing more than 80 percent of power quality problems in the power systems [15]. Voltage sag is defined as the RMS reduction of the AC voltage at fundamental frequency for the duration of a half-cycle to a few seconds [16]. Voltage swell is another kind of voltage instability which may occur under different scenarios. For example, high penetration of photovoltaic (PV) generation is one of the main reasons for voltage rise in the system due to reversed power flow to the network [17-18]. There are however, some solutions to overcome the voltage rise such as adjusting distribution transformer ratio [19-20] or reducing power line impedances by increasing conductor sizes [21-22]. But these approaches are not able to cover all extreme scenarios. There are some modern loads which are generally based on the electronic devices such as programmable logic controllers (PLC). These devices are very sensitive to voltage fluctuations and become less tolerant to power quality problems [23] including voltage sags, swells and harmonics.

Electric power loads can be either static or dynamic [24-25]. Moreover, they can be balanced loads such as three-phase electrical motors or unbalanced devices such as single phase loads [26-27], traction loads [28] or arc furnaces [29]. Many loads such as induction motors are very sensitive to voltage imbalances and even small voltage imbalances can result in overheating and unbalanced their electromagnetic torque. Therefore, it is very important to rectify voltage imbalances in the networks.

Generally, most of power system loads are resistive-inductive. If the inductive characteristic of loads increases, the power factor of network decreases and forces the utilities to inject more current in order to maintain the same level of active power [30].

Therefore, it is recommended to provide reactive power compensation for very high inductive loads. The conventional compensation of reactive power is based on connecting shunt capacitor or inductor banks to the system through mechanical switches. However, these methods have many disadvantages such as fixed compensation, resonance, large size and weight, as well as noise and losses. By controlling the reactive power within transmission and distribution networks, maximum active power flow and voltage regulation can be achieved. This type of controller can be applied by using various topologies. Flexible AC transmission systems (FACTS) devices are used to implement these topologies to improve the power quality [31]. The static synchronous compensator (StatCom) is a shunt connected FACTS device capable of generating or absorbing reactive power and can be controlled independently of the AC power system whose output can be varied in order to maintain control of specific parameters of the electric power system [32-34]. The StatCom is basically static and does not include any rotating parts like synchronous condenser and hence StatCom provides quicker response than synchronous condenser.

Therefore, in order to compensate the loads requirements, customers or utilities need to install FACTS devices. Thus, to improve the power factor and also to achieve load balancing, reactive power is injected into the network. As a result of implementing these devices, even when the loads are inductive and unbalanced, the grid is balanced and very closer to unity power factor [35].

StatCom usually generates a balanced set of three-phase sinusoidal voltages at the fundamental frequency with controllable amplitude and phase angle. Unlike most

conventional reactive power compensators, StatCom facilitates dynamic compensation of electrical power systems and improves the utilization of existing networks [36].

As mentioned above, the use of electronic devices is growing and therefore, the emergent applications of nonlinear loads and renewable resources such as converters, variable speed drives, smart appliances, distributed generations (DGs) and storage systems is increasing the injected harmonic currents that will ultimately propagate in the network and create voltage harmonics [37]. These distortions have injurious impacts on the network operation and its components such as overheating of power transformers, motors and cables; creating harmonic resonances; causing low power factor conditions and mal-operations of protection devices [37]. The acceptable limits of harmonic current and voltage distortions are provided by the power quality standards such as the IEEE-519 [38]. According standards, consumers are responsible to keep their injected harmonic current magnitudes and current total harmonic distortion (THDi) at their point of common couplings (PCCs) below the permissible levels while utilities are required to control the voltage total harmonic distortion (THDv) of the network and the individual buses [37-38]. The most common approaches for improving power quality is to require the consumers with nonlinear loads to either reduce their harmonic injections or install (passive, active and hybrid) filters. However, these technologies are designed to limit harmonic currents at the PCC without considering the THDv of other buses and the entire network [37]. Furthermore, restriction of injected current harmonics at PCCs within the permissible levels (e.g., THDi<5% for short-circuit ratios<20 [38]) does not necessarily result in acceptable bus and network voltage distortions (e.g., THDv<5% as recommended by most standards [37-38]). There are a few options to resolve the network voltage distortion issue:

i) the precise compensation of all injected current harmonics by installing active power filters (APFs [39]) at all buses with nonlinear loads which is not a practical solution, ii) installation of universal power quality conditioners (UPQCs) at the buses with sensitive loads that may not be efficient for large systems with many sensitive consumers, iii) optimal siting, sizing and connection of active power line conditioners (APLCs) to limit the network THDv.

APLCs are enhanced APFs with a few differences including [40-51]: i) they are only installed at a few selected buses, ii) they can control THDv and percentages of individual voltage harmonics at all buses within permissible limits, iii) instead of injecting equal-but-opposite harmonic currents to fully compensate the nonlinear load distortions, their reference currents are optimized to limit the overall network THDv.

While there are many publications on APFs, the research on APLCs has been very limited [40-51] mainly due to the unavailability of online network data. However, this problem has been recently resolved with wide spread installation of smart meters in smart grids (SGs) with sophisticated communication networks. The research on APLCs can be classified into optimal siting and sizing of single [40-46] and multiple [47-51] APLC units. However, all publications on APLC siting and sizing ignore the impacts of harmonic couplings imposed by the nonlinear devices.

1.1 Research Objectives

This thesis will first review the detrimental effects of nonlinear loads such as harmonic distortions and voltage instability in distribution networks and then will introduce some solutions to compensate the harmonic distortions and improve the power quality. APLC

with PSO-based algorithm control is introduced to compensate the voltage fundamental and harmonic distortions and to maintain the entire network voltage profile within the voltage and harmonic standards. The main objectives of this thesis are:

1) Optimal siting and sizing of multiple APLCs in distorted smart grid (SG) networks to control the network THDv without and with the consideration of harmonic couplings (Chapter 5).

2) Simultaneous compensation of the network fundamental voltage fluctuations (reactive power compensation) and network voltage harmonic distortions by optimal siting and sizing of advanced APLC units with both StatCom and APF functions (Chapter 4).

To achieve these objectives, two particle swarm optimization (PSO) algorithms are first implemented that rely on the transmitted online smart meter data including the node voltage profiles to compensate network harmonic distortions. Then, they are modified to also include reactive power compensation at the fundamental frequency.

Detailed simulations are performed in Matlab/Simulink to first find the optimal locations and sizes of the APLCs in a 15-bus network with six nonlinear loads (without and with consideration of harmonic couplings) and then investigate their performance and effectiveness in online compensation of both fundamental reactive power and harmonic distortions.

The main research goals are to formulate the optimal siting and sizing of APLCs problem, define the PSO objective function and select appropriate constraints of PSO such that the following requirements are fulfilled within a 24 hour period:

1. Limit the THDv of the entire network as well as THDv of each bus to 5%.

2. Limit each individual harmonic distortion of each bus to 3%.
3. Improving the voltage profile of each bus to reach the minimum magnitude voltage of 0.9 pu.
4. Optimally allocate APLCs through the network to minimize the harmonic distortions and improve voltage profile.
5. Sizing the APLCs to achieve optimal APLC sizes.
6. Optimal operation of allocated APLCs to compensate the harmonic distortions and improve the voltage profile of the entire network.

1.2 Thesis Contributions

In this thesis, PSO-based algorithms are proposed and implemented to improve the performance of smart grid networks at the fundamental and harmonic frequencies. The main contributions are:

- Optimal siting and sizing of multiple APLCs in distorted SG networks to control the network THDv.
- Including of harmonic couplings in the APLC siting and sizing solution.
- Extending the APLC function also to include fundamental reactive power compensation (in addition to the harmonic current compensations) and also improve the network voltage profiles at the fundament frequency.
- The online optimal operation of multiple APLCs in SG networks with the availability of online bus voltage data transmitted by smart meters.

- Minimizing the THDv of each bus, the THDv of the entire network and the individual harmonic distortion of each bus while also improving bus voltage profiles.

1.3 Thesis Outline

This thesis is organized into six chapters. Chapter 2 gives an introduction to SGs and FACTS devices. It highlights the importance of FACTS devices on improving voltage profiles. It also briefly reviews some of the FACTS devices with the focus on shunt compensation devices such as StatCom. This chapter also presents reviews on APF and APLCs. Chapter 3 represents the StatCom modelling and confirms its ability to compensate the reactive power to improve voltage profile. Chapter 4 demonstrates the APLC modelling and proposes a PSO-based algorithm for APLC siting and sizing. The algorithm is implemented in 15 bus system by finding the optimal locations of APLCs and confirming their ability to compensate the reactive power and harmonic distortions of the entire network. Chapter 5 develops and improves the accuracy of the PSO solutions by also considering the effects of harmonic couplings. Finally, Chapter 6 provides the conclusions.

CHAPTER 2: FACTS DEVICES IN SMART GRIDS

2.1 Smart Grid

SGs are attaining worldwide attention of interest among consumers to increase demand-size management quality by using smart meters and sensors [52] and also improve network efficiency and reliability [53-54].

New equipment and appliances such as computers, variable speed drives, TVs, smart appliances, hybrid vehicles, PEVs, home area networks and other electronic devices are occupying every home and business. These emerging demands will need new power grid infrastructure, but will also require innovative new concepts and technologies to continue to drive the economy forward. Most utilities believe that it is time to revisit the critical infrastructure of the power grids and re-examine their abilities to drive our security and prosperity for the next 100 years. In such a case, SG configurations would be the best candidates to assure real-time information, countless choices, rapid decisions, and fast responses.

Most industries are planning to develop SGs based on the following understandings, concepts and requirements:

- First, the appliances and equipment must be able to communicate and ultimately support the optimal operation of the entire grid. This requires a simple but smart interface for these devices to operate easily in alignment with the overall operational priorities of the grid.

- Second, consumers must also have the ability to understand grid operations and be able to accordingly and wisely adjust their electricity consumption. Subsequently, there should be simple interfaces between the grid and the consumer that allow them to support the needs of the grid. Consumers must be given the chance and ability to interact with the grid and adjust the energy consumption of their homes and businesses in harmony with their lifestyle choices, values, and unique and variable requirements.
- Third, the grid must be able to absorb easily and effectively new technologies and systems such as solar panels, wind turbines, fuel cells, storage batteries and PEVs to ensure a healthy growing economy.

SGs are already being created in most countries. Technologies that created the internet and modern communication are already revolutionizing how we deliver electricity.

2.1.1 What is Smart Grid

The electric industry is to make the transformation from the conventional centralized, producer-controlled network to the less centralized and more consumer-interactive. SG makes this transformation possible by bringing the philosophies, concepts and technologies of the internet to the utility and the electric grid. The move to the SG will change the industry's business model and its relationship with all stakeholders, utilities, regulators, energy service providers, technology and automation vendors and all consumers.

It is important to realize that devices such as wind turbines, solar arrays, PEVs and smart meters are not part of the smart grid. Rather, the smart grid offers the technology that

enables us to integrate, interface with and intelligently control them to optimize the overall system operation such as efficiency, voltage profile, reliability, stability and security.

2.1.2 Benefits of Smart Grid

The future smart grid will be an automated and widely distributed energy delivery network, characterized by two-way flow of electricity and information. It will be capable of monitoring everything from power plants to customer preferences to individual appliances. It incorporates into the grid the benefits of distributed computing and communications to deliver real-time information and enable the near-instantaneous balance of supply and demand at the device level.

In terms of overall vision, the SG is [55]:

- ***Efficient*–** capable of meeting increased consumer demand without adding infrastructure.
- ***Motivating*–** enabling real-time communication between the consumer and utility in order to provide the end users the opportunity to tailor their energy consumption based on individual preferences such as price and environmental concerns.
- ***Accommodating*–** accepting green energy from virtually any fuel source including solar and wind, capable of integrating new ideas and technologies such as PEVs, charging stations and energy storage technologies.
- ***Intelligent*–** capable of sensing system overloads and controlling power flow to prevent or minimize a potential outage, operate autonomously, respond faster than humans under emergency conditions.

- ***Opportunistic*–** creating new opportunities and markets by means of its ability to capitalize on plug-and-play innovation wherever and whenever appropriate.
- ***Resilient*–** increasingly resistant to attack and natural disasters as it became more decentralized and reinforced with SG security protocols.
- ***Green*–** slowing the advance of global climate change and offering a genuine path toward significant environmental improvement.
- ***Quality focused*–** capable of delivering a high quality of electricity to consumers which is free of sags, swells, spikes, harmonics, disturbances and interruptions.

2.2 Facts Devices

Power utilities are facing many challenges due to increasing complexity in their operation and structure and also growing integration of renewable energies. Voltage instability including voltage sag, swell and voltage harmonics is one of the most problems that power utilizes are facing with [13]. There are some loads that are sensitive to disturbances and become less tolerant to power quality problems [56]. FACTS devices are introduced to overcome these problems and solve voltage instabilities and also improve the power quality. The use of FACTS devices is back to 1970s when the static VAR compensator (SVC) was first established. FACTS devices have started with the growing capabilities of power electronic components. Since then a large attention was put on the development of FACTS devices. They offer many benefits to the power networks including increasing the capacity of installed networks, reduce the circulation of reactive power in transmission lines, improve the productivity of the generators, minimize the number of network

shutdowns and improve voltage stability [57]. FACTS devices are considered as both dynamic due to fast controllability of devices provided by power electronics and static because they have no moving parts.

In general, there are two main types of converters with gate turn-off switches which are used in FACTS devices including voltage source converter (VSC) and current source converter (CSC).

The VSC can be a boost converter in the ac to dc direction or a buck converter from dc to ac direction, while CSC is a buck converter in the ac to dc direction and a boost converter from dc to ac direction [58]. From an overall cost point of view, mostly VSCs have been used and therefore, it is the basis of most FACTS controllers [59-61]. The comparison of VSC and CSC is made by [62-63]. Lower initial costs and higher efficiency of VSCs make them more popular in FACTS device applications. Moreover, CSCs have extra losses caused by the linked inductor and also the extra diodes.

Fig. 2.1 shows the principle of VSC and CSC. As represented in Fig. 2.1a, the VSC is comprised of dc capacitor as its voltage source connected to switching devices parallel with the reverse diode. Fig. 2.1b shows a CSC consists of the dc reactor as its current source connected to the switching devices series with a diode.

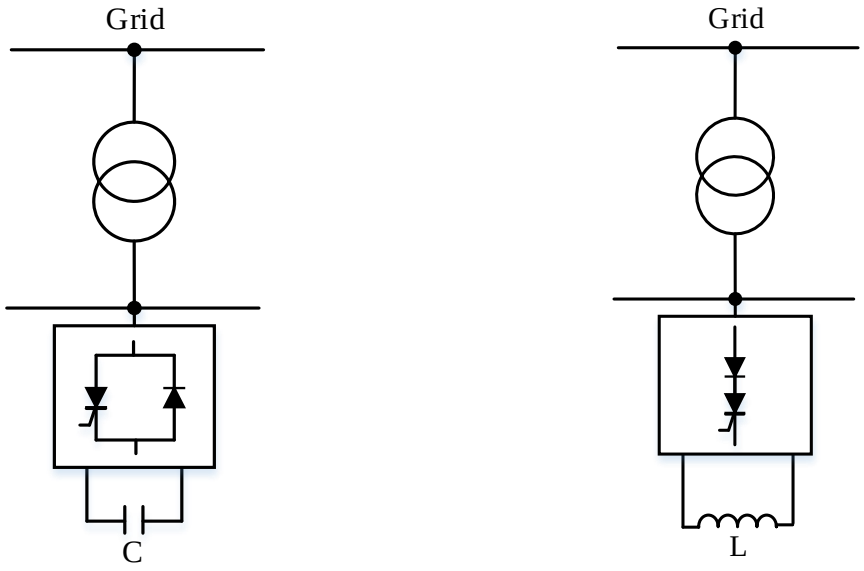


Figure 2.1: Shunt FACTS devices with; (a) VCS, (b) CSC [31]

By applying appropriate topology for VSC, a controllable output voltage with any magnitude and phase angle can be achieved. If there is no dc power source connected to the VSC and just dc capacitor is used as a dc device, the converter can work as a reactive power compensation and is not able to exchange active power. Therefore, the ac output voltage of VSC is maintained at 90 degrees leading or lagging with reference to the ac current. On the other hand, by applying appropriate topology for CSC, a controllable output current with any magnitude and phase angle can be achieved. Fig. 2.2 demonstrates different types of FACTS devices based on different connection structures. In general FACTS devices can be connected to the grid in shunt (Fig. 2.2a), series (Fig. 2.2b) or series-shunt (Fig. 2.2c).

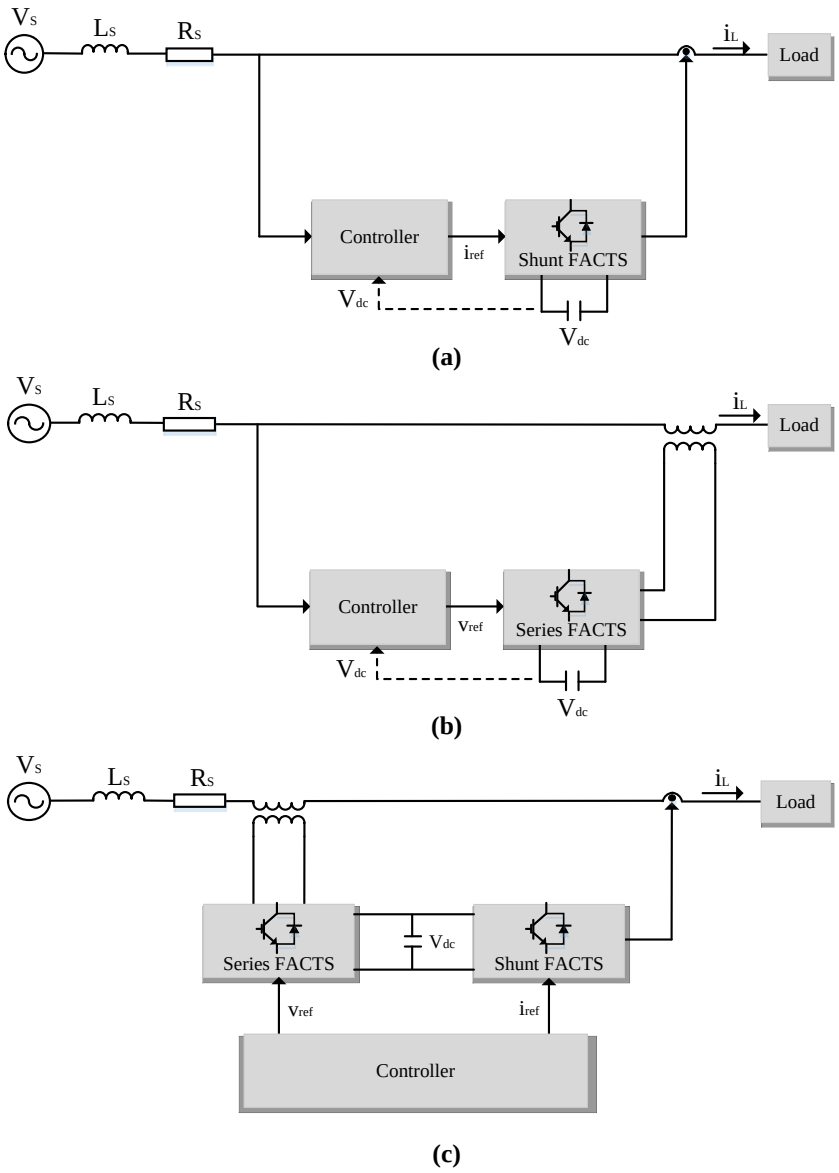


Figure 2.2: FACTS device connection topologies; (a) shunt, (b) series, (c) series-shunt [32]

Different connection types and switching devices of converters result into several different operating features. Therefore, the compensation of reactive power can be divided to the three main groups [64]. The first group is conventional mechanically switched devices including fixed shunt reactor (FR), fixed shunt capacitor (FC), mechanical switched shunt reactor (MSR) and mechanical switched shunt capacitor (MSC).

Second group is known as thyristor-based devices including force-commutated devices such as integrated gate-commutated thyristor (IGCT), insulated gate bipolar transistor (IGBT), gate turned-off thyristor (GTO) and MOS-controlled thyristor or self-commutated devices which are thyristor controlled reactor (TCR), thyristor switched capacitor or reactor (TSC/TSR), static VAR compensator (SVC), thyristor switched series compensator capacitor or reactors (TSSC/TSSR), thyristor controlled series compensator capacitors or reactors (TCSC/TCSR) [65], thyristor controlled braking resistors (TCBR), thyristor controlled phase shifting transformers (TCPST), thyristor controlled phase angle regulator (TCPR) and line commutated converter compensator (LCC).

The last group is identified as converter-based devices including StatCom, static synchronous series compensator (SSSC) [66], unified power flow controller (UPFC) [67], interline power flow controller (IPFC) [68] and self-commutated compensator (SCC).

Fig. 2.3 demonstrates some of these devices including TSR/TCR, TSC, TCSR/TSSR and TCSC/TSSC.

The conventional thyristor devices have only turn-on control and their turn-off capability depends on system conditions. Some devices such as GTO, IGBT, IGCT and other devices have turn-on and turn-off capability. However, compared to devices without turn-off capability, they are more expensive with higher losses. The conventional thyristor-based converters without turn-off capability can only be used in CSCs while devices with turn-off capability can be used in both VSCs and CSCs.

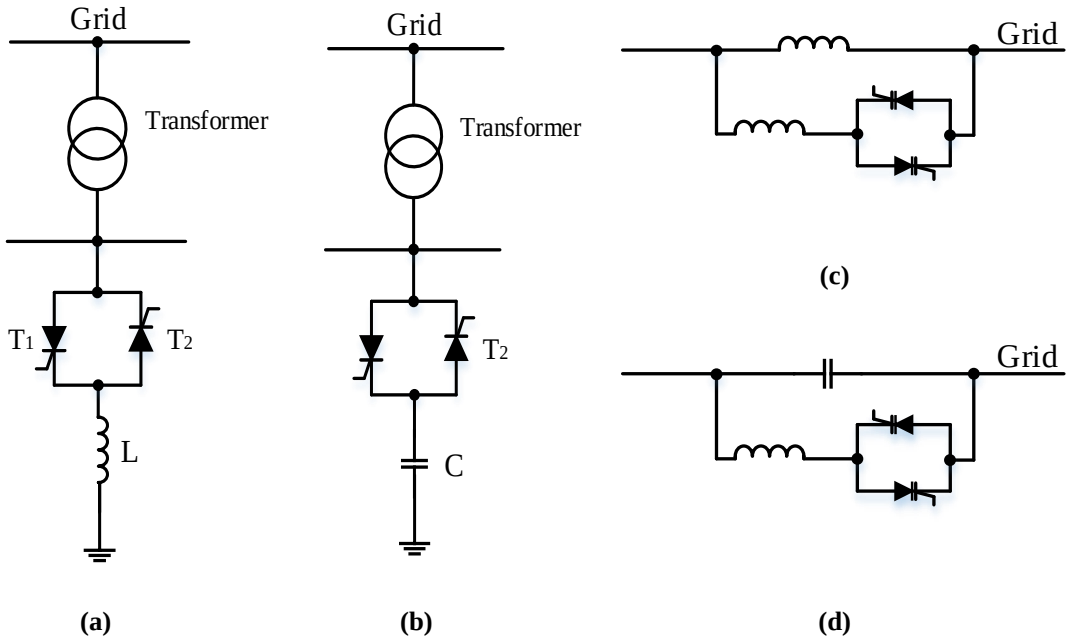


Figure 2.3: FACTS device building blocks; (a) TSR/TCR, (b) TSC, (c) TCSR/TSSR, (d) TCSC/TSSC [31]

The TCR is a shunt compensator which regulates the equivalent inductive reactance of distribution network line by adjusting the phase angle. It consists of bidirectional thyristor series with the reactor. The TSC is similar to TCR but using power capacitor in series with the bidirectional thyristor. The constraint of these compensators is that they only can perform continuous inductive or discontinuous capacitive compensation while most of the applications need continuous inductive or capacitive compensation. Then SVC is introduced as a device able to deliver continuous inductive and capacitive compensation. Fig. 2.4 shows classification of FACTS devices based on four groups of series, shunt, combined series-series and combined series-shunt converters.

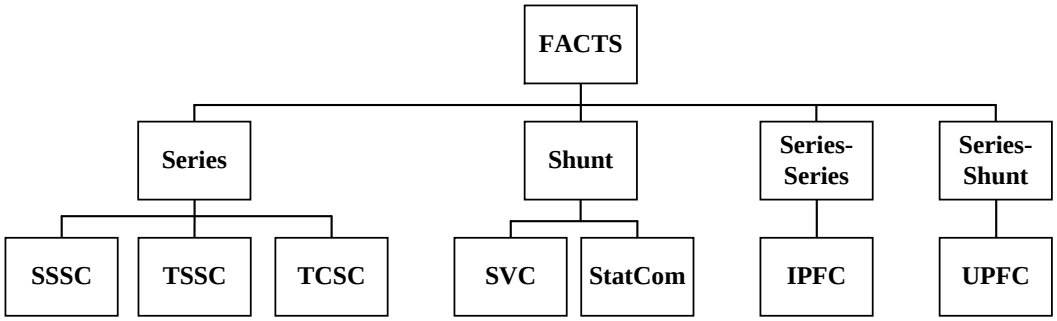


Figure 2.4: FACTS devices based on different connection topologies [31]

2.3 Control Methods of Shunt Converters for FACTS Applications

The basic shunt FACTS device control methods are studied based on PWM controls of VSC. However, the recent advanced shunt FACTS devices are based on multilevel VSCs. It is imperative to reduce the VSC losses to increase its efficiency. Among different losses of VSCs, switching losses are very important and thus, proper control method should be applied to limit the overall losses. Among different control methods, sinusoidal PWM (SPWM), selective harmonic elimination PWM (SH-PWM), space vector PWM (SV-PWM) and hysteresis control PWM (HYS-PWM) are strong and robust control methods [69-72].

Some other control methods such as linear, fuzzy, sigma-delta, optimized and proportional-resonant control methods are used in shunt FACTS devices [73-75].

2.3.1 Sinusoidal PWM (SPWM)

This method has been used extensively in shunt FACTS devices due to its easy structure and simple mathematical requirements. Even very basic and simple microcontrollers can

implement this simple method. It works based on comparing a triangle carrier waveform with a sinusoidal modulation signal to get the proper switching.

2.3.2 Space Vector PWM (SV-PWM)

This method is more suitable to be used in multilevel converters since it can produce 15 percent higher output voltage than the other control methods.

The circuit model of a three-phase voltage source PWM inverter is shown in Fig. 2.5. In this model, S1 to S6 are the six power switches, which are controlled by the switching variables a, a_1, b, b_1, c and c_1. When an upper transistor is switched on (i.e., when a, b or c is 1), the corresponding lower transistor is switched off (i.e., the corresponding a_1, b_1 or c_1 is 0). Therefore, the on and off states of the upper transistors S1, S3 and S5 can be used to determine the output voltage.

The relationship between the switching variable vectors (a, b, and c) and the line-to-line and phase voltage vectors are given by Eqs. 2.1 and 2.2, respectively:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.1}$$

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.2}$$

There are eight possible combinations of on and off patterns for the power switches. Based on Eqs. 2.1-2.2, the eight switching vectors, output line to neutral and line-to-line voltages in terms of dc-link (V_{dc}), are given in Table 2.1.

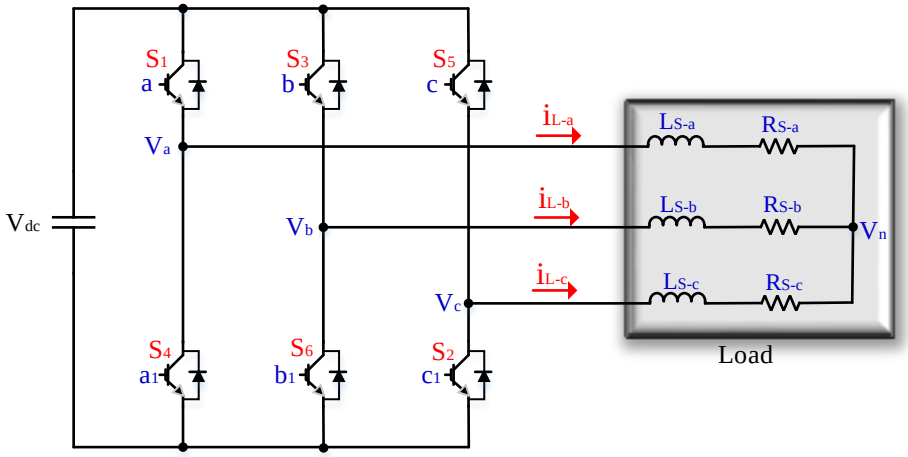


Figure 2.5: Three-phase voltage source PWM inverter [33]

According to Table 2.1, the six nonzero vectors (V1-V6) shape the axes of a hexagonal (Fig. 2.6) and feed electric power to the load.

Table 2.1: Eight inverter voltage vectors (V0-V7)

Voltage vectors	Switching Vectors			Line to Neutral Voltage			Line to Line Voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V0	0	0	0	0	0	0	0	0	0
V1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V2	1	1	0	1/3	1/3	-2/3	0	1	-1
V3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V4	0	1	1	-2/3	1/3	1/3	-1	0	1
V5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V6	1	0	1	1/3	-2/3	1/3	1	-1	0
V7	1	1	1	0	0	0	0	0	0

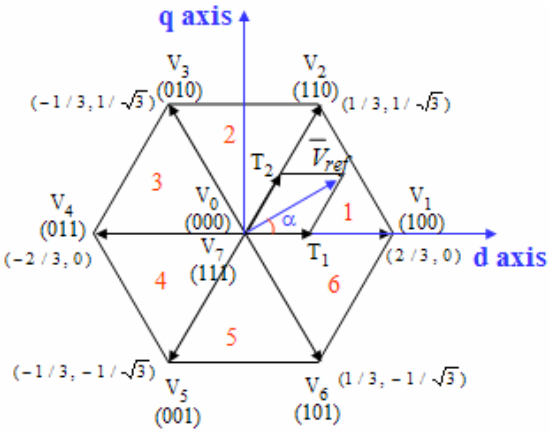


Figure 2.6: The basic switching vectors and sectors [33]

The angle between any adjacent two non-zero vectors is 60 degrees. Meanwhile, the two zero vectors (V0 and V7) apply zero voltage to the load. The objective of space vector PWM technique is to approximate the reference voltage vector V_{ref} using the eight switching patterns [76].

Fig. 2.7 shows a sample of SV-PWM control for StatCom application. The switching signals of SV-PWM modulator is produced by using the switching vector in complex space of (d, q). The three-phase voltage vectors are generated by power source pass α-β and d-q transformer blocks to be converted to two phase vectors. Then d-axis current and q-axis current are compared with their related reference currents. Then the error passes through PI controller and finally the SV-PWM generates the switching signals of the StatCom. Moreover, the Clark transformation is converting the three phase load currents to d-axis for controlling the dc voltage of the device and q-axis for controlling the reactive power of the network [77].

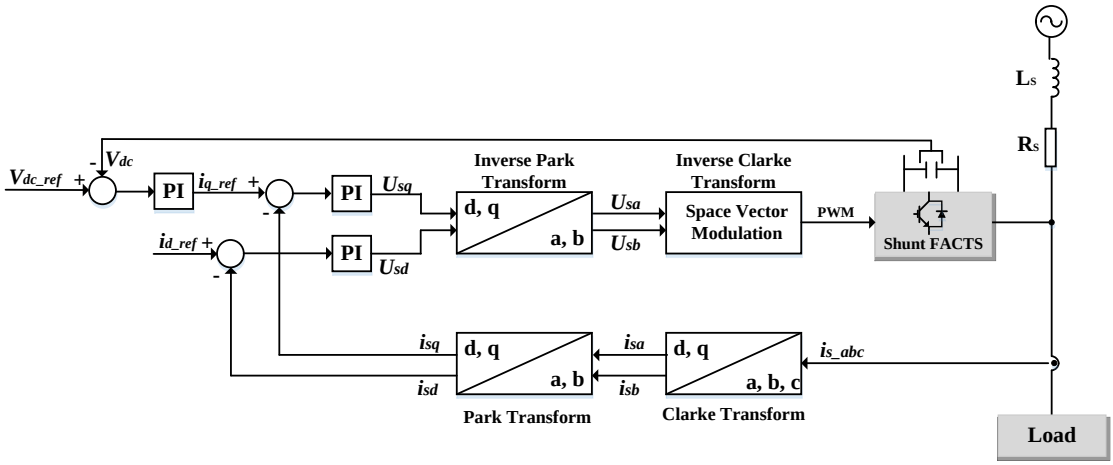


Figure 2.7: Space vector control for shunt FACTS devices [32]

2.3.3 Selective Harmonic Elimination PWM (SH-PWM)

This method eliminates predefined harmonic orders by using fundamental frequency theory. Therefore, the exact switching angles should be defined to eliminate the selected harmonics [78].

2.3.4 Hysteresis Band PWM (HYS-PWM)

Linear and nonlinear methods are two main groups of current controlled PWM techniques. Linear techniques comprise of feedback, PI and predicted controllers while nonlinear techniques are ramp, hysteresis and delta modulator controllers. Among these controllers, hysteresis band is more popular due to its simple structure and easy implementation. The HYS-PWM by performing proper switching of VSC, allow the load current to oscillate between the upper and lower limit of hysteresis band defined by the controller. The load currents are measured and then compared to their reference values [79].

2.4 Multilevel Power Converters

By growing the power system and increasing the power demand, many customers began to use electrical loads with higher power devices. Meanwhile, there are a big number of loads operating at medium voltages with medium power demands of megawatt power levels. For this level of voltage and power, it is very hard to use only one semiconductor switch for power quality purposes. Thus, multilevel converters were introduced to overcome these problems and to be used in medium voltage high power conditions. Moreover, another advantage of multilevel converters is using renewable energies such as wind, PV and fuel cells as an energy sources or interface between them [80-82]. The first three-level converter was introduced 1975 and then several topologies were developed [83-92]. The basic concept of multilevel converters is to use several semiconductor switches in series to achieve higher power ratings. Also, the dc source elements (capacitors, batteries or renewable energy voltage sources) are connected in series and the communication of power switches, combine these dc sources to reach high voltage levels at the output.

The most important benefits of multilevel converters over the conventional two-level converters are: i) staircase output voltage which not only results to have low distorted output voltage, also reduces the dv/dt stresses and consequently lower electromagnetic compatibility problems, ii) higher power outputs, iii) they draw input currents with low distortion, and iiii) they can operate at both high switching frequencies or fundamental switching frequencies.

However, multilevel converters have some disadvantages such as using a higher number of semiconductor switches which make their control topology to be more complicated and the overall system to be more expensive.

Many multilevel converter topologies are proposed by different researchers. Among them, three main multilevel converter structure are defined including diode clamped, cascaded H-bridge and flying capacitor multilevel converters. Moreover, many modulation techniques and control strategies are introduced such as SH-PWM, SPWM, SV-PWM, HYS-PWM. The multilevel converters can be used in several applications such as electrical medium voltage motors [82] [93], FACTS devices [94], interface for renewable energy systems [95] and traction drive systems [96]. Multilevel converters also have been used as variable speed drives and static SVCs [97-107].

2.4.1 Multilevel Power Converter Structures

The three multilevel converter structures including diode clamped, flying capacitor and cascaded H-bridge multilevel converters are described in this section.

2.4.1.1 Diode-Clamped Multilevel Converter

The first diode-clamped multilevel converter (DCMC) was introduced first by [84] in 1981 with three level diode clamped converter topology. Later on the 1990s, more DCMC topologies of four, five and six level diode-clamped converters have been developed. The DCMC uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To generate *m*-level phase voltage waveform, a DCMC needs *m-1* capacitors on the dc

bus. A three-phase, five-level DCMC is shown in Fig. 2.8. The dc bus consists of four capacitors: C1, C2, C3 and C4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes.

Table 2.2 represents the output voltage levels possible for phase A of this inverter. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has four complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch is turned off. The complementary switch pairs for phase leg A are (S_{a1} , $S_{a'1}$), (S_{a2} , $S_{a'2}$), (S_{a3} , $S_{a'3}$), and (S_{a4} , $S_{a'4}$). Table 2.2 also shows that for a five-level inverter, a set of four switches is on at any given time.

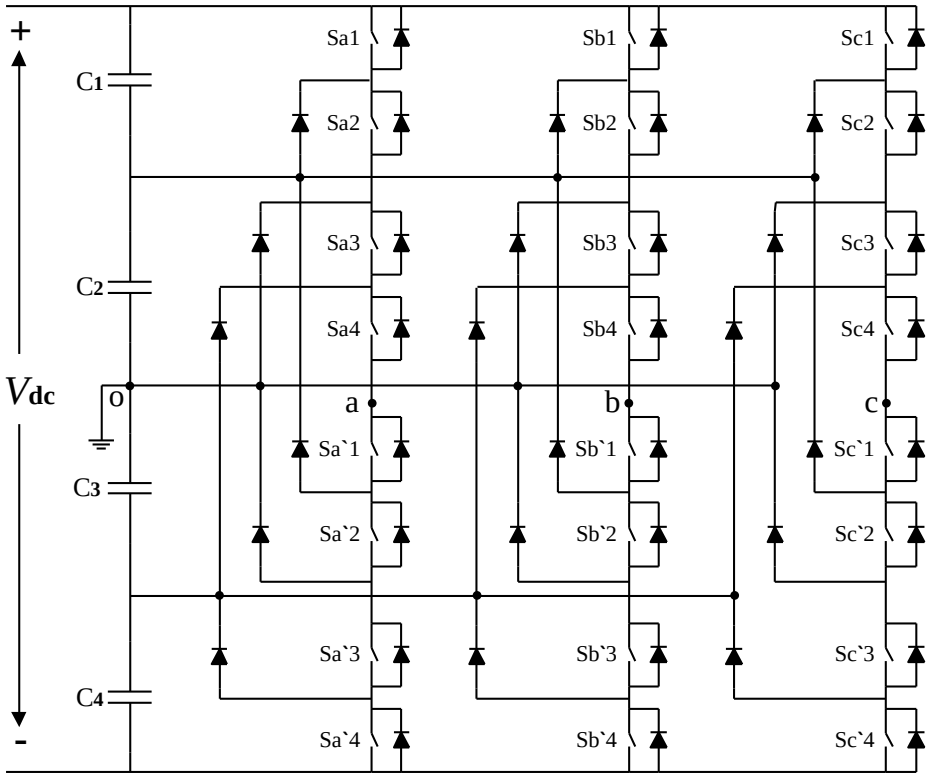


Figure 2.8: Three-phase five-level DCMC [80]

DCMCs have some advantages such as high efficiency for fundamental frequency switching, minimization of capacitance requirements of the converter due to share a common dc bus among all phases. Therefore, back to back topology can be used in this converter and is suitable for high voltage converters and speed drives. However, these multilevel converters have some disadvantages. One of them is the number of clamping diodes which are quadratic of the level numbers which can be increased dramatically with increasing the number of levels [80].

Table 2.2: Five-level inverter voltage levels of DCMC with corresponding switch states

V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_1 = 0$	0	0	0	0	1	1	1	1
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_4 = 3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0

2.4.1.2 Flying Capacitor Multilevel Converter

This multilevel converter was introduced by [108] in 1992. The structure of flying capacitor multilevel converter (FCMC) is similar to DCMC except that this converter uses capacitors instead of diodes. Fig. 2.9 shows the structure of FCMC. As can be seen, this topology has a ladder structure of dc capacitors for which the voltage on each capacitor differs from that on the next capacitor. To produce *m*-level staircase output voltage, *m*-1 capacitors in the dc bus are needed. Each phase leg has an identical structure. The size of the voltage rise between two capacitors determines the size of the voltage levels in the

output waveform. Table 2.3 represents the possible switch combination of the voltage levels and their corresponding switch states.

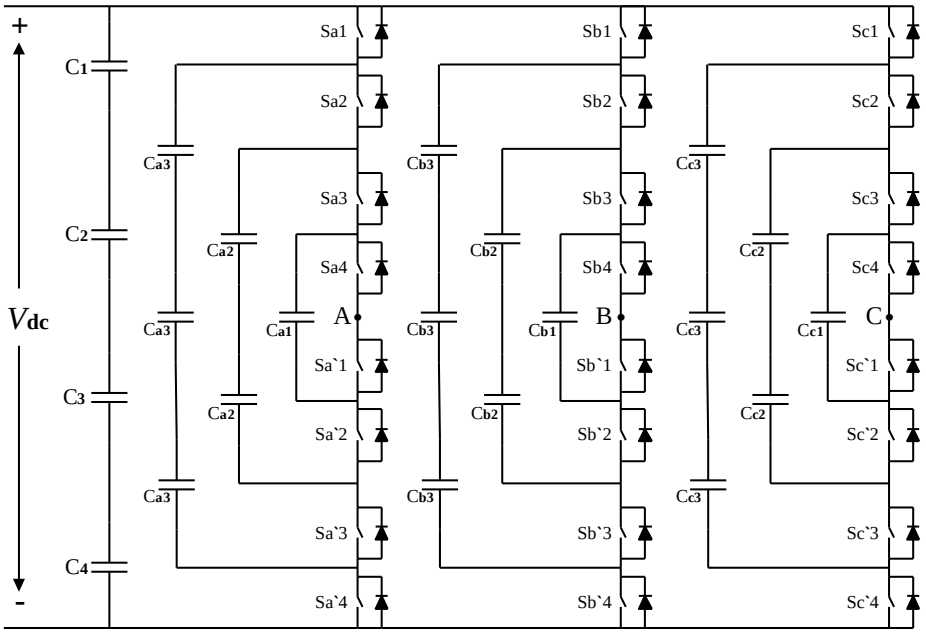


Figure 2.9: Three-phase five-level FCMC [80]

Table 2.3: Switch combinations of five-level FCMC voltage levels and their corresponding switch states

V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_3	S_4	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_1 = 0$	0	0	0	0	1	1	1	1
$V_2 = V_{dc}/4$	1	0	0	0	1	1	1	0
$V_3 = V_{dc}/2$	1	1	0	0	1	1	0	0
$V_4 = 3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0

2.4.1.3 Cascaded Multilevel Converters with Separated DC Sources

The cascaded multilevel converter (CMC) synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells or

solar cells. This new converter can avoid extra clamping diodes or voltage-balancing capacitors. The number of output phase voltage levels is defined by *m= 2N+1*, where *N* is the number of DC sources.

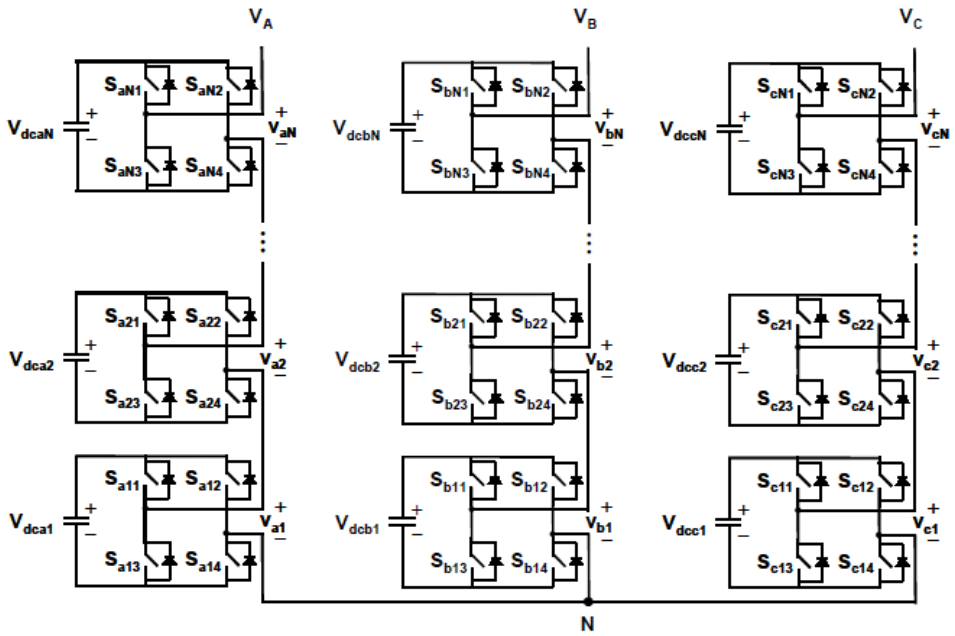


Figure 2.10: Three-phase (2N+1)-level CMC [80]

A three-phase structure of an m-level cascaded inverter is illustrated in Fig. 2.10. Each dc source is connected to separated inverter to produce three output voltages of $+V_{dc}$, 0 and $-V_{dc}$. This can be achieved by a different combination of switches S1, S2, S3 and S4. If switches S1 and S4 are turned on, $+V_{dc}$ is generated while this value is $-V_{dc}$ if switches S2 and S3 are turned on. Also, the output voltage is zero when switches S1 and S2 or S3 and S4 are turned on. Moreover, the output voltages of all inverters are connected in series in each phase to produce the synthesized voltage waveform of the sum of the inverter outputs.

CMCs can be used for interface with renewable energy sources, static VAR generation and battery based applications. They are ideal for connecting renewable energy sources

to an AC power networks because they need separated dc energy sources such as PV or fuel cells. Traction drive is another application of CMCs which is used in electric vehicles [103].

CMCs have some advantages over other multilevel converters. The number of output levels is more than the twice number of dc sources and due to the modularity of converters in CMCs, it is easier and quicker to process and manufacture them. The drawback of this converters is a requirement of dc sources for each module [106].

Some other researchers have proposed a different CMC topology which including the different value of dc levels instead of equal values (usually dc sources are multiple of each other) [104-105]. Moreover, they use a combination of two switching topologies of PWM switching and fundamental frequency switching. This topology enables the CMCs to have more output level comparing to the conventional CMCs.

2.4.2 Comparison among Multilevel Converters

According to the standards, the reliability of the system is proportional to the number of its components. For comparing different multilevel converters, the clamping diodes are used only in DCMC and are not required in the FCMC and CMC, while balancing capacitors are only used in FCMC. Based on Fig. 2.11, CMCs required the minimum number of total main components. However, they need more capacitors compared to DCMCs, but this is not considered as a disadvantage. Circuit layout flexibility is one of the advantages of using CMCs. This fact makes CMCs be more popular and easier to be built. Each level in CMCs has the same structure and also there are no extra voltage-balancing capacitors or clamping diodes which are required in FCMC and DCMC. To

achieve a higher number of output levels, only adding more numbers of modules is needed.

To achieve high voltage levels in FCMCs, an undesirable amount of capacitors is required. For an instance, in CMCs only three capacitors are required to get seven level output while this number is 15 in FCMCs plus six dc link capacitors.

Table 2.4 compares the power component requirements per phase leg among three multilevel converters of DCMC, FCMC and CMC.

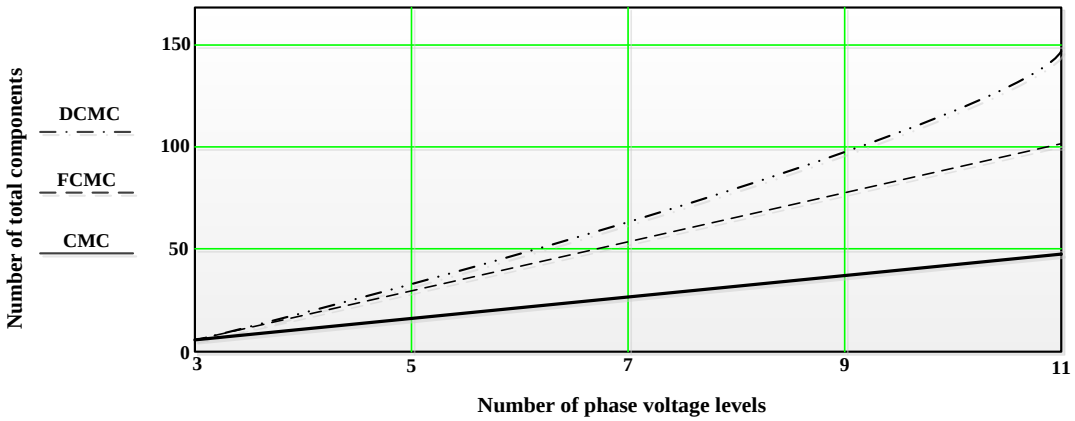


Figure 2.11: Number of components required in the multilevel converters as a function of the number of voltage levels [80]

Table 2.4: Comparison of power component requirements per phase leg among three multilevel converters

Converter Configuration	DCMC	FCMC	CMC
Main Switching Devices	2(n-1)	2(n-1)	2(n-1)
Main Diodes	2(n-1)	2(n-1)	2(n-1)
Clamping Diodes	(n-1)(n-2)	0	0
DC Bus Capacitors	n-1	n-1	(n-1)/2
Balancing Capacitors	0	(n-1)(n-2)/2	0
Total Components	n^2+2n-3	(n^2+8n-8)/2	(9/2)(n-1)

2.4.3 Asymmetric Multilevel Converters

The asymmetric hybrid multilevel converters synthesize the output voltage waveforms with lower harmonic contents compared to other multilevel converters. This advantage is achieved by using distinct voltage levels in different modules, which can generate more levels in output voltage waveform and reduces the THD ratio while preventing to increase the number of switching devices and sources. Usually, multilevel converters use equal dc voltage value for each cell. However, it is possible to increase the maximum number of output voltage levels by using different dc voltage values. Therefore, asymmetric multilevel converters can provide a higher number of output voltage levels compared to symmetric multilevel converters [109-111]. Consequently, due to lower THD of the output voltage, the filtering devices can be removed or can be selected optimally small and efficient and therefore, the converter efficiency is increased. The relationship among the dc-link voltages to provide a regularly stepped output voltage waveform could be binary (power of two) or trinary (power of three). The maximum numbers of output voltage levels are given by:

$$L_{asymmetric}^{binary} = 2^{(N+1)} - 1 \tag{2.3}$$

$$L_{asymmetric}^{trinary} = 3^{N} \tag{2.4}$$

Fig. 2.12 demonstrates a three-phase asymmetric multilevel converter. In these converters, if the ratio step of dc sources is binary then the output voltage levels of the converter are 15 levels (Eq. 2.3), while if this ratio is trinary, then 27 level output voltage is generated (Eq. 2.4). In these multilevel converters, it is possible to use high switching

frequency for one cell while the other cells can use low switching frequency. Therefore, the main cell can use IGBT while the rest use GTO as their switching devices [112].

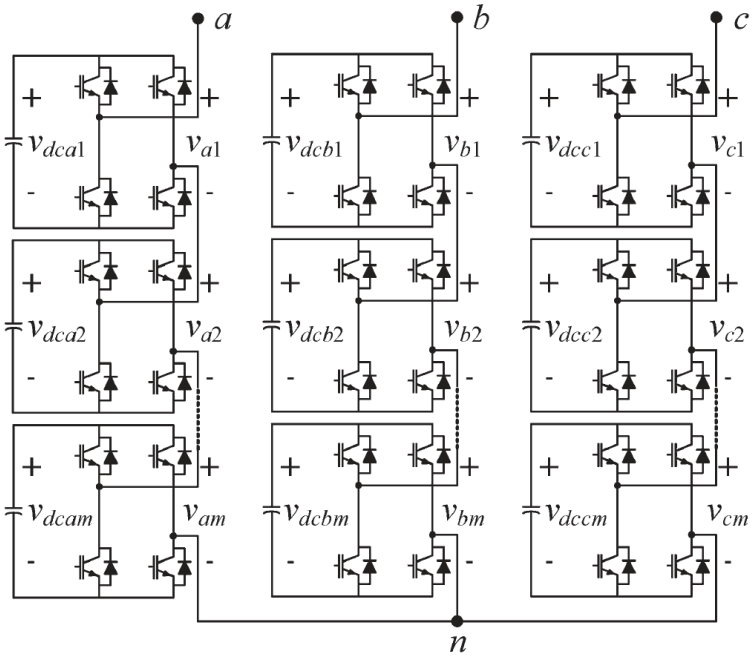


Figure 2.12: Three-phase asymmetric multilevel converter [109]

The switching of multilevel converters is divided to fundamental switching frequency and high switching frequency PWM. Fig. 2.13 illustrates different types of control techniques for multilevel converters.

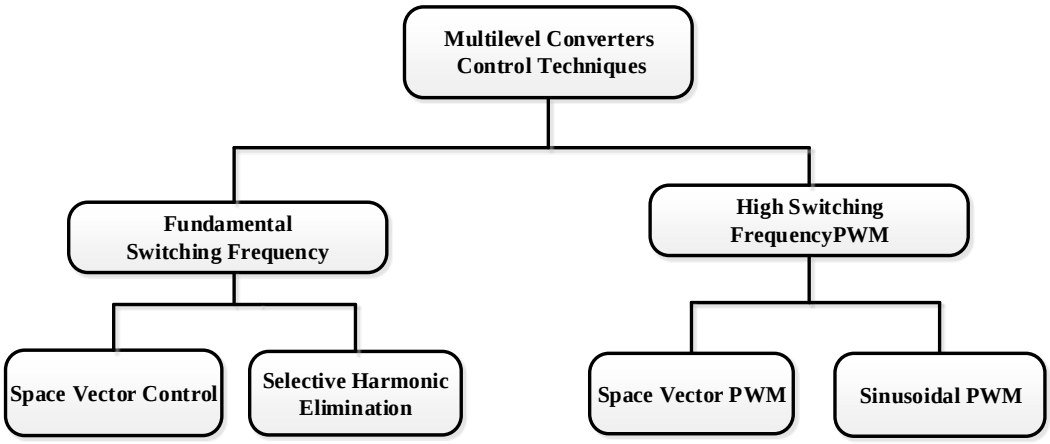


Figure 2.13: Different control techniques for multilevel converters [69]

2.5 StatCom

Power utilities are facing many challenges due to increasing complexity in the operation and structure of distribution systems as well as the growing appetite to increase the penetration of renewable energy resources. Voltage instability issues such as voltage sag and swell are among the main problems that power utilizes are facing [113-114]. Voltage sag and swell are the two most common issues contributing to the power quality problems in power systems [15]. The consequences of voltage sag can lead to partial or full power interruption in the system. The well-known solution to protect the network from voltage quality and voltage collapse problems is to inject or absorb reactive power to or from the network. High penetration of PV power generation has brought significant technical challenges to the distribution systems such as voltage rise, protection coordination and harmonic distortions. Among these problems, over-voltage caused by reverse power flow has become a significant issue for power systems [115]. There are a few solutions to overcome this issue such as changing the transformer ratio to have lower secondary voltage [20] or decrease the line impedances by changing conductor sizes [21]. However, these methods are not able to cover all problems. In addition, the voltage instability has harmful effects on most electronics devices. For example, modern industrial equipment are based on electronic devices which are very sensitive to disturbances [56] such as voltage sags, voltage swells and harmonics. Various methods have been proposed to improve the voltage instability.

The main approach is to compensate the reactive power. Capacitor banks were one of the first methods for reactive power control. They can be used to control the reactive power and improve the power factor by injecting the necessary reactive power of a connected

point and thus reduce the flow of reactive power in related lines which consequently improve the voltage profile of connected points. The amount of generated reactive power by capacitor bank is:

$$Q_C = \omega C V_C^2 \tag{2.5}$$

where ω is the angular frequency of the network, C represents the capacitance of the module and V_c is the amplitude voltage of the connected bus.

The VSC-based StatCom is gained more attention among other converters due to its high-quality technology compared to thyristor-based SVC and is used as a dynamic shunt compensator. On the other hand, GTO-based VSCs and also IGBTs and IGCTs are used in high power rating controllers. However, their implementation is mainly still in low to medium rating controllers due to some limitations.

The conventional compensation of reactive power such as shunt capacitor or inductor banks has many disadvantages such as fixed compensation, resonance, large size and weight, as well as noise and losses. However, these are not ultimate solutions due to uncontrollable reactive power compensation and high costs of installing new feeders. Recent approaches include the application of StatCom have proven their effectiveness not only for voltage instability correction but also for other power quality issues such as flicker suppression, power factor correction and harmonic control [116-118]. The main features of StatCom are quick response time, exceptional dynamic characteristics under various operating conditions, less space requirement and more flexible in operation. StatCom is a reactive power compensation device that is shunt connected to the AC distributions systems. It is defined as a self-commutated switching converter with the energy source (usually capacitor) connected to the power network injects or absorbs

reactive current through the power network to regulate the amount of reactive power of the connected point by exchange reactive power between the converter and connected network. In general, when two ac power sources of the same frequency are connected to each other, the active power flows from leading to lagging source. As a result, in StatCom the voltage angle of converter is tuned to be the same as the connected network to prevent active power exchange between two sources. However, in practice there is a small angle shift between two sources in order to compensate the losses of the converter. The reactive power flow is specified by the voltage magnitude difference between the converter and network. Therefore in StatCom, the reactive power flow can be controlled by changing the fundamental component of converter voltage. The StatCom is located between generators and loads. These principles make StatCom act as a source or either a load in power networks.

The more recent approach to improve the voltage profile is based on the application of distribution StatCom (D-StatCom) with the additional capability of sustaining reactive current at low voltage levels that can be utilized for both voltage and frequency support by replacing capacitor banks with batteries as the energy storage devices [119]. D-StatCom injects a compensation current into the system to correct the power quality disturbances such as voltage sag and swell. Its applications are mainly for protecting sensitive loads that may be significantly affected by oscillations in the system voltage and current [120-121].

As mentioned before, StatComs are considered as a FACTS family members who can replace SVCs in distribution networks. The StatCom is capable of improving the power quality of the distribution networks by performing several compensations such as voltage

flicker, sag and swell control, dynamic voltage control, damping the oscillations of power lines, and active and reactive power control of distribution networks. These achievements are reachable since StatCom uses voltage source converters, developed control methods and on-off switches.

As mentioned, StatComs mostly use VSC converters in most of their applications. These converters comprise of self-commutating solid-state turn-off switches such as IGBT, GTO and so on with a reverse diode connected in parallel to them. These switches can work with a different mode of operations including PWM mode with high switching frequencies in a cycle or square-wave mode with once per cycle or selective harmonic elimination with low switching frequencies. StatCom in general consists of six pulse VSC-converter, a dc bus connected to dc energy storage device, a controller and a coupling transformer interfacing the converter output and connected system voltage. The relation of active and reactive power injected by StatCom at the PCC is based on Eq. 2.6.

$$S = P - jQ = 3\frac{V_S V_C}{X_L}\sin\alpha - j3\left(\frac{V_S V_C}{X_L}\cos\alpha - \frac{V_S^2}{X_L}\right) \tag{2.6}$$

where S is the apparent power, P active power, Q reactive power, V_S phase voltage of connected bus, V_C fundamental output phase voltage of StatCom, X_L leakage reactance ($X_L = 2\pi fL$, f system frequency) and α the phase angle between V_S and V_C .

As can be seen from Eq. 2.6, if the phase angle of StatCom output voltage is controlled to be same as the network voltage angle, α will be zero and consequently there will be no active power exchange between two sources. Thus, the exchange of active power depends on the amount of α . In Eq. 2.6, if α equals to zero then Eq.2.7 is resulted:

$$Q = 3\frac{V_S}{X_L}(V_C - V_S) \tag{2.7}$$

To achieve optimal reactive power control, StatCom injects a current in quadrature with the network voltage (V_S) lagging or leading and react as an active or reactive load for the network. The magnitude and phase angle of injected current of StatCom are determined by the magnitudes of V_S, V_C and the phase difference between them (α). When the converter voltage (V_C) is bigger than network voltage (V_S), the StatCom injects reactive power to the network and StatCom operates in a capacitive mode; and when V_S is greater than V_C, the StatCom operates in inductive mode and absorbs reactive power from the connected network. For no reactive power exchange between StatCom and network, the magnitude of two sources is the same ($V_S = V_C$).

2.5.1 Comparison of SVC and StatCom

StatCom has some benefits over SVC such as smaller size due to the elimination of capacitor banks and reactors and faster response. Also, StatCom can be considered as a controllable current source beyond the limitation of bus voltage. Moreover, due to high dependency of SVC on the supply voltage (Eq. 2.5), its reactive power compensation is decreased with a decrease in supply voltage, while the StatCom can supply required reactive power even at low supply voltage. This feature of StatCom especially improves the transient stability of the system. On the other hand, the SVC is cheaper than StatCom and is a better choice for applications which need very high reactive power compensation due to its lower losses [31].

Fig. 2.14 shows an equivalent circuit of StatCom including dc source (capacitor), converter and filter. The filter consists of a resistance Rs and inductance Ls. The main objective of VSC is to produce almost pure sinusoidal AC voltage with the minimum of harmonic distortions from a dc voltage source. In Fig. 2.14 the series inductance (Ls) represents the leakage of the transformer and the resistance (Rs) signifies the active losses of the transformer and converter.

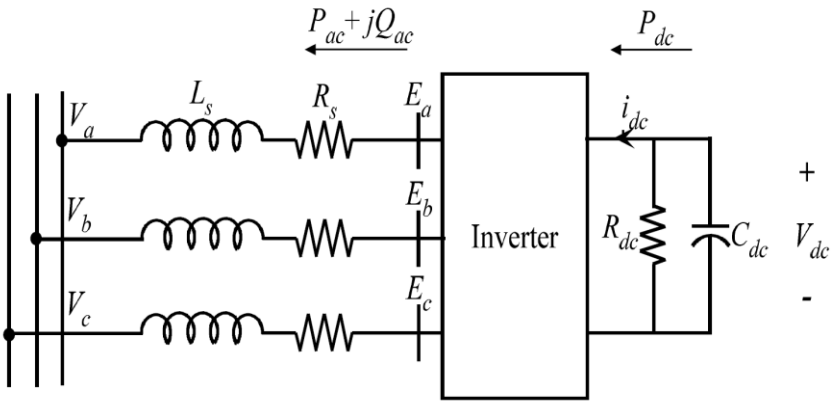


Figure 2.14: Equivalent circuit diagram of StatCom [33]

2.6 Harmonics as a Power Quality Problem

By developing the power electronic technology, the use of nonlinear loads in commercial, industrial and residential installations such as rectifiers, converters, adjustable speed drives, arc furnaces and computer power supplies is growing rapidly. As a result, the harmonic levels in power distribution networks are increased. These loads inject the harmonic currents into the system and distort the voltage waveforms. This distortion causes various unwanted effects for the linear loads connected at the same PCC. Harmonics were detected first around the 1920s [2]. Harmonic content (distortion), in the

system are measured based on the ratio of the amplitude of each harmonic to the amplitude of the fundamental component of the supply system voltage or current.

According to IEEE Standard 519-1992 [38], the maximum allowable THDv for distribution lines, i.e. 69 kV and below, is 5% and for each individual harmonic voltage is limited to 3%. The current harmonic limits differ based on the short circuit strength of the system. Basically, if the system is able to handle more harmonic currents, customers also are allowed to inject more harmonic currents. Tables 2.5 and 2.6 show the IEEE Standard 519-1992 for harmonic voltage and harmonic current, respectively.

2.6.1 Harmonic Sources

Generally, there are three main groups of harmonic sources including i) saturable devices, such as transformers, ii) arcing devices, such as arc welders and arc furnaces and iii) power electronic devices such as variable speed drives, battery chargers and most of rectifier and inverter applications.

2.6.2 Effects of Harmonics

Harmonics in power systems can have injurious impacts on the network operation and its components, such as overheating of power transformers, motors and cables; creating harmonic resonances; causing low power factor conditions and mal-operations of protection devices [37]. Therefore, it is essential to compensate these distortions to minimize their effects on the system and to increase the system efficiency.

Table 2.5: Harmonic voltage limits (IEEE Std. 519-1992) [38]

Bus voltage *V* at PCC	Individual harmonic distortion (%)	Total harmonic distortion THD (%)
$V \leq 1.0$ kV	5.0	8.0
1.0 kV$\leq V \leq$ 69 kV	3.0	5.0
69 kV $\leq V \leq$ 161 kV	1.5	2.5
161 kV $\leq V$	1.0	1.5*
*** High-voltage systems can have up to 2.0% THD where the cause is an HVDC terminal whose effects will Have attenuated at points in the network where future users may be connected.**		

Table 2.6: Harmonic current limits for general distribution systems (IEEE Std. 519-1992) [38]

Maximum Harmonic Current Distortion in Percent of IL						
Individual Harmonic Order (Odd Harmonics)						
Isc/IL	**h<11**	**11≤h<17**	**17≤h<23**	**23≤h<35**	**35≤h**	**TDD**
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g. half-wave converters, are not allowed.						
*** All power generation equipment is limited to these values of current distortion, regardless of actual *I*sc/*I*L.**						
Where ***I*sc = maximum short-circuit current at PCC.** ***I*L = maximum demand load current (fundamental frequency component) at PCC.** **TDD = Total demand distortion (RSS), harmonic current distortion in % of maximum demand load current (15 or 30 min demand).**						

2.7 Harmonic Mitigation Techniques

To eliminate the harmonics from the network, filtering devices are needed. There are different filter topologies presented in the literature for this purpose.

Basically, there are two approaches of compensating harmonic distortions including passive filters and active filters.

2.7.1 Passive Harmonic Filters

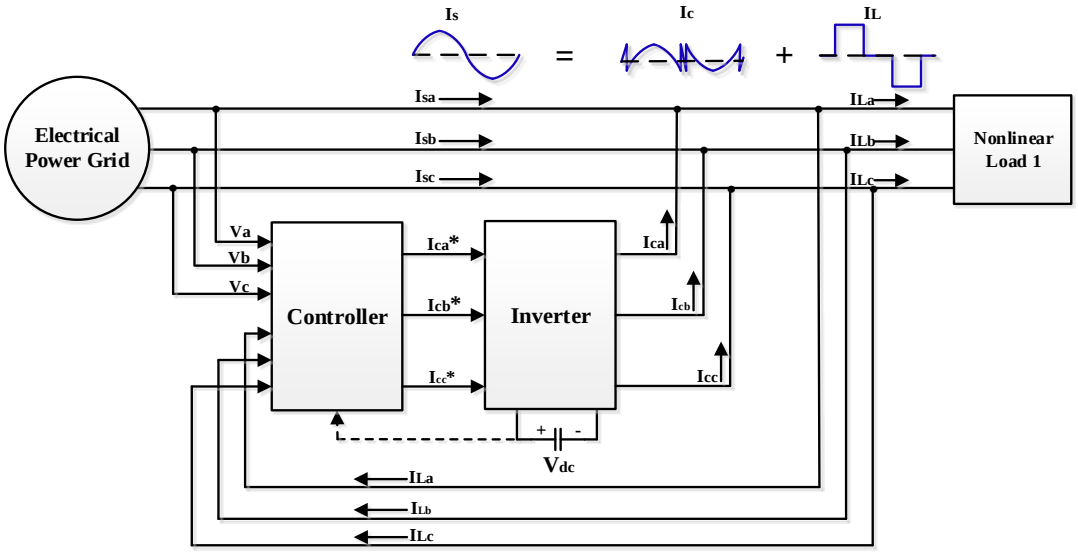
The Passive filters are mainly made of resistive, capacitive and inductive components. They usually eliminate harmonics by tuning the component to generate resonance at the selected harmonic frequency. They are connected in series or shunt with the power system. Series passive filters designed to have large impedances at selected harmonics to isolate the produced load harmonics from the power source. On the other hand, shunt passive filters designed to have a low impedance for selected harmonics to allow those harmonics pass through the filter to the ground. Although passive filters are relatively cheaper than other filters, they have some disadvantages preventing using them widely. Passive filters are designed to filter specific harmonic components and can not be applied for the elimination of large variation of harmonic components. Moreover, passive filters usually have big sizes and for applications with higher voltages can not be used. It is noticed in some cases; it is very hard to tune the filters due to interacting of other harmonics drawn from other power sources. Resonance is another drawback of these filters. Additionally, the capacitance component of passive filters can interact with the system impedance and result in resonance conditions and in some cases can increase the harmonic rates of power system results in a very bad voltage profile.

2.7.2 Active Filters

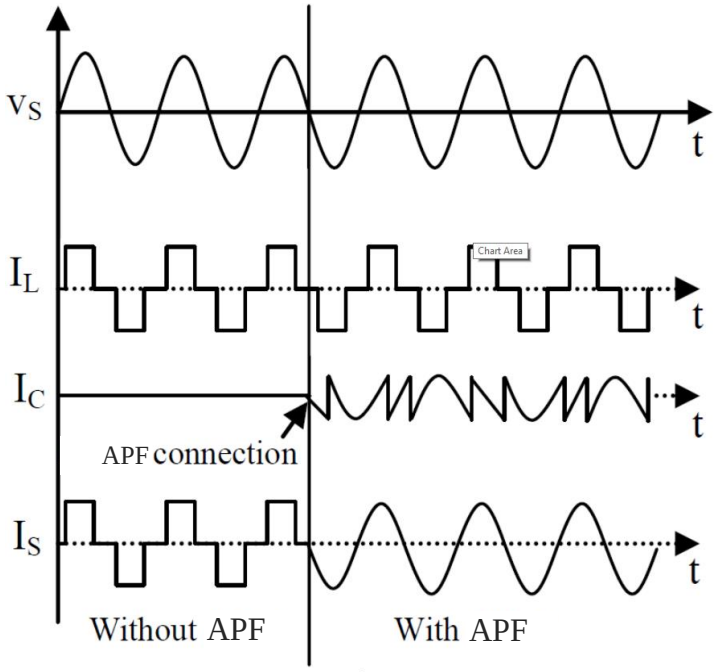
To overcome the drawbacks of passive filters, active compensation is introduced. APFs were introduced around 1970. The active power filtering devices can be connected in series (DVR), shunt (APF), or series-shunt configuration (UPQC) [122-133]. Generally, they use VSC as a controller while some other use CSC which is not popular. Also, they are divided into different classifications of single phase (two-wire) or three-phase (three-wire or four-wire) systems.

The VSC is more popular because it can be used in multilevel and multi-step converters to increase the power capacity of converter and be able to work with lower switching frequencies. Moreover, the dc capacitor in VSC can be replaced with energy storage devices to exchange active power with the network [134].

APF injects harmonic current equal but opposite to the harmonic current produced by the nonlinear load. It acts as a current source injecting harmonics. Fig. 2.15 shows the three-phase line diagram of APF with the corresponding waveforms.



(a)



(b)

Figure 2.15: APF; (a) three-phase circuit diagram, (b) voltage and current waveforms before and after connection of APF

Fig. 2.16 shows the DVR connected in series with the network including matching transformer capable of eliminating voltage harmonics and regulate and balance the voltage of connected bus. It injects voltage components in series with the main voltage and consequently, compensating voltage sag and swell on the load side. Also, the harmonic voltages are added to maintain almost pure sinusoidal voltage across the load.

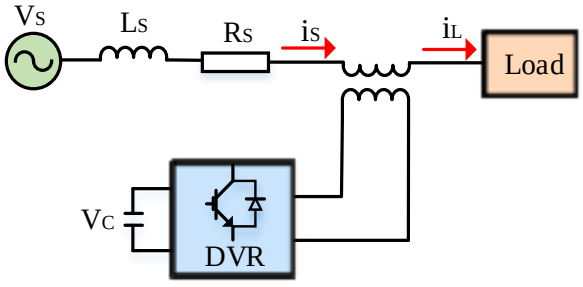


Figure 2.16: DVR circuit diagram [124]

Fig. 2.17 shows a three-phase three-wire UPQC comprises of shunt and series converters. There is a shared dc bus between two converters able to work as an active series and active shunt compensator. UPQC is considered as the most useful custom power devices capable of regulate and balance the voltage, compensating the reactive power and improving the power quality. However, its high installation costs and control complexity prevent it to be the only solution to the power quality. In general, UPQC has two topologies of right-shunt [127] and left-shunt [128].

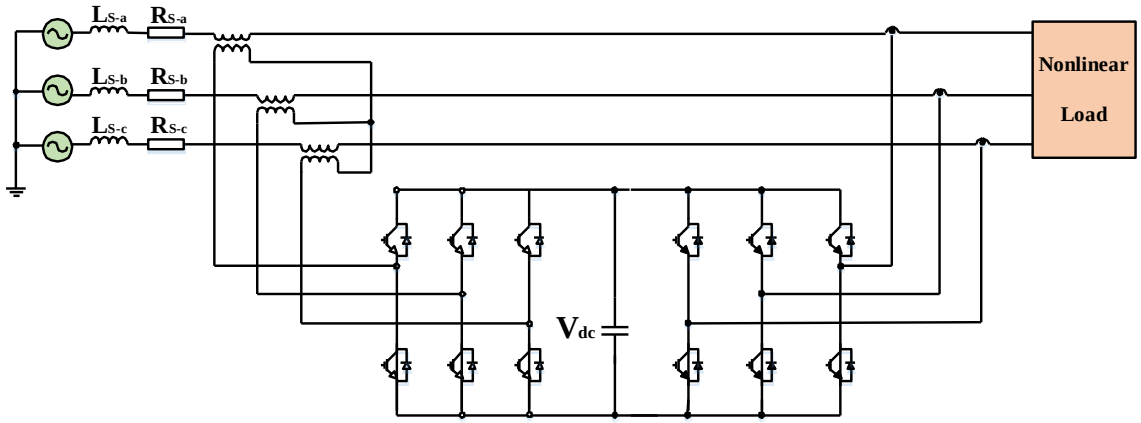


Figure 2.17: Three-phase three wire UPQC [128]

According to standards, consumers are responsible to keep their injected harmonic current magnitudes and THDi at their PCCs below the permissible levels while utilities are required to control the THDv of the network and the individual buses [37-38]. Therefore, each nonlinear load which exceeds the standard level must install APF at their connection point to eliminate their undesired harmonic current. However, by installing APF at each nonlinear load bus, the THD of related bus reduces to zero. This is because APF injects exactly the same amount of harmonic current produced by nonlinear load and hence, eliminates all harmonic currents of the nonlinear load. Fig. 2.18 shows how APF is connected to each nonlinear load in the network.

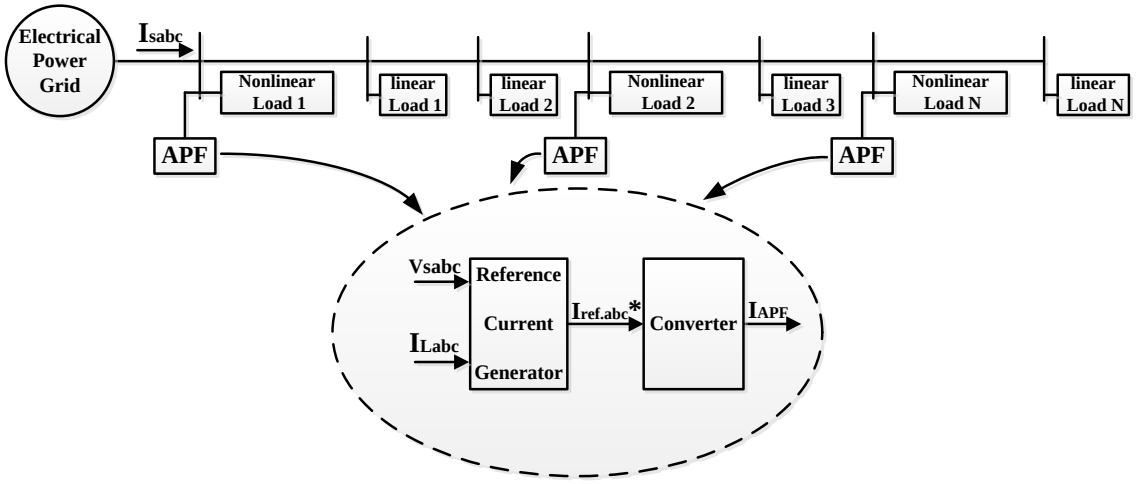


Figure 2.18: Single line diagram of APF connected to the distribution network

2.7.3 Harmonic Current Extraction Techniques

There are two fundamental approaches to extract harmonic currents in APFs applications which are a correction in time-domain and correction in frequency-domain [39] [132]. Fig. 2.19 represents different types of harmonic extraction techniques. The advantage of time-domain methods is the fast response for online applications without complicated control circuitry. This advantage occurs because time-domain control strategies operate on instantaneous values of the distorted waveform, rather than on at least one period, as in frequency-domain methods so that the required computational time can be relatively small. The shortcoming of time-domain methods is that, to obtain optimum results, relatively high switching frequencies are needed, which subsequently leads to excessive switching losses in the semiconductor switches. On the other hand, switching frequencies for frequency-domain methods can be much lower than in time-domain schemes, resulting in much lower semiconductor switching losses. Their main disadvantage is longer computational time than in the time-domain methods.

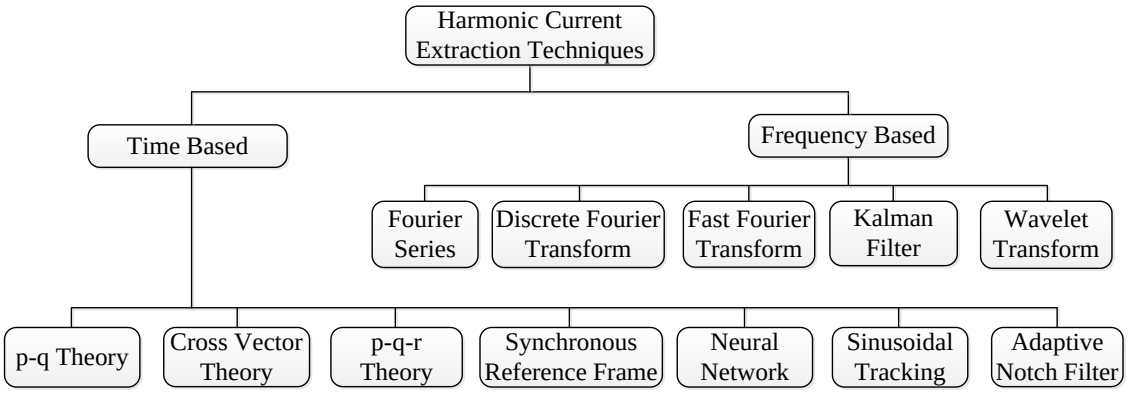


Figure 2.19: Harmonic extraction techniques [132]

2.7.4 APLC

As mentioned before, the principle concept of active filtering of harmonics was proposed in the 1970s. They are based on completely eliminate the harmonics of nonlinear loads. The general approach for harmonic compensation is to put regulations to force consumers with nonlinear loads to reduce their harmonic injections to the network or install filters. However, these methods compensate the harmonic injection of the nonlinear load at PCC without considering the entire network [37]. APLC is capable of compensating harmonics of the entire network to meet the network power quality requirements based on IEEE standard 519-1992 [38]. To achieve the entire network harmonic compensation, optimal siting and sizing of APLCs need to be considered. In general, APLCs are improved version of APFs with some differences [40-51]. They are installed only in optimal buses determined by optimal setting (Fig. 2.20), they control the THDv and individual voltage harmonics of the entire network within the limits and they inject reference currents not to fully compensate the nonlinear load distortions but just to limit the harmonic distortions within the limits.

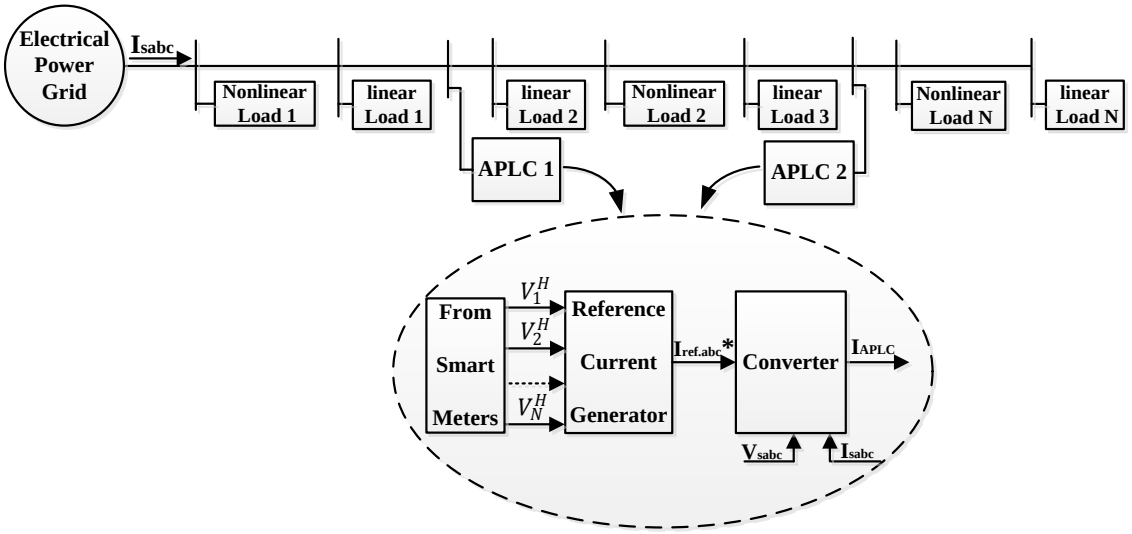


Figure 2.20: Single line diagram of APLC connected to distribution system

While there are many publications on APFs, the research on APLCs has been very limited [40-51] mainly due to the unavailability of online network data. However, this problem has been recently resolved with widespread installation of smart meters in SGs with sophisticated communication networks. The research on APLCs can be classified into optimal siting and sizing of single [40-46] and multiple [47-51] APLC units. However, all publications on APLC siting and sizing ignore the impacts of harmonic couplings imposed by the nonlinear devices.

Fig. 2.21 shows three-phase modular APLC with voltage source inverter connected to the grid. The VSC consists of six power transistors with dc link capacitor which is connected to the PCC through the inductor. The interface inductor acts here as a filtering device and suppressing the higher order harmonic components caused by the switching operation of the power transistors. The VSC generates current harmonics to reduce the harmonic distortion effects of nonlinear loads, and hence bring the total THDv of the network within the standard value.

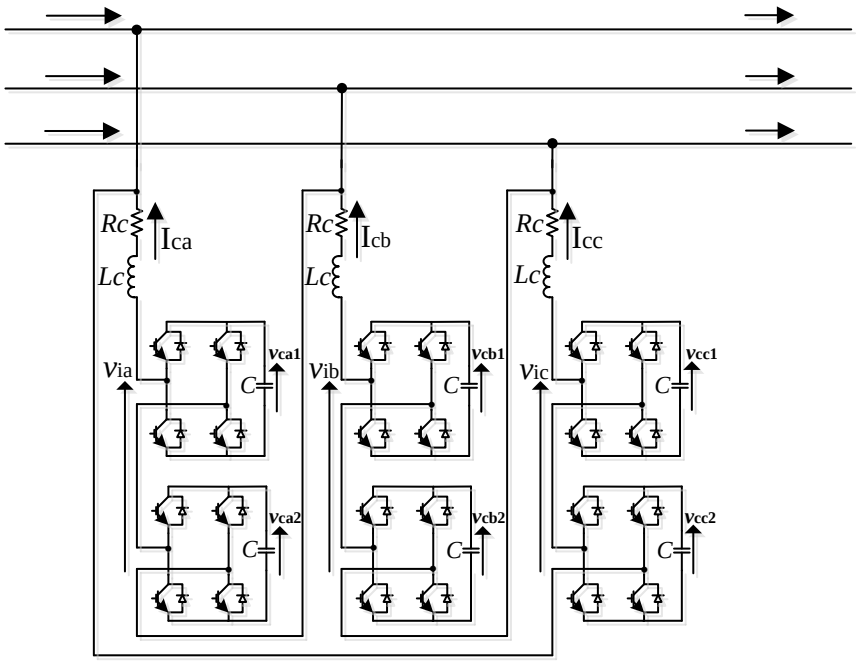


Figure 2.21: Three-phase asymmetric CMC APLC connected to the grid [109]

CHAPTER 3: REACTIVE POWER COMPENSATION USING STATCOM

3.1 StatCom as a Shunt Connected FACTS Device

As mentioned in chapter 2, recently there has been substantial interest in reactive power as one of the several supplementary services required for the reliability of the power systems due to its vital effect on power system security. Solid state power conversion devices are extensively engaged to control a wide range of electrical active and passive loads such as variable speed drives, uninterrupted power supply (UPS) and electric furnaces. These nonlinear loads draw harmonic currents and reactive power as well as active power from the main AC sources. Reactive power is relative to bus voltage levels and deficiency of enough reactive power supply leading to poor voltage profiles with the possibility of voltage collapse within power systems. Moreover, reactive power and harmonic components of load current reduce the system power factor leading to an increase in transmission network losses, overheating of devices and end-user voltage fluctuations. Furthermore, quick variations in reactive power consumption of large loads can lead to voltage oscillations which might cause power fluctuations within the network [13-14]. Voltage sag is defined as RMS reduction of AC voltage at the fundamental frequency for the duration of a half-cycle to a few seconds [16]. Voltage swell is another kind of voltage instability which may happen under different scenarios. High penetration of PV cells is one of the main reasons for voltage rise in the system due to reversed power flow to the network [17-18]. The conventional compensation of reactive power is based

on connecting shunt capacitor or inductor banks to the system through mechanical switches. However, these methods have many disadvantages such as fixed compensation, resonance, large size and weight, as well as noise and losses. By controlling the reactive power within transmission and distribution networks, maximum active power flow and voltage regulation can be achieved. The StatCom is a shunt connected FACTS device capable of generating or absorbing reactive power and can be controlled independently of the AC power system.

This section investigates and improves the voltage stability of distribution system consisting of local loads and rooftop PVs. This will be done by modeling and implementation of StatCom based on hysteresis current control (HCC). Simulations are performed and studied in Matlab/Simulink to explore the performance and ability of StatCom in compensating voltage quality issues.

3.1.1 The Principle of StatCom

The StatCom can be described as a voltage source converter with an energy storage unit which is usually a dc capacitor connected to the network through a transformer. The main objective of StatCom is to control reactive current by injecting or absorbing specified reactive power through the connected network. Usually, StatCom output voltage is set to be in phase with the system voltage with a small phase difference to compensate the losses of the converter. Consequently, there would be only reactive power exchange with no real power exchange between the StatCom and the power system [59] [135].

A single-line diagram of a StatCom power circuit is shown in Fig. 3.1a. The exchange of the reactive power between the converter and the power system is controlled by changing

the amplitude of output voltage (Es) of the converter, as exemplified in Fig. 3.1b. If the output voltage of the StatCom increases above the voltage of connected bus (E_t), then the current is injected from the converter to the power system and the StatCom provides capacitive power to the power system. On the other hand, if the output voltage of the StatCom decreases below the voltage of connected bus, then the current flows from the power system to the converter and the StatCom consumes inductive power from the network.

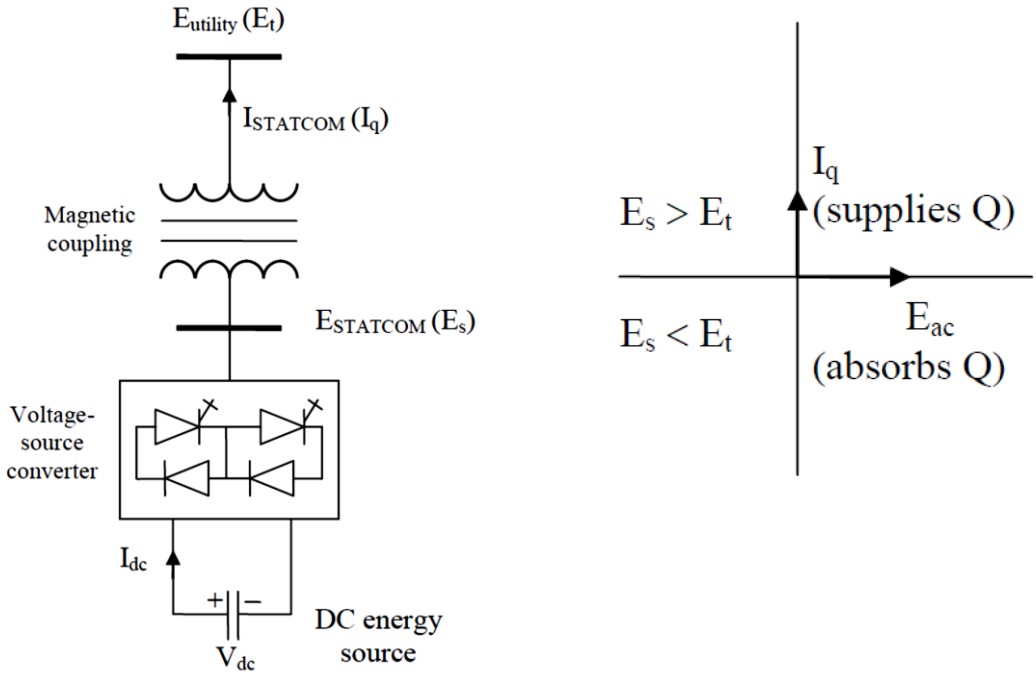


Figure 3.1 : StatCom principle diagram; (a) power circuit, (b) reactive power exchange [34]

Fig. 3.2 shows an equivalent circuit of StatCom including dc source (capacitor), converter and filter.

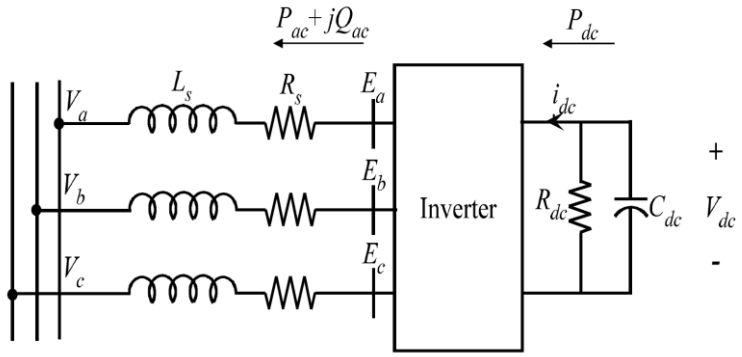


Figure 3.2: Equivalent circuit of StatCom [33]

This section is applying PSO to optimally control the reactive power of the network on Fig. 3.3. A complete explanation of PSO is given in section 3.2.1. The connected three-phase StatCom in Fig. 3.3 includes five-level neutral–point clamped inverter which is applying adaptive hysteresis current control design to control the voltage profile of the connected network. An inclusive description is provided in section 3.2.4 regarding the control system of designated StatCom.

The size of StatCom is calculated based on:

$$I_{StatCom-size} = \left| I_{StatCom}^{h=1} \right| \tag{3.1}$$

where h=1 indicating the compensation of StatCom only for fundamental voltage of the network.

The objective function is to minimize the amount of exchanged active power between StatCom and network:

$$\min\ F = P_{StatCom} \tag{3.2}$$

The selected constraint associated with Eq. 3.2 is the voltage magnitude at PCC:

$$V_{PCC} = 1pu \tag{3.3}$$

3.1.3 Simulation Results of StatCom in Distribution System of Fig. 3.3

The StatCom is modeled in Simulink/Matlab to investigate its performance (Fig. 3.3). The 25 kVA StatCom is used in a distribution system with the local loads and also rooftop PV for residential houses. The selected network is a very simple model with limited loads and is to only show the general performance of the StatCom. A complex network with linear and non-linear loads is simulated and discussed in Chapter 4.

Simulation results for the network of Fig. 3.3 are performed for three case studies to investigate the performance of StatCom in improving the voltage profile of network at PCC.

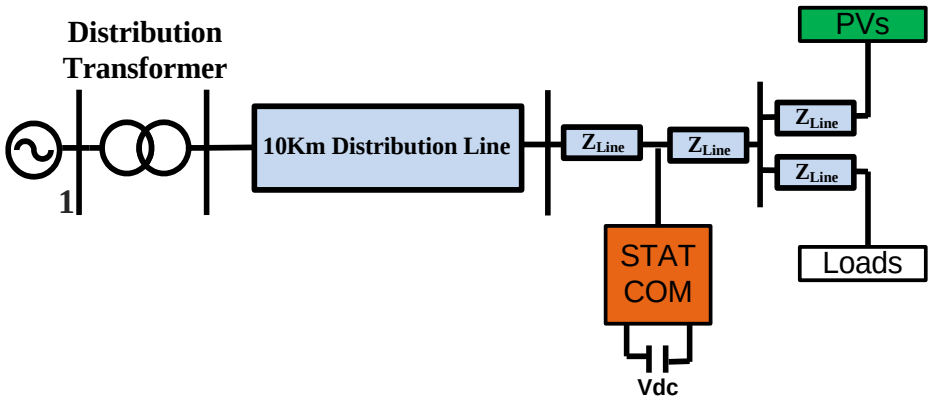


Figure 3.3: The simulated distribution network with StatCom for Cases 3-A to 3-C [33]

3.1.3.1 Case 3-A: Compensation of StatCom in Voltage Sag Conditions

One of the problems that utilities and networks are facing is the voltage sag. Voltage sag occurs in the system due to sudden load increase or due to faults. In some cases, the

voltage deep leads to partial or even full interruption of networks. Therefore, this issue should be considered to prevent more breaks to the networks. StatCom as a shunt converter is one of the solutions to mitigate the voltage sags.

Fig. 3.4 shows the simulation results for case 3-A. Fig. 3.4a displays the voltage profile of StatCom at PCC. As can be seen, the voltage of network is not always one pu. This can be due to some extra loads on the network. In Fig. 3.4a, the blue line is the voltage profile of PCC when StatCom is not connected while the black line is the voltage of the same point when the StatCom is in operation. At t=0.1sec, the network is facing overload problem and the line voltage drops to 0.95 pu. At t=0.2sec, a very large load is energized and consequently the network line voltage drops more to 0.8 pu. Then at t=0.3sec, the network continues on its normal conditions. As can be seen by implementing StatCom, the network voltage is maintained at one pu at all times (black line). Fig. 3.4b shows the injected active and reactive power by StatCom. The active power is always close to zero indicating good performance of PSO in satisfying the requirements of objective function. From Fig. 3.4b also can be realized that the injected reactive power to the network is increasing when the voltage of network is dropping. Fig. 3.4c illustrates the line current of StatCom. It is noticeable that by dropping the network voltage, the StatCom is injecting more reactive current to the network and the current is close to zero under normal conditions of the network.

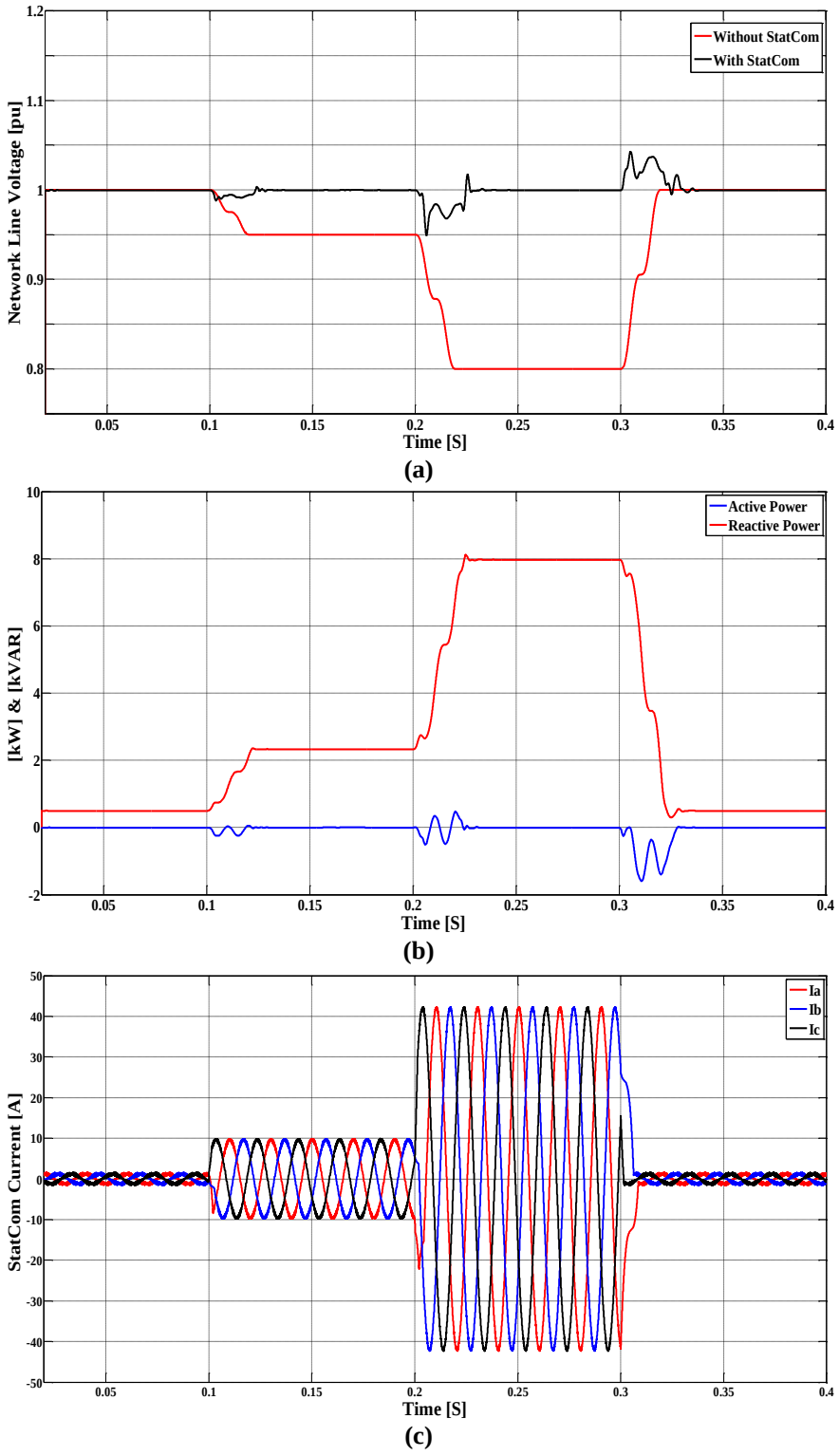
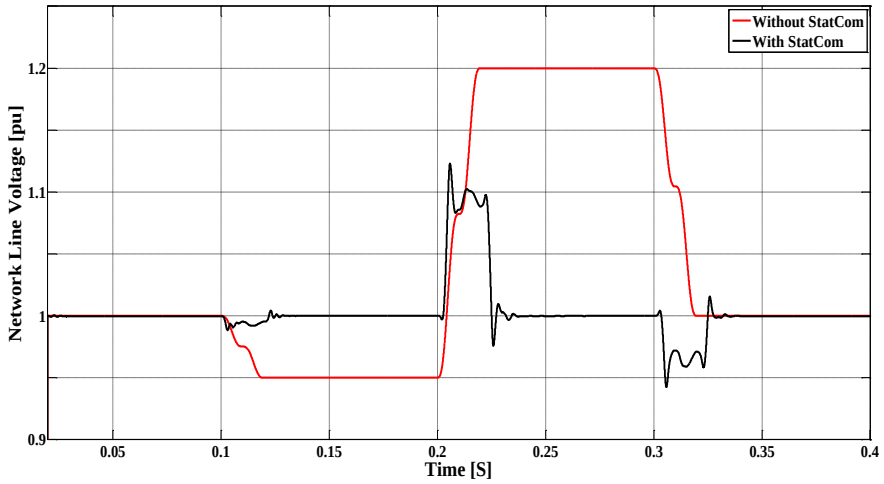


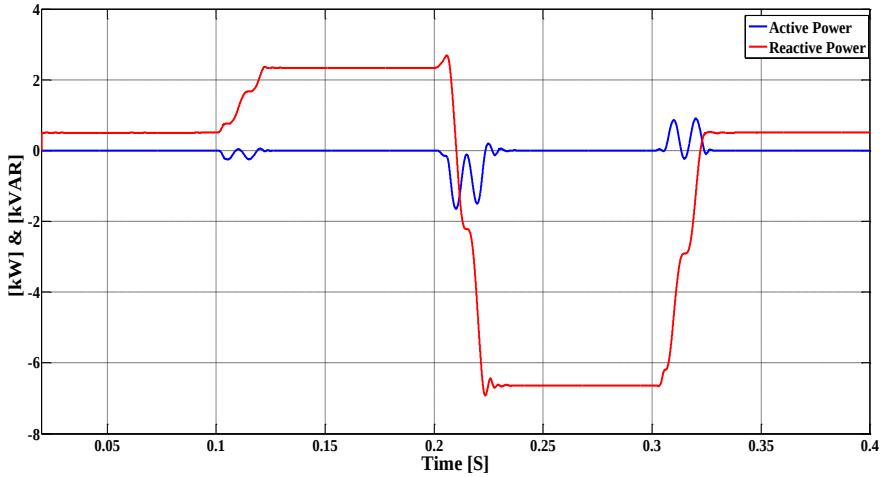
Figure 3.4: Simulation results for Case 3-A; (a) network line voltage, (b) injected active and reactive power of StatCom, (c) StatCom injected current.

3.1.3.2 Case 3-B: Compensation of StatCom in Voltage Swell Conditions

Due to growing the installation of rooftop PVs, the network is facing many problems such as voltage swell into the distribution networks. StatCom is one of the best solutions to prevent increase of voltage in distribution networks. Fig. 3.5 presents the simulation results for this part. Fig. 3.5a shows the voltage of network at PCC. The network voltage is one pu until t=0.1sec; then the voltage drops to 0.95 pu. After that, at t=0.2sec, the network voltage is raised to 1.2 pu which is coincided with a sunniest time of the day and the power flow from the PV to the network causes over-voltage on the system. Finally, at t=0.3sec, the network continues to its normal conditions. The black line shows the line voltage at PCC after using the StatCom which is maintained at one pu. The transferred active power is still zero and the reactive power is changing based on network requirements (Fig. 3.5b). Until t=0.2sec, the reactive power is injected into the network but between t=0.2 till 0.3sec, the StatCom is absorbing reactive power from the network to drop the voltage from 1.2 pu to 1 pu. At t=0.3sec, the StatCom is changed from capacitive mode to inductive mode. This can also be observed from Fig. 3.5c. This figure shows the phase shift between voltage and current of the StatCom. Before t=0.2sec, the StatCom acts as a capacitive load and the current leads the voltage, but after that and until t=0.3sec, the current lags the voltage and the StatCom performance is like the inductive load.



(a)



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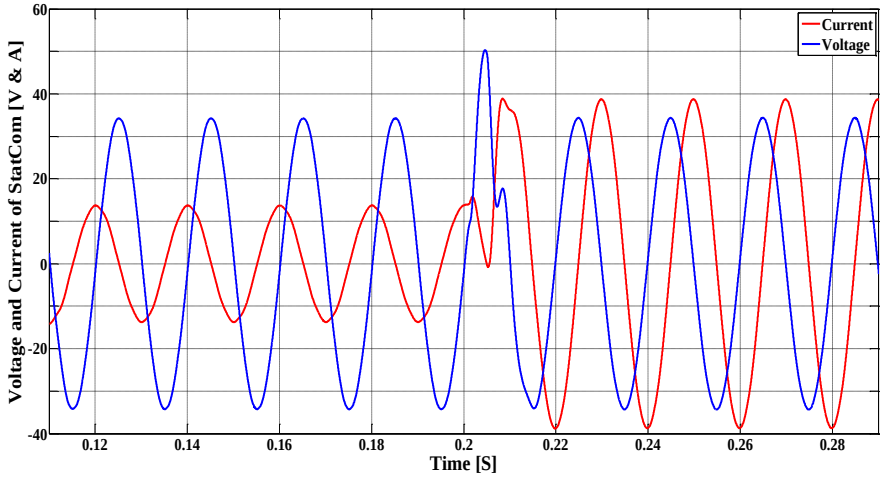


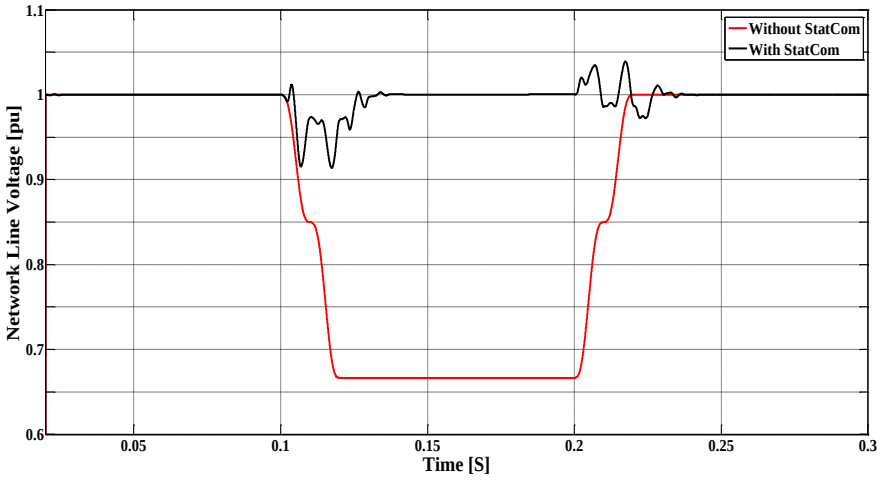
(c)

Figure 3.5: Simulation results for Case 3-B; (a) network line voltage, (b) injected active and reactive power of StatCom, (c) voltage and current of StatCom

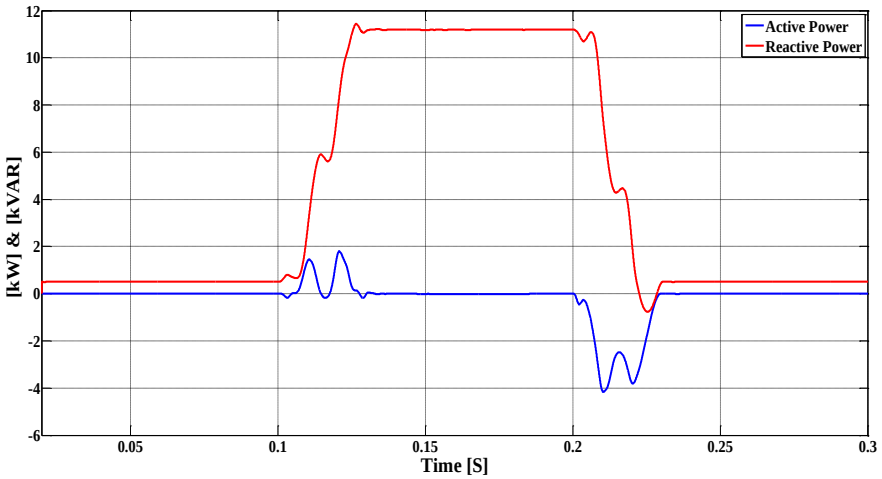
3.1.3.3 Case 3-C: Compensation of StatCom in Short-circuit Conditions

Another main issue of the power networks especially distribution systems is the short circuit. Many times when short circuit happens, the related line or network will be isolated and the system will be out of service. In this part a three-phase short circuit via a fault resistance of 1 mΩ is simulated.

Fig. 3.6 illustrates the simulation results for case 3-C. The voltage profile of network on Fig. 3.6a is maintained at one pu during the fault time (between t=0.1sec and 0.2sec).



(a)



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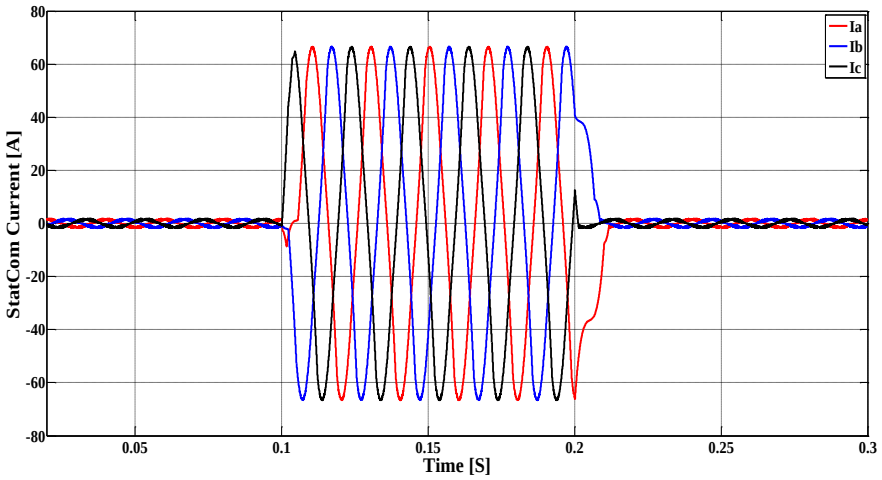


(c)

Figure 3.6: Simulation results for Case 3-C; (a) network line voltage, (b) injected active and reactive power of StatCom, (c) StatCom injected current

Fig. 3.6b shows how the StatCom injects reactive power to the network during the fault time. The line current of StatCom is presented in Fig. 3.6c which is zero except during the fault time.

3.2 Siting and Sizing of StatCom in Balanced and Unbalanced Distribution Networks

StatCom usually generates a balanced set of three-phase sinusoidal voltages at the fundamental frequency with controllable amplitude and phase angle. Unlike most conventional reactive power compensators, StatCom facilitates dynamic compensation of electrical power systems and improves the utilization of existing networks [36].

However, the loads are not always balanced and some industrial loads draw unequal load currents from the three-phase power system. Large unbalanced loads usually result in voltage imbalances in the power networks which affect other customers within that network. Furthermore, many loads such as induction motors are very sensitive to voltage imbalances and even small voltage imbalances can result in overheating and unbalanced

electromagnetic torques. Therefore, it is very important to rectify voltage imbalances in the networks.

This section explores voltage instability in the distribution system including within local loads as well as balanced and unbalanced large industrial loads. Thus, illustrating how StatCom can mitigate the voltage instability problems. Also, particle swarm optimization (PSO) technique is used for optimally allocation and sizing of StatComs in the distribution network. Therefore, a brief explanation of PSO is given in the following section.

3.2.1 Particle Swarm Optimization Method

Optimal siting and sizing of FACTS devices in distribution networks is an important subject in the electrical engineering area. Among different optimization techniques, PSO is a common optimizer tool for optimal siting and sizing of FACTS devices. In [47] it is proved that PSO is more accurate compared to non-linear programming and genetic algorithm [136]. Therefore, PSO is applied to find optimal siting and sizing of StatComs. It is assumed that StatCom units receive network data from smart meters in a SG with sophisticated communication networks.

The PSO is an optimization technique based on individual population sizes. Each individual is referred to as particle and the population is known as a swarm. Each particle in a swarm should move toward the best position within the population which is the optimal result. The movement of particles in each iteration is updated by adaptive velocity (3.4). In each run for PSO, there is an objective function. The best value of this objective function (minimum answer) for each particle is described as a Pbest and the global best position among all particles (best Pbest) is represented as a Gbest. Furthermore, the

velocity of the particle is determined based on the relative location from Pbest and Gbest [137]:

$$V_j^{n+1} = \omega V_j^n + C_1\varphi_1(pbest_j^n - X_j^n) + C_2\varphi_2(gbest^n - X_j^n) \quad (3.4)$$

where V_j^n and X_j^n are the velocity and location of particle j at iteration n, respectively. ω is the inertia weight factor, φ_1 and φ_2 are random numbers between 0 and 1 and C_1 and C_2 are called the acceleration factors.

3.2.2 Problem Formulation of Siting and Sizing of StatCom

The total size of StatComs connected to the network can be expressed as:

$$I_{StatCom\text{-}size} = \sum_{k=1}^{K} \left| I_{k,StatCom}^{h=1} \right|, \quad k = 1,...,K \quad (3.5)$$

where *k* and *h* are the bus number and the harmonic order respectively while *K* represents the maximum number of buses.

The objective function (OF) for optimal siting and sizing of StatComs is to minimize their sizes:

$$\min OF = I_{StatCom\text{-}size} \quad (3.6)$$

The selected constraints associated with (3.6) are the lower limit of voltage magnitude (|V|) for each bus according to the Australian standard [138] and also the maximum size of StatCom ($I_{k,\max}$):

$$|V|_k \geq 0.9 pu \quad (3.7)$$

$$I_{k,StatCom-size} = \left| I_{k,StatCom}^{h=1} \right| \leq I_{k,\max} \tag{3.8}$$

where $|V|_k$ is the voltage magnitude of bus k.

A PSO technique is used to solve (3.5)-(3.8). The fundamental current of StatCom consists of both magnitude and phase angle. Therefore, each magnitude and phase angle of the StatCom current at each bus are assigned as the position of a particle during the optimization process. The first step of this optimization is to specify the system input data including all load data and system configurations such as the voltage of all buses and the maximum current of StatCom. The PSO factors and iterations are also determined in this step. Then one particle is allotted for each magnitude and each phase angle of StatCom current at all buses. The next stage is to determine the optimal locations and sizes of StatComs. Therefore, the PSO runs the Simulink file and returns the values for voltage of all buses and the sizes of StatComs. Then, based on this data and (3.4)-(3.8), the current of StatCom at each bus is calculated.

3.2.3 System Specifications of 15-Bus Test System

To assess the effectiveness of the proposed approach, optimal placement and sizing of three-phase StatComs will be performed for the 15-bus radial power system of Fig. 3.7 [139]. The system contains four large loads located at buses 5, 7, 10 and 13. The detailed specifications of this system are presented in Tables 3.1 and 3.2.

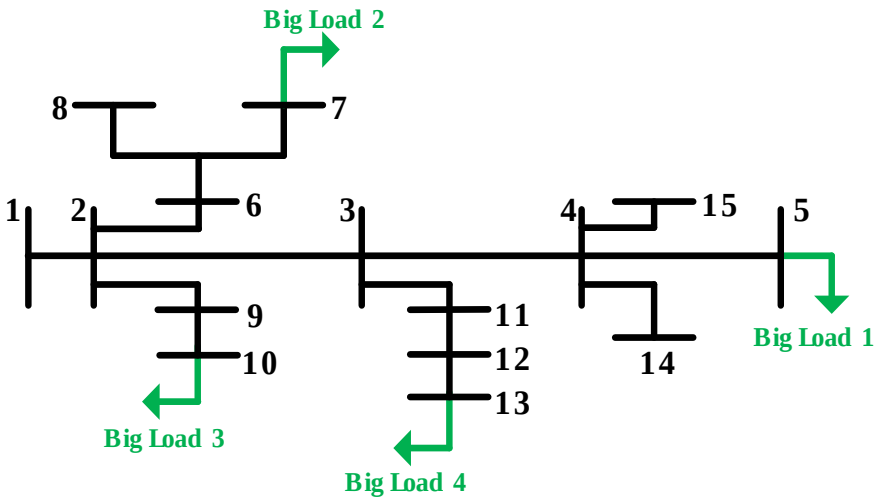


Figure 3.7: The 15-bus test system [139] including local loads and four large loads

Table 3.1: Line data of the network in Fig. 3.7

Branch	From Bus	To Bus	R (ohm)	X (ohm)
1	1	2	1.35309	1.32349
2	2	3	1.17024	1.14464
3	3	4	0.84111	0.82271
4	4	5	1.52348	1.02760
5	2	9	2.01317	1.35790
6	9	10	1.68671	1.13770
7	2	6	2.55727	1.72490
8	6	7	1.08820	0.73400
9	6	8	1.25143	0.84410
10	3	11	1.79553	1.21110
11	11	12	2.44845	1.65150
12	12	13	2.01317	1.35790
13	4	14	2.23081	1.50470
14	4	15	1.19702	0.80740

Table 3.2: Linear load data of the network in Fig. 3.11

Bus	KVA	Bus	KVA	Bus	KVA
1	0	6	200	11	200
2	63	7	200	12	100
3	100	8	100	13	63
4	200	9	100	14	100
5	63	10	63	15	200

3.2.4 Three-Phase StatCom with Five-Level NPC Inverter

The StatCom inverters are designed with the five level neutral-point clamped (FL-NPC) configuration [34] [140]. The topology of a three-phase FL-NPC inverter supplying a series RL impedance (filterR_f and $L_f$impedances) and an ac back EMF (v_{abc}) is shown in Fig. 3.8. Five output voltage levels can be integrated by this structure including $0, \pm V_{dc}/4$ and $\pm V_{dc}/2$.

3.2.4.1 Adaptive Hysteresis Current Control Design

For the StatCom inverter, an adaptive hysteresis current control (AHCC) approach is used [36]. Assuming that the grounded neutral point of the system is connected to the midpoint of the FL-NPC inverter and applying KVL for phase-a:

$$u_a = R_f i_{StatComa} + L_f \frac{d}{dt} i_{StatComa} + v_a \tag{3.9}$$

where v_a, $i_{StatCom\ a}$, u_a are the phase-a PCC voltage (ac side), the phase-a inverter output current (or StatCom output current) and the phase-a inverter output voltage (dc side), respectively.

To maintain the switching frequency constant, the fundamental components of the inverter output voltages is used to adjust the hysteresis bands instead of using the system parameters. If the phase-a leg of the FL-NPC inverter (shown in Fig. 3.8) is assigned to generate and inject $i_{StatComa}$ at PCC, then the inverter must generate a voltage greater than the PCC voltage.

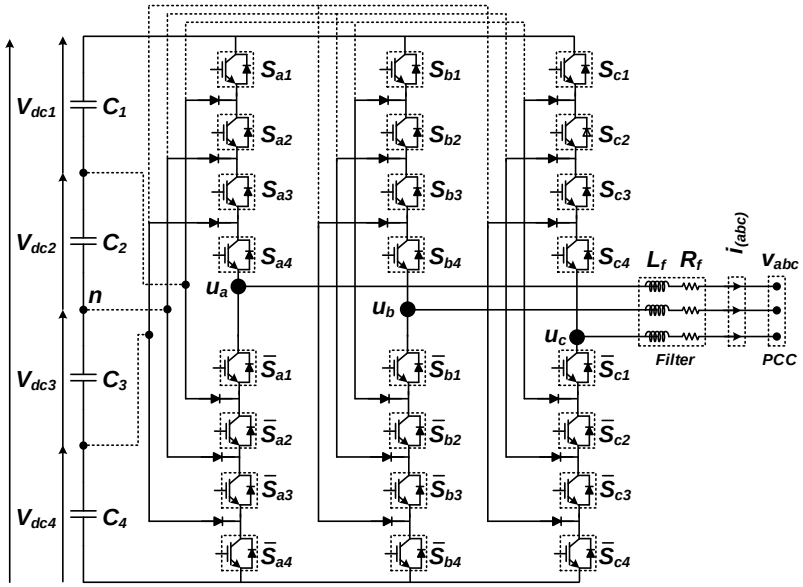


Figure 3.8: Detailed FL-NPC inverter structure of the shunt FACTS devices [140]

For the ideal case, the inverter creates the blue sinusoidal voltage waveform of Fig. 3.9a; however, in reality the red non-sinusoidal waveform is produced since the inverter utilizes a modulation technique. As a result, the actual modulated current will include two components related to the created realistic voltage including fundamental ($i_{sStatCom-F}$) and switching ripple ($i_{THStatCom-R}$) components:

$$i_{StatCom} = i_{StatCom-F} + i_{StatCom-R} \tag{3.10}$$

Assuming the voltage drop caused by the switching ripple across R_f is considerably less than across L_f and substituting Eq. 3.10 into Eq. 3.9:

$$\frac{d_{i_{StatCom-R}}}{dt} = \frac{u_a - L_f \frac{d}{dt} i_{StatComa-F} - v_a}{L_f} = \frac{u_a - v_{ideal} - a}{L_f} \tag{3.11}$$

where $v_{ideal-a}$ is the fundamental component of the inverter output voltage for phase-a. As realized in Fig. 3.9a, there are four different areas (Area 1-4) depending on the ideal voltage value. Based on this figure, the following switching periods are obtained:

$$\begin{cases} T_{1a} = \dfrac{V_{dc}}{4}\dfrac{1}{v_{ideal-a}}\left(\dfrac{2h_{a1}L_f}{V_{dc}/4 - v_{ideal-a}}\right) \\ T_{2a} = \dfrac{V_{dc}}{4}\left(\dfrac{2h_{a2}L_f}{(V_{dc}/2 - v_{ideal-a})(v_{ideal-a} - V_{dc}/4)}\right) \\ T_{3a} = \dfrac{V_{dc}}{4}\dfrac{1}{-v_{ideal-a}}\left(\dfrac{2h_{a3}L_f}{V_{dc}/4 + v_{ideal-a}}\right) \\ T_{4a} = \dfrac{V_{dc}}{4}\left(\dfrac{-2h_{a4}L_f}{(V_{dc}/2 + v_{ideal-a})(v_{ideal-a} + V_{dc}/4)}\right). \end{cases} \quad (3.12)$$

According to Figs. 3.9b-e, the switching periods for Areas 1-2 and Areas 2-4 are similar. Therefore, we need to have $T_1 = T_3 = 1/f_{sw}$ and $T_2 = T_4 = 1/f_{sw}$ in order to maintain a constant switching frequency. Using Eq. 3.12, we have:

$$\begin{cases} h_{a1} = h_{a3} = h_{a13} = h_{\max}\dfrac{|v_{ideal-a}|}{V_{dc}/4}\left(1 - \dfrac{|v_{ideal-a}|}{V_{dc}/4}\right) \\ h_{a2} = h_{a4} = h_{a24} = h_{\max}\left(2 - \dfrac{|v_{ideal-a}|}{V_{dc}/4}\right)\left(\dfrac{|v_{ideal-a}|}{V_{dc}/4} - 1\right) \end{cases} \quad (3.13)$$

where $h_{a13max} = V_{dc}/(8L_f f_{sw})$.

3.2.4.2 Selection of Hysteresis Band Shape

Based on Eq. 3.13, depending on the amplitude of the fundamental component of the inverter output voltage and the absolute value of the ideal voltage, there are two hysteresis band shapes that must be properly selected for the correct AHCC operation with a constant switching frequency. The key for the selection between the hysteresis shapes is the margin voltage level of $V_{dc}/4$. The difference between ideal and margin voltages specifies the beginning and end of utilization of hysteresis shapes. Hence, the following equation is derived for the transition between the two band shapes:

$$T_{trans} = |v_{ideal} - a| - V_{dc}/4 \quad (3.14)$$

where T_{trans} is the transition time between h_{a13} and h_{a24}. Fig. 3.10 shows the hysteresis band shapes obtained from Eq. 3.13 which are controlled and selected by Eq. 3.14. The switching between the two shapes to construct the whole hysteresis band h_a is organized by $T_{trans.}$ During time intervals corresponding to $T_{trans} < 0$, the h_{a13} activation pulse is changed from zero to one (red pulse in Fig. 3.10) and the control system designates h_{a13} for the hysteresis band, otherwise h_{a24} is used.

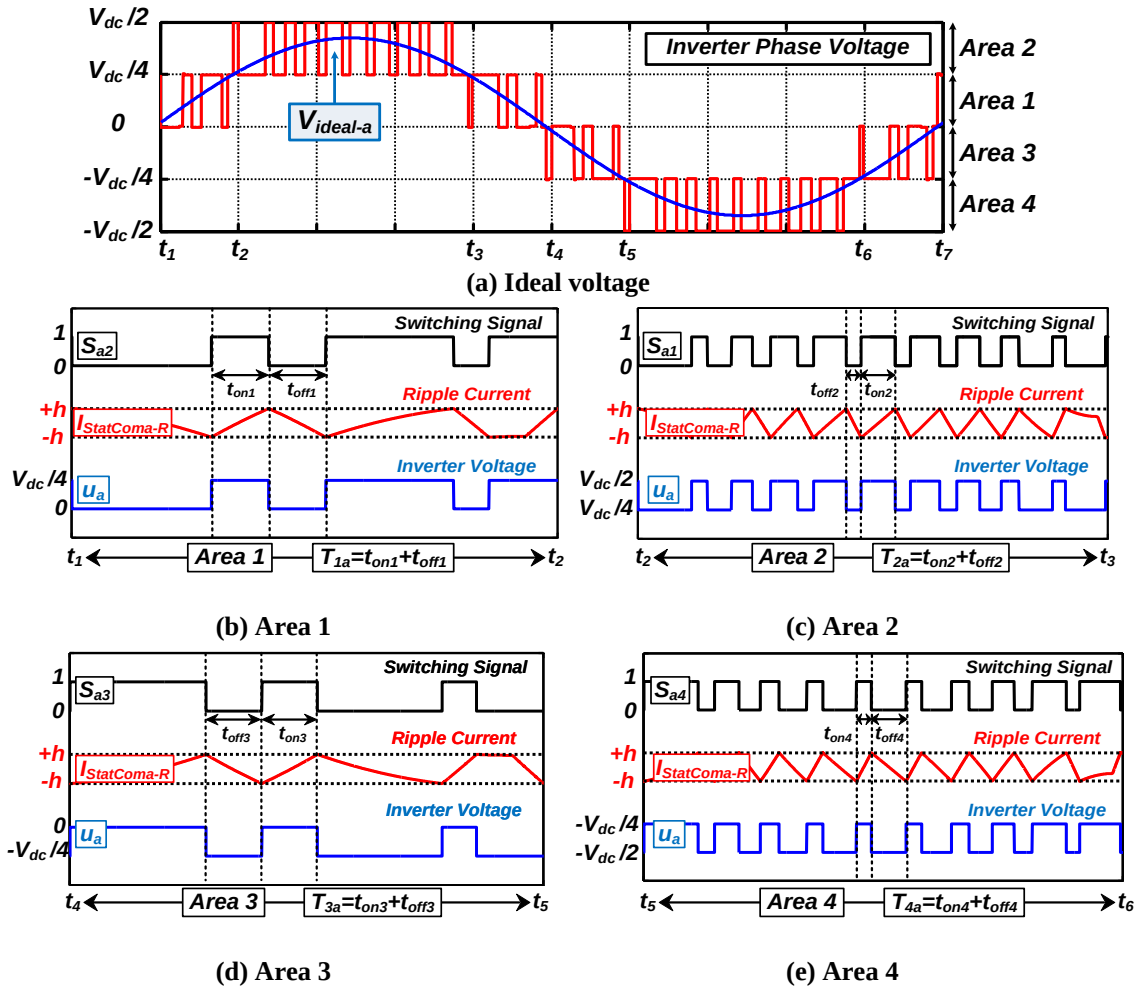


Figure 3.9: The APLC generated FL-NPC inverter voltage using HCC; (a) ideal (blue) and actual (red) waveforms, (b)-(e) detailed waveforms for Areas 1 to 4 [140]:

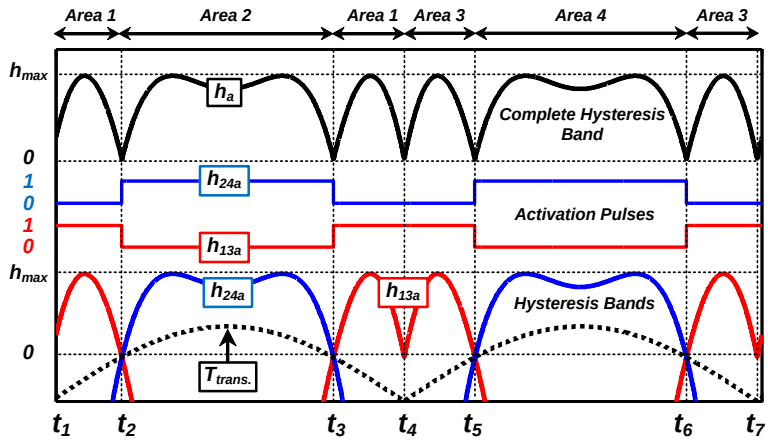


Figure 3.10: Hysteresis-shape selection according to Eqs. 3.13-3.14 [140]:

3.2.5 Simulation Results of Siting and Sizing of StatCom in Distribution Network

Simulation results for the proposed network of Fig. 3.7 are performed for eight case studies to show the performance of StatCom under various operating conditions.

3.2.5.1 Case 3-D: Balanced System Operation without StatCom

Voltage sag is a significant problem for most utilities. Voltage sag usually occurs due to a sudden increase in the load, or due to faults. In some cases, the voltage drop leads to partial or even full interruption of the networks. This case illustrates the worse operating condition of the network with maximum loadings of all local loads plus four large loads. Simulation results are presented in Table 3.3 (column 2). Clearly, the voltage magnitude of all buses except buses 1 (swing bus) and 2 are less than the permitted limit of 0.9 pu.

3.2.5.2 Case 3-E: Siting and Sizing of StatComs in Balanced System

The PSO is used to find the optimal locations and sizes of the StatComs for the 15-bus network of Fig. 3.7. Simulation results are summarized in Table 3.3 (columns 3-4).
As a result, just one StatCom is allocated at bus 11 to compensate the voltage drops of the network. To maintain the voltage of all buses at the minimum value of 0.9 pu, one StatCom with the size of 0.260 pu is needed at bus 11.

3.2.5.3 Case 3-F: Siting and Sizing of StatComs with an Additional Constraint for Maximum Size of StatComs (0.15 pu) in Balanced System

In practice, utilities may also require a maximum limit for the StatCom rating. This can be accomplished by repeating the simulation of Case 3-E with an additional constraint for the maximum size of StatComs which is selected to be 0.15 pu (3.13). In this case two StatComs are nominated to be allocated at buses 3 and 13 with sizes of 0.15 pu and 0.114 pu, respectively, with the total StatCom size of 0.264 pu. The results are illustrated in Table 3.3 (columns 5-6).

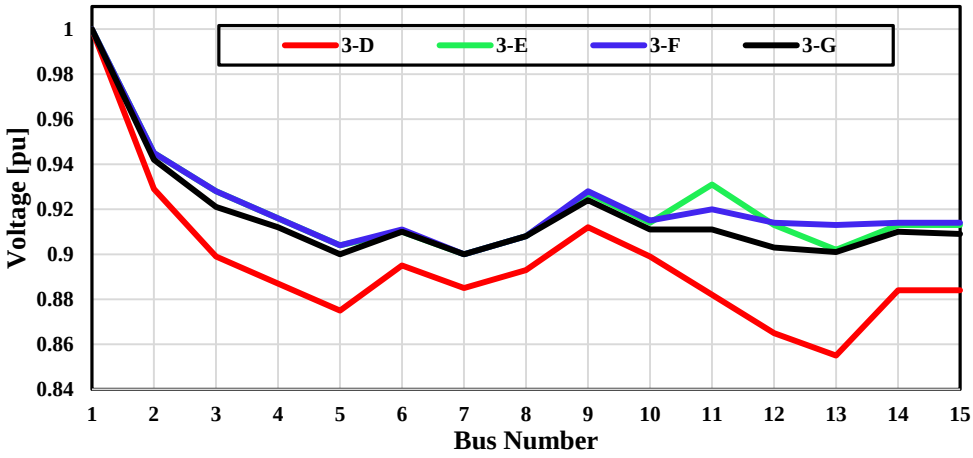
3.2.5.4 Case 3-G: Siting and Sizing of StatComs with an Additional Constraint for Maximum Size of StatComs (0.10 pu) in Balanced System

This case is identical to case 3-F with the different constraint on maximum sizing of StatCom (0.1 pu). In this case, 3 StatComs are located at buses 4, 6 and 13 with sizes of 0.085, 0.029 and 0.096, respectively; with the total StatCom size of 0.210 pu as illustrated in Table 3.3 (columns 7-8).

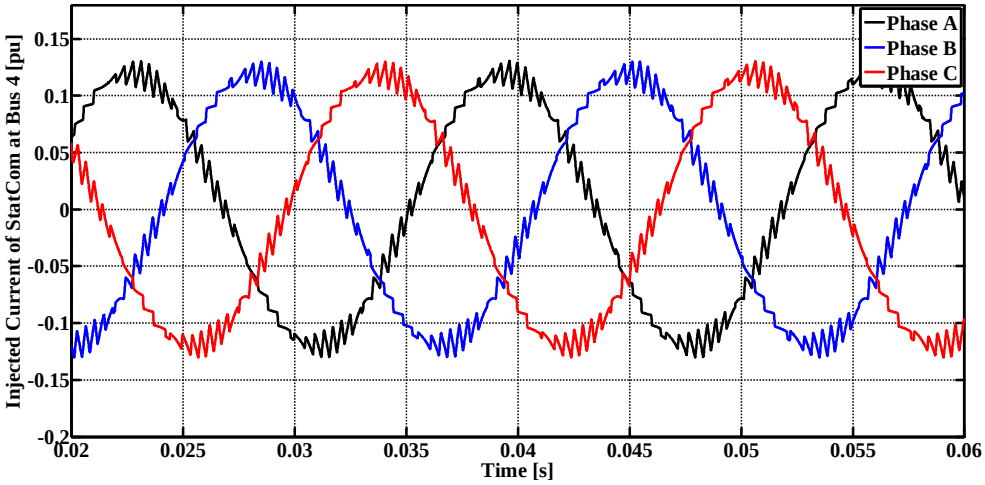
In all cases of 3-E to 3-G, the V_{rms} of all buses is maintained higher than the standard value of 0.9 pu. It can be seen that different values for the maximum size of StatCom can result in different numbers of required StatComs. Fig. 3.11a shows the voltage magnitude of cases 3-D to 3-G for all buses. Fig. 3.11b displays the three-phase injected current of StatCom at bus 4 for case 3-G while Fig 3.11c illustrates the voltage of bus 13 for case 3-G, indicating that the StatCom can improve the voltage profile of the system. From Fig. 3.11b it can be observed that the three phase injected currents of StatCom are equal due to balanced operatopn of implemented power system.

Table 3.3: Cases 3-D to 3-G; Operation of the network in Fig. 3.7 with and without StatCom in balanced system

Bus Number	Case 3-D	Case 3-E		Case 3-F		Case 3-G	
	|V| [pu]	|V| [pu]	$I_{StatCom}$ [pu]	|V| [pu]	$I_{StatCom}$ [pu]	|V| [pu]	$I_{StatCom}$ [pu]
1	1.000	1.000	-	1.000	-	1.000	
2	0.929	0.945	-	0.945	-	0.942	
3	0.899	0.928	-	0.928	0.150	0.921	
4	0.887	0.916	-	0.916	-	0.912	0.085
5	0.875	0.904	-	0.904	-	0.900	
6	0.895	0.910	-	0.911	-	0.910	0.029
7	0.885	0.900	-	0.900	-	0.900	
8	0.893	0.908	-	0.908	-	0.908	
9	0.912	0.927	-	0.928	-	0.924	
10	0.899	0.914	-	0.915	-	0.911	
11	0.882	0.931	0.260	0.920	-	0.911	
12	0.865	0.913	-	0.914	-	0.903	
13	0.855	0.902	-	0.913	0.114	0.901	0.096
14	0.884	0.913	-	0.914	-	0.910	
15	0.884	0.913	-	0.914	-	0.909	
Ave. /Total	0.897	0.922	0.260	0.922	0.264	0.918	0.210



(a)



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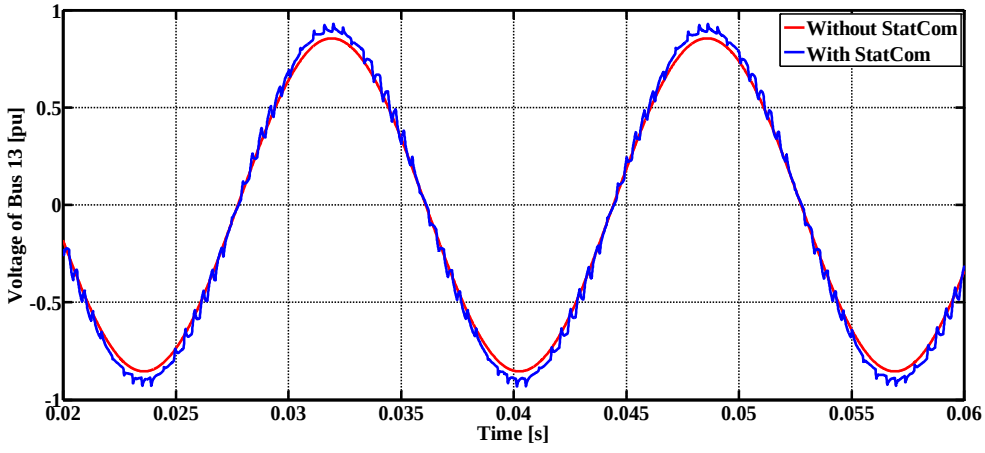


(c)

Figure 3.11: Simulation results of StatCom in the balanced network; (a) |V| of buses for a network of Fig. 3.7 for cases 3-D to 3-G, (b) injected current of StatCom at bus 4 for case 3-G, (c) voltage profile of bus 13 with and without StatCom for case 3-G

In all these cases the simulations are performed in a balanced network. However, there are sometimes large unbalanced industrial loads which lead to an imbalanced power network. Cases 3-H to 3-K investigate the operation of StatCom in unbalanced load conditions.

3.2.5.5 Cases 3-H and 3-J; Unbalanced System Operation without StatCom

The voltage magnitudes of network buses of Fig. 3.7 are presented in Tables 3.4 and 3.5 for Cases 3-H and 3-J, respectively. These cases present the voltage profile of network without employing StatComs under two different unbalanced operating conditions. The variation of voltage magnitude values between Cases 3-H and 3-J is executed due to the dissimilarity of unbalanced loads.

3.2.5.6 Cases 3-I and 3-K; Siting and Sizing of StatComs in an Unbalanced Network

The simulation of these cases resulted into allocation of two StatComs at buses 3 and 13. Tables 3.4-3.5 and Figs. 3.12-3.13 show the simulation results for these cases.

Before t=0.1sec, the network data are selected based on case 3-H. At t=0.1sec, the network switched to case 3-J. As can be seen from Fig. 3.12, in both cases the StatComs maintained the voltage magnitude of all buses at the minimum value of 0.9 pu by injecting unequal three-phase fundamental currents (Figs. 3.13b and 3.13c). Fig. 3.13a displays the voltage profile of bus 13 with and without StatCom for three phases. Figs. 3.13b and 3.13c illustrate the three-phase injected currents of StatCom at buses 3 and 13, respectively. It

is observed that due to the operation of unbalanced loads and based on Eqs. 3.6 and 3.7, the injected currents of StatComs for each phase are unequal.

Table 3.4: Cases 3-H and 3-I; Operation of the network in Fig. 3.7 with and without StatCom in unbalanced system

Bus Number	Case 3-H			Case 3-I			
	$\|V\|_a$ **[pu]**	$\|V\|_b$ **[pu]**	$\|V\|_c$ **[pu]**	$\|V\|_a$ **[pu]**	$\|V\|_b$ **[pu]**	$\|V\|_c$ **[pu]**	$I_{StatCom}$ **[pu]**
1	1.000	1.000	1.000	1.000	1.000	1.000	
2	0.913	0.935	0.949	0.960	0.943	0.951	
3	0.876	0.906	0.925	0.967	0.921	0.929	0.257
4	0.862	0.895	0.917	0.951	0.910	0.920	
5	0.847	0.886	0.912	0.935	0.900	0.915	
6	0.870	0.904	0.925	0.915	0.912	0.927	
7	0.856	0.896	0.919	0.900	0.903	0.921	
8	0.868	0.902	0.922	0.913	0.909	0.924	
9	0.891	0.921	0.940	0.937	0.928	0.942	
10	0.874	0.910	0.934	0.919	0.918	0.936	
11	0.856	0.890	0.911	0.948	0.914	0.917	
12	0.833	0.872	0.896	0.928	0.909	0.906	
13	0.818	0.862	0.888	0.915	0.910	0.900	0.070
14	0.860	0.893	0.915	0.949	0.907	0.918	
15	0.860	0.893	0.914	0.949	0.907	0.918	
Ave. /Total	0.872	0.904	0.924	0.939	0.919	0.928	0.327

Table 3.5: Cases 3-J and 3-K: Operation of the network in Fig. 3.7 with and without StatCom in unbalanced system

Bus Number	Case 3-J			Case 3-K			
	$\|V\|_a$ [pu]	$\|V\|_b$ [pu]	$\|V\|_c$ [pu]	$\|V\|_a$ [pu]	$\|V\|_b$ [pu]	$\|V\|_c$ [pu]	$I_{StatCom}$ [pu]
1	1.000	1.000	1.000	1.000	1.000	1.000	
2	0.935	0.949	0.913	0.943	0.951	0.960	
3	0.906	0.925	0.876	0.921	0.929	0.967	0.277
4	0.895	0.917	0.862	0.910	0.920	0.951	
5	0.886	0.912	0.847	0.900	0.915	0.935	
6	0.904	0.925	0.870	0.912	0.927	0.915	
7	0.896	0.919	0.856	0.903	0.921	0.900	
8	0.902	0.922	0.868	0.909	0.924	0.912	
9	0.921	0.940	0.891	0.928	0.942	0.937	
10	0.910	0.934	0.874	0.918	0.936	0.919	
11	0.890	0.911	0.856	0.914	0.917	0.947	
12	0.872	0.896	0.833	0.909	0.906	0.925	
13	0.862	0.888	0.818	0.909	0.900	0.912	0.067
14	0.893	0.915	0.860	0.907	0.918	0.949	
15	0.893	0.914	0.860	0.907	0.918	0.949	
Ave. /Total	0.904	0.924	0.872	0.919	0.928	0.939	0.344

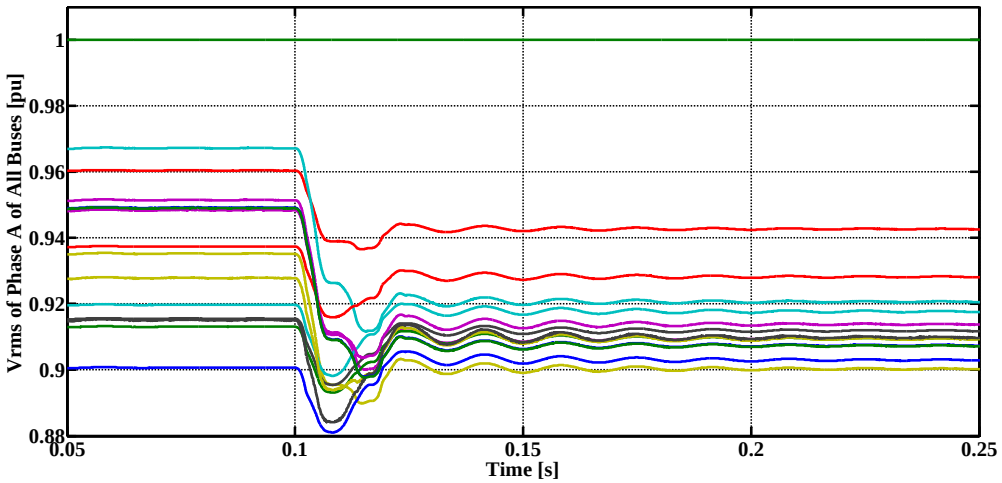
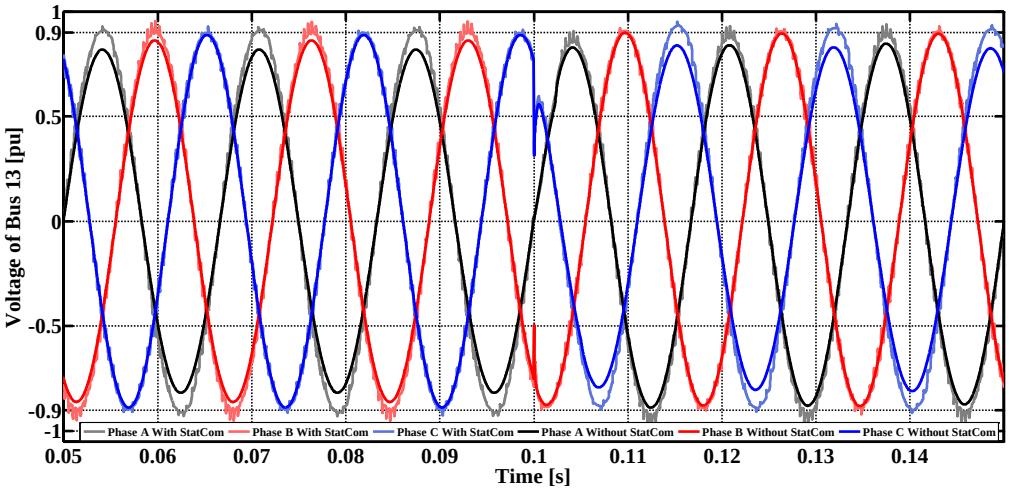
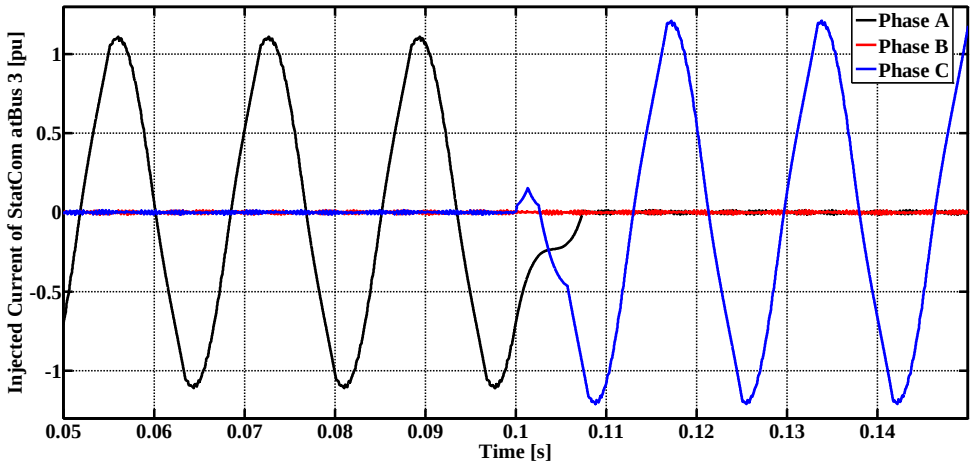


Figure 3.12: |V| of all buses for cases 3-I and 3-K Simulation in unbalanced network of Fig 3.7



(a)



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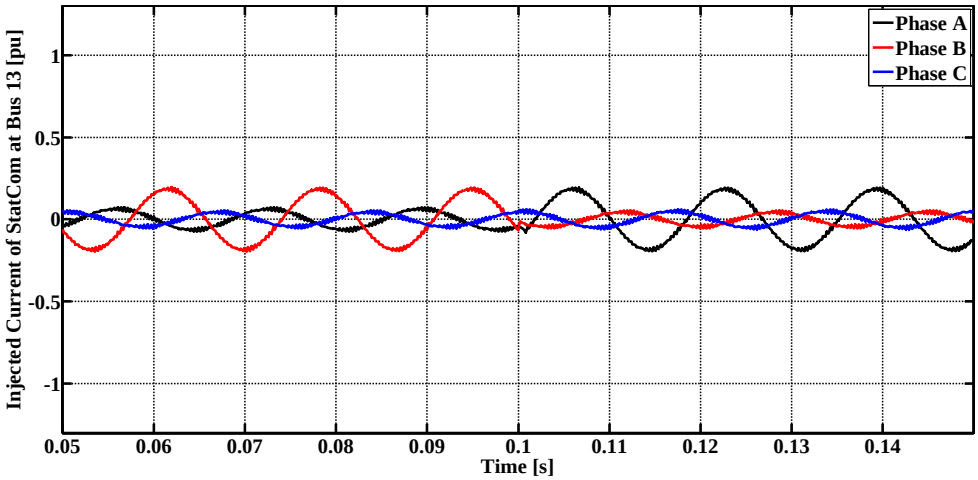


(c)

Figure 3.13: Simulation results of StatCom in unbalanced network of Fig 3.7; (a) voltage profile of bus 13 with and without StatComs for cases 3H to 3-K, (b) injected current of StatCom at bus 3 for cases 3-I and 3-K, (c) injected current of StatCom at bus 13 for cases 3-I and 3-K

CHAPTER 4: OPTIMAL SITING AND SIZING OF MULTIPLE APLCs FOR FUNDAMENTAL AND HARMONIC VOLTAGE COMPENSATION

The reactive power and harmonic compensation can be achieved by using shunt FACTS devices. Usually, StatCom can be used for reactive power compensation (Chapter 2) while APF compensate harmonic distortions. As mentioned before, APFs compensate 100% of nonlinear load harmonics and improve the power quality of power systems. However, this approach needs one APF for each nonlinear load which is not economical. Therefore, APLC as a custom power device is proposed to reduce the harmonics of the entire network to meet the minimum requirements of network specified by IEEE Standard 519-1992 [38]. Most of the researches are based on compensating only reactive power or voltage harmonic distortions of the network. However, some of them try to compensate both the reactive power and voltage harmonics together [141-146]. In [141] the APF is designed to provide reactive power and harmonics compensation for linear and non-linear single-phase loads. [142] proposes universal active filter topology for single-phase systems applications without transformer with a combination of parallel and series active filters. In [143-146] they talk about StatCom with harmonic elimination capability. In other publications [147-150] a custom power device consists of series and shunt converter called UPQC is investigated to compensate the line current distortion and also maintain the bus voltage.

All mentioned publications compensate the voltage and harmonic distortion of only one load at PCC. Just [147] considers compensation of entire network and discussed the

allocation of UPQC in the radial distribution network. However, in [147] only the reactive power compensation of a distribution network is considered and the UPQCs based on three objectives functions of rating of UPQC, network power loss and percentage of nodes with under-voltage problem are allocated.

This chapter compensates both the reactive power and harmonic distortion of entire radial distribution network by using just shunt APLC. It proposes two PSO-based algorithms for optimal siting (placement), sizing (rating) and online control (operation) of multiple APLCs in distorted SGs that rely on smart meter recorded and transmitted data. The objective function consists of minimization of the overall network THDv and total APLC injected current while the constraints include the fundamental voltage ($V_{\mathbf{Fund}}$) of each bus, network THDv and individual bus voltage harmonics with an optional limit for the maximum APLC sizes. Detailed simulations are presented and analyzed for the 15-bus network of [139] with six nonlinear loads. The impacts of the weighting factors in the objective function for APLC size and THDv as well as the effect of including an upper limit for APLC ratings are also investigated.

4.1 Modelling for Optimal Siting and Sizing of APLC for Fundamental and Harmonic Voltage Compensation

The APLCs are modeled as decoupled harmonic current sources injecting harmonic currents at PCCs. This section proposes a PSO-based algorithm for optimal siting and sizing of multiple APLCs. The size of an APLC connected to bus *k* can be expressed as [37-48]:

$$I_{k,APLC\ size} = I_{k,APLC-fundamental} + I_{k,APLC-harmonics} = I^1_{k,APLC} + \sqrt{\sum_{h=2}^{H} \left| I^h_{k,APLC} \right|^2}, \quad k = 1,...,K, \ \ h = 2,...,H \tag{4.1}$$

where *k* and *h* are the bus number and the harmonic order while *K* and *H* represent their maximum values, respectively.

The objective function for optimal siting and sizing of APLCs is to minimize their sizes and the overall network THDv:

$$\min \ F = W_{size}\, I_{APLC\ sizes} + W_{THD}\, THD_{v-network} = W_{size} \sum_{k=1}^{K} I_{k,APLC\ size} + W_{THD} \sum_{k=1}^{K} \sqrt{\sum_{h=2}^{H} \left| V^h_k \right|^2} \Big/ \left| V^1_k \right| \tag{4.2}$$

where W_{size} and W_{THD} are the weighting factors for APLC size and network THDv while V^1_k and V^h_k represent the fundamental and harmonic voltages at bus *k*, respectively. The selected constraints associated with Eq. 4.2 are lower limit for $V_{\mathbf{Fund}}$, the upper limits for the THDv and individual voltage harmonics of each bus according to the IEEE-519 standard [37-38]:

$$V_{Fund-k} \geq 0.9\, pu \tag{4.3}$$

$$THD_{v,k} = \sqrt{\sum_{h=2}^{H} \left| V^h_k \right|^2} \Big/ \left| V^1_k \right| \leq THD^{\lim it}_{v,bus} = 0.05 \tag{4.4}$$

$$\left| V^h_k \right| / \left| V^1_k \right| \leq \left| V \right|^{\lim it}_{bus} = 0.03 \tag{4.5}$$

where V_{Fund-k} is the fundamental voltage of bus k.

A PSO algorithm is used to solve Eqs. 4.2-4.5. The proposed PSO algorithm for siting and sizing of APLCs is demonstrated in the flowchart of Fig. 4.1a. Based on this figure, an APLC unit is installed temporarily at each bus except the swing bus and then PSO

performs an optimization solution for Eqs. 4.1 to 4.5. At the last step, APLCs with sizes greater than a desired lower limit (e.g., $I_{min,APLC\ size}$= 0.01pu) are selected.

4.2 Optimal Online Operation of APLCs for Fundamental and Harmonic Voltage Compensation

The problem formulation for online control of APLCs based on the received smart meter data at each APLC bus is similar to Eqs. 4.1-4.5 with the following differences (Fig. 4.1b):

- APLCs are only installed at the optimal locations determined by the first PSO algorithm (Fig. 4.1a) of Section 4.1.
- Network status and optimization of the objective function are updated at time steps Δt for the period of 24 hours:

$$\begin{aligned} \min\ F(t) = & W_{THD} \sum_{k=1}^{K} [\sqrt{\sum_{h=2}^{H} \left|V_k^h(t)\right|^2} / \left|V_k^1\right|(t)] \\ & + W_{size} \sum_{k=1}^{K} I_{k,APLC\ size}(t); \quad for\ t = \Delta t,\ 2\Delta t,\ 3\Delta t, ... \end{aligned} \tag{4.6}$$

- An additional constraint is included for the maximum sizes of the installed APLCs according to their ratings:

$$I_{m,APLC\ size} = \sqrt{\sum_{h=1}^{H} \left|I_m^h\right|^2} \le I_{m,\max} \tag{4.7}$$

where m and $I_{m,max}$ are the optimal locations and ratings of APLCs as determined by the first PSO algorithm.

The flowchart of the second PSO algorithm is shown in Fig. 4.1b. It consists of the following main steps:

1) The optimal number, locations and ratings of the required APLCs are determined based on the first PSO algorithm of Fig. 4.1a. The APLCs are installed at the selected optimal locations (buses).

2) The SG central control (SGCC) receives the recorded information by smart meters through the communication network on online basis with time steps of Δt, executes the second PSO algorithm of Fig. 4.1b, and sends the optimal inverter reference currents to the APLCs. The value of Δt depends on SG communication design and the required time to transmit data to SGCC and APLCs.

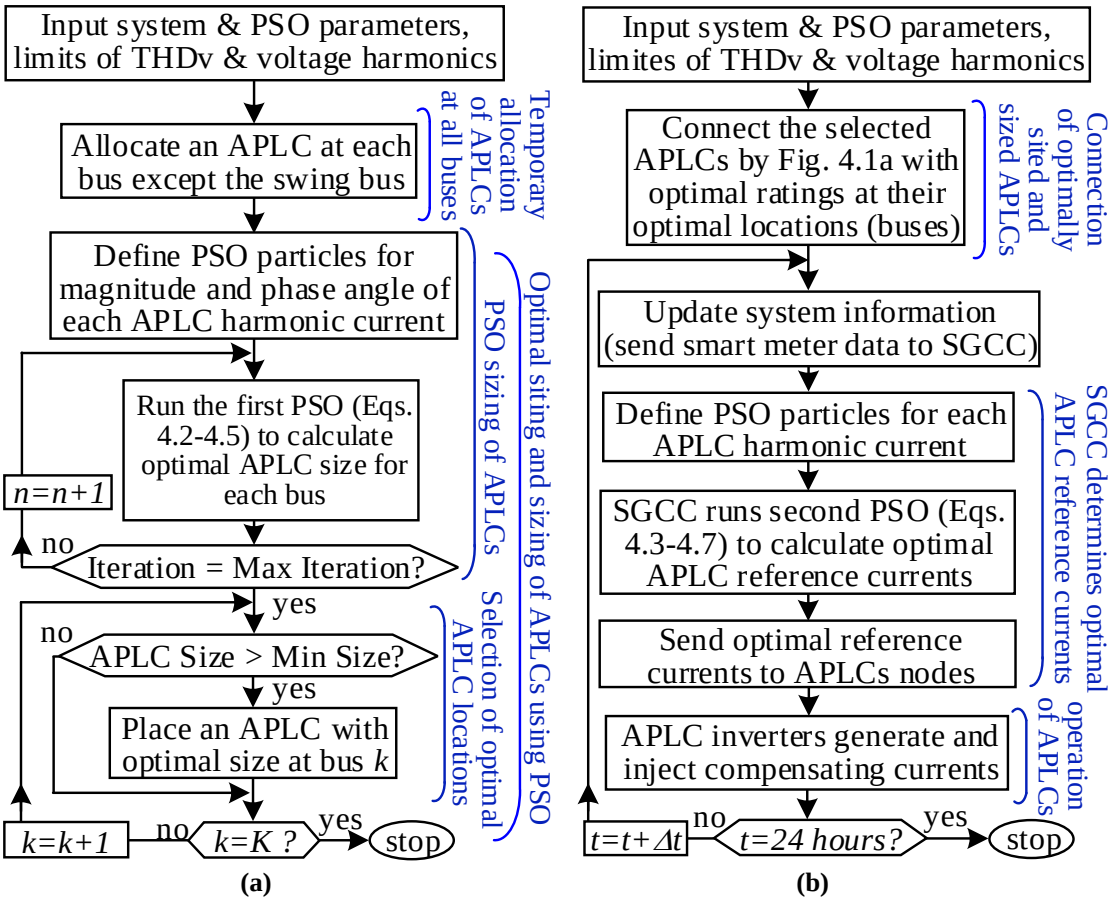


Figure 4.1: Flowchart of the proposed PSO algorithm for fundamental and harmonic voltage compensation; (a) optimal siting and sizing of multiple APLCs based on Eqs. 4.1-4.5, (b) optimal online control of the installed APLCs based on Eqs. 4.3-4.7

4.3 Simulation Results

To assess the performance of the proposed approaches for optimal siting, sizing and online operation of APLCs, the 15-bus, 60 Hz radial network of Fig. 4.2 is considered [139]. System line and load parameters are presented in Tables 3.1-3.2. There are six nonlinear loads connected to buses 5, 7, 8, 10, 13, and 15. Decoupled harmonic current sources are used for the nonlinear load modeling (Table 4.1). Each nonlinear load is modeled with decoupled harmonic current sources injecting harmonic currents that are equal to the current distortions of the exact model (three-phase full wave resistive rectifier) with rated sinusoidal voltage excitation. Therefore, the injected current harmonics are fixed and independent of system operating conditions (not considering harmonic couplings). The selected values for base power and base voltage are 2.5MVA and 11 kV. The optimal siting and sizing simulations are performed for the worse scenario with maximum linear and non-linear loading conditions.

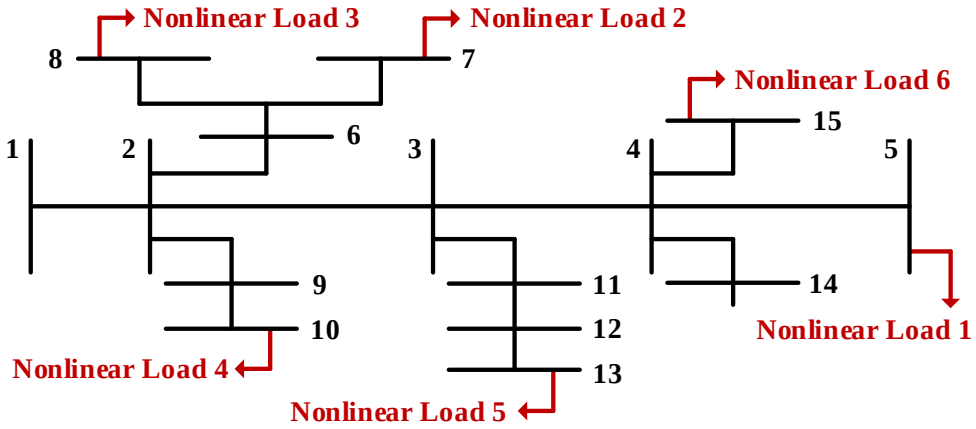


Figure 4.2: Single-line diagram of the 15-bus distorted system [139] with six nonlinear loads (Tables 3.1-3.2)

Four study cases are simulated and the results are presented in Tables 4.2-4.9. These cases include: 1) system operation without APLCs (Case 4-A), 2) optimal siting/sizing of APLCs (Case 4-B), 3) optimal siting/sizing of APLCs considering a maximum APLC current of 0.15pu (Case 4-C) and 4) optimal siting/sizing of APLCs considering a maximum APLC current of 0.1pu (Case 4-D).

Table 4.1: Current harmonic injection of the nonlinear loads (in percentage of the fundamental component) in the network of Fig. 4.2

	Harmonic Order of The Approximated Decoupled Model				
Harmonic order	5	7	11	13	17
percentage of the harmonic order to fundamental component [%]	22.60	11.34	9.02	6.49	5.63

4.3.1 System Operation without APLCs (Case 4-A)

This case illustrates the worse operating condition of the network with maximum loadings of all linear and nonlinear loads. Simulation results for this case are presented in Table 4.2 for individual voltage harmonics (columns 2-6), THDv (column 7) and V_{Fund} (column 8) of all buses. Fig. 4.3 also illustrates the individual harmonic distortions and THDv of Case 4-A.

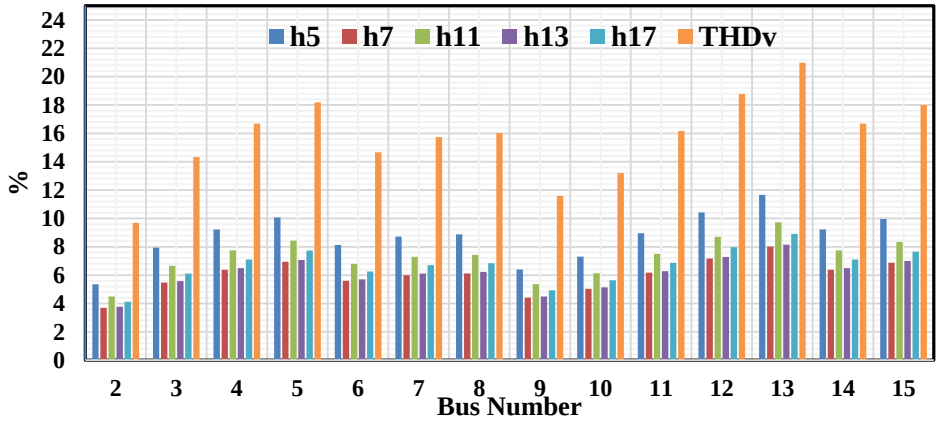


Figure 4.3: Simulation results for Case 4-A (operation of the network in Fig. 4.2 without any APLCs, Table 4.2)

Table 4.2: Case 4-A; Operation of the network in Fig. 4.2 without any APLCs

Bus Number	Case 4-A						
	Harmonic Voltage Distortion (%)					THDv [%]	V_{Fund} [pu]
	5	7	11	13	17		
2	5.35	3.70	4.50	3.77	4.13	9.69	0.925
3	7.94	5.48	6.66	5.58	6.11	14.34	0.891
4	9.23	6.38	7.75	6.49	7.10	16.69	0.877
5	10.07	6.95	8.44	7.07	7.74	18.19	0.869
6	8.13	5.60	6.80	5.70	6.26	14.67	0.883
7	8.72	6.00	7.30	6.11	6.71	15.74	0.875
8	8.88	6.12	7.43	6.23	6.84	16.03	0.873
9	6.40	4.42	5.37	4.50	4.94	11.58	0.911
10	7.31	5.04	6.13	5.14	5.64	13.21	0.901
11	8.96	6.18	7.50	6.28	6.87	16.17	0.874
12	10.42	7.17	8.71	7.29	7.97	18.77	0.854
13	11.66	8.02	9.73	8.15	8.91	20.99	0.842
14	9.23	6.38	7.75	6.49	7.10	16.69	0.875
15	9.96	6.88	8.35	7.00	7.66	18.00	0.868
Ave. /Total	8.73	6.02	7.32	6.13	6.71	15.77	0.880

Clearly, the entire network is highly distorted, the THDv of all buses are greater than the permitted limit of 5% and the voltage harmonics of most buses are above the acceptable level of 3%. Moreover, the fundamental voltage (V_{Fund}) of most buses is less than the standard value of 0.9 pu. Bus 13 is the worst distorted point of the network (Table 4.2, Fig. 4.3) due to its remote location from bus 1. This is the farthest bus from the swing bus (e.g., the higher line impedance) with the THDv and V_{Fund} values of 20.99% and 0.84 pu, respectively.

4.3.2 Optimal Siting and Sizing of Multiple APLCs (Case 4-B) for Fundamental and Harmonic Voltage Compensation

The PSO algorithm of Fig. 4.1a is used to find the optimal locations and sizes of the APLCs for the 15-bus network of Fig. 4.2. Simulation results are summarized in Table 4.3. The values of weighting factors in Eq. 4.6 are selected to be W_{THD} = 0.5 and W_{size} =0.5. Section 4.3.2.1 investigates the impacts of weighting factors on the optimal siting and sizing of multiple APLCs.

Table 4.3: Case 4-B; Optimal siting and sizing of multiple APLCs for the network of Fig. 4.2 for fundamental and harmonic voltage compensation

Bus Number	Case 4-B							
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	I_{APLC} [pu]
	5	7	11	13	17			
2	0.65	0.79	1.20	0.58	0.46	1.74	0.945	0
3	0.14	0.59	1.25	0.33	0.16	1.45	0.924	0.1669
4	1.25	1.41	2.26	1.17	1.02	3.32	0.909	0
5	1.99	1.92	2.89	1.70	1.61	4.63	0.901	0
6	1.25	1.38	1.82	0.92	0.74	2.86	0.910	0.1020
7	1.78	1.75	2.27	1.30	1.15	3.80	0.902	0
8	1.93	1.85	2.40	1.40	1.27	4.06	0.900	0
9	1.62	1.46	2.03	1.27	1.24	3.47	0.930	0
10	2.46	2.04	2.74	1.87	1.92	4.99	0.920	0
11	0.14	0.45	0.91	0.28	0.61	1.23	0.913	0
12	0.14	0.27	0.50	0.97	1.47	1.86	0.904	0
13	0.14	0.16	0.41	1.57	2.19	2.73	0.901	0.1163
14	1.25	1.41	2.26	1.17	1.02	3.32	0.907	0
15	1.89	1.86	2.81	1.63	1.53	4.46	0.900	0
Ave. /Total	1.19	1.24	1.84	1.15	1.17	3.14	0.912	0.385

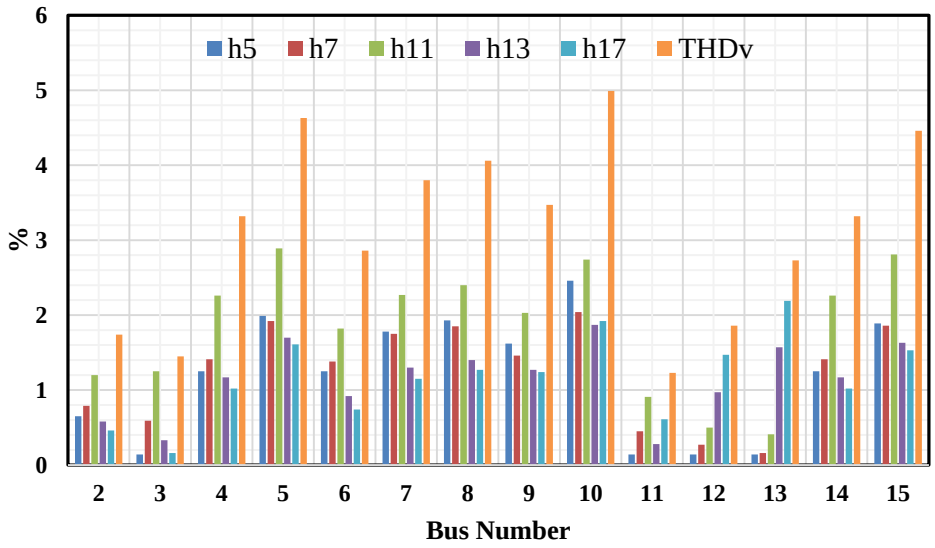


Figure 4.4: Simulation results for Case 4-B (Table 4.3)

The solution of Case 4-B requires three APLCs at buses 3, 6 and 13 with ratings of 0.167 pu, 0.102 pu and 0.116 pu respectively. Based on Table 4.3 and Fig. 4.4, by implementing APLCs with their optimal locations and sizes, the THDv of entire network is reduced to less than standard value of 5% (Table 4.3, column 7), individual voltage harmonic of all buses to less than 3% (Table 4.3, columns 2-6) and the $V_{\mathbf{Fund}}$ of entire network is maintained to be minimum 0.9 pu (Table 4.3, column 8).

4.3.2.1 The Impact of Objective Function Weighting Factors on Optimal Siting and Sizing of APLCs (Case 4-C)

Our investigations show the significant impacts of the objective function weighting factors on the APLC siting/sizing solution of Eq. 4.2 (Table 4.4). Large values of W_{size} result in smaller amount of APLC ratings with most THDv values approaching the maximum limit of 5%. On the other hand, lager values of W_{THD} result in lower THDv

levels. However, both options require many APLC units similar to the conventional approach of connecting APFs at all nonlinear buses that is not a practical solution. Therefore, equal values for W_{size} and W_{THD} are selected (Table 4.4, last row).

Table 4.4 demonstrates the optimal siting and sizing of APLCs for different weighting factors. Also, Fig 4.5 shows the effects of weighting factors on optimal siting and sizing of APLCs. For $W_{THD} = 0$ and $W_{size} = 1$, the PSO allocates 6 APLCs (exactly one at each nonlinear load bus) to result in minimum total APLC size ($I_{APLC} = 0.339$ pu). In this case, the THDv of the network is 4.53% which is very close to 5%. Moreover, by increasing the value of W_{THD} and decreasing W_{size}, the THDv of network reduces while the total APLCs currents increase. In this chapter, the weighting factors of $W_{THD} = 0.5$ and $W_{size} = 0.5$ are chosen. The results for equal weighting factors are represented in Table 4.3. Tables 4.5-4.10 illustrate the simulation results for other values of weighting factors based on Table 4.4.

Based on Tables 4.4-4.10 and Fig. 4.5, some points can be concluded:

- In all cases, the individual harmonic distortions and THDv of all buses are below the limited value of 3% and 5%, respectively. Also, the $V_{\mathbf{Fund}}$ of all buses is more than the minimum value of 0.9 pu.
- In case 4-C1 ($W_{THD} = 0$, $W_{size} = 1$), the minimum $I_{\mathbf{APLC}}$ and maximum THDv is achieved by allocating APLC at each nonlinear bus. Based on Table 4.5, the THDv of most buses is close to 5% which is the PSO constraint while the total APLC current is minimum. However, this case is not applicable due to a high number of allocated APLCs ($W_{size} = 1$).

- In Case 4-C7 (W_{THD} = 1, W_{size} =0), the performance of APLCs is like APFs and each APLC injects exactly equal but opposite direction of harmonic currents produced by the nonlinear load. As a result, the THDv of the network is zero while the total APLC current is maximum. This case also is not applicable. Fig. 4.6 shows the voltage profile of bus 13 for Cases 4-A (without APLC), 4-C1 and 4-C7.
- Case 4-C4 (W_{THD} = 0.5, W_{size} =0.5) results lower number of required APLCs. This case is selected for the rest of this chapter simulations. Moreover, by applying maximum size of APLC, the desired selection can be made based on available size on the market.

Table 4.4: Case 4-C; Impact of the objective function weighting factors (Eq. 4.2) on optimal APLC siting and sizing solutions

Case	Weighting Factors (Eq. 4.2)		PSO Solutions for Eq. 4.2								
			Objective Function			Optimal APLC Locations/Sizes					
	W_{THD}	W_{size}	THD_{Net}	I_{APLC}	$min\ F$	APLC 1	APLC 2	APLC 3	APLC 4	APLC 5	APLC 6
4-C1	0	1.0	4.53	0.339	0.339	Bus 5 0.0426	Bus 7 0.0358	Bus 8 0.0620	Bus 10 0.0181	Bus 13 0.1258	Bus 15 0.0543
4-C2	0.2	0.8	4.13	0.361	1.1148	Bus 5 0.0396	Bus 8 0.1032	Bus 9 0.0412	Bus 13 0.1259	Bus 15 0.0507	
4-C3	0.4	0.6	3.76	0.367	1.724	Bus 4 0.114	Bus 8 0.1018	Bus 9 0.0309	Bus 13 0.1206		
4-C4	0.5	0.5	3.14	0.379	1.760	Bus 3 0.1617	Bus 6 0.1009	Bus 13 0.1163			
4-C5	0.6	0.4	2.77	0.387	1.817	Bus 4 0.1192	Bus 8 0.1071	Bus 9 0.0390	Bus 13 0.1215		
4-C6	0.8	0.2	1.50	0.394	1.279	Bus 5 0.0546	Bus 8 0.1003	Bus 9 0.0470	Bus 13 0.1294	Bus 15 0.0626	
4-C7	1.0	0	0.12	0.406	0.12	Bus 5 0.0521	Bus 7 0.0487	Bus 8 0.0709	Bus 10 0.0445	Bus 13 0.1287	Bus 15 0.0614
Selected Parameters for Case 4-D (Table 4.11) Considering Maximum Individual APLC Size of 0.15 pu											
4-D	0.5	0.5	3.33	0.383	1.857	Bus 3 0.15	Bus 6 0.1128	Bus 13 0.1205			

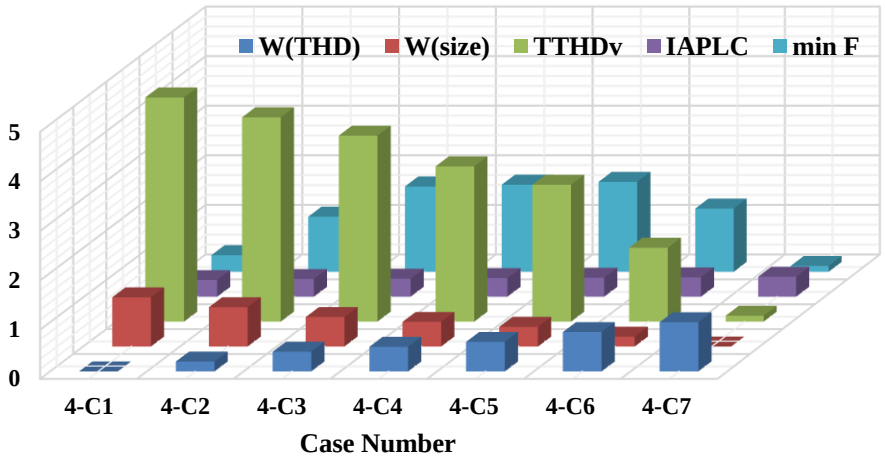


Figure 4.5: Impact of the objective function weighting factors (Eq. 4.2) on optimal APLC siting and sizing solutions

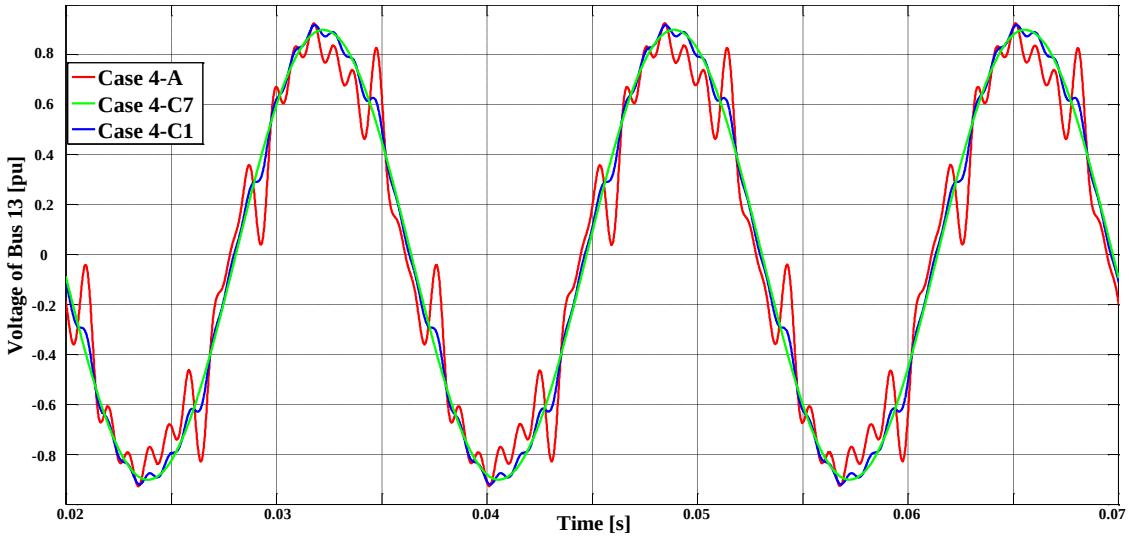


Figure 4.6: Impact of the objective function weighting factors (Eq. 4.2) on voltage profile of bus 13 on a network of Fig. 4.2

Table 4.5: Optimal siting and sizing of multiple APLCs for the network of Fig. 4.2 for W_{THD} = 0, W_{size} = 1 and without constraint on maximum APLC current (Case 4-C1)

Bus Number	Case 4-C1							
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	I_{APLC} [pu]
	5	7	11	13	17			
2	1.77	1.10	1.21	0.94	1.52	3.00	0.942	-
3	2.33	1.42	1.61	1.30	2.12	4.03	0.919	-
4	2.63	1.60	1.85	1.52	2.48	4.62	0.907	-
5	2.90	1.70	1.95	1.60	2.68	4.98	0.900	0.0426
6	2.70	1.68	1.80	1.42	2.37	4.58	0.907	-
7	2.89	1.85	1.91	1.53	2.62	4.96	0.900	0.0358
8	2.95	1.80	1.98	1.53	2.51	4.95	0.900	0.0620
9	2.42	1.51	1.63	1.21	1.87	3.97	0.928	-
10	2.97	1.87	1.99	1.44	2.17	4.81	0.918	0.0181
11	2.50	1.49	1.71	1.38	2.28	4.30	0.910	-
12	2.73	1.59	1.85	1.50	2.49	4.68	0.902	-
13	2.92	1.68	1.97	1.59	2.67	4.99	0.900	0.1258
14	2.63	1.60	1.85	1.52	2.48	4.62	0.905	-
15	2.75	1.73	2.01	1.68	2.68	4.97	0.900	0.0543
Ave.	2.65	1.62	1.81	1.44	2.35	4.53	0.910	0.339

Table 4.6: Optimal siting and sizing of multiple APLCs for the network of Fig. 4.2 for W_{THD} = 0.2, W_{size} = 0.8 and without constraint on maximum APLC current (Case 4-C2)

Bus Number	Case 4-C2							
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	I_{APLC} [pu]
	5	7	11	13	17			
2	1.43	0.82	1.05	0.74	1.35	2.49	0.942	-
3	2.15	1.35	1.58	1.11	1.90	3.71	0.919	-
4	2.53	1.65	1.89	1.29	2.22	4.39	0.907	-
5	2.78	1.83	2.07	1.37	2.46	4.83	0.900	0.0396
6	2.22	1.34	1.72	1.15	2.25	4.01	0.908	-
7	2.76	1.71	2.17	1.53	2.67	4.97	0.900	-
8	2.01	1.19	1.55	0.94	2.23	3.71	0.903	0.1032
9	1.59	0.70	1.08	0.84	1.52	2.68	0.928	0.0412
10	2.43	1.27	1.78	1.43	2.17	4.18	0.918	-
11	2.37	1.49	1.72	1.23	2.06	4.07	0.910	-
12	2.69	1.69	1.91	1.40	2.27	4.57	0.903	-
13	2.95	1.86	2.07	1.54	2.45	4.98	0.901	0.1259
14	2.53	1.65	1.89	1.29	2.22	4.39	0.905	-
15	2.74	1.82	2.08	1.43	2.35	4.76	0.900	0.0507
Ave. /Total	2.37	1.45	1.76	1.24	2.15	4.13	0.910	0.361

Table 4.7: Optimal siting and sizing of multiple APLCs for the network of Fig. 4.2 for W_{THD} = 0.4, W_{size} = 0.6 and without constraint on maximum APLC current (Case 4-C3)

Bus Number	Case 4-C3							
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	I_{APLC} [pu]
	5	7	11	13	17			
2	1.15	0.78	1.09	0.54	1.31	2.27	0.943	-
3	1.45	1.21	1.58	0.78	1.81	3.16	0.920	-
4	1.60	1.31	1.85	0.97	2.19	3.67	0.909	0.1140
5	2.34	1.82	2.47	1.49	2.77	4.98	0.900	-
6	1.86	1.07	1.71	0.89	2.37	3.74	0.908	-
7	2.40	1.44	2.16	1.26	2.79	4.68	0.900	-
8	1.61	0.80	1.52	0.64	2.43	3.45	0.902	0.1018
9	1.55	0.92	1.27	0.59	1.38	2.67	0.929	0.0309
10	2.39	1.49	1.97	1.18	2.03	4.16	0.918	-
11	1.58	1.55	1.73	0.78	1.81	3.43	0.910	-
12	1.75	2.01	1.93	0.78	1.81	3.83	0.903	-
13	1.89	2.40	2.09	0.78	1.81	4.19	0.900	0.1206
14	1.60	1.31	1.85	0.97	2.19	3.67	0.907	-
15	2.25	1.76	2.39	1.42	2.69	4.81	0.900	-
Ave. /Total	1.82	1.42	1.83	0.93	2.10	3.76	0.911	0.367

Table 4.8: Optimal siting and sizing of multiple APLCs for the network of Fig. 4.2 for W_{THD} = 0.6, W_{size} = 0.4 and without constraint on maximum APLC current (Case 4-C5)

Bus Number	Case 4-C5							
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	I_{APLC} [pu]
	5	7	11	13	17			
2	0.75	0.00	0.69	0.25	1.26	1.64	0.943	-
3	1.07	0.15	0.94	0.27	1.76	2.28	0.920	-
4	1.19	0.27	1.12	0.28	2.13	2.72	0.909	0.1192
5	1.93	0.23	1.74	0.79	2.71	3.85	0.900	-
6	1.11	0.25	1.30	0.59	2.31	2.95	0.908	-
7	1.65	0.61	1.75	0.97	2.74	3.82	0.900	-
8	0.69	0.05	1.10	0.35	2.37	2.73	0.902	0.1071
9	0.95	0.00	0.70	0.25	1.27	1.76	0.929	0.0390
10	1.79	0.57	1.39	0.84	1.92	3.14	0.918	-
11	1.25	0.15	0.94	0.27	1.75	2.37	0.911	-
12	1.49	0.16	0.94	0.26	1.75	2.50	0.903	-
13	1.69	0.16	0.94	0.26	1.75	2.63	0.900	0.1215
14	1.19	0.27	1.12	0.28	2.13	2.72	0.907	-
15	1.84	0.17	1.66	0.72	2.64	3.69	0.900	-
Ave. /Total	1.33	0.22	1.17	0.46	2.04	2.77	0.911	0.387

Table 4.9: Optimal siting and sizing of multiple APLCs for the network of Fig. 4.2 for W_{THD} = 0.8, W_{size} = 0.2 and without constraint on maximum APLC current (Case 4-C6)

Bus Number	Case 4-C6							
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	I_{APLC} [pu]
	5	7	11	13	17			
2	0.43	0.17	0.48	0.48	0.67	1.07	0.942	-
3	0.31	0.09	0.35	0.40	0.66	0.91	0.919	-
4	0.25	0.05	0.28	0.35	0.66	0.85	0.907	-
5	0.19	0.02	0.23	0.32	0.67	0.81	0.901	0.0546
6	1.35	0.60	1.45	1.28	1.63	2.93	0.908	-
7	1.88	0.96	1.90	1.66	2.05	3.88	0.900	-
8	1.20	0.40	1.43	1.26	1.63	2.81	0.903	0.1003
9	0.37	0.14	0.43	0.51	0.70	1.05	0.928	0.0470
10	1.20	0.71	1.12	1.10	1.35	2.50	0.918	-
11	0.28	0.04	0.31	0.40	0.66	0.88	0.910	-
12	0.23	0.03	0.27	0.40	0.66	0.85	0.903	-
13	0.20	0.09	0.23	0.40	0.66	0.83	0.901	0.1294
14	0.25	0.05	0.28	0.35	0.66	0.85	0.905	-
15	0.22	0.06	0.26	0.33	0.67	0.83	0.900	0.0626
Ave. /Total	0.60	0.24	0.64	0.66	0.95	1.50	0.910	0.394

Table 4.10: Optimal siting and sizing of multiple APLCs for the network of Fig. 4.2 for W_{THD} = 1, W_{size} = 0 and without constraint on maximum APLC current (Case 4-C7)

Bus Number	Case 4-C7							
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	I_{APLC} [pu]
	5	7	11	13	17			
2	0.01	0.01	0.00	0.00	0.01	0.13	0.942	-
3	0.01	0.01	0.00	0.01	0.01	0.13	0.919	-
4	0.01	0.01	0.00	0.01	0.02	0.13	0.907	-
5	0.02	0.01	0.01	0.01	0.02	0.13	0.900	0.0521
6	0.01	0.01	0.01	0.00	0.01	0.13	0.907	-
7	0.01	0.01	0.01	0.00	0.01	0.13	0.900	0.0487
8	0.01	0.01	0.01	0.00	0.01	0.13	0.900	0.0709
9	0.01	0.01	0.00	0.00	0.01	0.13	0.928	-
10	0.01	0.01	0.00	0.01	0.02	0.13	0.918	0.0445
11	0.01	0.01	0.01	0.01	0.01	0.09	0.910	-
12	0.01	0.01	0.01	0.01	0.02	0.09	0.902	-
13	0.02	0.01	0.01	0.01	0.02	0.09	0.900	0.1287
14	0.01	0.01	0.00	0.01	0.02	0.13	0.905	-
15	0.01	0.01	0.00	0.01	0.02	0.13	0.900	0.0614
Ave. /Total	0.01	0.01	0.01	0.01	0.01	0.12	0.910	0.0406

4.3.3 Optimal Siting and Sizing of Multiple APLCs for Fundamental and Harmonic Voltage Compensation with an Additional Constraint for Maximum Size of APLCs of 0.15 pu (Case 4-D)

In practice, utilities may also require a maximum limit for the APLC rating. This can be accomplished by repeating the simulations of Case 4-B with an additional constraint on the maximum size of APLCs which is selected to be 0.15 pu in this case. Simulation results are presented in Table 4.11.

Table 4.11: Case 4-D; Optimal siting and sizing of multiple APLCs considering a maximum APLC current of 0.15 pu for the network of Fig. 4.2 for fundamental and harmonic voltage compensation (W_{THD} = 0.5, W_{size} = 0.5)

Bus Number	Case 4-D									
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	$I_{APLC-total}$ [pu]	$I_{APLC-total}$ [pu]	
	5	7	11	13	17				$I_{APLC-fundamental}$	$I_{APLC-harmonic}$
2	0.91	0.57	1.19	0.41	0.49	1.73	0.945	0	0	0
3	0.91	0.31	1.18	0.09	0.12	1.53	0.923	0.15	0.1188	0.09154
4	2.10	1.11	2.18	0.84	0.97	3.47	0.909	0	0	0
5	2.84	1.62	2.81	1.37	1.57	4.79	0.900	0	0	0
6	1.00	0.97	1.89	0.76	0.95	2.64	0.910	0.1128	0.07778	0.08173
7	1.53	1.34	2.34	1.13	1.37	3.57	0.902	0	0	0
8	1.68	1.44	2.46	1.24	1.49	3.83	0.900	0	0	0
9	1.89	1.24	2.01	1.11	1.28	3.47	0.930	0	0	0
10	2.73	1.82	2.73	1.71	1.96	5.00	0.920	0	0	0
11	0.94	0.33	0.79	0.68	0.85	1.67	0.913	0	0	0
12	0.96	0.37	0.39	1.58	2.01	2.78	0.905	0	0	0
13	0.99	0.40	0.51	2.33	2.97	3.96	0.902	0.1205	0.1075	0.05442
14	2.10	1.11	2.18	0.84	0.97	3.47	0.907	0	0	0
15	2.75	1.56	2.73	1.30	1.49	4.62	0.900	0	0	0
Ave. /Total	1.67	1.01	1.81	1.10	1.32	3.33	0.912	0.383	0.30408	0.22769

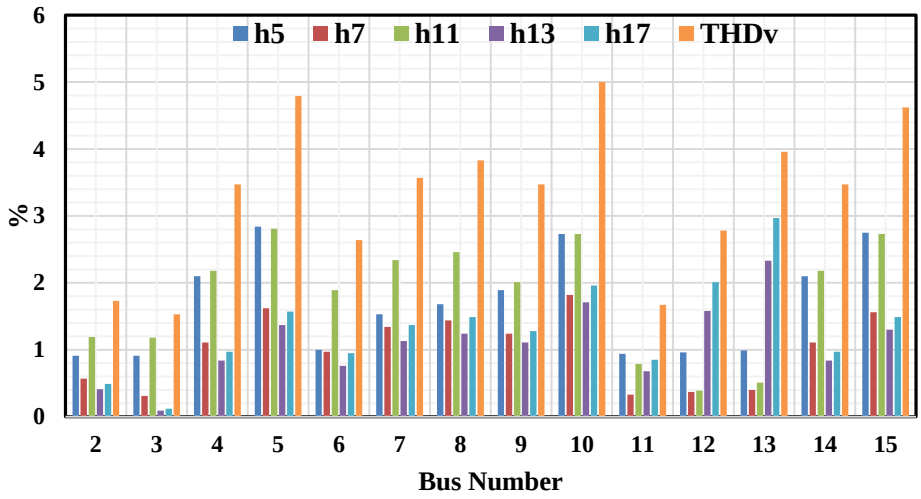


Figure 4.7: Simulation results for Case 4-D (Table 4.11)

In this case, the PSO assigned 3 APLCs at buses 3, 6 and 13 with optimal sizes of 0.15 pu, 0.1128 pu and 0.1205 pu. Columns 10 and 11 in Table 4.11 are showing the fundamental current and harmonic currents of APLCs, respectively. The total current of APLCs (fundamental plus harmonic currents) is presented at column 9. It confirms that each APLC is contributing in fundamental voltage compensation (StatCom application, column 10) and harmonic voltage compensation (APF application, column 11).

It is also noticed that the calculated objective function value of this case (Eq. 4.6) is more than case 4-B. Although, adding a constraint of the maximum size of 0.15 pu leads to the same location of APLCs compared to case 4-B but different reference currents (APLCs sizes) are concluded. Fig. 4.7 reveals the individual harmonic distortions and THDv values of Case 4-D.

4.3.4 Optimal Siting and Sizing of Multiple APLCs for Fundamental and Harmonic Voltage Compensation with an Additional Constraint for Maximum Size of APLCs of 0.10 pu (Case 4-E)

This case is identical to Case 4-D with different selected maximum size of APLCs (0.10 pu). As a result, four APLCs are located at buses 3, 6, 11 and 13 with optimal sizes of 0.100 pu, 0.100 pu, 0.098 pu and 0.087 pu, respectively. The results for this case are presented in Table 4.12. Comparing results of Cases 4-D and 4-E, a lower limit for APLC sizes result in more APLC units. Fig. 4.8 shows the individual harmonic distortions and THDv of Case 4-E.

Table 4.12: Case 4-E; Optimal siting and sizing of multiple APLCs considering a maximum APLC current of 0.10 pu for the network of Fig. 4.2 for fundamental and harmonic voltage compensation (W_{THD} = 0.5, W_{size} = 0.5)

Bus Number	Case 4-E									
	Harmonic Voltage Distortion (%)					THDv (%)	V_{Fund} [pu]	$I_{APLC-total}$ [pu]	$I_{APLC-total}$ [pu]	
	5	7	11	13	17				$I_{APLC-fundamental}$	$I_{APLC-harmonic}$
2	1.17	0.76	0.65	1.01	0.11	1.84	0.945	0	0	0
3	0.99	0.66	0.25	1.00	0.73	1.74	0.924	0.100	0.0626	0.0780
4	2.17	1.47	1.20	1.84	0.30	3.43	0.909	0	0	0
5	2.92	1.98	1.82	2.37	0.87	4.70	0.901	0	0	0
6	1.93	1.16	1.23	1.60	0.29	3.04	0.910	0.100	0.0741	0.0671
7	2.46	1.53	1.68	1.98	0.16	3.90	0.902	0	0	0
8	2.61	1.63	1.80	2.09	0.27	4.14	0.900	0	0	0
9	2.15	1.43	1.47	1.70	0.70	3.50	0.931	0	0	0
10	2.99	2.01	2.18	2.30	1.37	4.99	0.920	0	0	0
11	0.54	0.52	0.57	0.55	1.73	2.05	0.918	0.098	0.0877	0.0439
12	1.06	1.29	0.54	0.55	2.36	2.99	0.907	0	0	0
13	1.50	1.95	0.51	0.55	2.88	3.87	0.902	0.087	0.0813	0.0314
14	2.17	1.47	1.20	1.84	0.30	3.43	0.907	0	0	0
15	2.82	1.92	1.74	2.30	0.80	4.54	0.900	0	0	0
Ave. /Total	1.96	1.41	1.20	1.55	0.92	3.44	0.913	0.385	0.3057	0.2204

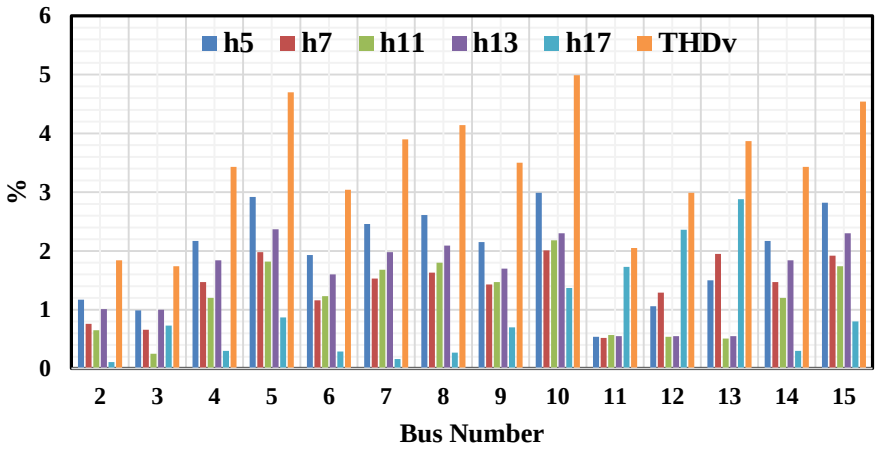


Figure 4.8: Simulation results for Case 4-E (Table 4.12)

From economical point of view, among the three study cases of 4-B, 4-D and 4-E:

- Case 4-B presents the best result with a small objective function value of 1.7625 resulting in allocations of three APLCs.
- Case 4-C considers the extra constraint of maximum APLC size equal to 0.15pu and results in the same number of APLCs as Case 4-B; however, the values of the objective function is increased to 1.8565.
- Case 4-D which is similar to Case 4-C with the maximum APLC size of 0.10pu, also results in allocation of 4 APLCs with a slightly larger objective function value of 1.9125.

4.3.5 Optimal Online Operation of the Allocated APLCs (Case 4-F) for Fundamental and Harmonic Voltage Compensation

For the optimal online operation of the network with APLCs (Figs. 4.2 and 4.9), the first PSO algorithm of Fig. 4.1a is implemented to find the optimal number, locations and sizes

of the required APLCs. The operation is done based on the results from case 4-D with equal values of waiting factors ($W_{size} = W_{THD} = 0.5$) and maximum size of APLC of 0.15 pu. The APLCs are located on buses 3, 6 and 13 with maximum selected sizes of 0.150, 0.115 and 0.125 pu, respectively. After that, at each time step (Δt), SGCC receives grid information recorded by smart meters through the SG communication network, calculates the optimal APLC reference currents by running the second PSO algorithm (Fig. 4.1b) and sends them to the APLCs.

Simulations are performed for different penetrations of simultaneously activated nonlinear loads and the results are summarized in Table 4.13.

In each case (4-F1 to 4-F6), the THD and $V_{\mathbf{Fund}}$ with and without APLCs are presented. For cases 4-F5 and 4-F6 the $V_{\mathbf{Fund}}$ is similar for with and without applying APLCs for all buses because the $V_{\mathbf{Fund}}$ before applying APLCs is higher than the standard value of 0.9 pu and the APLCs not injecting any reactive power in these two cases ($I_{\mathbf{APLC\text{-}fundamental}} = 0$). Consequently, the APLCs sizes drops dramatically from 0.132 (case 4-F4) to 0.042 (case 4-F5) pu. Figure 4.9, represent the 15-bus, 60 Hz radial network of Fig. 4.2 modeled in Matlab/Simulink.

Figure 4.10 illustrates the voltage waveform of bus 13 (worst distorted bus of Fig. 4.9) for with and without APLCs. It can be noticed that the blue waveform which is the voltage of bus 13 after applying APLCs still not completely sinusoidal. The fact is that the THDv of the network is reduced to less than 5% and not zero.

Table 4.13: Case 4-F; System operation with different numbers of simultaneously activated nonlinear loads and APLCs as allocated and sized in Cases 4-D for fundamental and harmonic voltage compensation (W_{THD} = 0.5, W_{size} = 0.5)

		Bus Number														Ave./ Total
		2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Case 4-F1: The 15-bus distorted system (Fig. 4.2) with six nonlinear loads at buses 5,7,8,10,13 and 15																
Without APLC	THD	9.69	14.34	16.69	18.19	14.67	15.74	16.03	11.58	13.21	16.17	18.77	20.99	16.69	18.00	15.77
	V_{Fund}	0.925	0.891	0.877	0.869	0.883	0.875	0.873	0.911	0.901	0.874	0.854	0.842	0.875	0.868	0.880
With APLC	THD	1.73	1.53	3.47	4.79	2.64	3.57	3.83	3.47	5.00	1.67	2.78	3.96	3.47	4.62	3.33
	V_{Fund}	0.945	0.923	0.909	0.900	0.910	0.902	0.900	0.930	0.920	0.913	0.905	0.902	0.907	0.900	0.912
APLCs sizes		-	0.150	-	-	0.113	-	-	-	-	-	-	0.121	-	-	0.384
Case 4-F2: The 15-bus distorted system (Fig. 4.2) with five nonlinear loads at buses 5,7,8,10 and 15																
Without APLC	THD	8.02	11.03	13.32	14.78	12.93	13.98	14.27	9.88	11.49	11.02	11.01	11.01	13.32	14.59	12.19
	V_{Fund}	0.932	0.904	0.890	0.881	0.889	0.882	0.880	0.918	0.908	0.896	0.890	0.889	0.888	0.881	0.895
With APLC	THD	1.71	1.38	3.45	4.80	2.60	3.53	3.79	3.47	5.00	0.85	1.22	2.05	3.45	4.63	2.99
	V_{Fund}	0.945	0.924	0.909	0.900	0.910	0.902	0.900	0.931	0.920	0.915	0.909	0.908	0.907	0.900	9.13
APLCs sizes		-	0.150	-	-	0.105	-	-	-	-	-	-	0.017	-	-	0.272
Case 4-F3: The 15-bus distorted system (Fig. 4.2) with four nonlinear loads at buses 8,10,13 and 15																
Without APLC	THD	6.53	9.61	10.79	10.79	9.02	9.02	10.29	8.36	9.94	11.36	13.84	15.97	10.79	12.02	10.60
	V_{Fund}	0.939	0.910	0.900	0.899	0.909	0.907	0.899	0.924	0.914	0.892	0.872	0.860	0.898	0.891	0.901
With APLC	THD	1.86	1.98	2.71	2.71	2.87	2.87	4.00	3.50	5.00	2.12	2.78	3.55	2.71	3.69	3.02
	V_{Fund}	0.945	0.923	0.912	0.911	0.915	0.913	0.905	0.931	0.921	0.912	0.903	0.900	0.910	0.903	9.15
APLCs sizes		-	0.038	-	-	0.028	-	-	-	-	-	-	0.124	-	-	0.19
Case 4-F4: The 15-bus distorted system (Fig. 4.2) with three nonlinear loads at buses 5,7 and 13.																
Without APLC	THD	4.57	7.45	8.49	9.87	6.76	7.74	6.76	4.57	4.57	9.16	11.59	13.68	8.49	8.49	8.01
	V_{Fund}	0.947	0.919	0.909	0.900	0.918	0.910	0.916	0.944	0.943	0.901	0.881	0.868	0.907	0.907	0.912
With APLC	THD	2.04	2.68	3.66	4.98	4.03	4.99	4.03	2.04	2.04	3.19	3.91	4.52	3.66	3.66	3.53
	V_{Fund}	0.952	0.929	0.919	0.910	0.924	0.916	0.921	0.949	0.948	0.917	0.905	0.900	0.917	0.917	0.923
APLCs sizes		-	0.037	-	-	0.006	-	-	-	-	-	-	0.089	-	-	0.132
Case 4-F5: The 15-bus distorted system (Fig. 4.2) with two nonlinear loads at buses 10 and 15																
Without APLC	THD	3.20	4.72	5.86	5.86	3.20	3.20	3.20	4.98	6.52	4.72	4.71	4.71	5.86	7.04	4.84
	V_{Fund}	0.953	0.931	0.920	0.919	0.938	0.936	0.935	0.939	0.928	0.923	0.916	0.915	0.918	0.911	0.927
With APLC	THD	1.81	2.22	3.18	3.18	1.80	1.80	1.80	3.50	5.00	2.22	2.22	2.22	3.18	4.26	2.74
	V_{Fund}	0.953	0.931	0.920	0.919	0.938	0.936	0.935	0.939	0.928	0.923	0.916	0.915	0.918	0.911	0.927
APLCs sizes		-	0.042	-	-	0	-	-	-	-	-	-	0	-	-	0.042
Case 4-F6: The 15-bus distorted system (Fig. 4.2) with one nonlinear load at bus 5																
Without APLC	THD	1.47	2.82	3.83	5.16	1.46	1.46	1.46	1.47	1.47	2.81	2.81	2.81	3.83	3.83	2.62
	V_{Fund}	0.961	0.939	0.929	0.920	0.946	0.944	0.943	0.958	0.957	0.931	0.924	0.923	0.927	0.927	0.938
With APLC	THD	1.39	2.66	3.67	5.00	1.38	1.38	1.38	1.39	1.39	2.66	2.66	2.66	3.67	3.67	2.50
	V_{Fund}	0.961	0.939	0.929	0.920	0.946	0.944	0.943	0.958	0.957	0.931	0.924	0.923	0.927	0.927	0.938
APLCs sizes		-	0.003	-	-	0	-	-	-	-	-	-	0	-	-	0.003

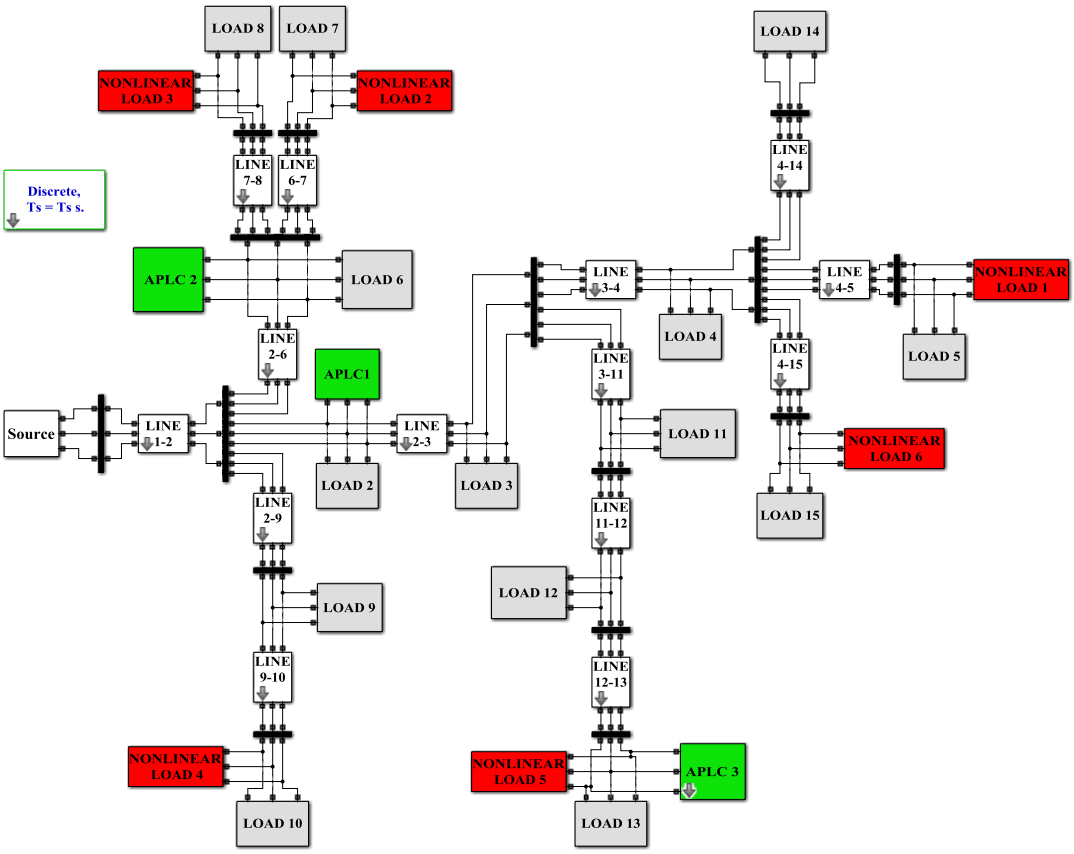


Figure 4.9: Line diagram of the three-phase 15-bus distorted system [139] in Matlab/Simulink with six nonlinear loads (Tables 3.1 and 3.2)

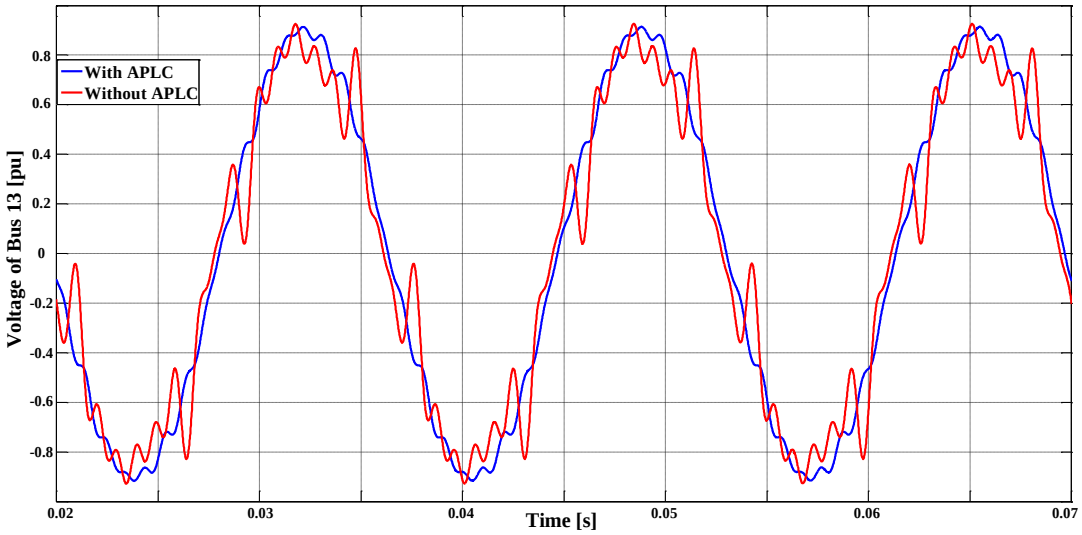


Figure 4.10: Voltage waveform of bus 13 before (red line) and after (blue line) operation of APLCs

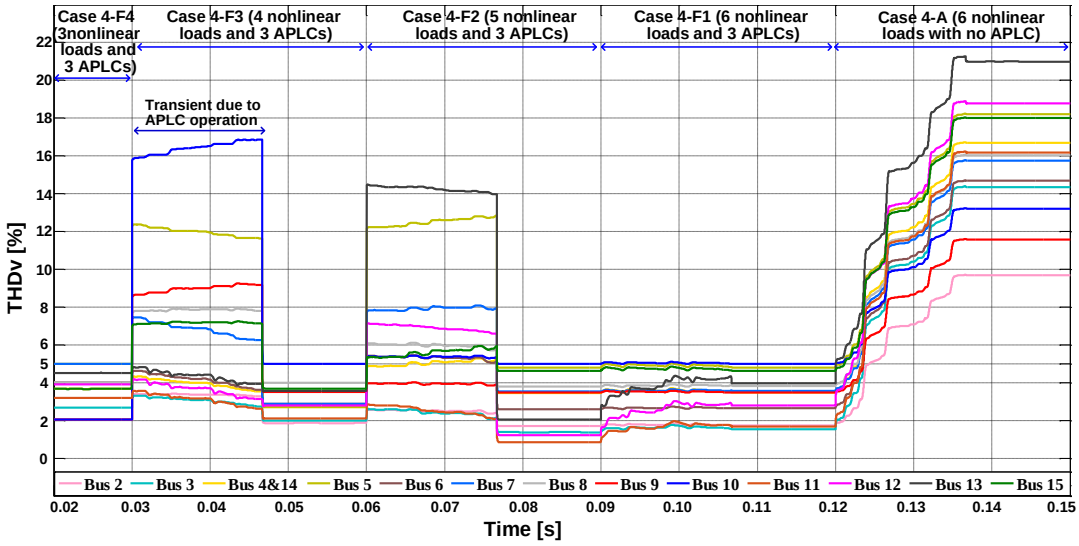


Figure 4.11: The THDv profiles of all buses for the optimal online operation of the 15-bus network of Fig. 4.2 for Cases 4-F4 to 4-F1

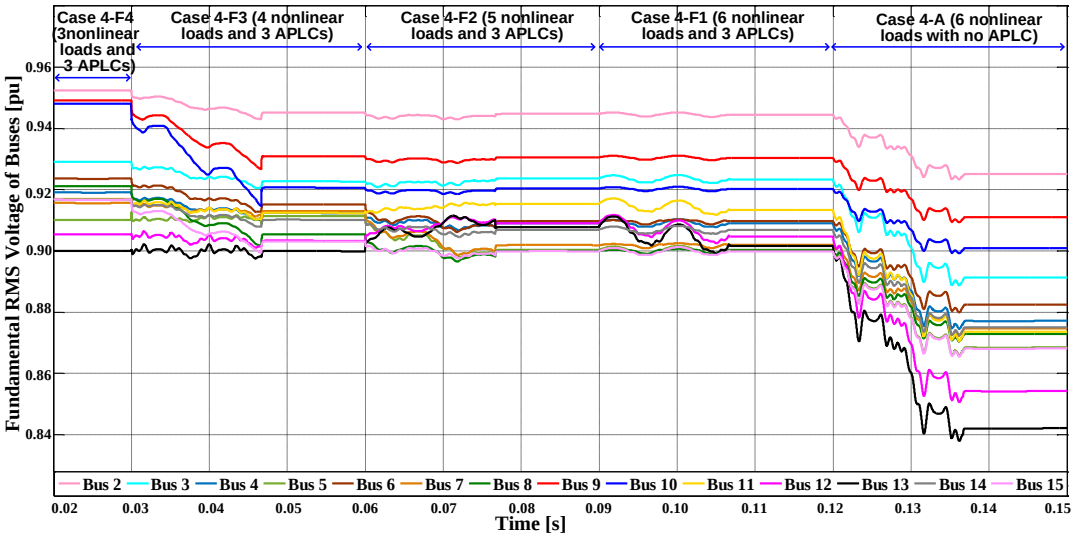


Figure 4.12: The V_{Fund} profiles of all buses for the optimal online operation of the 15-bus network of Fig. 4.2 for Cases 4-F4 to 4-F1

Figs. 4.11-4.13 demonstrate the online optimal operation of 15-bus network with the three APLCs installed at optimal locations and ratings determined in Case 4-D. The number of nonlinear loads is gradually changed from 3 to 6 units (Cases 4-F4 to 4-F1). Fig. 4.11 shows the THDv of all buses of Fig. 4.9. Based on this figure, the THDv of bus 13 before applying APLCs is 20.99% which this value after implementing APLCs is 3.96%, 2.55%, 3.55 and 4.52% for Cases 4-F1, 4-F2, 4-F3 and 4-F4,

respectively (Tables 4.2 and 4.11). Fig. 4.12 illustrates the V_{Fund} of all buses in Fig. 4.9 for cases 4-F4 to 4-F1. As can be noticed, V_{Fund} is maintained more than the limit value of 0.9 pu during the operation.

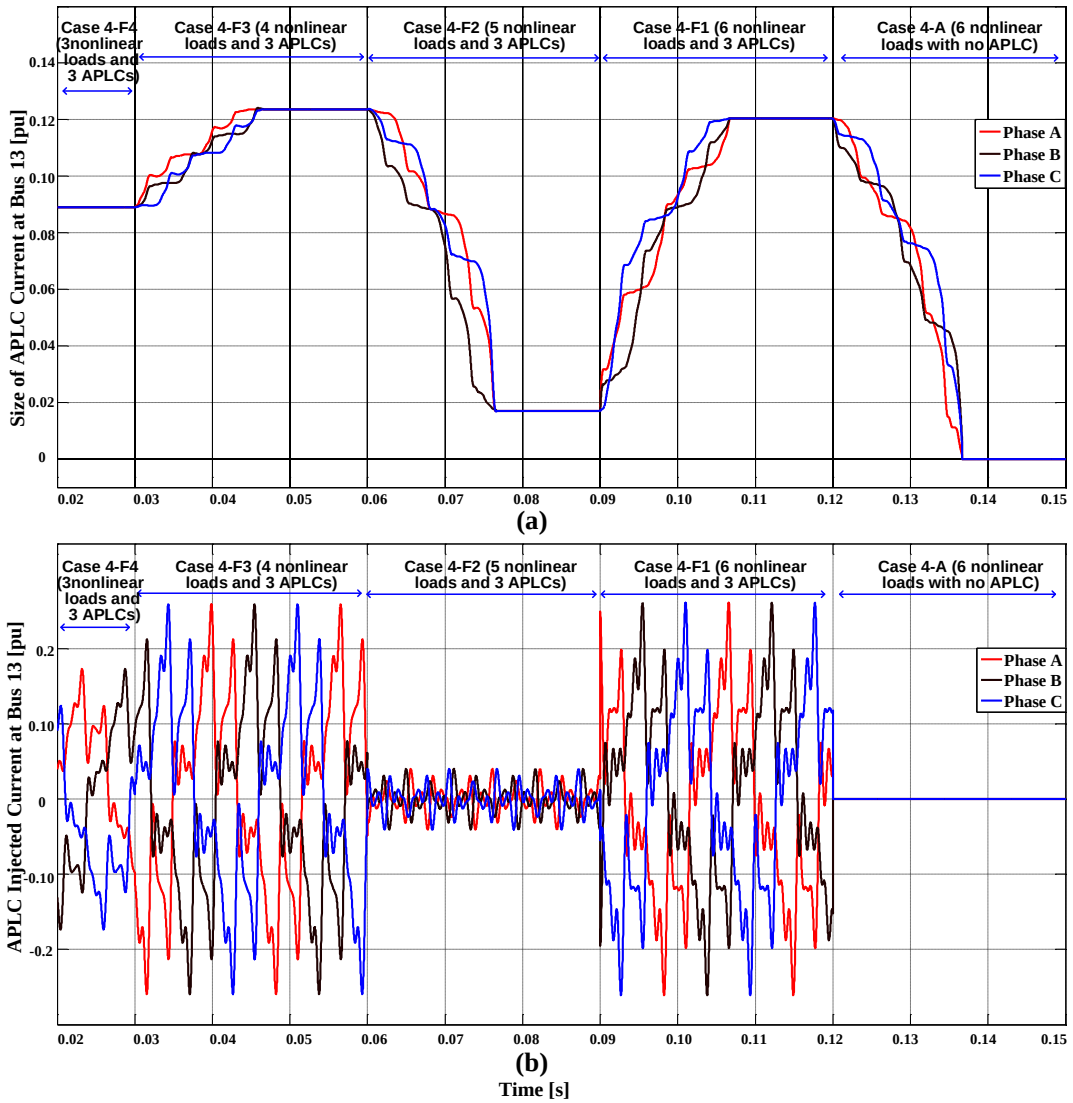


Figure 4.13: Optimal online operation of the 15-bus network of Fig. 4.2 for Cases 4-F4 to 4-F1; (a) Magnitude of APLC injected currents at bus 13, (b) The APLC injected currents waveform at bus 13

Fig. 4.13a shows the magnitude size of three-phase APLC injected current at bus 13 while Fig. 4.13b represents the three-phase APLC current waveforms at bus 13. The

magnitude of APLC current at bus 13 is 0.089 pu, 0.124 pu, 0.017 pu, 0.121 pu and zero for cases 4-F4, 4-F3, 4F2, 4F1 and 4-A, respectively.

Simulations are initially started with three nonlinear loads (at buses 5, 7 and 13) with three APLCs at buses 3, 6 and 13 (see Fig. 4.9) followed by four switching actions: i) at *t*=0.03sec, nonlinear loads at buses 5 and 7 are switched off and nonlinear loads at bus 8, 10 and 15 are switched on, ii) at *t*=0.06sec, nonlinear loads at buses 5 and 7 are switched back in operation and nonlinear load at bus 13 is switched off while nonlinear loads at buses 8, 10 and 15 are still in operation, iii) at *t*=0.09sec, the only nonlinear load at bus 13 which was switched off is switch back again and all nonlinear loads are in operation, and iv) at *t*=0.12sec, all APLCs are switched off while all nonlinear loads are still in operation.

Note that:

- The transient network conditions are due to the switching actions and changes in the number of nonlinear loads.
- Without APLCs in operation (t>0.12sec), the THDv and $V_{\mathbf{Fund}}$ of all buses are above the recommended value of 5% and below 0.9 pu, respectively, while during the operation of APLCs, the steady-state values of THDv at all buses for all cases are less than 5% and $V_{\mathbf{Fund}}$ at all buses are more than 0.9 pu.
- At t=0.06sec (Case 4-F2), just nonlinear load at bus 13 is switched off. Therefore as confirmed by Table 4.13 and Figs. 13a and 13b, the injected current of APLC at bus 13 is reduced.

CHAPTER 5: IMPACTS OF HARMONIC COUPLINGS ON OPTIMAL SITING, SIZING AND ONLINE CONTROL OF MULTIPLE APLCs

In the literature, the effects of harmonic couplings are neglected in the optimal design and operation of APLCs since they are commonly modeled as decoupled harmonic current sources injecting harmonic currents at PCCs.

5.1 Nonlinear Modeling and Control of APLCs

To properly include the impacts of harmonic couplings, a detailed nonlinear model is used for the APLCs and their performances are considered under different conditions. The APLC inverters are designed with the five level neutral-point clamped (FL-NPC) configuration (section 3.2.4, Eqs. 3.14-3.19).

This chapter implements a PSO-based algorithm for optimal siting and sizing of multiple APLCs where the impacts of harmonic couplings are considered by using nonlinear models for APLCs and nonlinear loads in Matlab/Simulink. The size of an APLC is calculated based on:

$$I_{k,APLC\,size} = \sqrt{\sum_{h=2}^{H} \left| I_{k,APLC}^{h} \right|^2}, \quad k = 1,...,K, \;\; h = 2,...,H \tag{5.1}$$

where k and h are the bus number and the harmonic order while K and H represent their maximum values, respectively.

The objective function for optimal siting and sizing of APLCs is to minimize the total cost associated with their sizes and the overall network THDv:

$$min\ Cost = C_{size} I_{APLCs} + C_{THD} THD_V = C_{size} \sum_{k=1}^{K} I_{k,APLC} + C_{THD} \sum_{k=1}^{K} \left(\sqrt{\sum_{h=2}^{H} \left| V_k^h \right|^2} \Big/ \left| V_k^1 \right| \right) \quad (5.2)$$

where C_{size} and C_{THD} are the cost weighting factors for APLC size and network THDv while V_k^1 and V_k^h represent the fundamental and harmonic voltages at bus *k*, respectively.

The selected constraints associated with Eq. 5.2 are:

- Upper limits for the network THDv and the individual voltage harmonics of each bus according to Eqs. 4.4 and 4.5.

- An upper limit for the size of each APLC:

$$I_{m,APLC} \le I_{max} \quad for \ \ m = 1,\ldots,M \in MC \quad (5.3)$$

  where I_{max} is the maximum APLC size selected/suggested by the utility whereas *M* and *MC* are the number and the set of candidate/feasible buses for APLC placement suggested by the utility, respectively. As will be discussed in Section 5.3.3 (Table 5.5), I_{max} can be selected to reduce the overall APLC investment and insulation costs (e.g., larger values will result in fewer but bigger APLC units).

A PSO algorithm is used to optimally allocate and size the APLCs. The flowchart of the first PSO algorithm for siting and sizing of APLCs is shown in Fig. 5.1a. The idea is to:

1) Temporarily install APLC units at all candidate buses $m \in MC$.
2) Perform the PSO optimization according to Eqs. 4.4-4.5 and 5.2-5.3 to find the optimal APLC locations and sizes.
3) Only select APLCs with sizes greater than a desired lower limit I_{min} value.

The first PSO algorithm of Fig. 5.1a is performed for the worst operating condition (maximum linear and nonlinear loadings):

- The input parameters of the first PSO algorithm are fundamental and harmonic voltages (V_k^1 and V_k^h) of each bus, cost weighting factors for APLC size and network THDv ($C_{size} = 0.5$ and $C_{THD} = 0.5$), upper limits for network THDv and individual bus voltage harmonics (0.05 and 0.03 [37-38]), the per unit minimum and maximum APLC sizes (I_{min}=0.01pu and I_{max}=0.07pu [47]), and the utility suggested set of candidate/feasible buses for the APLC placements *MC* (here all buses except the swing bus).
- The output parameters of the first PSO algorithm are the optimal APLC locations $n \in MC_{optimal} \in MC$ and sizes $I_{n,optimal}$ that are among the candidate buses and within the allowable limits of Eq. 5.3.

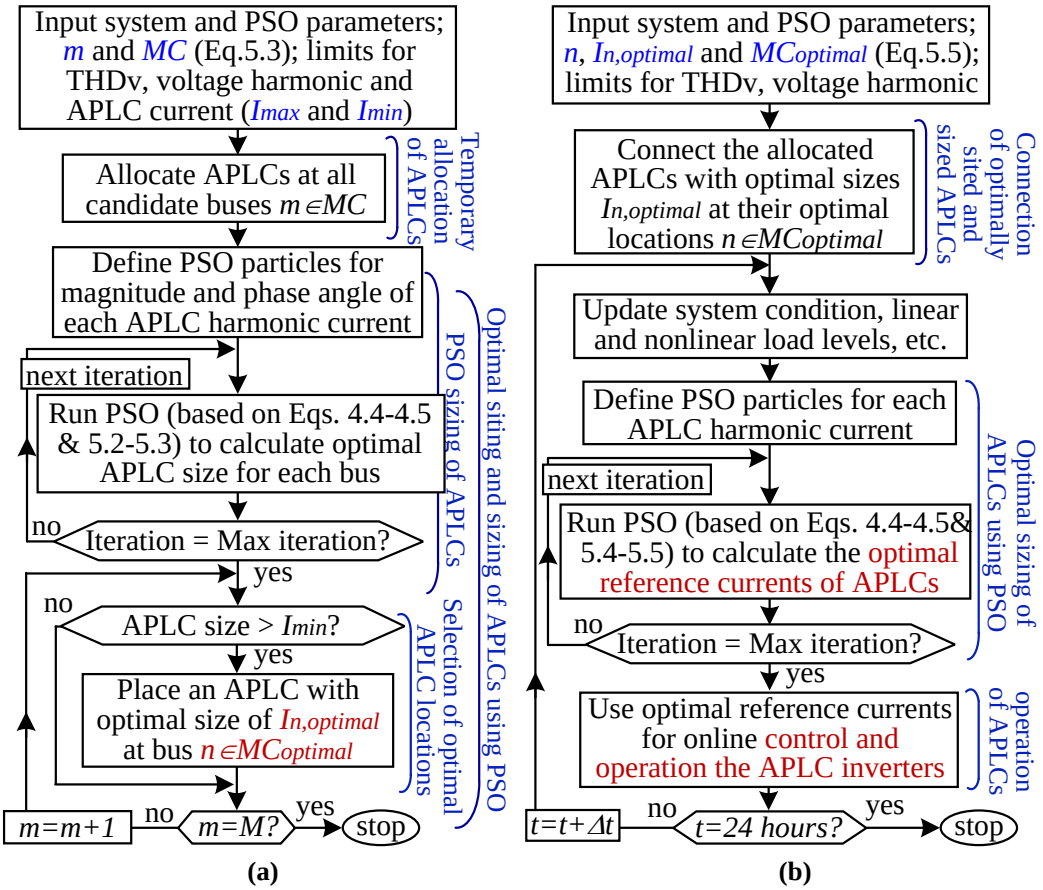


Figure 5.1: Flowchart of the proposed PSO algorithms with considering harmonic couplings; (a) optimal siting and sizing of multiple APLCs based on Eqs. 4.4-4.5 and 5.2-5.3, (b) optimal online control of the installed APLCs based on Eqs. 5.1, 4.4-4.5 and 5.4-5.5

5.2 Optimal Online Operation of APLCs Considering Harmonic Couplings

The second PSO algorithm (Fig. 5.1b) for online control of the n allocated APLCs ($I_{n,optimal};\ n \in MC_{optimal}$) is based on the online bus data information received from the smart meters through the SG communication infrastructure. The problem formulation is similar to Eqs. 4.4-4.5 and 5.2-5.3 with the following differences:

- APLCs are only installed at optimal locations ($MC_{optimal}$) with optimal sizes ($I_{n,optimal}$) as determined by the first PSO algorithm of Fig. 5.1a.
- Network status and optimization of the objective function (Eq. 5.4) are updated at time steps of Δt for the period of 24 hours:

$$min\ THD_V(t) = \sum_{k=1}^{K}\left(\sqrt{\sum_{h=2}^{H}\left|V_k^h(t)\right|^2}\Big/\left|V_k^1(t)\right|\right)\ \ for = \Delta t, 2\Delta t,... \tag{5.4}$$

- The bus numbers and limits of Eq. 5.3 are modified as follows:

$$I_{n,APLC} \le I_{n,optimal} \quad for \quad n \in MC_{optimal} \tag{5.5}$$

where $I_{n,optimal}$ and $MC_{optimal}$ are the optimal sizes and locations of APLCs as determined by the first PSO algorithm (Fig. 5.1a).

The flowchart of the second PSO algorithm for optimal operation/control of the allocated APLCs is shown in Fig. 5.1b:

- The input parameters of the second PSO algorithm are the same as those for the first PSO algorithm (Fig. 5.1a) with the exceptions of: i) the bus fundamental and harmonic voltages (V_k^1 and V_k^h) are transmitted online by the smart meters and updated at each time step Δt, ii) the maximum APLC sizes are the ratings of the selected APLCs ($I_{n,max} = I_{n,optimal}$), iii) the candidate buses are $MC_{optimal}$.
- The output parameters of the second PSO algorithm are the optimal APLC

reference currents at time steps of Δt for the period of 24 hours such that the overall network THDv and the individual bus voltage harmonics are within the limits of IEEE-519 standard [37-38].

5.3 Simulations for Optimal Siting/Sizing of APLCs with Considering Harmonic Couplings

The simulated network in this chapter is the same as chapter 4 (the 15-bus, 60Hz radial network, Fig 4.2). However, the nonlinear loads are the actual Matlab/Simulink model including three-phase full bridge rectifiers with resistive loads (Table 5.1) connected to buses 5, 7, 8, 10, 13, and 15. The optimal siting and sizing simulations are performed for the worse scenario with maximum linear and non-linear loading conditions.

Table 5.1: Current harmonic injection of the nonlinear loads (in percentage of the fundamental component) in the network of Fig.4.2

Harmonic Order				
5	**7**	**11**	**13**	**17**
The Exact Nonlinear Model with Harmonic Couplings*				
Exact Calculation	Exact Calculation	Exact Calculation	Exact Calculation	Exact Calculation
The exact nonlinear load models and their harmonic injections are adopted from the Matlab/Simulink library. Therefore, the injected current harmonics (magnitudes and phase angles) depend on the nonlinear load characteristics, inherent couplings among harmonics, (non)sinusoidal terminal voltage, and system operating conditions.				
The Approximate Decoupled Model without Harmonic Couplings**				
22.60	**11.34**	**9.02**	**6.49**	**5.63**
Each nonlinear load is modeled with decupled harmonic current sources injecting harmonic currents that are equal (in magnitude and phase angle) to the current distortions of the exact model with rated sinusoidal voltage excitation. Therefore, the injected current harmonics are fixed and independent of system operating conditions.				

***) Exact nonlinear model is adopted from Matlab/Simulink library.**
****) Conventional modeling approach adopted in most APLC related publications [37-48].**

In this chapter, six study cases (Table 5.2) are simulated and the results are presented in Tables 5.3-5.7. In each case except Case 3, simulations are performed and compared with and without harmonic couplings.

Table 5.2: Simulated case studies for the distorted 15-bus network of Fig.4.2 with considering harmonic couplings

Case	System Description	Approach	Results
5-A	System operation without APLCs	-	Table 5.3
5-B	Optimal APLC siting/sizing not considering *Imax* (Eq. 5.3)	First PSO of Fig. 5.1a	Table 5.4
5-C	Impact of *Imax* (Eq. 5.3) on the APLC siting/sizing solution	First PSO of Fig. 5.1a	Table 5.5
5-D	Optimal APLC siting/sizing with *Imax*=0.07pu (Eq. 5.3).	First PSO of Fig. 5.1a	Table 5.6
5-E	System operation with four optimally located/sized APLCs of Case 5-D	Second PSO of Fig. 5.1b	Table 5.7
5-F	Online operation/control of APLCs under different operating conditions	Second PSO of Fig. 5.1b	Fig. 5.6

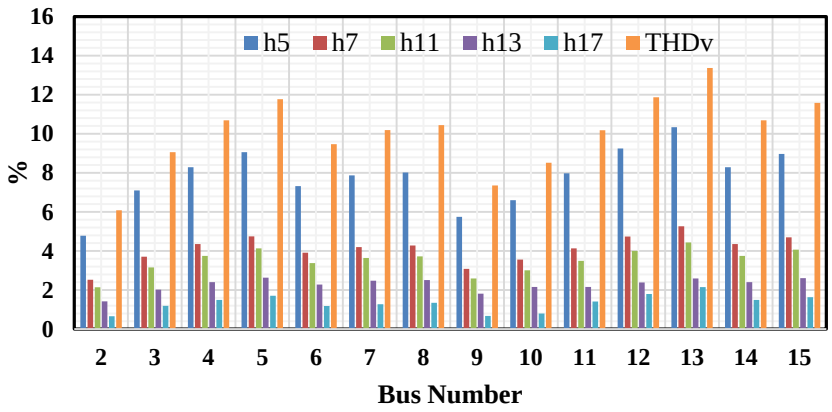
5.3.1 Case 5-A: System Operation without APLCs

This case illustrates the worse operating condition of the network with maximum loadings of all linear and nonlinear loads. Simulation results with and without harmonic couplings (Cases 5-A1 and 5-A2) are presented in Table 5.3 and Fig. 5.2 showing individual voltage harmonics (columns 2-6 and 8-12) and THDv of all buses (columns 7 and 13). Clearly, the entire network is highly distorted, the THDv of all buses are higher than the permitted limit of 5% and the voltage harmonics of most buses are above the acceptable level of 3%. Bus 13 is the worst distorted point of the network due to its remote location from bus 1 (the swing bus). Note that simulation results of Case 5-A2 are very different from the accurate results of Case 5-A1; therefore, disregarding harmonic couplings as adopted in most APLC related publications [40-51] may result in significant errors. For example, the worst bus THDv (Table 5.3, bus 13) and the network THDv (last row) are increased from 13.37% and 10.09% (Case 5-A1) to 20.99% and 15.77% (Case 5-A2) indicating errors of 56% and 57%, respectively (Fig 5.2c).

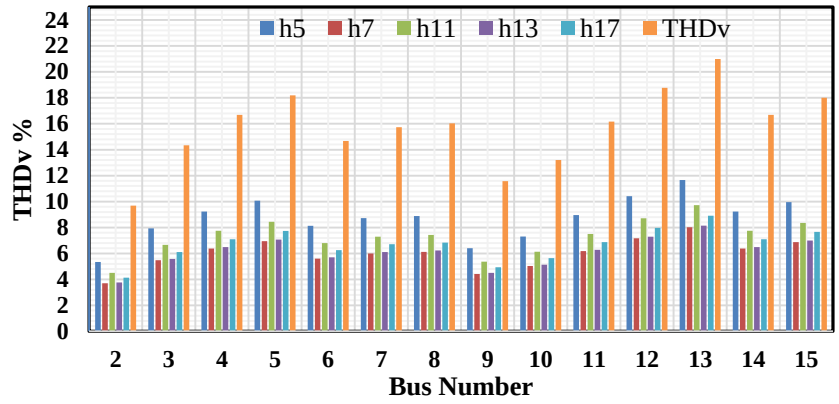
Table 5.3: Case 5-A; Operation of the network in Fig.4.2 without any APLCs

Bus	Case 5-A1: Considering Harmonic Couplings (Table 2, rows 3-5)						Case 5-A2: Not Considering Harmonic Couplings (Table 2, rows 6-8)					
	Harmonic Voltage Distortion (%)					THDv (%)	Harmonic Voltage Distortion (%)					THDv (%)
	5	7	11	13	17		5	7	11	13	17	
2	4.78	2.53	2.14	1.42	0.66	6.08	5.35	3.70	4.50	3.77	4.13	9.69
3	7.10	3.71	3.16	2.02	1.19	9.06	7.94	5.48	6.66	5.58	6.11	14.34
4	8.29	4.35	3.75	2.40	1.49	10.69	9.23	6.38	7.75	6.49	7.10	16.69
5	9.06	4.75	4.13	2.63	1.71	11.77	10.07	6.95	8.44	7.07	7.74	18.19
6	7.32	3.91	3.38	2.28	1.18	9.47	8.13	5.60	6.80	5.70	6.26	14.67
7	7.87	4.20	3.64	2.48	1.27	10.19	8.72	6.00	7.30	6.11	6.71	15.74
8	8.02	4.28	3.72	2.51	1.35	10.44	8.88	6.12	7.43	6.23	6.84	16.03
9	5.75	3.08	2.59	1.81	0.67	7.35	6.40	4.42	5.37	4.50	4.94	11.58
10	6.60	3.56	3.01	2.16	0.80	8.52	7.31	5.04	6.13	5.14	5.64	13.21
11	7.98	4.13	3.49	2.16	1.41	10.18	8.96	6.18	7.50	6.28	6.87	16.17
12	9.25	4.74	4.00	2.39	1.80	11.87	10.42	7.17	8.71	7.29	7.97	18.77
13	10.34	5.26	4.44	2.59	2.15	13.37	11.66	8.02	9.73	8.15	8.91	20.99
14	8.29	4.35	3.75	2.40	1.49	10.69	9.23	6.38	7.75	6.49	7.10	16.69
15	8.97	4.70	4.07	2.61	1.63	11.58	9.96	6.88	8.35	7.00	7.66	18.00
Avg.	7.83	4.11	3.52	2.28	1.34	10.09*	8.73	6.02	7.32	6.13	6.71	15.77*

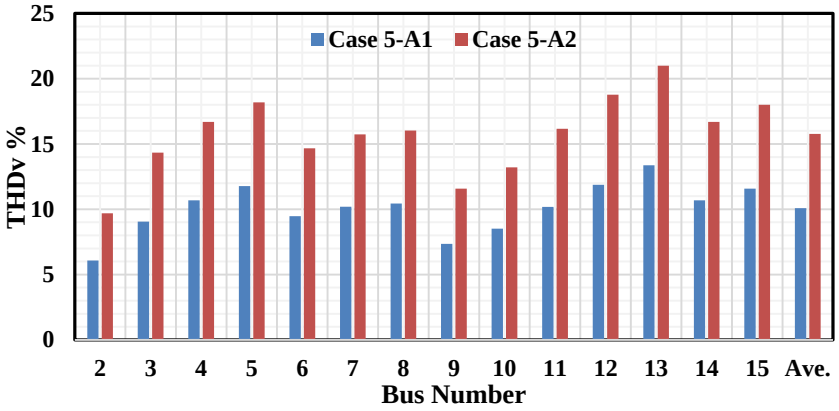
***) Network Average THDv.**



(a)



(b)



(c)

Figure 5.2: Simulation results for Case 5-A; (a) Case 5-A1, (b) Case 5-A2, (c) comparing THDv of all buses for Cases 5-A1and 5-A2

5.3.2 Case 5-B: Optimal Siting and Sizing of Multiple APLCs without Considering the Maximum APLC Size

The PSO algorithm of Fig. 5.1a is used (without considering I_{max} in Eq. 5.3) to find the optimal locations and sizes of the APLCs for the 15-bus network of Fig. 4.2. Simulation results are summarized in Table 5.4 for Cases 5-B1 and 5-B2 in columns 2-8 and 9-15, respectively and Fig 5.3. Both cases use the first PSO algorithm of Fig. 5.1a. However, decoupled harmonic current sources are used for the nonlinear load modeling in Case 5-B2.

Table 5.4: Case 5-B; Optimal siting and sizing of multiple APLCs (the first PSO algorithm of Fig. 5.1a and not considering a maximum APLC size)

Bus	Case 5-B1: Considering Harmonic Couplings (Table 5.1, rows 3-5)							Case 5-B2: Not Considering Harmonic Couplings (Table 5.1, rows 6-8)						
	Harmonic Voltage Distortion (%)					THDv (%)	Allocated I_{APLC} (pu)	Harmonic Voltage Distortion (%)					THDv (%)	Allocated I_{APLC} (pu)
	5	7	11	13	17			5	7	11	13	17		
2	0.29	0.66	0.70	0.61	0.46	2.13	0	0.67	0.52	1.03	0.46	0.82	1.64	0
3	1.22	1.74	1.71	1.79	0.89	4.15	0.205	0.09	0.15	0.87	0.14	0.25	0.94	0
4	0.09	1.23	0.82	1.11	0.40	3.45	0	1.16	0.99	1.90	0.79	1.09	2.79	0
5	0.78	1.09	0.37	0.72	0.71	3.73	0	1.93	1.52	2.55	1.34	1.70	4.15	0
6	1.70	1.52	1.66	1.02	0.73	4.12	0.040	1.52	1.01	1.76	1.08	2.11	3.47	0.062
7	2.21	1.83	1.83	1.14	0.86	4.71	0	2.07	1.39	2.22	1.47	2.56	4.46	0
8	2.36	1.92	1.94	1.23	0.93	5.00	0	2.22	1.49	2.35	1.58	2.68	4.73	0
9	1.24	0.99	0.87	0.55	0.77	3.09	0	1.66	1.21	1.87	1.17	1.62	3.43	0
10	2.08	1.41	1.32	0.78	1.16	4.30	0	2.52	1.80	2.60	1.79	2.31	4.99	0
11	0.37	1.55	1.31	1.48	0.81	3.77	0	2.75	1.59	1.02	2.08	2.29	4.55	0.173
12	1.05	1.48	1.02	1.08	0.95	4.07	0	1.47	0.70	0.33	1.16	1.26	2.39	0
13	2.14	1.66	1.21	0.85	1.25	4.98	0	0.39	0.06	1.11	0.38	0.38	1.29	0
14	0.09	1.23	0.82	1.11	0.40	3.44	0	1.16	0.99	1.90	0.79	1.09	2.79	0
15	0.69	1.06	0.36	0.75	0.64	3.56	0	1.83	1.45	2.47	1.27	1.62	3.97	0
Avg.	1.16	1.38	1.14	1.01	0.78	3.89*	0.245**	1.53	1.06	1.71	1.11	1.56	3.26*	0.235**

***) Network Average THDv**
****) Total size of allocated APLCs**

Note that the accurate solution of Case 5-B1 that includes harmonic couplings requires two APLCs at buses 3 and 6 (Table 5.4: column 8, rows 5 and 8) with ratings of 0.205pu and 0.040pu, respectively. However, the approximate modeling of Case 5-B2 indicates different locations (buses 6 and 11) and sizes (0.062pu and 0.173pu) of APLCs (Table 5.4: last column, rows 8 and 13).

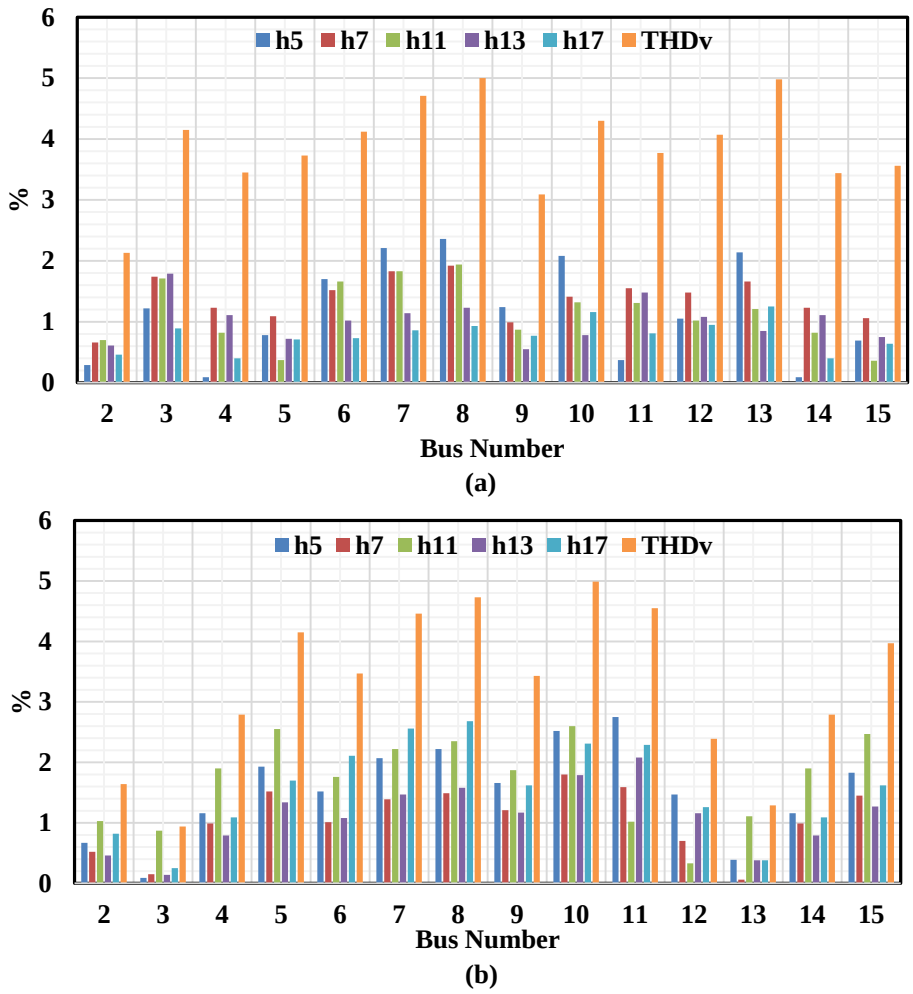


Figure 5.3: Simulation results for Case 5-B; (a) Case 5-B1, (b) Case 5-B2

5.3.3 Case 5-C: Impacts of Maximum APLC Size (I_{max}) on Optimal Siting and Sizing Solution

To investigate impacts of the selected maximum APLC size on the optimal siting/sizing solution of the first PSO algorithm of Fig. 5.1a, simulations are repeated for I_{max} = 0.05pu, 0.07pu, 0.10pu, 0.15pu, 0.20pu and 1.0pu. The results are summarized and compared in Table 5.5. Note that:

- Larger limits of I_{max} result in better optimal solutions with smaller overall costs (Table 5.5, column 4) and less network THDv distortions (Table 5.5, column 2);

however, the total size of the APLCs increases (Table 5.5, column 3). Furthermore, fewer (but larger) APLC units are allocated that may also reduce the APLC investment and maintenance costs for the electric utilities.

- On the other hand, smaller limits of I_{max} reduce the total APLC size (Table 5.5, column 3); however, the THDv and overall cost (Table 5.5, column 2 and 4) as well as the number of APLC units will increase. Furthermore, it is unlikely to install more than a few APLCs in practical applications.
- From technical and practical points of view, it is better to select larger limits for I_{max}. This will result in lower costs with better voltage qualities, fewer APLC units and less maintenance and investment costs. A possible limitation may occur on the availability of large APLC units.
- In this chapter, the compromised value of I_{max}=0.07pu [47] is selected and used.

Table 5.5: Case 5-C; Impact of maximum APLC size on the optimal siting and sizing solution

I_{max} (Eq. 5.3) [pu]	Solutions of the first PSO Algorithm (Fig. 5.1a) including harmonic couplings (Table 5.1, rows 3-5)								
	Cost Function (Eq. 5.2)			Optimal APLC Locations/Sizes					
	THD_{Net}	I_{APLC}	min Cost	APLC 1	APLC 2	APLC 3	APLC 4	APLC 5	APLC 6
1.00	3.88	0.245	2.062	Bus 3/ 0.205pu	Bus 6 /0.040pu				
0.30	3.88	0.245	2.062	Bus 3 /0.205pu	Bus 6 /0.040pu				
0.20	3.86	0.266	2.063	Bus 3 /0.200pu	Bus 6 /0.066pu				
0.15	4.07	0.234	2.152	Bus 3 /0.140pu	Bus 6 /0.054pu	Bus 12 /0.040pu			
0.10	4.10	0.214	2.157	Bus 3 /0.100pu	Bus 6 /0.060pu	Bus 12 /0.054pu			
0.07*	4.16	0.212	2.186	Bus 4 /0.069pu	Bus 6 /0.053pu	Bus 9 /0.037pu	Bus 12 /0.053pu		
0.05	4.18	0.204	2.192	Bus 3 /0.043pu	Bus 5 /0.048pu	Bus 8 /0.050pu	Bus 9 /0.031pu	Bus 12 /0.032pu	

***) Selected for the remaining simulations and analyses of this paper**

5.3.4 Case 5-D: Optimal Siting and Sizing of Multiple APLCs with I_{max} = 0.07pu

As deliberated in the previous case study, utilities may require a maximum limit for the individual APLC rating/size due to practical and economic considerations. In this section, simulations of Case 5-B are repeated assuming I_{max} = 0.07pu [47] and the results are summarized in Table 5.6 and Fig. 5.4. Note that the maximum size of 0.07 pu results in allocation of many CPDs while considering unit sizes larger than 0.07 pu may not be practical.

Table 5.6: Case 5-D; Optimal siting and sizing of multiple APLCs considering a maximum APLC current of 0.07pu (Table 5.5, row 9)

Bus	Case 5-D1: Considering Harmonic Couplings (Table 5.1, rows 3-5)							Case 5-D: Not Considering Harmonic Couplings (Table 5.1, rows 6-8)						
	Harmonic Voltage Distortion (%)					THDv (%)	Allocated I_{APLC} (pu)	Harmonic Voltage Distortion (%)					THDv (%)	Allocated I_{APLC} (pu)
	5	7	11	13	17			5	7	11	13	17		
2	1.10	0.60	0.80	0.58	0.70	2.43	0	1.36	1.35	0.07	0.14	0.25	1.92	0
3	1.28	1.14	1.28	0.91	1.00	3.50	0	1.42	1.53	0.44	0.46	0.41	2.19	0.070
4	1.58	1.52	1.45	1.15	1.17	4.21	0.069	2.65	2.39	0.63	0.45	0.70	3.69	0
5	2.27	1.75	1.63	1.42	1.29	4.99	0	3.00	2.93	1.27	0.99	1.30	4.94	0
6	2.21	1.08	1.15	0.97	1.19	4.13	0.053	2.06	2.21	0.22	0.31	0.39	3.00	0.070
7	2.74	1.37	1.13	0.98	1.31	4.66	0	2.61	2.59	0.25	0.69	0.80	3.78	0
8	2.89	1.46	1.22	1.07	1.38	4.95	0	2.77	2.70	0.37	0.79	0.92	4.01	0
9	1.40	0.50	0.91	0.57	0.83	2.98	0.037	2.37	2.04	0.90	0.85	1.03	3.50	0
10	2.15	1.03	0.92	0.82	1.08	3.99	0	3.00	2.64	1.62	1.46	1.72	5.00	0
11	1.04	1.30	1.61	1.06	1.12	3.85	0	1.02	1.21	1.19	1.06	0.81	2.36	0.070
12	0.78	1.56	2.15	1.38	1.33	4.54	0.053	2.34	2.12	0.11	0.15	0.35	3.16	0
13	1.60	2.07	1.94	1.33	1.16	5.00	0	3.00	2.90	0.86	0.67	1.19	4.79	0
14	1.58	1.52	1.45	1.15	1.17	4.21	0	2.65	2.39	0.63	0.45	0.70	3.69	0
15	2.17	1.68	1.54	1.36	1.23	4.75	0	3.00	2.86	1.19	0.92	1.22	4.78	0
Avg.	1.77	1.33	1.37	1.05	1.14	4.16*	0.212**	2.40	2.28	0.70	0.67	0.84	3.63*	0.204**

***) Network Average THDv.**
****) Total size of the optimally allocated APLCs.**

Note that the precise simulations of Case 5-D1 that include harmonic couplings requires four APLCs at buses 4, 6, 9 and 12 with the optimal sizes of 0.069pu, 0.053pu, 0.037pu and 0.053pu, respectively; while the results of Case 5-D2 without harmonic couplings indicate only three APLCs at buses 3, 6 and 11 with equal sizes of 0.070pu. Comparing results of Cases 5-B and 5-D, an upper limit for APLC sizes will result in more APLC units.

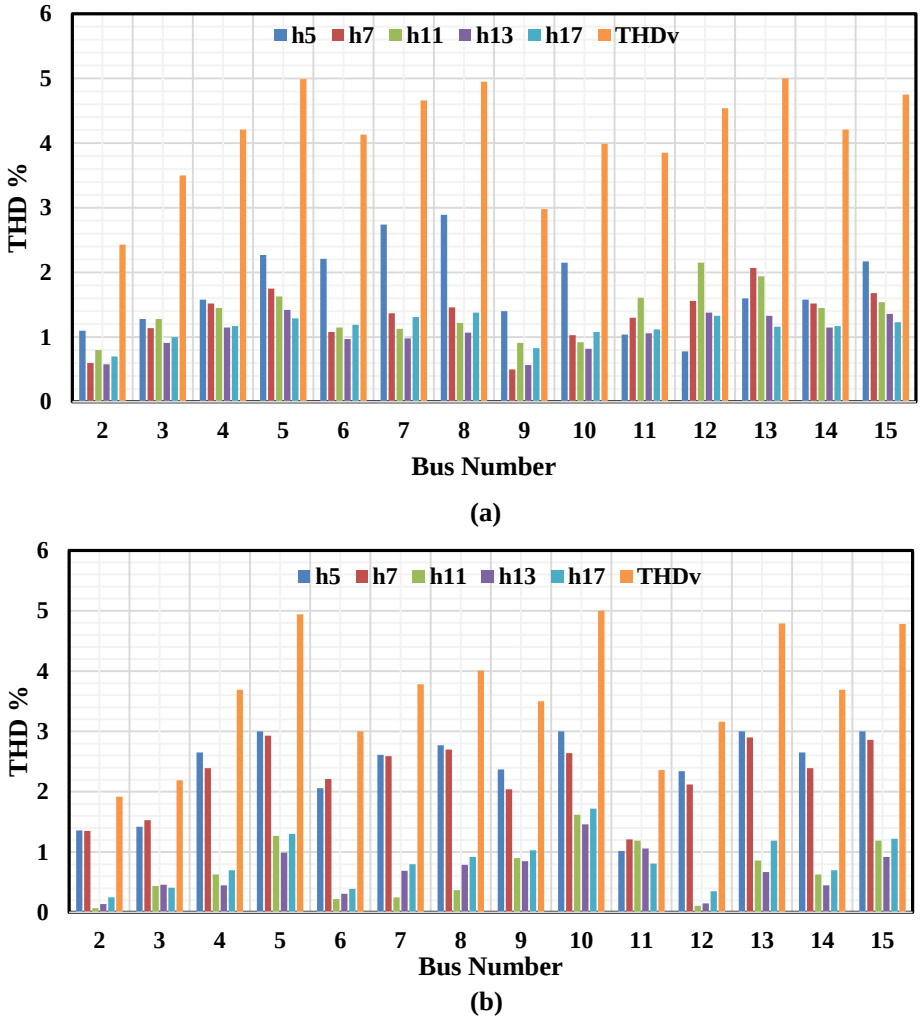


Figure 5.4: Simulation results for Case 5-D; (a) Case 5-D1, (b) Case 5-D2

5.4. Simulations for Optimal Operation of the Allocated APLCs

For optimal online operation of the network with APLCs (Figs. 4.2 and 5.5), the

following steps are executed:

- Step 1- The first PSO algorithm of Fig. 5.1a is implemented to find the optimal locations and sizes of the required APLCs ($I_{n,optimal};\ n \in MC_{optimal}$). This is done in Case 5-D for I_{max}=0.07pu with four APLCs allocated at buses 4, 6, 9 and 12 with optimal sizes of 0.069pu, 0.053pu, 0.037pu and 0.053pu, respectively (Table 5.6, column 8).
- Step 2- At each time step (Δt), the SG control center receives grid information recorded by the smart meters through the SG communication network, calculates the optimal APLC reference currents by running the second PSO algorithm of Fig. 5.1b, and sends them to the APLCs.
- Step 3- The APLC inverters use the reference signals of Step 2 to generate and inject optimal compensation currents. The applied switching frequency in this section is 5 kHz.

5.4.1. Case 5-E: System Operation with the Four Optimal APLC Locations and Sizes of Cases 5-D1 and 5-D2

This case study is intended to emulate the operation of real distorted systems with nonlinear loads being frequently activated and deactivated by the consumers. The 15-bus distorted network including the six nonlinear loads (Fig. 4.2) and the four allocated/sized APLCs of Cases 5-D1 and 5-D2 (Table 5.6, columns 8 and 15) is simulated and the APLCs are controlled using the second PSO algorithm of Fig. 5.1b. The simulation results are illustrated in Table 5.7. According to the detailed simulation results of Table 5.7:

Table 5.7: Case 5-E; System operation with the four optimally located/sized APLCs of Case 5-D1 and 5-D2 (Table 5.6, columns 8 and 15) considering a different number of nonlinear loads. Purple cells indicate unacceptable THDv levels caused by the inaccurate siting/sizing of Case 5-D2 due to the ignorance of harmonic couplings

		Bus Number														Ave./
		2	3	4	5	6	7	8	9	10	11	12	13	14	15	Total
Case 5-E1: The 15-bus distorted system (Fig. 4.2) with six nonlinear loads at buses 5, 7, 8, 10, 13 and 15																
THDv without APLCs		6.08	9.06	10.69	11.77	9.47	10.19	10.44	7.35	8.52	10.18	11.87	13.37	10.69	11.58	10.09
Using APLC sizes & locations of Case 5-D1	Injected APLC currents	-	-	0.069		0.053	-	-	0.037	-	-	0.057	-	-	-	0.216
	THDv with APLCs	2.42	3.44	4.22	4.99	4.17	4.70	4.98	3.28	4.21	3.79	4.67	5.00	4.22	4.75	4.20
Using APLC sizes & locations of Case 5-D2*	Injected APLC currents	-	0.067	-	-	0.068	-	-	-	-	0.069	-	-	-	-	0.204
	THDv with APLCs	4.90	7.97	7.95	8.25	7.03	6.94	7.11	5.68	6.54	9.62	9.15	9.03	7.95	8.05	7.58
Case 5-E2: The 15-bus distorted system (Fig. 4.2) with five nonlinear loads at buses 5, 7, 8, 10 and 15																
THDv without APLCs		5.57	7.76	9.45	10.57	9.08	9.82	10.08	6.90	8.12	7.74	7.74	7.74	9.45	10.37	8.60
Using APLC sizes & locations of Case 5-D1	APLC locations/sizes			0.061		0.054			0.039			0.018				0.172
	THDv with APLCs	2.35	3.08	3.93	4.87	4.13	4.70	4.99	3.41	4.42	3.10	3.76	3.75	3.92	4.63	3.93
Using APLC sizes & locations of Case 5-D2*	APLC locations/sizes	-	0.066	-	-	0.059	-	-	-	-	0.036	-	-	-	-	0.161
	THDv with APLCs	4.77	7.32	7.36	7.71	7.30	7.32	7.53	5.64	6.55	8.42	8.42	8.42	7.36	7.51	7.26
Case 5-E3: The 15-bus distorted system (Fig. 4.2) with four nonlinear loads at buses 8, 10, 13 and 15																
THDv without APLCs		4.64	6.73	7.64	7.64	6.60	6.60	7.62	6.13	7.45	7.88	9.67	11.29	7.64	8.62	7.58
Using APLC sizes & locations of Case 5-D1	APLC locations/sizes	-	-	0.030	-	0.015	-	-	0.026	-	-	0.056	-	-	-	0.127
	THDv with APLCs	2.48	3.25	3.84	3.84	3.97	3.97	5.00	3.62	4.79	3.55	4.46	4.98	3.83	4.61	4.01
Using APLC sizes & locations of Case 5-D2*	APLC locations/sizes	-	0.058	-	-	0.014	-	-	-	-	0.051	-	-	-	-	0.123
	THDv with APLCs	3.92	6.38	6.13	6.13	5.16	5.16	5.79	5.01	6.10	7.72	7.77	8.10	6.13	6.10	6.11
Case 5-E4: The 15-bus distorted system (Fig. 4.2) with three nonlinear loads at buses 5, 7 and 13																
THDv without APLCs		3.35	5.46	6.31	7.48	5.18	6.04	5.18	3.35	3.35	6.68	8.55	10.20	6.31	6.31	5.98
Using APLC sizes & locations of Case 5-D1	APLC locations/sizes	-	-	0.028	-	0	-	-	0	-	-	0.048	-	-	-	0.080
	THDv with APLCs	2.04	2.83	3.39	4.38	4.02	4.93	4.02	2.04	2.04	3.18	4.00	5.00	3.38	3.38	3.47
Using APLC sizes & locations of Case 5-D2*	APLC locations/sizes	-	0.041	-	-	0	-	-	-	-	0.057	-	-	-	-	0.098
	THDv with APLCs	2.66	4.63	4.61	4.88	4.05	4.79	4.05	2.66	2.66	6.00	6.20	6.70	4.61	4.61	4.51
Case 5-E5: The 15-bus distorted system (Fig. 4.2) with two nonlinear loads at buses 10 and 15																
THDv without APLCs		2.88	4.24	5.29	5.29	2.86	2.86	2.86	4.52	5.97	4.23	4.23	4.23	5.29	6.37	4.37
Using APLC sizes & locations of Case 5-D1	APLC locations/sizes	-	-	0.016	-	0	-	-	0.017	-	-	0	-	-	-	0.033
	THDv with APLCs	2.13	3.12	3.94	3.94	2.09	2.08	2.08	3.56	5.00	3.10	3.09	3.09	3.93	5.00	3.30
Using APLC sizes & locations of Case 5-D2*	APLC locations/sizes	-	0.042	-	-	0	-	-	-	-	0	-	-	-	-	0.042
	THDv with APLCs	2.43	3.59	4.14	4.14	2.41	2.41	2.41	3.96	5.35	3.58	3.58	3.58	4.14	4.87	3.62
Case 5-E6: The 15-bus distorted system (Fig. 4.2) with one nonlinear load at bus 5																
THDv without APLCs		1.44	2.78	3.79	5.15	1.43	1.43	1.43	1.44	1.44	2.77	2.76	2.76	3.79	3.79	2.59
Using APLC sizes & locations of Case 5-D1	APLC locations/sizes	-	-	0.004	-	0	-	-	0	-	-	0	-	-	-	0.004
	THDv with APLCs	1.36	2.65	3.65	4.98	1.34	1.34	1.34	1.36	1.36	2.62	2.61	2.61	3.64	3.64	2.46
Using APLC sizes & locations of Case 5-D2*	APLC locations/sizes	-	0.003	-	-	0	-	-	-	-	0	-	-	-	-	0.003
	THDv with APLCs	1.40	2.70	3.70	5.05	1.39	1.39	1.39	1.40	1.40	2.69	2.69	2.69	3.70	3.70	2.52

***) Not considering harmonic couplings.**

- The optimal APLC locations and sizes of Case 5-D2 without considering harmonic couplings are not accurate since they result in unacceptable percentages of THDv levels at many buses (Table 5.7, purple cells). This is particularly true with a large number of nonlinear loads such as Cases 5-E1 to 5-E3.
- As expected, the APLC compensation levels (APLC current injections) decrease at low penetrations of nonlinear loads (Cases 5-E4 to 5-E6). For example, for Case 5-E6 with only one nonlinear load connected at bus 5, the compensation currents of all APLCs are zero except the one connected at bus 4.

5.4.2. Case 5-F: Online Operation and Control of APLCs Considering Harmonic Couplings

The online optimal operation and control of the four allocated APLCs in Case 5-D1 (Table 5.6, columns 8 and 15) are performed using the second PSO algorithm of Fig. 1b with the consideration of harmonic couplings (Table 5.1, rows 3-5). The 15-bus network of Fig. 4.2 with the six nonlinear loads and the four allocated APLCs are accurately modeled in Matlab/Simulink (Fig. 5.5) and the number of nonlinear loads is gradually reduced from 6 to 3 units (Cases 5-E1 to 5-E3).

In Fig. 5.5, the nonlinear APLC modelings are based on the inverter design and control of Section 3.2.4 while for the nonlinear loads (three-phase full bridge rectifiers with resistive loads) exact model is adopted from the Matlab/Simulink library. Therefore, the harmonic couplings are properly incorporated in the network modeling, control and operation.

Figure 5.6a presents the three-phase APLC current waveforms at bus 13 while Fig. 5.6b shows the THDv of all buses. Fig. 5.6c demonstrates the zoomed waveform of

Fig. 5.6a from 0.065 to 0.07 second (less than half a cycle).

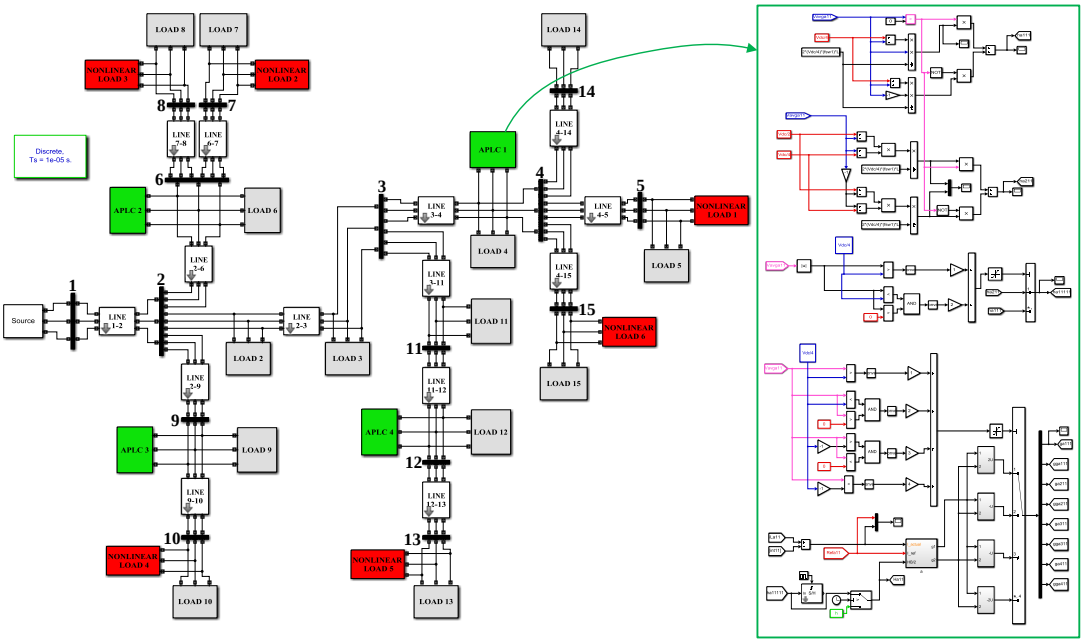


Figure 5.5: Simulink three-phase 15-bus distorted system [139] line diagram in Matlab/Simulink with six nonlinear loads (Tables 3.1 and 3.2) considering harmonic couplings

Simulations are initially started with all six nonlinear loads (at buses 5, 7, 8, 10, 13 and 15) activated without any APLCs followed by four switching actions: i) at t=0.03sec, the four APLCs at buses 4, 6, 9 and 12 are activated, ii) at t=0.06sec, the nonlinear load at bus 13 is switched off, iii) at t=0.09sec, the nonlinear load at bus 13 is back in operation but nonlinear loads at buses 5 and 7 are switched off, and iv) at t=0.12sec, the nonlinear loads at buses 5 and 7 are switched on again while the nonlinear loads at buses 8, 10 and 15 are not in operation. Note that in Fig. 5.6b:

- The transient network conditions are due to the switching actions and changes in the number of nonlinear loads.
- Prior to the activation of APLCs (at t=0.03sec), all bus THDv are above the recommended value of 5% while after the activation of APLCs, the steady-state values of THDv at all buses for all cases are less than 5%.

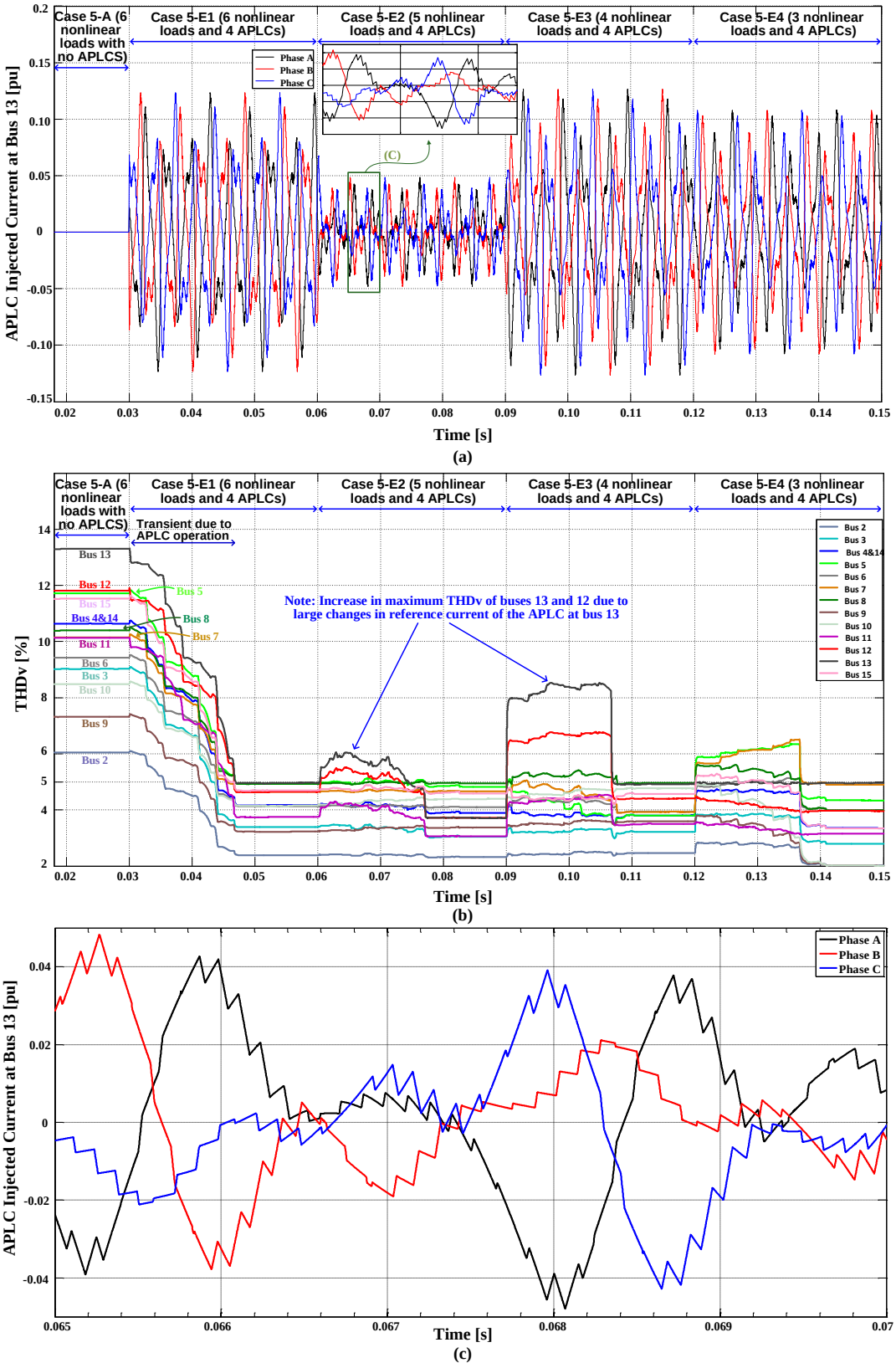


Figure 5.6: Optimal online operation of the 15-bus network of Fig. 4.2 (using the second PSO algorithm of Fig. 5.1b considering harmonic couplings (Table 5.1, rows 3-5)) for Cases 5-E1 to 5-E4 with four APLCs at buses 4, 6, 9 and 12; (a) The APLC injected currents at bus 13, (b) THDv of all buses, (c) zoomed waveform of Fig. 5.6a

- At *t*=0.06sec (Case 5-E2), the nonlinear load at bus 13 is switched off. Therefore, as confirmed by Table 5.7 and Fig. 5.5a, harmonic compensation current of APLC at bus 13 is reduced.
- Comparing THDv waveforms of Cases 5-E2 and 5-E3, the increase in maximum THDv values at buses 12 and 13 are due to the large compensation of the APLC unit at bus 13. Furthermore, these cases simulate different operating conditions with different numbers and locations of nonlinear loads.

CHAPTER 6: CONCLUSION

Detailed literature review on harmonic distortions and voltage instability problems of smart grids are discussed in this thesis. By reducing harmonic distortions and also controlling the reactive power of the entire network, maximum voltage regulation can be achieved. Therefore, FACTS and custom power devices are introduced to improve the power quality of networks.

StatCom as a shunt FACTS device is investigated and studied in Chapter 3. The ability of StatCom to compensate the reactive power of connected network and regulation of network voltage profile is simulated and examined. They have been verified to be an effective way to improve the voltage qualities considerably, which may be aggravated by increasing integration of large quantities of renewable powers. Moreover, optimal siting and sizing of StatComs are simulated and their capability of voltage regulation under balanced and unbalanced distribution network are demonstrated. In this case, a PSO-based algorithm is implemented and tested for optimal placement and sizing of StatComs in distorted unbalanced/balanced power systems that relies on the smart meter transmitted data allocated at each bus. The 15 bus test system with balanced and unbalanced linear and nonlinear loading conditions (Fig. 3.7) is simulated in Matlab/Simulink for reactive power compensation. Detailed simulation results are demonstrated by properly allocating and sizing of StatComs within the system, confirming that the $V_{\mathbf{Fund}}$ of the entire network can be improved and maintained within the standards.

Harmonic distortions are another concern of smart grids. APFs as a shunt connected devices are used to compensate the harmonic distortions of nonlinear loads. Despite extensively use of APFs on compensating harmonic distortions of nonlinear loads,

their limitation of compensating only harmonic currents of the nonlinear load at PCC (not the entire network), has motivated the researchers and utilities to develop the implementation of APLCs. Chapters 4 and 5 have investigated the effectiveness of APLCs on limitation of harmonic distortions of the entire network according to the power quality standards such as the IEEE 519-1992. APLC is an enhanced APF which can limit THDv and individual harmonic distortion of the entire network below 5% and 3%, respectively; recommended by most power quality standards. Most of the studies are based on compensating of either reactive power flow or harmonic distortions of the network. Therefore, Chapter 4 has investigated the performance of APLCs on compensation both reactive power flow (fundamental voltage) and voltage harmonic distortions of the entire network. It has proposed two PSO-based algorithms (Fig 4.1) for optimal siting and sizing and optimal online control of APLCs based on smart meter transmitted data. Detailed results of Chapter 4 show that how allocated APLCs can mitigate the voltage profile of all buses to be minimum 0.9 pu and limit the THDv and individual voltage harmonic distortion of the entire network to 5% and 3%, respectively (Tables 4.3, 4.11 and 4.12). It is also revealed that the weighting factors of the PSO objective function (Eq. 4.2) have significant impacts on APLC siting and sizing solutions (Table 4.4-4.10).

In the literature, the effects of harmonic couplings in the optimal design and operation of APLCs are neglected and consequently they are commonly modeled as decoupled harmonic current sources injecting harmonic currents at PCCs. Chapter 5 has investigated the impacts of harmonic couplings on optimal siting and sizing of APLCs. Two PSO-based algorithms for optimal siting and sizing and optimal online control of APLCs are introduced (Fig. 5.1). Harmonic couplings are included by accurate

network simulation in Matlab/Simulink with nonlinear models for the APLCs and nonlinear loads (Fig. 5.5). The optimization is based on the following main steps:

1) The first PSO algorithm (Fig. 5.1a based on Eq. 4.4-4.5 and 5.2-5.3) finds the optimal locations (buses) and sizes (ratings) of multiple APLCs for the worst case scenario with all linear and nonlinear loads being simultaneously activated at their maximum levels. The objective function is the minimization of costs associated with the network THDv and APLC sizes while the constraints are upper limits for individual bus THDv levels (5%) and bus voltage harmonics (3%) as well as the maximum APLC rating suggested by the electric utiliti (I_{max}=0.07pu). The input parameters for first PSO algorithm are the limits for the optimization constraints (Eqs. 4.4, 4.5 and 5.3) as well as the set of candidate buses for APLC placement ($m \in MC$) while the outputs are the optimal APLC locations $n \in MC_{optimal} \in MC$ and sizes $I_{n,optimal}$. Detailed simulations are performed and compared without and with the consideration of harmonic couplings (Tables 5.4, 5.6 and 5.7).
2) The second PSO algorithm (Fig. 5.1b; based on Eqs. 4.4-4.5 and 5.4-5.5) continuously calculates the optimal APLC inverter reference current signals for optimal online control of the allocated APLCs with time steps of Δt. Problem formulation and constraints are similar to the first PSO (Fig. 5.1a) with the exceptions that the online objective function (Eq. 5.4) only includes THDv minimization, MC is replaced with $MC_{optimal}$ and I_{max} is replaced with the optimal sizes (ratings) of the allocated APLCs $I_{n,optimal}$ (Eq. 5.5). Detailed simulations are performed and compared for various operating conditions emulating operation of real distorted systems with nonlinear loads being frequently activated and deactivated by the consumers (Table 5.7 and Fig. 5.6).

The main conclusions based on detailed simulations (Chapters 4 and 5) for a 15-bus network with six nonlinear loads (Figs. 4.2 and 5.5) are:

- Compensation of both fundamental voltage fluctuations and voltage harmonic distortions of the entire distorted SG network by optimal siting and sizing of advanced APLC units which include both StatCom and APF functions. This is done in Chapter 4 by implementing two particle swarm optimization (PSO) algorithms (Fig. 4.1) that rely on the transmitted online smart meter data including the bus voltage profiles.
- Compensation of voltage harmonic distortion of the entire distorted SG network by optimal siting and sizing of APLCs with and without considering harmonic couplings by implementing the proposed two PSO algorithms (Fig. 5.1 - Chapter 5).
- Weighting factors of the PSO objective function in Chapter 4 (Eq. 4.2) have significant impacts on APLC siting and sizing solutions (Table 4.4-4.10). Large values of W_{size} result in smaller total APLC size with most THDv values close to 5% while lager values of W_{THD} result in lower THDv values. Both options result in many APLC units that may not be a practical option. Therefore, the values of W_{size}=$W_{THD} = 0.5$ are selected (Table 4.4, last row).
- Harmonic couplings have great impacts on APLC siting and sizing solution as well as their online control and operation. Disregarding them will result in inaccurate APLC locations and sizes (Tables 5.3, 5.4 and 5.6) as well as imprecise online compensations of harmonic distortions (Table 5.7).
- The proposed three-step strategy of Section 5.4 for online control and operation of APLCs shows promising satisfactory dynamic and online performances under

various distorted operating conditions (Fig. 5.6b and Table 5.7, rows 5-6, 11-12, 17-18, 23-24, 29-30, 35-36 associated with APLC allocations of Case 5-D1).

- The maximum APLC size (I_{max}) suggested by the electric utilities (Eq. 5.3) will have an impact on the optimal siting and sizing solution of the first PSO algorithm (Table 5.5). From technical and practical points of view, it is better to select higher limits for I_{max}. This will result in lower over costs with better voltages qualities, fewer APLC units and less maintenance and investment costs.

6.1 6.1 Recommendations and Future Research Directions

The 15-bus test system has been used in this project to simulate the optimal siting and sizing of APLCs in order to improve the voltage profile of the system. PSO-based algorithm is applied to find the best locations and number of APLCs to satisfy the power quality standards such as the IEEE 519. The simulated network includes 14 linear and 6 nonlinear loads. However, there limited number of buses, linear and nonlinear loads without any renewable energy resources and microgrid formations. The future research can be directed towards optimal siting and sizing of APLCs of larger smart grids with nonlinear loads, solar and wind distributed generations considering micogrid connections.

Simulations are performed using Matlab/Simulnk that usually requires considerable computing time. This may not be a practical software option for large networks with many buses. The PSO program at each iteration runs the Simulink file. Accordingly, the required data will be transferred to PSO program to compute the best solution. For example, if the number of PSO iterations and population are equal to 100, each Simulink run takes about 30 seconds and the Simulink file is executed 10000 times,

then it will take about 84 hours to complete the simulations for one case study. This time also depends on the number of PSO particles. For example, to find the allocation of APLCs for Case 5-A, 168 particles are defined: (14 bus)x(12 harmonics magnitude and phase angles)=168 particles.

The number of APLCs depends on several factors including the PSO objective function and constraints as well as the designated maximum size of each APLC. As an example, in Case 5-B1, only 2 APLCs are selected at buses 3 and 6 while for Case 5-D1 which includes an extra constraint for maximum APLC size, 4 APLCs are allocated at buses 4, 6, 9 and 12. However, the size of each APLC is different in each Case.

In larger networks with many nonlinear loads, microgrid and renewable energy sources, the number of APLCs will be increased and their locations will be significantly affected by the network configuration. Therefore, the number and locations of APLCs should be designed based on the worst case scenario with all nonlinear loads, microgrids and renewable energy sources connected to the network.

The main purpose of utilizing the Matlab/Simulink in this thesis was to accurately model harmonic couplings and investigate their impacts on optimal APLC siting/sizing problem. This was done for a small 15-bus network using a personal computer with conventional microprocessor. For larger networks, it is recommended to use faster processor systems. Alternatively, Matlab coding and steady-state load flow calculations can used instead of the slow Simulink modelling if the impacts of harmonic couplings are not considered.

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