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A novel generalized concept for three phase cascaded multilevel inverter topologies

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***Abstract*— Many new cascaded multilevel inverter (MLI) topologies have recently been proposed and published in the literature. All proposed topologies demand significant amount of semiconductor components and input dc supplies, which is considered the main drawback for the implementation of three phase cascaded MLIs. This paper proposes a new generalized concept that could be employed within any existing cascaded MLI topology in order to reduce its size in terms of device count including semiconductor switches, diodes, and dc power supplies. The new generalized concept involves two stages namely; cascaded stage (CS) and phase generator stage (PGS). The PGS stage is a combination of conventional three phase two level inverter (CTPTLI) and three bidirectional (BD) switches, while the cascaded stage can be modified using any existing cascaded topology. The proposed concept is validated through extensive simulation and experimental analyses. Results show the capability of the proposed technique in reducing device count of the existing topologies while maintaining its performance.**

Keywords—Power electronic device counts, new cascaded topology, THD.

I. INTRODUCTION

Owing to the several advantages of cascaded multi-level inverters (CMLIs) including its ability to generate high voltage by utilizing low voltage power electronic devices [1-3], low voltage stress (dv⁄dt) on the switches [4, 5], and low harmonic distortion in the output waveforms, applications of CMLIs in power systems have received much attention and several CMLI topologies have been recently proposed and published in the literature [5-13]. Based on the operating principle and the structure, CMLI topologies can be classified into three groups: (1) topologies with level generator and polarity generator [5, 7, 13, 14]; (2) modified CMLI topologies [6, 8, 9, 12, 15-18] and (3) three phase CMLI topologies [1, 3, 10, 19-22].

There are many cascaded MLI topologies, which contain two parts; level generator and polarity generator as shown in Fig. 1a [23-27]. The level generator is a cascaded connection of series cells, which is responsible to generate multilevel unipolar voltage while the polarity generator converts this unipolar voltage into bipolar voltages [5, 27, 28]. While level generator structure is unique for different topologies, the structure of polarity generator has been always an H-bridge connection involving four semiconductor switches. The number of cascaded cells in the level generator may be increased to enhance the number of voltage levels in the output without any change in the polarity generator [5, 27]. The level generator switches may work with high frequency, but the polarity generator switches always work with line voltage frequency [27].

Many new CMLI topologies are proposed, which are able to generate bipolar voltage without using polarity generator and they can be classified under the modified CMLI category as shown in Fig. 1b [29-33]. Some other creative CMLI topologies such as cross-switched topologies and modified H-bridge topologies also undergoes in this classification [12, 15, 16, 34-36].

Some CMLI topologies are mainly developed for three phase applications, they can't be directly used for single phase applications [4, 37-43]. These topologies are considered within the category of three phase CMLI topologies as depicted in Fig. 1c, they have three identical phase arms. A few hybrid three phase topologies can also be included under this category such as topologies published in [19, 37, 41].

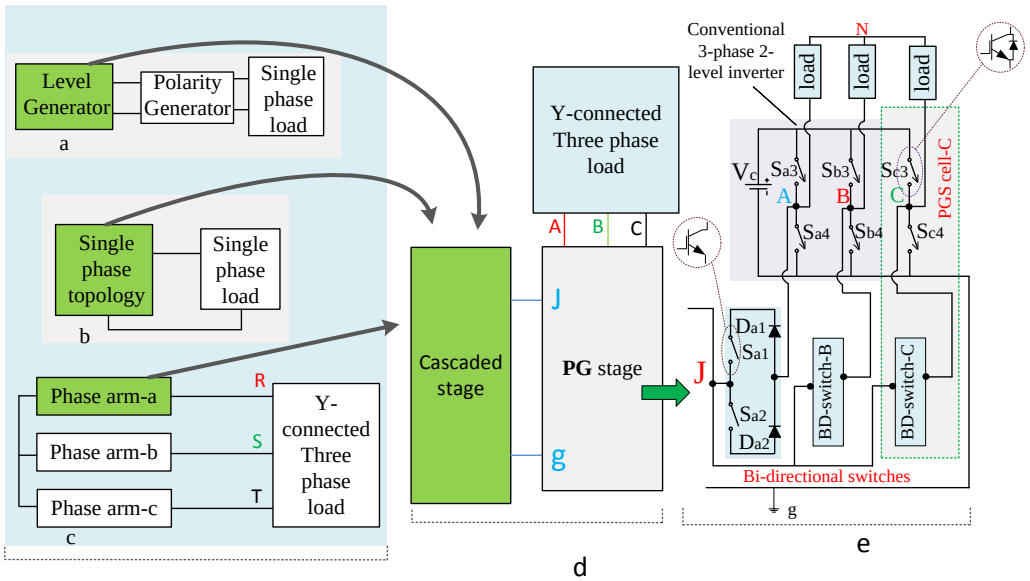

Fig. 1. Block diagrams: (a) the level generator and polarity generator based CMLI topology, (b) the CMLI topology which don't need polarity generator, (c) the 3-phase CMLI topologies, (d) the proposed new three phase CMLI, (e) Circuital model of the PG-stage

The magnitude of the input dc-supplies among the cascaded cells could be of symmetric or asymmetric methods as proposed for different topologies [3, 15, 16]. Asymmetric methods allow generating more output voltage levels in comparison to the symmetric methods [4, 10, 17, 40].

Three-phase CMLI has been widely used in large-scale renewable energy and high power medium-voltage applications [3, 4]. Although several topologies have been proposed in order to reduce the device count and increase the number of output voltage levels of single phase cascaded MLIs, majority of these topologies cannot be extended to three phase applications while the number of components have to be tripled for other single phase topologies when extended to three phase MLI [26-28, 34-36, 44, 45]. The main contribution of this paper is the presentation of a new generalized CMLI topology that could be employed by any existing single-phase CMLI topology to extend it to three-phase structure without tripling the components used within the single phase structure which may significantly reduce the device count, physical structure, complexity and cost of the 3-phase CMLI. The proposed topology can also be employed by existing three phase CMLI to reduce its device count without affecting its performance.

II. Proposed Generalized Structure for Three Phase CMLI

Figs. 1a, 1b and 1c represents the block diagrams of the three different types of the existing cascaded MLI topologies, which are described in the section-1. Fig. 1d shows the block diagram of the proposed three phase CMLI, where cascaded stage is connected with the PGS stage at junction point 'J'. The structure of the cascaded stage is not fixed and it depends on which existing cascaded MLI topology is chosen. The green shaded portion of the existing CMLI topology is needed to employ as a cascaded stage. The PGS stage has a specific circuital structure, which is a combination of three BD switches and a conventional three phase two level inverter (CTPTLI). Each of the BD switches consists of two Insulated Gate Bipolar Transistors (IGBT) and two diodes, where the IGBTs do not need internal diodes. Both of the IGBTs in a BD switch work simultaneously for turning on or off the BD switch. There exists three phase arms A, B, and C in the PGS stage. A BD switch and two switch in the CTPTLI can be considered a PGS cell in each phase arm. Hence, there are three PGS cells in the PGS stage. The CTPTLI is fed by a dc-voltage supply 'Vc'. The magnitude of the Vc is set in such a way that it becomes greater than the summation of the input supply voltages in the cascaded stage.

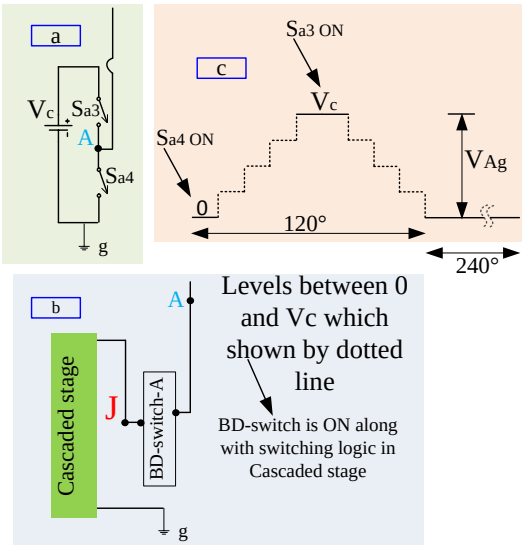

Fig. 2 Simplified structure of the proposed CMLI, (a) structure responsible to generate maximum and zero voltage, (b) intermediate level generation structure, (c) desired pole voltage waveform

Each pair of the switches, (S_{a3}, S_{a4}), or (S_{b3}, S_{b4}), or (S_{c3}, S_{c4}) of CTPTLI in different PGS cells are responsible for generating Vc and zero voltage level in the multilevel output voltage at the output nodes A, B, C, where each pair of switches operates keeping 120^0 phase difference among themselves. For any PGS cell, the PD-switch is kept turned off while the two switches in CTPTLI operate to generate Vc and zero voltage level. On the other hand, both of switches of the CTPTLI in a PGS cell are kept turned off while the PD-switch is turned on. It means the switches pair in the CTPTLI and the BD switch in any PGS cell always function in a toggle mode.

The main functions of the PD-switches are to allow the cascaded stage to connect with the output points a, b, c and to block the high voltage, Vc for the cascaded stage. As mentioned in Figs. 1a, 1b, 1c, and 1d that a specific portion of any existing CMLI topology can be utilized as cascaded stage. No change is required in the switching logic for any existing CMLI topology in cascaded stage, while generating different voltage levels. In any PGS cell, the PD-switch is turned on only for conducting the voltage levels, which are generated by the cascaded stage to the output points A, B, C. Three BD-switches, which are connected with the cascaded stage at the junction point 'J' as shown in Fig. 1e and they are operated with a 120^0 phase difference. Fig. 2a shows the simplified structure of the PGS stage while it generates level V_C and level 0, by the toggle operation of switches Sa3 and Sa4. Fig. 2b shows the operation path of the inverter while it generates the levels between V_C and 0 with the help of BD-switch and cascaded stage for PGS Cell-A. Fig. 2c shows the contribution of CTPTLI switches and BD-switch for phase arm-A to generate pole voltage V_{Ag}.

If V_{Ag}, V_{Bg},V_{Cg} are the pole voltage from the output point A, B, C to ground, respectively, then the line voltage in derived from the following equation,

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} V_{Ag} - V_{Bg} \\ V_{Bg} - V_{Cg} \\ V_{Cg} - V_{Ag} \end{bmatrix} \quad (1)$$

III. Proposed CMLI Using H-Bridge Topology At Cascaded Stage

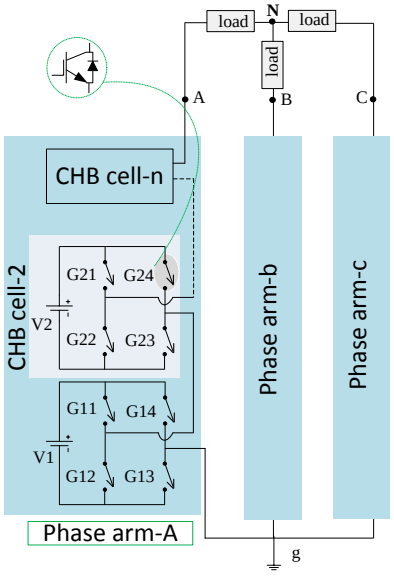

Fig. 3 Conventional three phase CHB-MLI

Cascaded H-bridge (CHB) MLI topology is a well-established structure for single and three phase applications as shown in Fig. 3 for n-number of CHB cells [3, 10, 30, 40, 46]. The proposed generalized cascaded MLI is facilitated to utilize any single or three phase structure as previously shown in Fig. 1.

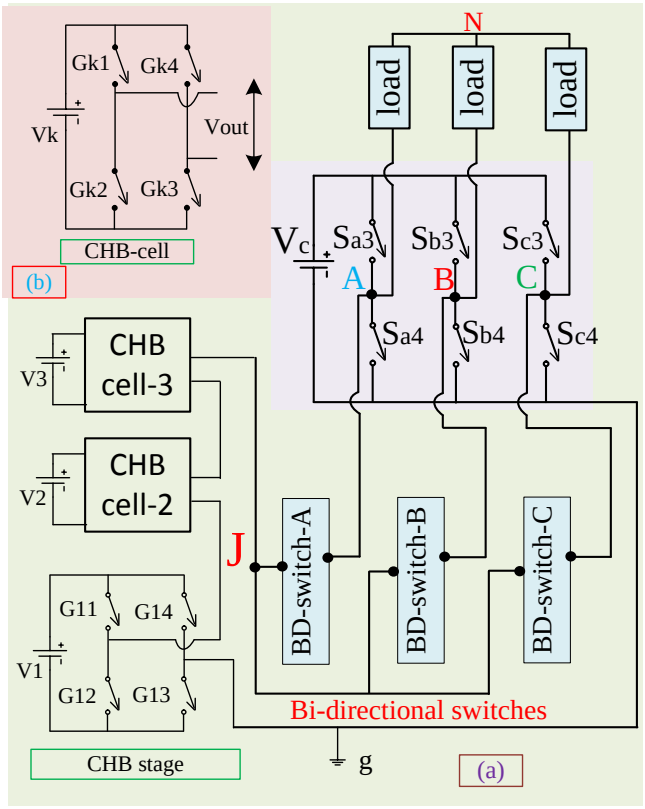

Fig. 4 Proposed three phase CMLI (a) CHB cells are considered as cascaded stage, (b) a standard CHB cell

The conventional cascaded CHB MLI topology is chosen to verify the proposed three phase inverter concept. As shown in Fig. 1, the proposed three phase structure of the new three phase MLI can be represented as shown in Fig. 4a which contains three CHB cells in the cascaded stage. Similarly, it is possible to keep any number of CHB cells in the cascaded stage in order to achieve more levels in the output voltage. Each H-bridge (k) cell contains four switches (G_{k1}, G_{k2}, G_{k3}, G_{k4}) and a dc-power supply (V_k) as depicted in Fig. 4b. Any CHB cell is able to produce three different voltages, 0, $\pm V_k$ in the output, V_{out}, where Table 1 shows the switching logic or the turn on switches to achieve the aforementioned three output voltages.

$$\begin{aligned} V_1 &= v \\ V_2 &= v \\ &\cdots\cdots \\ &\cdots\cdots \\ V_n &= v \end{aligned} \tag{3}$$

Table 1 Generalized switching logic for a cascaded cell

V_{out}	Turn on switches
V_k	G_{k1}, G_{k3}
0	G_{k1}, G_{k4}
$-V_k$	G_{k2}, G_{k4}

Symmetric and asymmetric structures are proposed for conventional CHB MLI topology in [3, 30] and [10, 33, 40, 46], respectively. Asymmetric methods are found superior than the symmetric one in terms of the reduced device count and increased number of levels in the output voltage as presented in [10, 33, 40, 46]. In [33], an asymmetric CHBMLI is presented, where the dc voltage ratios are kept in binary form (1:2… 2n). The Trinary ratio format (1:3:….: 3n) has been also proposed for CHBMLI asymmetric structure as depicted in [4, 40]. The new three phase CHB concept proposed in this paper can adopt both symmetric and asymmetric structure of the CHB MLI.

$$\begin{aligned} V_1 &= v \\ V_2 &= 2^1 v \\ &\cdots\cdots \\ &\cdots\cdots \\ V_n &= 2^{n-1} v \end{aligned} \tag{4}$$

As mentioned in section-2, the magnitude of the Vc is greater than the summation of the connected voltage supplies in the cascaded stage. The input voltage supplies in the cascaded stages are connected with some specific ratio.0 Hence if V_1, V_2, ……., V_3 are the input voltage supplies for n-number of cells in the cascaded stage, then we can get the following equations for symmetric, binary related and Trinary related input supplies, respectively.

$$\begin{aligned} V_1 &= v \\ V_2 &= 3^1 v \\ &\cdots\cdots \\ &\cdots\cdots \\ V_n &= 3^{n-1} v \end{aligned} \tag{5}$$

Where ‘v’ is the per unit voltage value.

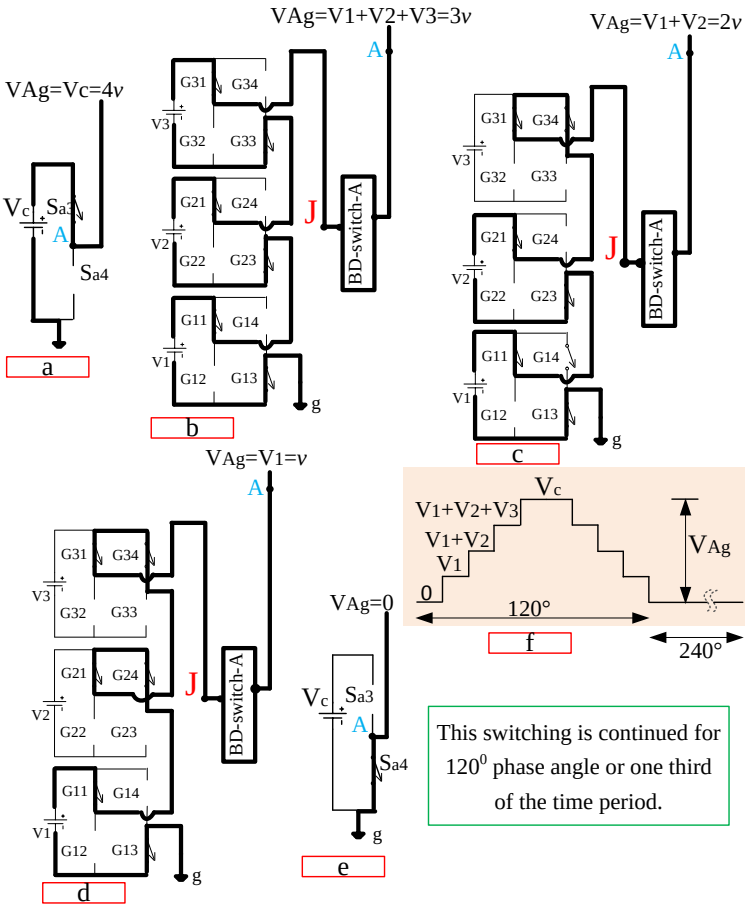

Fig. 5 Different switching logics for generating four levels in the pole voltages

Now the input voltage-supply of the CTPTLI, V_C can be represented by,

$$V_C = \sum_{0}^{n} V_n + V_1 = (V_1 + V_2 + ... + V_n) + v \qquad (6)$$

Fig. 5 shows switching logic and conduction path for the pole voltage, VAg generation, while the magnitudes of the CHB cells and CTPTLI input supply voltage are considered according to (3) and (6); respectively. Here the input voltage of the CHB cells and CTPTLI input supply are $V_1=V_2=V_3 = v$; $V_C=4v$.

With the contribution of CTPTLI and CHB cells along with BD-switches the pole voltages, V_{Ag}, V_{Bg}, V_{Cg} are produced. Only the CTPTLI switches operate to generate the voltage levels, Vc and 0 as shown in Figs. 5a and 5e, respectively. The other voltage levels, $V_1+V_2+V_3$, V_1+V_2, V_1 exist between the levels Vc and 0 are produced with the different switching logic among the CHB cells, when the BD-switches turned on. Finally, the combined multilevel waveform is achieved, which is shown in Fig. 5e. While the Fig. 5 shows for the generation of pole voltage, V_{Ag}; the other two pole voltages follow same switching logics but keeping 120^0 phase shift among the PGS-cells. The switching function for each phase arm last for 120^0 phase angle.

IV. Implementation of the Proposed MLI

The proposed MLI topology, which is shown in Fig. 4 is controlled with a low frequency staircase modulation strategy [47]. The switching states follows a sequence in the d-q plane. The number of states, S in the d-q plane to generate any number of level generation is can be expressed by,

$$S = 6(N_P - 1)\,;\ N_P>1 \text{ and always integer} \qquad (7)$$

Where N_P is the number of levels in the pole voltages, V_{Ag}, V_{Bg}, V_{Cg}.

For different values of N_P, the number of switching states, S form different hexagons. In Fig. 6, the smallest hexagon represents the switching states for $N_P=2$ and the following hexagons for $N_P=3$, $N_P=4$, and $N_P=5$; respectively. According to Fig. 5, the proposed topology requires switching states, which will generate $N_P=5$ in the pole voltages. The upper most hexagon in Fig. 6 is appropriate for getting 24 switching states to generate five levels, 4*v*, 3*v*, 2*v*, *v*, 0 in the pole voltages, V_{Ag}, V_{Bg}, V_{Cg}. The 24 switching states are, 044, 043, 042, 041, 040, 140, 240, 340, 400, 430, 420, 410, 400, 401, 402, 403, 404, 304, 204, 104, 004, 014, 024, 034.

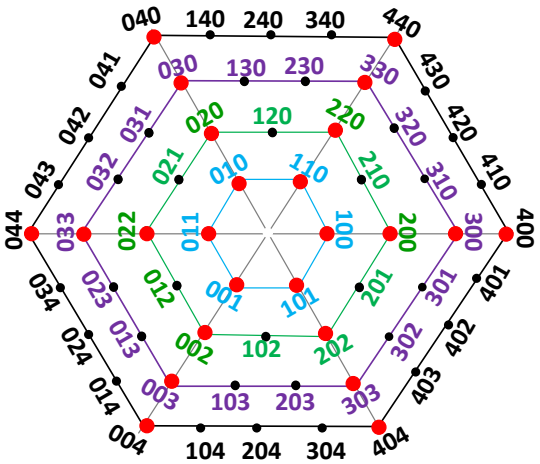

Fig. 6 Generalized switching states for generating different number of levels in the pole voltage

Each of the switching states has three switching vectors, S_a, S_b, S_c for three phase voltage generation. The pole voltages, V_{Ag}, V_{Bg}, V_{Cg} are taken as reference to achieve the three switching vectors in each switching states at any instant of time [47]. In general, the switching angle for each of the switching states are equal and can be expressed as,

$$\text{Switching angle} = 360^0/S \qquad (8)$$

Hence, the switching angle of each of the 24 switching state is 15^0. That means, a new switching state will come into operation every 15^0. In the switching sequence of 24 switching states, the switching vectors 4, 3, 2, 1, 0 are combined in an organised manor to generate three phase pole voltages and the switching vectors always abide by the Table 2 for different vo

Table 2 Switching logic for different switching vector

Switching vector, Sa/Sb/Sc	Switching logic
4	Fig. 5a
3	Fig. 5b
2	Fig. 5c
1	Fig. 5d
0	Fig. 5e

The proposed topology is simulated by using Matlab/Simulink software and a laboratory prototype inverter is developed to confirm the simulation results and validate the feasibility of the proposed inverter. The real time switching signals are obtained by using digital signal processor, TMS320F2812. The implementation of the topology required 12 IGBT for three CHB cells in the cascaded stage and 12 IGBT in the PGS cells. A total of twenty-one GPIO (General-Purpose Input/Output) pins are required in the DSP, TMS320F2812 for achieving all real time switching signals. Sixteen (GPIOA0-GPIOA15) pins are chosen from GPIO-A and remaining one pin is chosen from GPIO-B (GPIO B0) pin array [48]. The gate signals for CHB stage are identical for phase-A, B and C. The gate signals of phase B and C within the three PG-cells have similar pattern as in phase-A with a phase shift of 120^0 and 240^0, respectively.

Six insulated gate bipolar transistors (IGBTs), IRG4BC40W, 600V/20A along with six diodes, RHRP1540, 400V/15A are used to implement the BD-switches in PG-stage while eighteen IGBTs, HGTG20N60B3D, 600V/40A are used to build the CHB cells and CTPTLI.

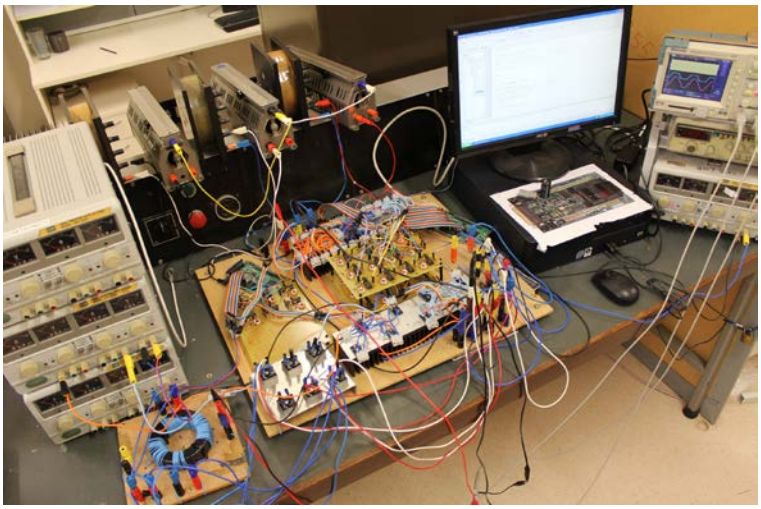

Fig. 7 Experimental prototype

V. RESULTS AND DISCUSSIONS

Fig. 7 shows various parts of the hardware prototype. The input dc-voltage sources are connected such as $V_1=V_2=V_3=v=70$ V and $V_C=4v=280$ V. Inductive 3-phase load (Z=55+j37.68) Ω/phase) is considered for testing the inverter performance. The experimental results are provided in Fig. 8, where Figs. 8 presents junction voltage, V_{Jg} and phase voltages, V_{Ag}, V_{Bg}, V_{Cg}, respectively. The pole voltages contain five levels (280 V, 210 V, 140 V, 70V, 0) while V_{Jg} comprises three levels (210 V, 140 V, 70 V).

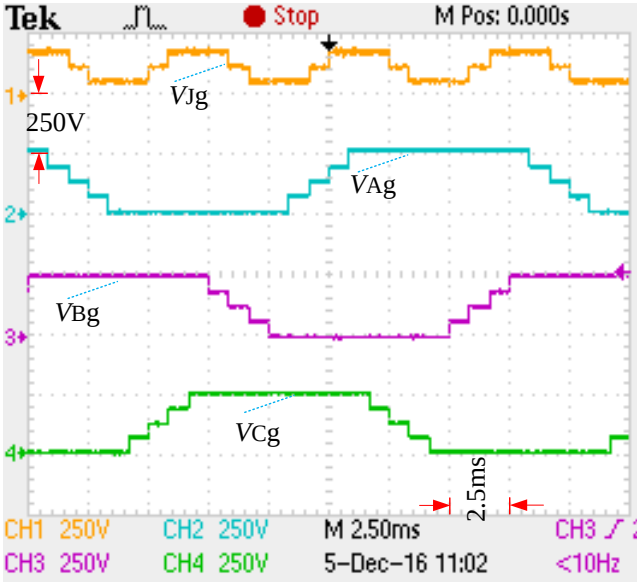

Fig. 8 Experimental results of Junction voltage, V_{Jg} and Pole voltages, V_{Ag}, V_{Bg}, V_{Cg} when the CHB-cells are fed by symmetric dc-power supplies

Fig. 8 proves that the CHB stage does not take part in the generation of minimum (0) and maximum (V_C) levels of the pole voltages. The line voltage, V_{ab} in Fig. 8c reveals that each line voltage waveform comprises nine levels (±280 V, ±210 V, ±140 V, ±70 V, 0.

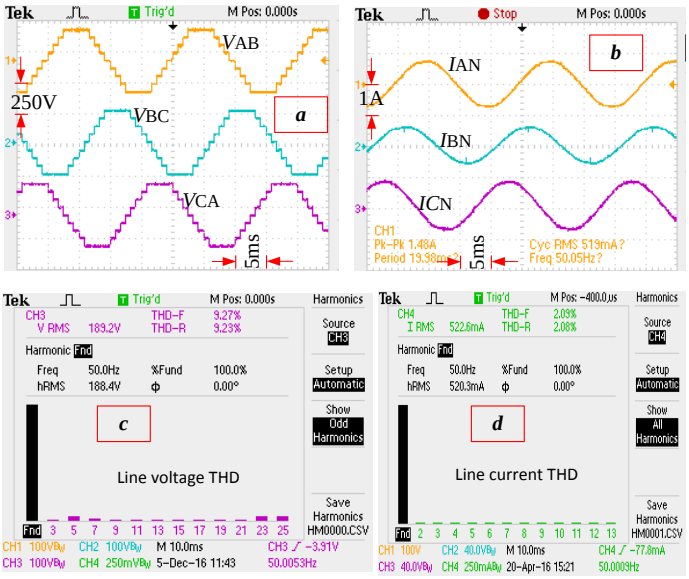

Fig. 9 Experimental results, (a) line voltages, (b) line currents, (c) THD of the line voltage, (c) THD of the line current, when CHB cells are fed by Symmetric dc power supplies

Fig. 9a shows the line voltages, V_{AB}, V_{BC}, V_{CA}. Fig. 9b present the three phase line currents, I_{AN}, I_{BN}, I_{CN}. No filter is utilized while taking the results of the voltage and current. The unfiltered line voltage and line current total harmonic distortion (THD) are shown in Figs. 9c and 9d, respectively. The THD of the line current and voltage must be less than 5%, to comply with the IEEE standard [49].

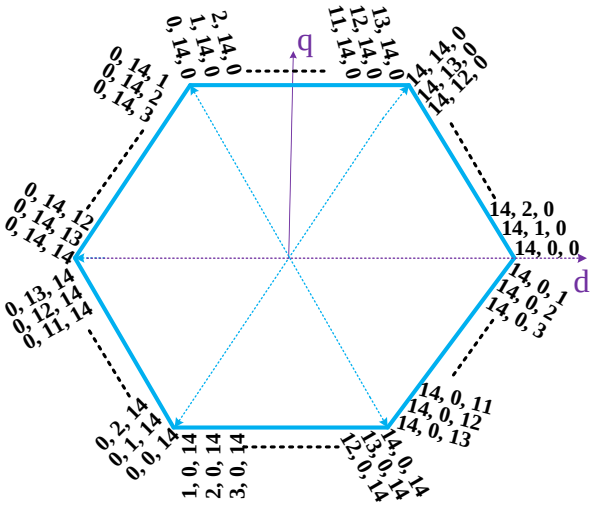

Fig. 10 switching states for generating 15-levels in the pole voltage

The current THD complies with the mentioned standard, while voltage THD is more than 5% in the implemented 9-level CMLI topology. By increasing the number of levels in the output voltage, the amount of THD can be reduced which may be achieved through considering Trinary input dc supply method among input dc supplies as shown in (5) or adding more CHB cells to the cascaded stage. Keeping same magnitude in the V_C, the input dc-supply voltages of V_1, V_2, V_2 to the three CHB cells are adjusted as Trinary method according to (5). Hence, after the adjustment, the magnitudes of V_1, V_2, V_3 and V_C can be written as 20 V, 60 V, 180 V, 280 V; respectively. This configuration is able to generate 15-levels in the pole voltage output, where N_P=15. Hence it needs 84-switching states to generate three phase output voltages according to (7). The 84-switching states can be shown as hexagonal form in Fig. 10.

Table 3 switching logic in the different CHB cells and PG-stage for generating 15 levels in the pole voltage

Switching vector, Sa	Pole voltage		Switching logic	
14	V_C	280 V	Fig. 5a	
13	v+3v+9v	260 V	$V_1+V_2+V_3$	BD-Switch-A ON
12	0+3v+9v	240 V	$0+V_2+V_3$	
11	-v+3v+9v	220 V	$-V_1+V_2+V_3$	
10	v+0+9v	200 V	V_1+0+V_3	
9	0+0+9v	180 V	$0+0+V_3$	
8	-v+0+9v	160 V	$-V_1+0+V_3$	
7	v-3v+9v	140 V	$V_1-V_2-V_3$	
6	0-3v+9v	120 V	$0-V_2+V_3$	
5	-v-3v+9v	100 V	$-V_1-V_2+V_3$	
4	v+3v+0	80 V	V_1+V2+0	
3	0+3v+0	60 V	$0+V_2+0$	
2	-v+3v+0	40 V	$-V_1+V_2+0$	
1	v+0+0	20 V	V_1+0+0	
0	0	0	Fig. 5e	

Table 3 shows the switching logics in case of different switching vectors. Finally, the inverter generates 15-levels in the pole voltages and 29-levels in the line voltage. The junction voltage, V_{Jg}, pole voltages, V_{Bg}, V_{Bg} and line voltage V_{AB} are shown in Fig. 11a. The THD of the unfiltered 29-level line voltages is shown in Fig. 11b, which is nearly to 5%.

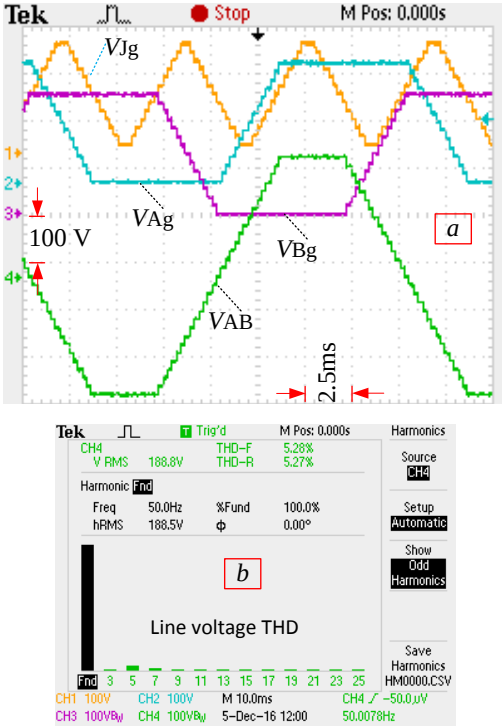

Fig. 11 Experimental results, (a) Junction voltage, pole voltages, line voltages and currents, (b) THD of the line voltage, when CHB cells are fed by trinary related dc power supplies

VI. Comparison of the Proposed Concept with Current Topologies

The proposed three phase MLI concept does not only confine to a specific cascaded MLI topology, but it is also applicable for any existing cascaded MLI topology as it can be adopted to extend existing single phase topologies to three phase without tripling the used components as per the current conventional methods.

Table 4: Comparison among different symmetric existing cascaded MLI topologies and proposed three phase new MLI concept for generating 15 levels in the line voltage

Topology	Single phase topology [5]		Three phase Cross-switched inverter [34, 36]		Three phase Half bridge inverter [43]		Single phase H-bridge [30]	
	Existing Single phase	proposed new concept for 3-phase	Existing 3-phase	proposed new concept	Existing 3-phase	proposed new concept	Existing single phase	proposed new concept for 3-phase
No of switches	16	24	48	28	42	26	84	40
No of diodes	16	24	48	28	42	26	84	40
No of gate driver	16	24	48	28	42	26	84	40
No of dc supplies	7	8	21	8	21	8	21	8

Furthermore, the proposed concept is able to reduce the size of the existing cascaded MLI topologies in terms of device count without degrading the quality of the output voltage. A comparison is performed in order to show the effectiveness of the proposed three phase cascaded MLI concept over various existing topologies. Different factors such as number of power semiconductor components, number of gate driver circuits and number of dc-supplies are considered in the comparison. Table 4 lists a brief comparison among the symmetric structure of the proposed concept and some proposed topologies in the literatures to produce 15-levels in the line-line voltage. Considered topologies used in this comparison include single phase topology proposed in [5], three phase cross-switched inverter proposed in [34, 36], 3-phase Half-bridge topology proposed in [43], and single phase H-bridge topology proposed in [30]. As can be seen in Table 4, the proposed MLI concept reduces the size of the all existing 3-phase cascaded MLI in terms of device count. In addition, it can be observed that existing single-phase topologies can be extended to 3-phase structures using the new proposed concept without tripling the hardware components.

Table 5: Comparison among the conventional three-phase CHB topology and the proposed new three phase cascaded MLI for different symmetric and asymmetric methods

Topology	Symmetric Two CHB cell topology[3]		Binary related Two CHB cell topology [50]		Ternary related three CHB cell topology [4]		Ternary related four CHB cell topology [33]	
	Existing 3-phase	proposed new concept	Existing 3-phase	proposed new concept	Existing 3-phase	proposed new concept	Existing 3-phase	proposed new concept
No of levels in line voltage	5	7	7	9	27	29	81	83
No of switches	24	20	24	20	36	24	48	28
No of diodes	24	20	24	20	36	24	48	28
No of gate driver	24	20	24	20	36	24	48	28
No of dc supplies	6	3	6	3	9	4	12	5

Table 5 shows a comparison among existing three phase CHBMLI symmetric and asymmetric topologies and the proposed three-phase MLI concept. In the symmetric CHB topology proposed in [3], each phase arm contains two CHB cells and the comparison shows that the new three phase MLI concept demands for less device counts with better output waveform in terms of number of voltage levels. The asymmetric CHB inverter proposed in [50], has two CHB cells and binary relation is maintained between the cells input dc-supplies in each phase arm. On the other hand, trinary related three and four CHB cells in each phase arm is considered in [4] and [33], respectively A significant reduction in the device counts takes place when the new three-phase cascaded MLI

concept is applied to these existing asymmetric topologies as can be seen in Table 5. The percentage of reduction of device count and the input dc supplies is increasing when the number of CHB cells in each phase arm is increasing. For example, 17% reduced power electronic components are achieved in the proposed three phase cascaded MLI concept for two CHB cell, while 33% and 42% reduction will be achieved when the new three phase MLI concept is applied for three and four CHB cells in each phase arm of the existing topologies, respectively.

VII. CONCLUSIONS

This paper shows a new design and implementation of a three phase CHBMLI. Both simulation and experimental results proves the practical feasibility of the proposed new three-phase MLI concept. Comparison with existing single and three phase MLI topologies shows the superiority of the proposed new concept that can be adopted to extend any single phase MLI structure to 3-phase without tripling its components as per the current practice. The new technique can also be used to reduce the device count in existing three phase topologies without degrading its performance. Since the number of component is directly related with the cost, complexity and the installation area, the new three phase concept is a cost effective technique that is expected to have a great potential for renewable power generation systems and smart grid applications.

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