

A High Frequency Linked Modular Cascaded Multilevel Inverter

Md Mubashwar Hasan¹, A. Abu-Siada²,

Department of Electrical and Computer Engineering, Curtin University, Perth, Australia

¹m.hasan12@postgrad.curtin.edu.au, ²a.abusiada@curtin.edu.au

Abstract— In this paper, a high frequency linked cascaded multilevel inverter (CMLI) is presented, which brings simplicity for CMLI to connect in renewable systems and electronic vehicular applications. The requirement of multiple isolated dc-supplies and their balancing is a critical drawback in CMLI and for this reason; it is very difficult to connect a CMLI directly with any system. The utilization of multi-winding transformer eradicates the problem associated with the aforementioned drawbacks by establishing a permanent voltage balancing and manage all the multiple isolated dc-supplies from a single dc-supply. Even multilevel inverter output voltage magnitude can be controlled by controlling the magnitude of the single dc-supply. A scale down laboratory prototype model is developed and different results are provided to verify the practical feasibility.

Keywords—cascaded multilevel inverter, low frequency control, THD, isolated dc-supply

I. INTRODUCTION

Cascaded Multilevel inverters are drawing more attention in recent years as they are able to produce more levels in the output voltage by utilizing reduced device counts while compared with diode clamp and flying capacitor MLI topologies that suffer from capacitor voltage balancing and complexity of control algorithms [1]. Other advantages of CMLI topologies include: they are suitable for high-power, medium-voltage applications by utilizing low rated power electronic devices, low switching losses, improved electromagnetic compatibility, and low harmonic contents in the output waveforms [2-6]. Moreover, CMLI topologies contain modular structure that allows reduced implementation and maintenance complexity and hence improves the inverter reliability [3, 7, 8]. Although CMLI are considered as the most reliable topologies in the MLI family, it still exhibits some drawbacks including the requirement for a number of isolated dc supplies and their voltage balancing [9-11]. Any unbalance among the isolated input dc supplies causes distortion to the inverter output voltage and current waveforms [12]. Furthermore, the desired levels in the output voltages are not achieved if any unbalance occurs among the input dc supplies [13, 14].

To overcome the issue of voltage balancing among multiple input isolated dc supplies, a number of transformer-based topologies have been proposed in the literatures.

Cascaded transformer-based CMLI is proposed in [15, 16], where all the secondary windings of the used transformers are connected in series while the primary winding of each transformer is connected to an H-bridge module with all H-

bridge modules connected to a common dc supply. Although this topology is validated through several experimental results, it calls for a large number of single phase transformers; for example, it requires 21 single phase transformers along with 21 H-bridge modules for three phase voltage generation where each H-bridge module requires four IGBT/MOSFET, which may make the inverter system too bulky, expensive and unrealistic for high-power and medium- voltage applications. The transformer-based cascaded MLI topologies in [15, 16], are implemented only for symmetric input voltage concept and it may be very complex to apply asymmetric method such as binary related or trinary related input voltage modes to these topologies as all the input terminals of the H-bridge modules are connected in parallel with the same dc source [17-19].

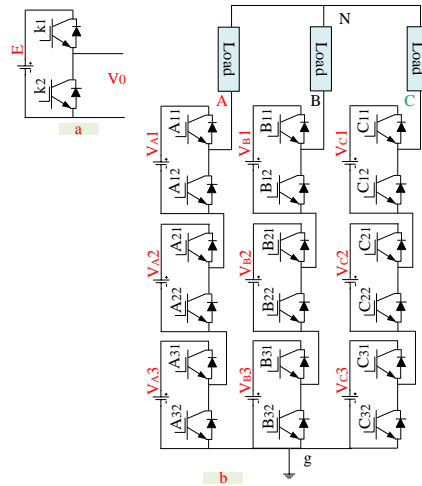


Fig. 1. Modular half-bridge CMLI, (a) a basic half-bridge module, (b) Modular cascade MLI where each phase arm contains three half-bridge module

In this paper, a high frequency multi-winding transformer based three phase modular half-bridge CMLI is demonstrated, where the isolated dc-voltage supplies are managed precisely by high frequency magnetic link. The magnetic link allows the half-bridge CMLI to operate in symmetric as well as asymmetric dc-supply voltage methods.

II. PROPOSED CMLI INVERTER AND CONTROL TECHNIQUE

Fig. 1a shows the basic half-bridge module (k), which requires two power electronic switches (k1, k2) and a dc-power supply (E). A half-bridge module is able to generate two levels, 0, E at the output voltage (V_0) for two different switching

patterns, which is explained in Table 1. Fig. 1b shows the three phase modular cascaded half-bridge inverter where three half-bridge modules are considered in each phase arm (A, B, C) and all the dc-power supplies in the modules are isolated from each other. The magnitudes of the dc-supplies in each phase arm can be arranged in symmetric and asymmetric binary related configuration by the following equations (1) - (2); respectively.

$$V_{x1}=V_{x2}=V_{x3}=V_{dc} \quad (1)$$

$$V_{x1}=V_{dc}, V_{x2}=2V_{dc}, V_{x3}=4V_{dc} \quad (2)$$

Where ‘x’ represents phase arm a, b and c.

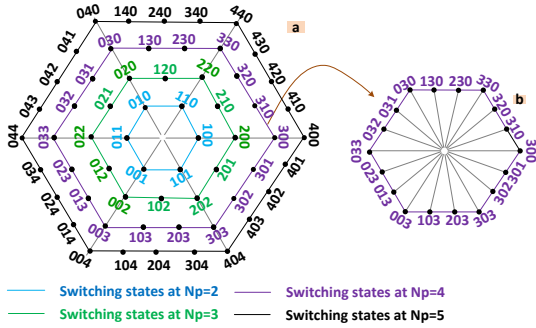


Fig. 2. Generalized switching states in d-q plane, (a) Switching states for generating different number of levels in the phase to ground voltage, N_p ; (b) switching state for

The asymmetric configuration allows to produce more levels in the output voltage without increasing the number of devices counts. The line voltages, V_{AB} , V_{BC} , V_{CA} related with the phase to ground voltages, which can be expressed by the following equation.

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} V_{Ag} - V_{Bg} \\ V_{Bg} - V_{Cg} \\ V_{Cg} - V_{Ag} \end{bmatrix} \quad (3)$$

The considered modular structure generates 4- levels in the phase to ground voltages while symmetric structure is chosen according to equation (1), while 8-levels is obtained in the phase to ground voltages for asymmetric structure of equation (3). The maximum number of levels in the phase to ground voltage, N_p determines the number of levels in the line voltage and their relation can be expressed by following equation.

$$N_{level}=2N_p-1 \quad (4)$$

Staircase modulation is chosen for as control technique for the modular topology shown in Fig. 1b. The phase to ground voltage is utilized as the reference for achieving the proper switching states. The reference phase to ground voltage can be written as

$$\left. \begin{aligned} V_{Ag,ref} &= \frac{(N_p - 1) * V_{dc}}{2} \left(m_i * \cos(2\pi ft) + \left[1 - \frac{m_i}{6} \cos(6\pi ft) \right] \right) \\ V_{Bg,ref} &= \frac{(N_p - 1) * V_{dc}}{2} \left(m_i * \cos(2\pi ft - \frac{2\pi}{3}) + \left[1 - \frac{m_i}{6} \cos(6\pi ft) \right] \right) \\ V_{Cg,ref} &= \frac{(N_p - 1) * V_{dc}}{2} \left(m_i * \cos(2\pi ft + \frac{2\pi}{3}) + \left[1 - \frac{m_i}{6} \cos(6\pi ft) \right] \right) \end{aligned} \right\} \quad (5)$$

TABLE 1 BASIC SWITCHING PATTERN OF HALF-BRIDGE MODULE

Cell output voltage (V_o)	Turn on Switches
0	K2
+E	K1

Where m_i is the modulation index; and f =line voltage frequency, t =instantaneous time.

Then the switching states (S_a , S_b , S_c) can be obtained by the following equation:

$$\left. \begin{aligned} S_a &= \text{round} \left\{ \frac{(N_p - 1)}{V_{Ag,max}} * V_{Ag,ref} \right\}; \\ S_b &= \text{round} \left\{ \frac{(N_p - 1)}{V_{Bg,max}} * V_{Bg,ref} \right\}; \\ S_c &= \text{round} \left\{ \frac{(N_p - 1)}{V_{Cg,max}} * V_{Cg,ref} \right\} \end{aligned} \right\} \quad (6)$$

The switching state can be represented in d-q axis by the following equations,

$$V = V_q - jV_d \quad (7)$$

$$\left. \begin{aligned} V_d &= \frac{(\text{maximum phase to ground voltage})}{\sqrt{3}(N_p - 1)} (S_c - S_b); \\ V_q &= \frac{(\text{maximum phase to ground voltage})}{3(N_p - 1)} (2S_a - S_b - S_c) \end{aligned} \right\} \quad (8)$$

In Fig. 2, the calculated switching states are shown for generating $N_p=2, 3, 4$ and 5 . Similarly, all the switching states for generating any number of levels in the phase to ground voltage can be represented in d-q plane as a form of hexagon.

The relation between N_p and the number of switching states, S in the d-q axis can be written by following equation

$$S=6(N_p-1) \quad (9)$$

If the frequency, f_{line} of the desired line voltage is 50 Hz, the duration of each of the switching state, ‘T’ can be written by

$$T=1/[(f_{line}) * S] = 0.02/6(N_p-1) \quad (10)$$

For example, if $N_p=4$, then the time period of each of the switching states is $T1=T2=...=T18= 1.1111$ ms.

Table 2 presents the switching combination for a complete cycle (50 Hz) to generate three phase seven level line voltage while the magnitude of isolated dc-power supplies are kept in symmetric form according to equation (1).

III. HIGH FREQUENCY LINK

The High frequency link in Fig. 3 consists of (1) a full bridge square wave voltage generator, (2) multi-winding transformer (MWT), and (3) full-bridge diode rectifier. The full bridge square wave voltage generator consists of a voltage source, E_s and two pairs of switches, ($Q1, Q3$), and ($Q2, Q4$). The voltage source, E_s is the one, who manages all the required dc-supplies in the half-bridge modules. The aforementioned two pairs of the switches always operate in toggle mode to generate high frequency square wave and the generated high frequency square wave voltage is fed directly to the primary winding of the multi-winding transformer. The number of secondary windings depend on the number isolated dc-supplies requirement in the CMLI. The applied primary winding voltage in the multi-winding transformer can be written by

$$V_{rms} = 4 f N A_e B_{max} \quad (9)$$

Where, f = frequency of square wave voltage, N = number of

turns in the primary winding, A_e = cross-sectional area of the toroidal core, B_{max} = magnetic flux density.

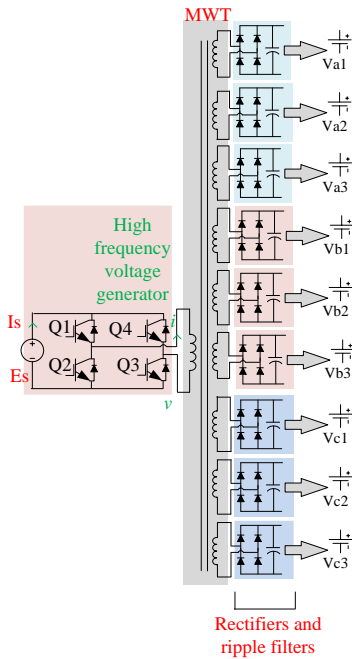


Fig. 3 Different sections of High frequency link

According to the above equation, the toroidal core is inversely proportional with the square wave voltage and hence high frequency, 20 KHz is considered in the square wave voltage. FERROXCUBE, T102/66/25-3C90, with $A_e=445.32\text{mm}^2$; $B_{max}=200\text{ mT}$ is utilized as the toroidal core to make the HFL transformer. According to (9), for $V_{rms}=240\text{V}$, the least number of turns in the primary winding of the implemented toroidal transformer is $N=34$. The primary winding of the implemented HFL is designed with 36 turns to ease the calculation of the secondary winding turns.

Table 2 Switching states sequence for a complete one cycle of three-phase line voltage generation

Switching states, S_a, S_b, S_c	300	310	320	330	230	130	030	031	032	033	023	013	003	103	203	303	302	301
T[s]	T1	T2	T3	T4	T5	T6	T7	T8	T9	T ₀	T11	T12	T13	T14	T15	T16	T17	T18
A11, A12'	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1
A21, A22'	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1
A31, A32'	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
B11, B12'	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
B21, B22'	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
B31, B32'	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
C11, C12'	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
C21, C22'	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
C31, C32'	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0
V_{AB}	3	2	1	0	-1	-2	-3	-3	-3	-3	-2	-1	0	1	2	3	3	3
V_{BC}	0	1	2	3	3	3	2	1	0	-1	-2	-3	-3	-3	-2	-1	0	0
V_{CA}	-3	-3	-3	-3	-2	-1	0	1	2	3	3	3	2	1	0	-1	-2	-2

The symmetric structure is considered in the CMLI where the ratio between the primary and multiple secondary windings would be 1:1 for producing ($V_{a1}, V_{a2}, V_{a3}, V_{b1}, V_{b2}, V_{b3}, V_{c1}, V_{c2}, V_{c3}$). It is worth mentioning that although ferrite material has been widely utilized as toroidal core, some other magnetic materials such as Hitachi Finmet, and metglas may provide better performance in terms of compact size, power capacity and efficiency [20].

At the end, Schottky full bridge rectifier module, KBPC5010, 1kV, 50A is utilized to achieve output dc voltage from the developed HFL. The practical rectified output dc voltages involve some spikes every time the input square voltage changes its magnitude between positive and negative levels. For this reason, it is essential to employ a proper filter to eliminate these spikes.

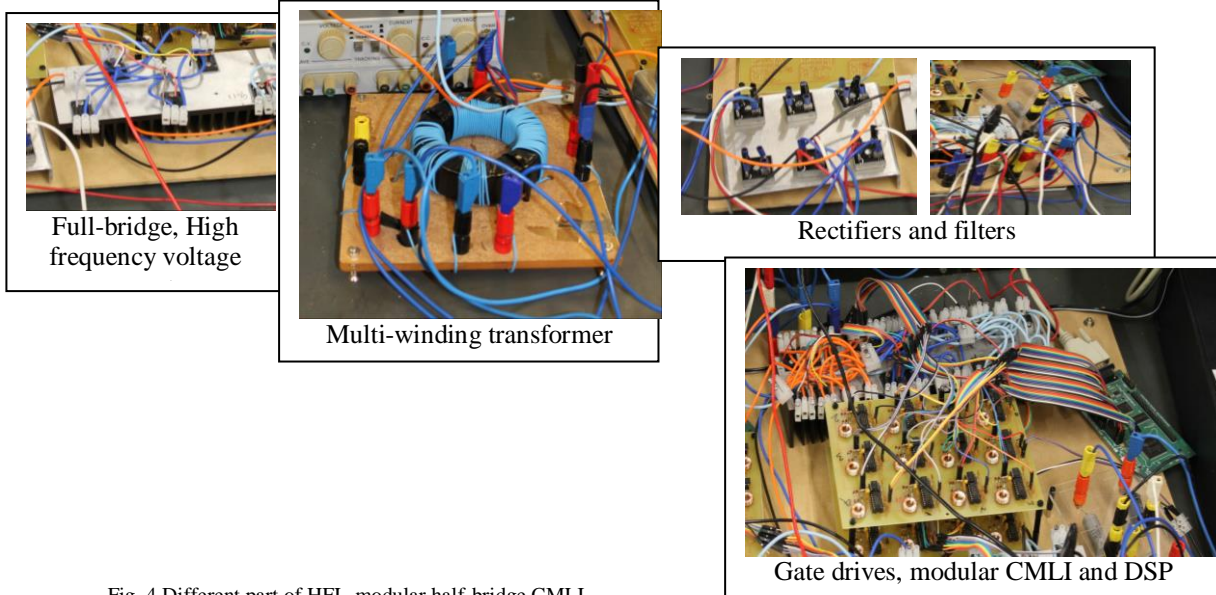


Fig. 4 Different part of HFL-modular half-bridge CMLI

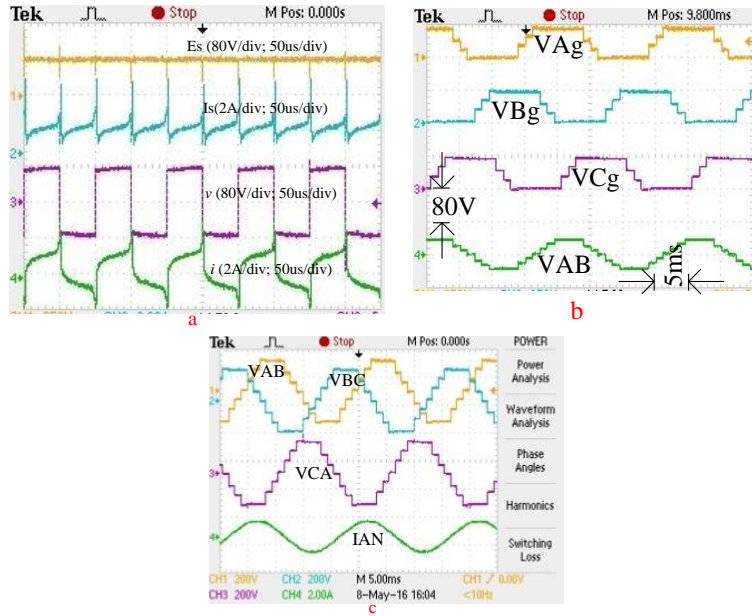


Fig. 5 Waveforms, (a) input-output voltage and current waveforms of high frequency square wave voltage generator, (b) phase to ground voltage, V_{Ag} , V_{Bg} , V_{Cg} waveforms of CMLI, (c) line voltage, V_{AB} , V_{BC} , V_{CA} waveforms of CMLI

IV. RESULTS AND DISCUSSION

The major parts of the scale down laboratory prototype is shown in Fig. 4, where 18 bipolar insulated gate bipolar transistor (IGBT) are utilized to build the modular multilevel half-bridge CMLI, and four IGBTs are needed for the full-bridge high frequency square wave generator. Same IGBT, HGTG20N60B3D utilized for both CMLI and high frequency full-bridge square wave voltage generator. Digital signal processor (DSP), TMS320F2812 is employed to generate the switching gate signal for the multilevel inverter and high frequency full-bridge square wave voltage generator. In Fig. 5a, the high frequency (20 KHz) input-output voltage and current, (E_s , I_s) and (v , i) are presented. Figs. 5b and 5c shows the experimental results of phase to ground voltages, line voltages and line current. The E_s is fixed to 80 V and three phase inductive load ($Z=115+j39.27$ ohm /phase) is utilized while taking the results.

Fig. 6 shows the line voltage and line current THD. While the line current THD satisfies the IEEE standard, the line voltage THD is more than 5%. Line voltage THD reduces while number of levels are increased and it can be done by adopting asymmetric method according to (2). The same structure is able to generate 15-levels in the line voltage, which significantly reduces the THD.

V. CONCLUSION

The implemented high frequency linked modular CMLI able to operate by utilizing a single dc-source. The single dc-source may exist in the form of either a battery source, PV-output voltage, rectified wind generator output or a dc-bus. The proposed concept of high frequency linked modular CMLI will find easy application in vehicular system and renewable system.

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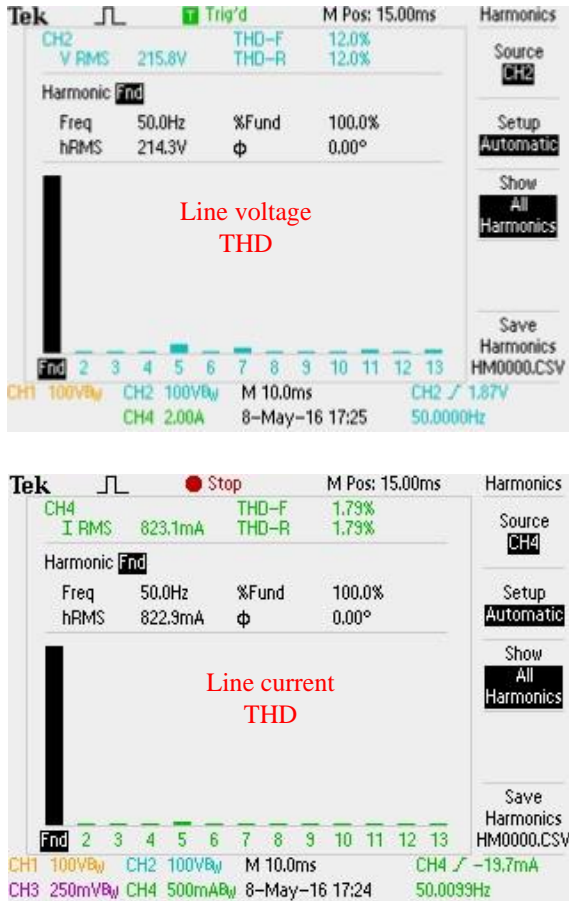


Fig. 6 line voltage and line current THD

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