A Novel Three Phase Cascaded Multilevel Inverter Topology

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***Abstract*—** A new Cascaded Multilevel inverter (CMLI) concept is presented in this paper, which is applicable to any existing CMLI topologies. The proposed new three phase MLI topology consists of level generator stage (LGS) and phase generator stage (PGS). While the PGS contains a specific structure of 12-semiconductor switches and 12-diodes, the LGS structure depends on the existing CMLI topologies. The main feature of the proposed new CMLI topology is to reduce the device counts of the existing CMLI topologies while they are implemented as dc/ac three phase power converters. The conventional cross-switched CMLI topology is considered as LGS in the experimental prototype. Simulation and experimental results are provided to verify the proposed new three phase CMLI concept.

Keywords*— *Cascaded multilevel inverter; Semiconductor devices; dc power supplies.

I. INTRODUCTION

Cascaded Multilevel inverters (CMLI) are becoming very attractive as three-phase power converters (DC/AC). The easiness to implement, further extension, modular structure, avoidance of capacitor voltage balancing have made the CMLI more preference over diode clamped and flying capacitor MLI topologies. A number of CMLI topologies have already been proposed and based on the operating principle and the structure, CMLI topologies can be classified into three groups: (1) topologies with level generator and polarity generator [1-10]; (2) modified CMLI topologies [8, 11-16] and (3) three phase CMLI topologies [17-21]. The each CMLI topologies in first category contains a level generator and a polarity generator. While the level generator is a series connection of cascaded cells which is responsible for generating unipolar multilevel voltage, the polarity generator is a full bridge with four semiconductor switches which convert the unipolar multilevel voltage into bipolar AC voltage [5, 8]. The CMLI topologies in the second group contains a number of series connected cascaded cells and able to generate multilevel AC voltage avoiding the polarity generator [12-14]. On the other hand, the topologies in the third group are proposed only for three phase applications and three phase hybrid topologies, naming hybrid H-bridge, hybrid half-bridge also undergo in this group [19, 20, 22].

Although several topologies have been proposed in order to reduce the device count and increase the number of output voltage levels of single phase cascaded MLIs, majority of these topologies cannot be extended to three phase applications while the number of components have to be tripled for other single phase topologies when extended to three phase MLI [4, 5, 9, 23-27]. The main contribution of this paper is the presentation of a new generalized CMLI topology that could be employed by any existing single phase CMLI topology to extend it to three phase structure without tripling the components used within the single phase structure which may significantly reduce the device count, physical structure, complexity and cost of the 3-phase CMLI. The proposed topology can also be employed by existing three phase CMLI to reduce its device count without affecting its performance.

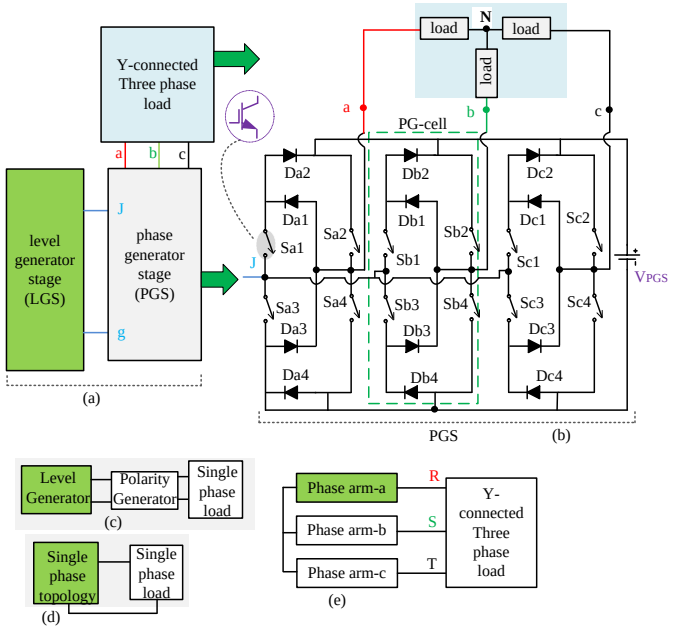

Fig. 1. Different stages of the proposed three phase MLI : (a) block diagram of proposed topology, (b) circuital model of the PG stage, (c) block diagram of the CMLI topologies based on level generator and polarity generator as discussed in section I, (d) block diagram of the innovative CMLI topologies as discussed in section I, (e) block diagram of the conventional three phase CMLI topologies as discussed in section I

II. PROPOSED GENERALIZED STRUCTURE FOR THREE PHASE CMLI

Fig 1a shows the block diagram proposed CMLI where the LGS is connected with PGS at junction point 'J'. PGS stage contains three identical PG-cells, which are responsible to generate the three phases as shown in Fig. 1b where each cell has four diodes (Dx1-Dx4) and four semiconductor switches (Sx1-Sx4), x represents phase-a, b, c. Three PG-cells are connected with a common dc-source, VPGS. The structure of LGS depends on the existing CMLI. Figs. 1c, 1d, 1e represents

the three types of the CMLI as described in section-I. The LGS block in Fig. 1a can be replaced by the green marked portion of Figs. 1c, 1d and 1e.

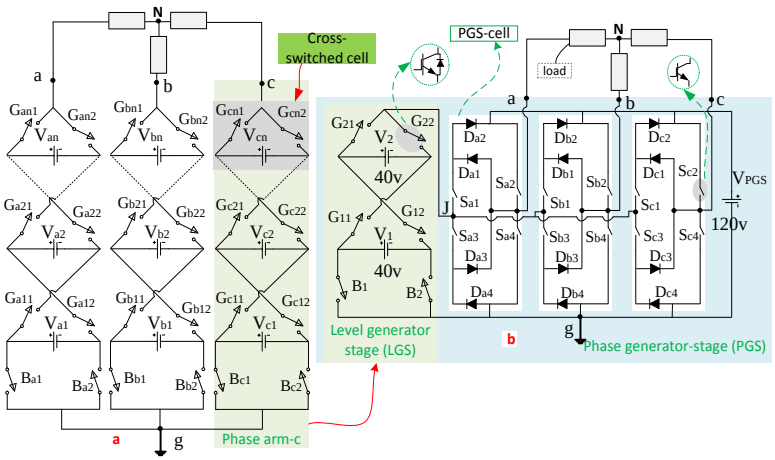

Fig. 2 Three phase CSMLI topology (a) conventional three phase CSMLI topology, (b) proposed in this paper

Fig. 2a shows three-phase conventional cross-switched CMLI and any phase arm of this structure can be utilized as LGS in the proposed new three-phase CMLI [24, 26]. Fig. 2b presents the new three-phase CMLI while the cross-switched structure is considered as LGS. Each cross-switched cell contains two switches (Gn1, Gn2) and a dc –supply, Vn; where n=1, 2, 3,… All the cross-switched cells are connected in series and the cross-switched series is mounted on two fixed base switches (B1, B2). Each pair of the switches in LGS, (Gn1, Gn2) and (B1, B2) always operates in toggle mode. The magnitudes of the cross-switched cells can be either symmetric or asymmetric. For symmetric mode thy can be written as,

$$V_1 = V_2 = V_3 = ... = V_n = V_{dc} \quad (1)$$

While the asymmetric configuration with binary ratio, the magnitudes of the input dc supplies can be expressed as,

$$V_1 = V_{dc}; V_2 = 2^1 V_{dc}; V3 = 2^2 V_{dc}; ....; V_n = 2^{n-1} V_{dc} \quad (2)$$

The other asymmetric methods are proposed in [26], also applicable here.

Both symmetric and asymmetric configurations, the magnitude of the VPGS can be expressed by,

$$V_{PGS} = \sum_{k=1}^{n} V_k + V_1 \quad (3)$$

While the main responsibility of the PGS is to generating the phase angles, PGS also contributes the output pole voltages (V_{ag}, V_{bg}, V_{cg}) by producing the maximum and minimum voltage levels, V_{PGS} and 0; respectively. V_{PGS} is appeared in the pole voltage (V_{xg}) when S_{x2} is turned on and zero (0) is appeared while S_{x4} is turned on. S_{x1} and S_{x3} always turn on together while both S_{x2} and S_{x4} are kept turned off. The voltage levels which are generated by LGS can get access to the pole voltage output while S_{x1}, S_{x3} are kept turned on.

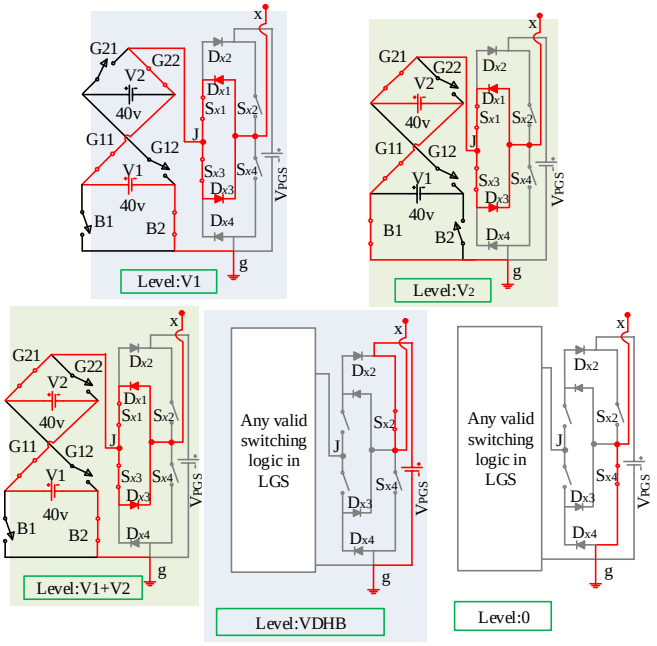

Fig. 3. Different switching mode to generate the possible levels in the pole voltage, Level: (V_1), Level: (V_2), (V_1+ V_2), Level: V_{DHB}, Level: 0

Fig. 3 shows the different output levels generation in the pole voltage (V_{xg}) output while two cross-switched cells are considered in the CSC-stage for simplicity. The levels in the pole voltage (V_{xg}) can be expressed by,

$$V_{xg} = V_{Jg} + V_{PGS} + 0 \quad (4)$$

Where V_{xg} ε (V_{ag}, V_{bg}, V_{cg})

The levels in the unipolar voltage (V_{Jg}) of the level generator output can be demonstrated by

$$V_{Jg} = V_1 + V_2 + ... + V_n \quad (5)$$

The maximum number of levels, N_p in the pole voltage can be calculated from:

$$N_p = \left(\frac{V_{xg,max}}{V_{dc}} \right) + 1 \quad (6)$$

Where x ε (a, b, c) and $V_{xg,\,max}$=V_{PGS}.

The three phase line-line voltage can be obtained from

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} V_{ag} - V_{bg} \\ V_{bg} - V_{cg} \\ V_{cg} - V_{ag} \end{bmatrix} \quad (7)$$

Table 1 Switching states sequence for a complete one cycle of three phase line voltage generation

Switching states *Sa,Sb,Sc*	G11, G12′	G21, G22′	B1, B2′	Sa1, Sa3	Sa2	Sa4	Sb1, Sb3	Sb2	Sb4	Sc1, Sc3	Sc2	Sc4	Vab	Vbc	Vca
300	**1**	**0**	**0**	0	1	0	0	0	1	0	0	1	3	0	-3
310	1	0	0	0	1	0	1	0	0	0	0	1	2	1	-3
320	1	1	0	0	1	0	1	0	0	0	0	1	1	2	-3
330	**1**	**1**	**0**	0	1	0	0	1	0	0	0	1	0	3	-3
230	1	1	0	1	0	0	0	1	0	0	0	1	-1	3	-2
130	1	0	0	1	0	0	0	1	0	0	0	1	-2	3	-1
030	**1**	**0**	**0**	0	0	1	0	1	0	0	0	1	-3	3	0
031	1	0	0	0	0	1	0	1	0	1	0	0	-3	2	1
032	1	1	0	0	0	1	0	1	0	1	0	0	-3	1	2
033	**1**	**1**	**0**	0	0	1	0	1	0	0	1	0	-3	0	3
023	1	1	0	0	0	1	1	0	0	0	1	0	-2	-1	3
013	1	0	0	0	0	1	1	0	0	0	1	0	-1	-2	3
003	**1**	**0**	**0**	0	0	1	0	0	1	0	1	0	0	-3	3
103	1	0	0	1	0	0	0	0	1	0	1	0	1	-3	2
203	1	1	0	1	0	0	0	0	1	0	1	0	2	-3	1
303	**1**	**1**	**0**	0	1	0	0	0	1	0	1	0	3	-3	0
302	1	1	0	0	1	0	0	0	1	1	0	0	3	-2	-1
301	1	0	0	0	1	0	0	0	1	1	0	0	3	-1	-2

III. SIMULATION AND IMPLEMENTATION

Staircase modulation technique is applied as a switching control strategy for the proposed new CMLI [28]. The proposed inverter structure in Fig. 1b, is simulated in Matlab/Simulink while Digital signal processor (DSP), TMS320F2812 is used to achieve the real time switching gate signals. The pole voltages (V_{ag}, V_{bg}, V_{cg}) are considered as reference parameter to obtain the appropriate switching states, S_a, S_b, S_c. The number of switching states (S) directly related with the maximum number of levels (N_p) in the pole voltage (V_{xg}).

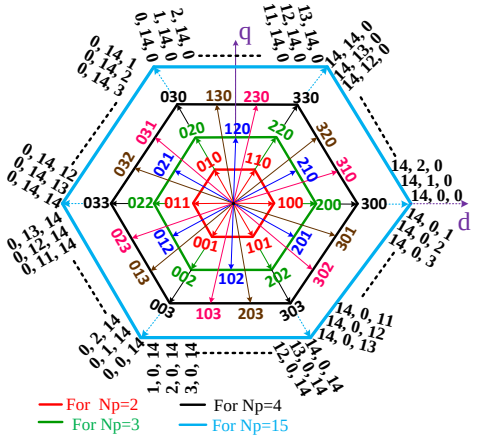

Fig. 4. Generalized switching vectors in d-q complex plane.

The switching states for the different value of N_P can be arranged in Fig. 4 by hexagonal diagram of d-q co-ordinate where each hexagon contains switching states (S) equivalent to $6(N_P\text{-}1)$ and each switching state performs for $0.02/6(N_p\text{-}1)$ second, where 0.02s is obtained from the desired frequency (50 Hz) of the line voltage. While the cascaded stage of the proposed new CMLI in Fig. 1b can be asymmetric, symmetric structure with two cascaded cross-switched cells are considered for simplicity where LG and PG-stage input voltages are set as ($V_1=V_2=V_{dc}=40V$) and $V_{PG}=\sum V_n+V_1=3V_{dc}=120V$, respectively. There would have four levels (0, V_{dc}, $2V_{dc}$, $3V_{dc}$) in the pole voltages (V_{xg}) where $N_p=4$ and hence 18-switching states are required for generating the aforementioned levels in the pole voltages.

The complete switching states are depicted in Table 1 for achieving output of a complete cycle, where the switching logics of the three PG-cells switches (S_{x1}, S_{x2}, S_{x3}, S_{x4}) are alike with 120^0 phase shift among each other and they are responsible to generate phase difference in the output voltages. 12 insulated gate bipolar transistors (IGBTs), IRG4BC40W, 600V/20A along with 12-diodes, RHRP1540, 400V/15A are used to implement the PG-stage while six IGBTs, HGTG20N60B3D, 600V/40A are used to build the LG-stage.

IV. RESULTS AND DISCUSSION

Simulation and experimental results are provided in Fig. 5 and Fig. 6, respectively. In the results, the junction voltage VJg appears two levels (80 V and 40 V), pole voltages (V_{ag}, V_{bg}, V_{cg}) show four levels (120 V, 80 V, 40 V, 0) and line voltages (V_{ab}, V_{bc}, V_{ca}) contain seven levels (±120 V, ±80 V, ±40 V, 0). No filter is utilized while taking the results of the voltages and line currents (I_a, I_b, I_c).

The total harmonic distortion of unfiltered line voltage and line current is shown in Figs. 7e and 7f. Though the line current

THD is less than 5% while the voltage THD is more than IEEE standard [29].

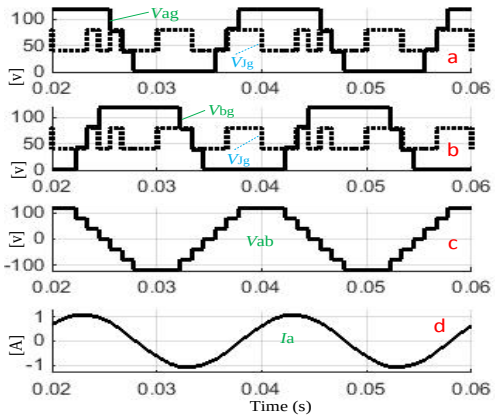

Fig. 5. Simulation results: (a) Intermediate voltage, V_{Jg} and pole voltages, (V_{ag}), (b) Intermediate voltage, V_{Jg} and pole voltages, (V_{bg}), (c) Line voltage, (V_{AB},), (d) The line currents, (I_a)

The voltage THD can be reduced by increasing the number of levels in the line voltage and it can be achieved by adopting asymmetric method or adding more cross-switched cells in the LG-stage. If $V_1=V_{dc}$, $V_2=2V_{dc}$ and $V_{PGS}= 4V_{dc}$, then the same configuration in the Fig. 2b produces 9-levels in the line voltage and THD is found about 9%.

Table 2 Comparison between different single phase, three phase existing CMLI topologies and proposed three phase new MLI concept for generating 15 levels in the line voltage

Topology	Single phase topology [10]		Three phase Cross-switched inverter [24,26]		Three phase Half bridge inverter [22]	
	Existing Single phase	proposed new concept for 3-phase	Existing 3-phase	proposed new concept	Existing 3-phase	proposed new concept
No of switches	16	24	48	28	42	26
No of diodes	16	24	48	28	42	26
No of gate driver	16	24	48	28	42	26
No of dc supplies	7	8	21	8	21	8

V. COMPARISON OF PROPOSED NEW CONCEPT WITH THE CURRENT TOPOLOGIES

The proposed new three phase cascaded MLI topology by employing LG-stage and PG-stage is a generalized configuration, which does not confine only to cross-switched topology but also applicable to any existing CMLI topology without tripling the used components as per the current conventional methods. The proposed new concept reduces the size of the existing topologies without degrading the quality of the output voltage in terms of voltage levels. Table 2 shows a brief comparison among the symmetric structure of the proposed concept and some proposed topologies in the literatures to produce 15-levels in the line-line voltage. Considered topologies used in this comparison include single phase topology proposed in [10], three phase cross-switched inverter proposed in [24, 26], 3-phase Half-bridge topology proposed in [22]. As can be seen in Table 2, the proposed MLI concept reduces the size of the all existing 3-phase cascaded MLI in terms of device count. Also, it can be observed that existing single phase and three phase topologies can be extended to 3-phase structures using the new proposed concept without tripling the hardware components.

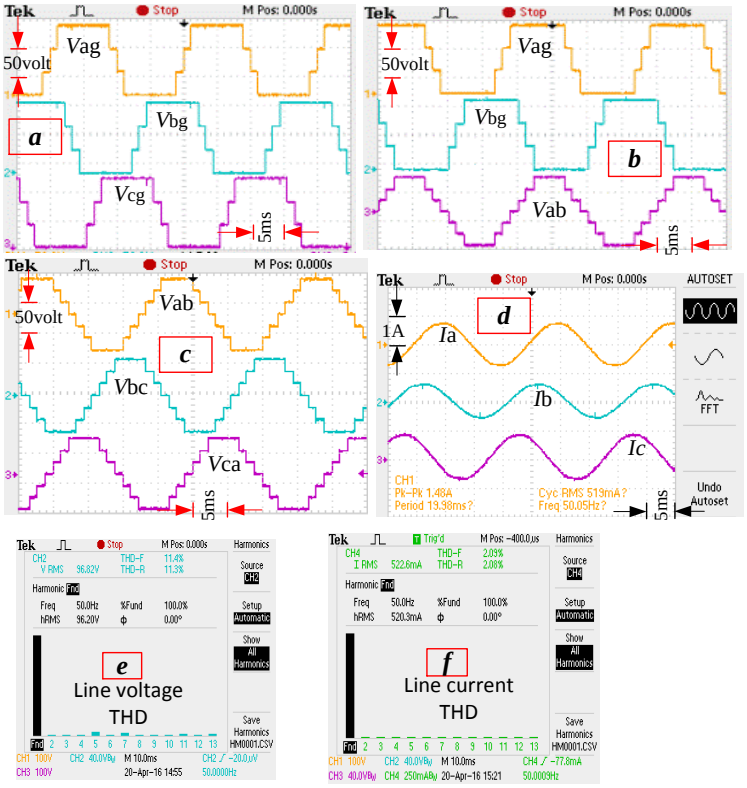

Fig. 6. Simulation results: (a) Intermediate voltage, V_{Jg} and pole voltages, (V_{ag}), (b) Intermediate voltage, V_{Jg} and pole voltages, (V_{bg}), (c) Line voltage, (V_{AB},), (d) The line currents, (I_a), (e) line voltage THD, (f) line current THD

VI. CONCLUSION

This paper introduces a new design and implementation of three-phase CMLI. The experimental results validate the simulation results and the comparison among the several existing topologies show the real time feasibility of the proposed new CMLI concept. As the number of power electronic devices is reduced, hence this technique also minimizes the installation cost and area.

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