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# A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations

Quan Li, *Member, IEEE*, and Peter Wolfs, *Senior Member, IEEE*

**Abstract**—The annual world photovoltaic (PV) cell/module production is growing at almost an exponential rate and has reached 1727 MW in 2005. Building integrated PV (BIPV) projects are emerging as the strongest part of the PV market and grid interactive inverters are a key component in determining the total system cost. Module integrated converter (MIC) technology has become a global trend in grid interactive PV applications and may assist in driving down the balance of system costs to secure an improved total system cost. This paper concentrates on the topology study of the PV MICs in the power range below 500 W and covers most topologies recently proposed for MIC applications. The MIC topologies are classified into three different arrangements based on the dc link configurations. A systematic discussion is also provided at the end of the paper that focuses on the major advantages and disadvantages of each MIC arrangement. These are considered in detail and will provide a useful framework and point of reference for the next generation MIC designs and applications.

**Index Terms**—AC module, module integrated converter (MIC), photovoltaic (PV), single-phase inverter.

## I. INTRODUCTION

GLOBAL demand for electrical energy is constantly growing. Along with the declining production of the dominating energy supplies since the industrial revolution, fossil fuels, there has been a growing interest in exploring renewable energies internationally. Among a variety of the renewable energy sources, photovoltaic (PV) sources have no supply limitations and are predicted to become the biggest contributors to electricity generation among all renewable energy candidates by 2040 [1]. The annual world PV cell/module production between 1988 and 2005 is shown in Fig. 1 and that in 2005 presented a growth of 45% over 2004 [2].

Electronic power inverter is one of the enabling technologies required for utilizing PV energy and its cost is becoming more visible in the total price of the PV system [3], [4]. The price per watt of a crystalline PV module has dropped from \$4.23 US in 1992 to \$1.72 US in 2002 [5]. PV cell costs below \$1 US per watt can be achieved with evolving technologies if the cells are manufactured at a sufficiently large scale [6], [7]. In the world PV market, grid interactive PV is the fastest growing segment and its percentage has increased from 29% in 1992 to

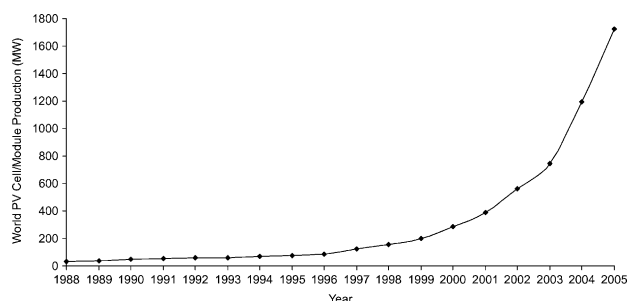


Fig. 1. Annual world PV cell/module production (1988–2005).

83% in 2004 of the total PV capacity installed among the 19 countries participating the International Energy Agency Photovoltaic Power Systems Program, who account for more than three quarters of the global installed PV system capacities [8]. Currently, there are three widely used grid interactive PV systems: the centralized inverter system, the string inverter system and the ac module or the module integrated converter (MIC) system [9]–[11]. Among these, the MIC system offers “plug and play” concept and greatly optimizes the energy yield [4], [12]. With these advantages, the MIC concept has become the trend for the future PV system development but challenges remain in terms of cost, reliability and stability for the grid connection [13]–[17].

The commercial solar energy market has been significantly stimulated by the German Renewable Energy Sources Act, which was approved in 2000 [18]. In addition, globally government subsidized large projects aiming at boosting the solar energy usage have emerged over the last decade including the 70 000 Roof Program launched in Japan in 1996, the One Million Solar Roof Initiative announced in US in 1997, the 100 000 Roof Program started in Germany in 1999, the SOL-1000 Project (1 000 PV roof-tops) launched in Denmark in 2001, the 10 000 Roof Program promoted in Italy in 2001 and the 100 000 Solar Roof Project approved in China in 2005 [19]–[21]. Among these building integrated PV (BIPV) projects, the MIC technology has significantly benefited the project implementations [22]–[27].

A number of single-phase power inverter topologies have been reviewed recently and the interest has been mainly focused on the number of the conversion stages and the design specifications [4], [10]–[12], [26], [28], [29]. This paper concentrates on the topology study of the single-phase PV converters with up to 500-W power rating and attempts to cover a comprehensive set of the MIC topologies proposed in the recent publications.

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The authors are with the Faculty of Sciences, Engineering and Health, Central Queensland University, Rockhampton QLD 4702, Australia (e-mail: q.li@cqu.edu.au; p.wolfs@cqu.edu.au).

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According to the dc link configurations, the proposed MIC topologies can be classified into three different arrangements:

- 1) MIC with a dc link;
- 2) MIC with a pseudo dc link;
- 3) MIC without a dc link.

The reviewed MIC topologies in this paper are based on a range of generic converter topologies including half bridge converter, full bridge converter, push-pull converter, buck boost converter, flyback converter, Cuk converter, Zeta converter, D2 converter and two-inductor boost converter. Finally, the discussion for the three different arrangements is provided thoroughly and the favourable features of each arrangement are clearly identified as a sound foundation for future MIC applications.

## II. POSSIBLE MIC TOPOLOGIES

In order to achieve good system performance, at least four issues must be considered in the MIC design.

1) *Power Density*: The power density is a sole indicator of the compactness of a MIC. One of the highest MIC power densities achieved to date in the prototype design is  $0.6 \text{ W/cm}^3$  for a 110-W converter [24], [25]. The power densities of the commercial MIC inverters are much lower and the goal for the next generation MIC aims at around  $1 \text{ W/cm}^3$  [30].

2) *Efficiency*: A high efficiency is a must in obtaining a compact MIC design. However, compared with large converters, MICs have smaller power ratings and tend to have lower efficiencies [4], [31]. The highest reported MIC efficiency seen, for an isolated design, is 94% achieved by NKF OK4-100 at 40% of the maximum input power [32]. A “future” target of 95% was set in 1998 to further decrease the temperature stress and increase the lifetime of the systems [30]. It is not known if this has been achieved amongst the commercial MICs with isolated designs and less than 500-W power rating although larger PV inverters have achieved efficiencies higher than 98% [33].

3) *Reliability*: Because MICs are mounted on the PV module, it is important that the lifetime of the MIC is comparable to that of the PV module, which lasts more than 20 years [34]. However, inverters are still shown to be the most vulnerable component in PV systems [35]. The MIC reliability can be measured by two indices, i.e., mean time between failures (MTBF) and mean time to first failure (MTFF). Currently a typical figure for MTBF is ten years and that for MTFF is five years [35], [36]. Recently, the second prototype PV2GO inverter has been reported to have an estimated MTBF of about 25 years and an MTFF of ten years has also been proposed for the next generation PV inverters [37], [38].

4) *Balance of System Cost*: Balance of system (BOS) is defined as the parts of the PV system other than the PV array cost and will become increasingly important as the PV module costs drop [39], [40]. The major component of BOS cost in the MIC systems is the cost of the inverters due to the absence of the storage batteries. On the commercial market, OK4-100 has achieved \$1 US per watt-peak and PV2GO has a prediction of 0.5 per watt-peak [32], [37]. The objective of less than \$0.5 US per watt-peak set more than a decade ago has not yet been achieved while more painstaking efforts have to be paid to achieve less than \$0.25 US per watt-peak for larger PV inverters

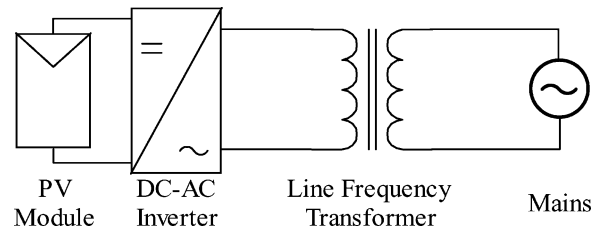


Fig. 2. MIC with a line frequency transformer.

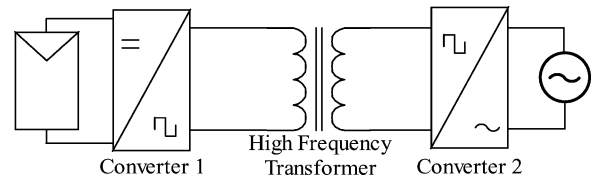


Fig. 3. MIC with a high frequency transformer.

[41], [42]. Although the price of the MICs will still be uncompetitive with that of the central converters with much higher power ratings, the cost of the PV systems with MICs may be not significantly higher than that with the central converters considering the additional cables, the installation cost and the higher cable losses [43]–[45].

Considering the above four issues, different MIC designs have been proposed. In general, as the solar panel most often supplies low level dc voltage to the MIC, it is required that both the voltage amplification and the dc–ac inversion be accomplished in the power conversion process. Generally, an MIC can be implemented with either a line frequency or a high frequency transformer respectively shown in Figs. 2 and 3.

In Fig. 2, the dc–ac inversion is implemented first followed by the voltage amplification through a line frequency transformer. The topologies recently proposed in [46]–[48] and as well as some commercial inverters for MIC applications such as Sun-Sine and Dorfmueller DMI series employ this arrangement [49], [50]. However, a low-power line-frequency transformer is bulky and may not be very efficient [4], [51]. Small line frequency transformers, especially those of a few hundred volt-amperes and below, pose efficiency challenges. Therefore, the topology shown in Fig. 2 is regarded as a poor solution and will not be further discussed in this paper [11], [12].

In Fig. 3, voltage amplification is largely obtained through a high frequency transformer instead and this topology will be the focus of this paper. MICs with high frequency transformers can be classified into three arrangements according to the dc link configurations and these will be discussed in detail in the following sections.

Some important performance parameters of nine commercial ac module inverters with power ratings below 500 W are compared in Table I, [52]–[60].

## III. MIC WITH AC–DC LINK

Fig. 4 shows the MIC implementation with a dc link, where the dc voltage is amplified to a higher level compatible with the ac grid by a dc–dc converter and a dc–ac converter follows. Four topologies have been proposed as shown in Figs. 5–8, [61]–[65].

TABLE I  
COMMERCIAL AC MODULE INVERTERS

Inverter Name	Manufacturer	Transformer Type	Nominal Power (W)	Power Density (W/cm <sup>3</sup> )	Maximum Efficiency
SOLADIN 120	MASTERVOLT	High Frequency	90	0.15	93%
OK4-100	NKF	High Frequency	100	0.30	94%
SUNMASTER 130S	MASTERVOLT	High Frequency	110	0.13	92%
SOLCOLINO	HARDMEIER	Unknown	180	-	91.7%
GRIDFIT 250	EXENDIS	High Frequency	200	0.13	>90%
OK5-LV	NKF	High Frequency	280	0.23	93%
DMI 350/50	DORFMÜLLER	Low Frequency	300	0.09	92.8%
SUNSINE 300	ASCENSIONTECH	Low Frequency	300	0.10	91%
EVO 500	PHILIPS	Unknown	500	0.17	95%

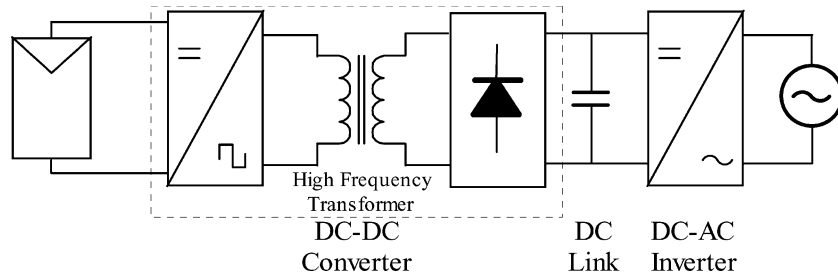


Fig. 4. MIC with a dc link.

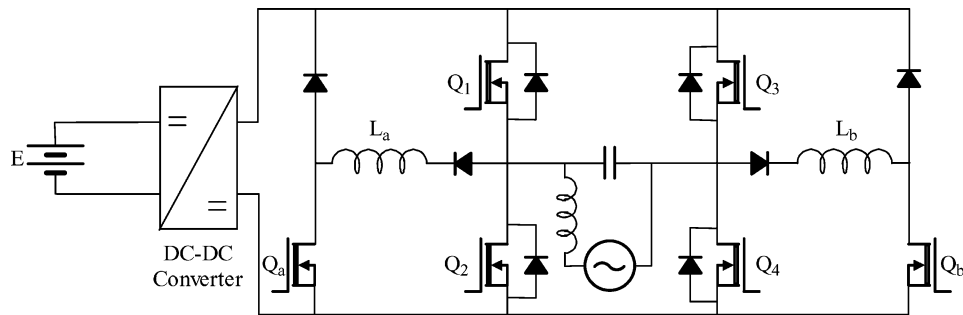


Fig. 5. Topology proposed in [61].

The topology shown in Fig. 5 utilizes a soft-switched dc-ac converter [61]. The detailed dc-dc converter topology is not provided as the improvement is concentrated on the dc-ac conversion stage, where a zero-voltage-transition (ZVT) pulsewidth modulated (PWM) inverter is employed. The soft-switched inverter removes the switching losses which would otherwise be inherent with the conventional hard-switching PWM control.

The topology shown in Fig. 6 employs a series resonant half bridge converter in the dc-dc conversion stage [62]. The dc-ac converter is a modified full bridge inverter, with two additional diodes. The left leg switches operate at high frequencies to control the current injected to the grid while the right leg switches are controlled by the polarity of the grid voltage and switch synchronously with the zero crossings of the grid voltage. This control approach might allow the switching loss in the inverter to be reduced compared with that in the conventional hard-switched PWM inverter. However, this bridge does have less modulation range opportunities. A conventional bridge can achieve frequency doubling by applying phase shifted switching control between the bridge legs.

The inverter in Fig. 7 is a flyback converter as the dc-dc conversion stage cascaded with a current PWM inverter as the dc-ac conversion stage [63], [64].

The topology shown in Fig. 8 employs a ZVS two-inductor boost converter in the dc-dc conversion stage [65]. A conventional PWM converter follows to convert the dc voltage to the grid compatible ac voltage.

Several key parameters of the above MIC systems are summarized in Table II.

Among the four topologies listed in Table II, the converter shown in Fig. 7 has the smallest component count and this could lead to a lower converter cost and greater converter reliability. However, both the dc-dc and the dc-ac conversion stages in Fig. 7 employ the hard-switching solutions, which will make it impossible to maintain high converter efficiencies under high switching frequencies. The converters shown in Figs. 5, 6, and 8 are able to remove the switching losses either in the dc-dc or the dc-ac conversion stages or both by employing the soft-switching technologies. High efficiencies can be obtained but at the cost of higher component counts. The switches in these

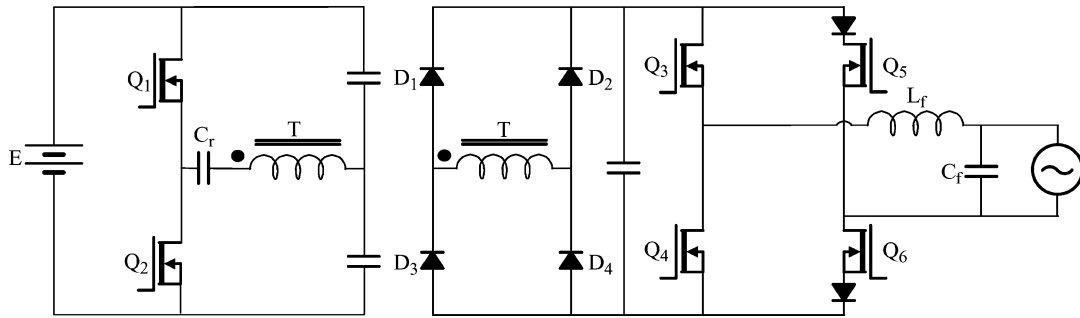


Fig. 6. Topology proposed in [62].

TABLE II  
COMPARISONS OF MIC WITH A DC LINK

MIC	Power Rating (W)	Component Count				Maximum Efficiency	PCB Size (mm × mm)
		Active Switch	Diode	Magnetic Core	Copper Winding		
Fig. 5, [61]	200	>6	>4	>2	>2	96%	100 × 480
Fig. 6, [62]	250	6	6	1	2	-	-
Fig. 7, [63] and [64]	100	5	1	1	2	-	-
Fig. 8, [65]	100	6	4	4	5	90%	-

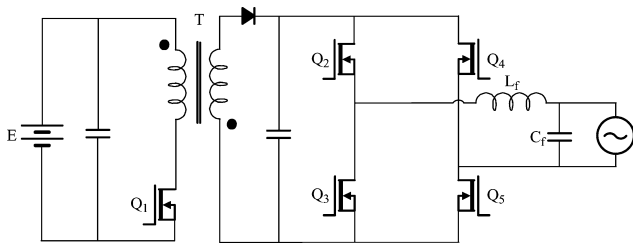


Fig. 7. Topology proposed in [63] and [64].

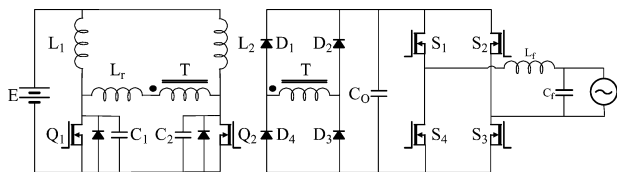


Fig. 8. Topology proposed in [65].

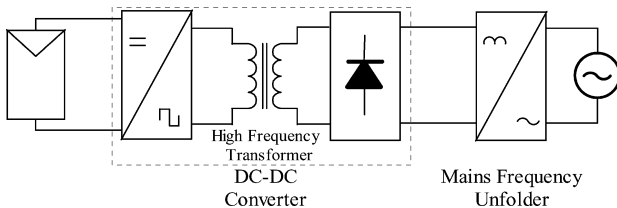


Fig. 9. MIC with a pseudo dc link.

converters also demand higher voltage and current ratings due to the nature of the resonant circuit.

#### IV. MIC WITH A PSEUDO DC LINK

Fig. 9 shows the MIC implementation with a pseudo dc link, where a modulated dc–dc converter or the cascade of a modulated dc–dc converter and a nonmodulated dc–dc converter produces a rectified sinusoidal voltage on the dc link. A grid-commutated dc–ac converter with the square-wave control

unfolds the link voltage to the sinusoidal form in phase with the grid. Thirteen topologies have been proposed as shown in Figs. 10–20, [66]–[82].

The topology shown in Fig. 10 utilizes a boost converter to increase the voltage level [66]. A push-pull converter is then modulated to generate a rectified sinusoidal waveform, which is finally unfolded by a current source inverter (CSI).

The topology shown in Fig. 11 is a current fed push-pull converter, which boosts the voltage level, followed by a modulated buck converter, which produces a rectified sinusoidal waveform [67]. This is finally unfolded by a CSI.

The inverter in Fig. 12 employs a modulated flyback converter to generate a rectified sinusoidal waveform, which is unfolded by the following CSI [68], [69]. This topology is very similar to that shown in Fig. 7 except for the control strategy. The sinusoidal modulation is applied to the operation of the flyback converter in this topology therefore a grid-commutated line frequency unfolders can be utilized.

The inverter in Fig. 13 is a modulated series-parallel resonant full bridge converter with lossless snubbers [70]. This topology is originally based on the topology previously proposed in [71], [109]. A CSI follows to unfold the rectified sinusoidal current produced by the dc–dc conversion stage.

The topology shown in Fig. 14 is based on the cascade of the buck boost and the flyback converters [72], [73]. This topology can be improved as shown in Fig. 15 [74]. In this topology, the energy is transferred to the transformer magnetising inductance through the buck boost switch and then to the intermediate capacitor through the flyback switch. Finally, the energy is transferred to the output grid through the centre-tapped transformer and the two switches. The buck boost switch and the two switches on the transformer secondary side are required to be series connected with the diodes to block the reverse current. Compared with that shown in Fig. 14, the topology shown

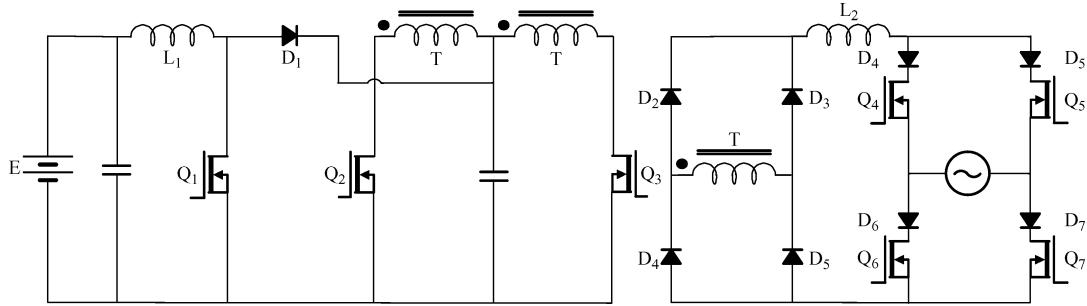


Fig. 10. Topology proposed in [66].

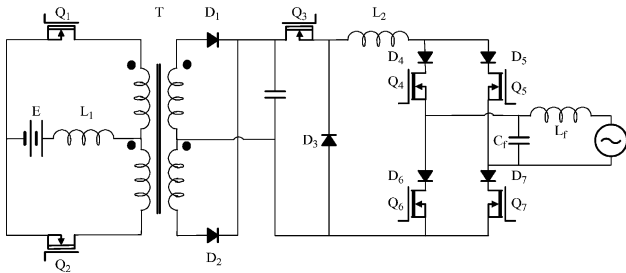


Fig. 11. Topology proposed in [67].

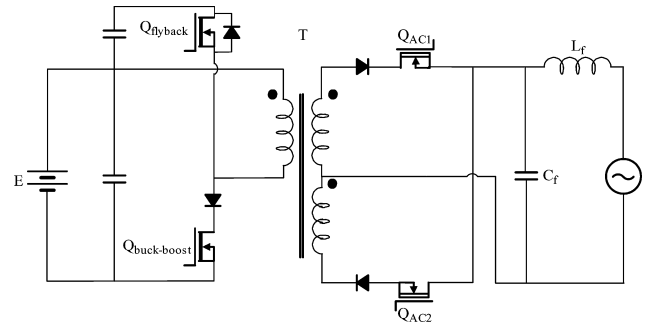


Fig. 14. Topology proposed in [72] and [73].

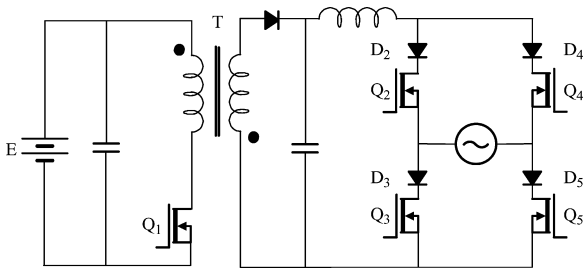


Fig. 12. Topology proposed in [68] and [69].

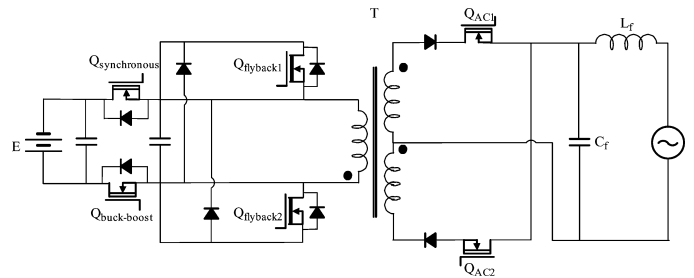


Fig. 15. Topology proposed in [74].

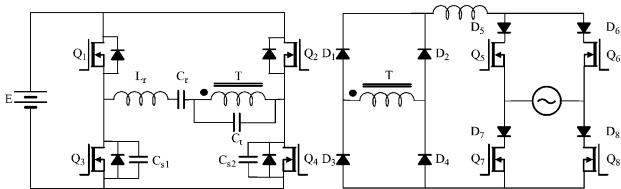


Fig. 13. Topology proposed in [70] and [71].

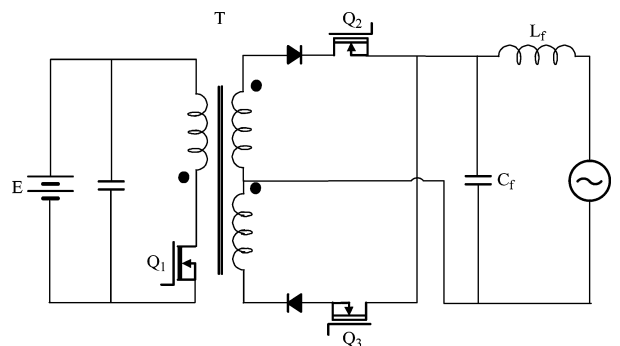


Fig. 16. Topology proposed in [76].

in Fig. 15 offers an important feature in recovering the energy stored in the transformer leakage inductance into the intermediate capacitor. Two variations of the topology shown in Fig. 15 with different power decoupling circuits are also briefly discussed in [75].

The dc–dc conversion stage in Fig. 16 is a modulated flyback converter and this is the same as that in Fig. 12 [76]. However, a centre-tapped transformer is used in this topology to generate the sinusoidal waveforms. A similar topology is also proposed in [77], where the polarities of the dc voltage source and the primary side MOSFET are reversed.

The topology shown in Fig. 17 is also based on the flyback converter with the centre-tapped transformer [78]. In the converter primary side, an auxiliary switch is added to offer ZVT so that the overall switching loss can be reduced.

The topologies shown in Fig. 18(a) and (c) are, respectively, based on a single and two flyback converters and that shown

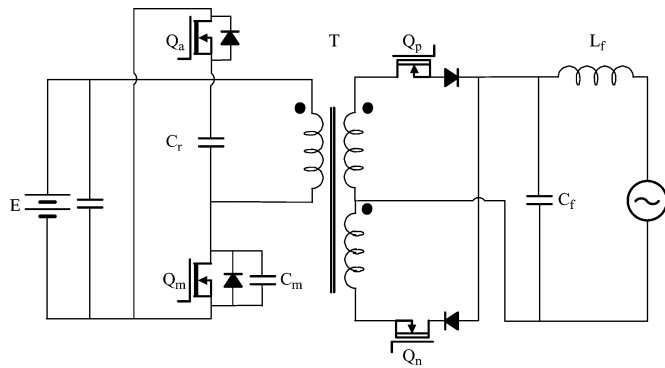


Fig. 17. Topology proposed in [78].

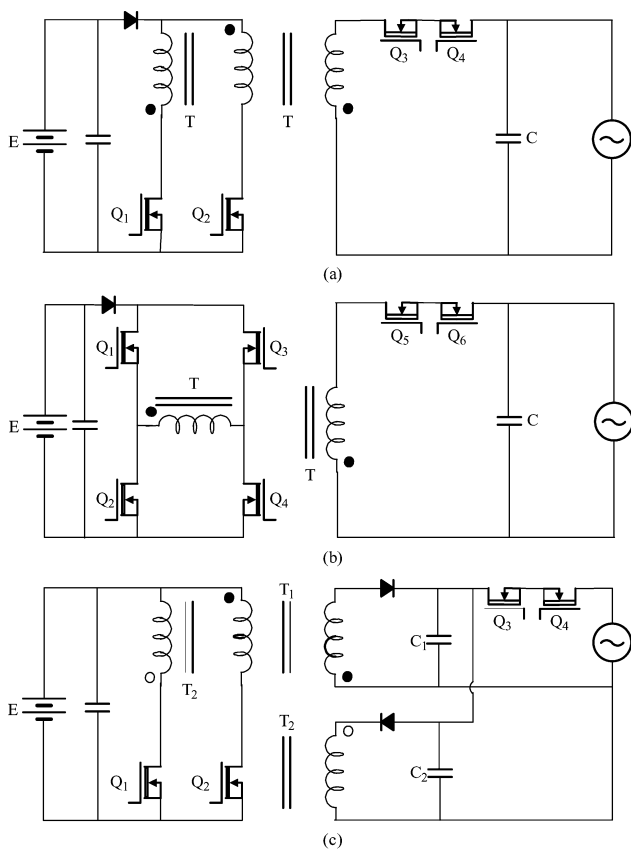


Fig. 18. Topology proposed in [79] (a) Topology based on single flyback converter (b) Topology based on full bridge converter (c) Topology based on two flyback converters.

in Fig. 18(b) is based on a full bridge converter [79]. A bidirectional switch pair is employed on the transformer secondary side and each switch conducts in the positive or the negative half cycle of the grid voltage to produce sinusoidal waveforms.

The topology shown in Fig. 19 employs a highly efficient and sinusoidally modulated two-phase synchronous buck converter cascaded with a two-inductor boost converter to produce a rectified sinusoidal waveform and a voltage unfolding stage follows [80], [81]. Passive nondissipative snubbers are also used

in the converter to partly recover the switching loss in the hard-switched two-inductor boost converter.

The ZVS two-inductor boost topology shown in Fig. 8 can also be employed as part of the dc–dc conversion stage in the MIC design shown in Fig. 19 in order to avoid the switching loss in the two-inductor boost converter under high frequency operations [82], [83]. The topology is shown in Fig. 20.

Several key parameters of the above MIC systems with high frequency transformers are summarized in Table III.

Among the thirteen topologies listed in Table III, the topologies shown in Figs. 12–18 consist of two conversion stages while those shown in Figs. 10, 11, 19, and 20 consist of three conversion stages. In the two-stage MIC implementations, the converter tends to have a smaller size and component count, leading to a lower system cost. In this arrangement, modulation is provided in the front-end dc–dc converter. The topologies shown in Figs. 12 and 13 include a dc–dc conversion stage and a dc–ac unfolding stage. The topologies shown in Figs. 14–17 remove the rectification stage in the dc–dc converter and a centre-tapped transformer replaces the dc–ac unfolder. This arrangement presents an even more simple design however high frequency switching is required on the transformer secondary side. The topologies shown in Fig. 18 have a similar arrangement as those in Figs. 14–17 but employ bidirectional switches to produce sinusoidal waveforms. In the three-stage MIC implementations, two dc–dc conversion stages are cascaded before the unfolding stage. Modulation only applies to one dc–dc converter and this provides an opportunity to optimize the design of the unmodulated dc–dc converter including the size, cost and power loss. It is worth mentioning that at least one step-down stage must be employed in the dc–dc conversion in order to achieve the zero crossing of the demanded sinusoidal waveform.

In the MIC arrangement with a pseudo dc link, if a nonisolated dc–dc converter is employed, high frequency transformer can be removed to offer space and cost saving. Four topologies based on the buck boost converter have been proposed for the multiple-stage inverter as shown in Figs. 21–24, [84]–[87]. In these topologies, the buck boost converter is modulated to generate the rectified sinusoidal current, which is unfolded by the following CSI.

Further size and cost reduction of the MICs can be achieved by the single-stage converter topology. Eight topologies have been proposed as shown in Figs. 25–30, [88]–[99]. These topologies normally consist of two relatively independent converters with possible shared passive components and each converter produces a half cycle sinusoidal waveform 180° out of phase.

The topologies shown in Figs. 25–27 are based on the buck boost converter [88]–[93]. The topologies shown in Fig. 28 are respectively based on the Cuk converter, the Zeta converter and the D2 converter [94]–[97]. The topology shown in Fig. 29 is based on the combination of the Cuk converter and the Zeta converter [98]. The topology shown in Fig. 30 is based on the flyback converter [99].

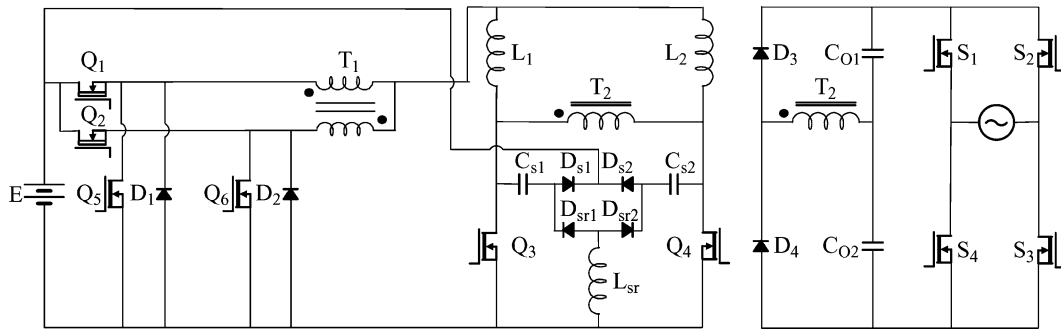


Fig. 19. Topology proposed in [80] and [81].

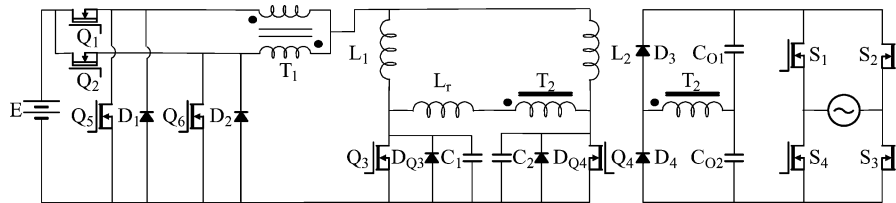


Fig. 20. Topology proposed in [82] and [83].

TABLE III  
COMPARISONS OF MIC WITH A PSEUDO DC LINK

MIC	Power Rating (W)	Minimum Component Count				Maximum Efficiency	PCB Size (mm × mm)
		Active Switch	Diode	Magnetic Core	Copper Winding		
Fig. 10, [66]	350	6	5	3	5	90%	100 × 480
Fig. 11, [67]	300	7	7	3	6	80%	-
Fig. 12, [68]	150	5	1	2	3	-	-
Fig. 13, [70]	60	8	4	3	4	-	-
Fig. 14, [72] and [73]	100	4	3	1	3	70%	140 × 150
Fig. 15, [74]	160	6	4	1	3	86.7%	-
Fig. 16, [76]	100	3	2	1	3	96%	-
[77]	300	3	2	1	3	89%	-
Fig. 17, [78]	70	4	2	1	3	84%	-
Fig. 18(a), [79]	130	4	1	1	3	84.8%	-
Fig. 18(b), [79]	130	6	1	1	2	83%	-
Fig. 18(c), [79]	130	4	2	2	4	84.1%	-
Fig. 19, [80] and [81]	100	10	8	3	7	92%	125 × 200
Fig. 20, [82] and [83]	100	10	4	4	7	91%	125 × 225

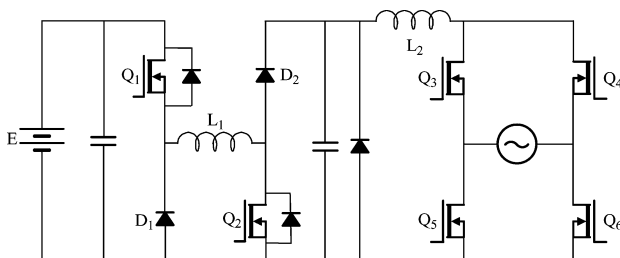


Fig. 21. Topology proposed in [84].

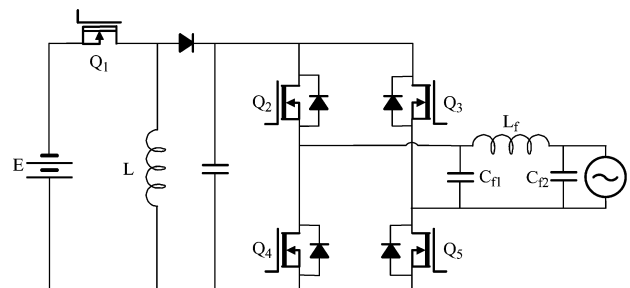


Fig. 22. Topology proposed in [85].

V. MIC WITHOUT A DC LINK

Fig. 31 shows the MIC implementation without a dc link, where the dc voltage is transformed to a high frequency ac voltage and amplified to a higher level compatible with the ac grid. A frequency changer follows and directly translates the ac

voltage or current of the high frequency to that of the grid frequency in the absence of any kinds of the dc links. Three topologies have been proposed as shown in Figs. 32–34, [100]–[102].

In Fig. 32, a VSI transforms the dc voltage to the ac voltage of the high frequency and this is converted to current source



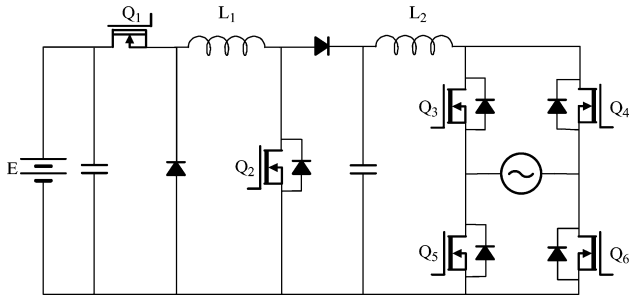


Fig. 23. Topology proposed in [86].

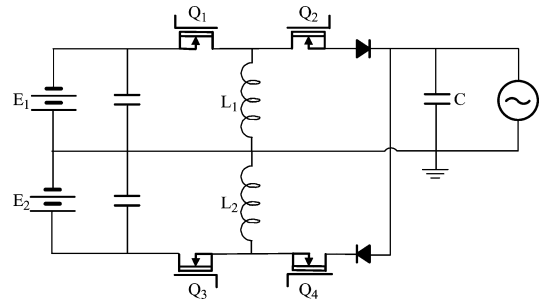


Fig. 27. Topology proposed in [92] and [93].

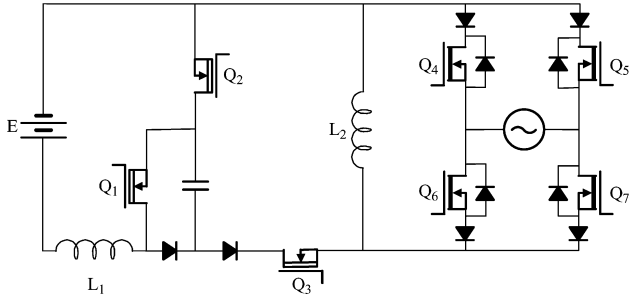


Fig. 24. Topology proposed in [87].

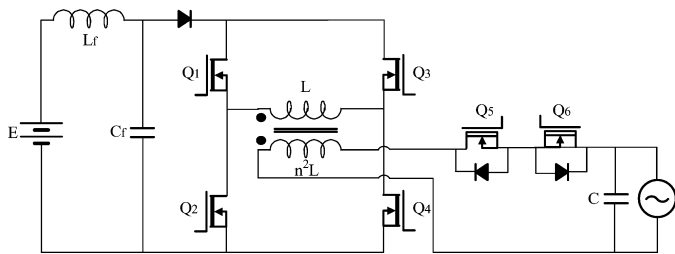


Fig. 25. Topology proposed in [88].

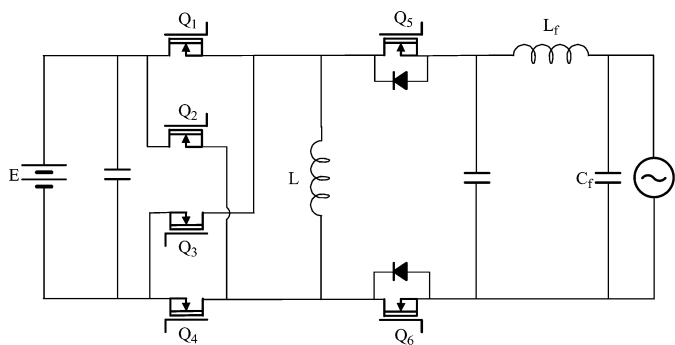
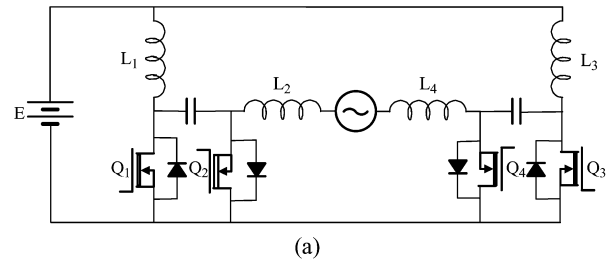


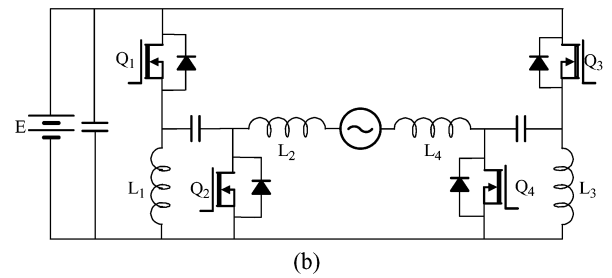
Fig. 26. Topology proposed in [89]–[91].

through an impedance-admittance conversion circuit [100]. Finally, a forced-commutated cycloconverter transforms the current of the high frequency to that of the line frequency.

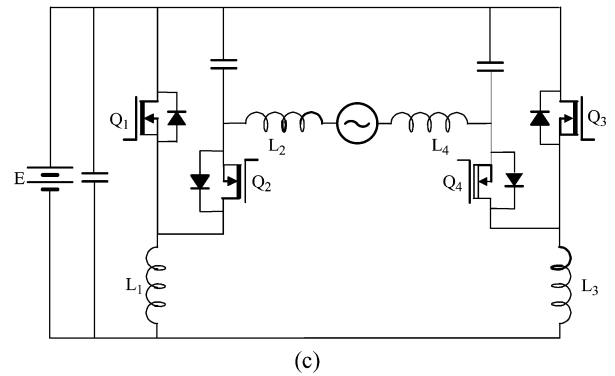
The topology shown in Fig. 33 is a push-pull converter, which transforms the dc voltage to the ac waveform [101]. The high frequency ac voltage is then converted directly to the ac voltage of the grid frequency through a forced-commutated cycloconverter.



(a)



(b)



(c)

Fig. 28. Topology proposed in [94]–[97]. (a) Topology based on Cuk converter. (b) Topology based on Zeta converter. (c) Topology based on D2 converter.

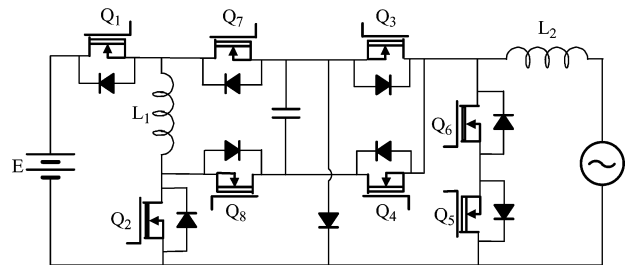


Fig. 29. Topology proposed in [98].

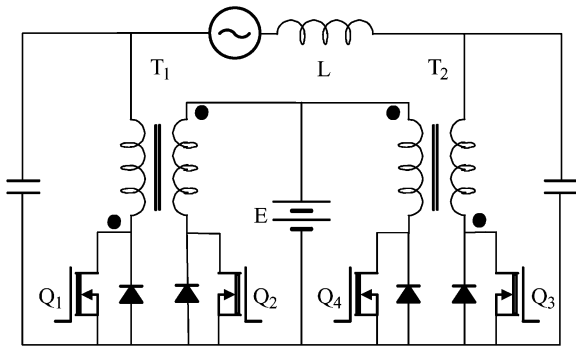


Fig. 30. Topology proposed in [99].

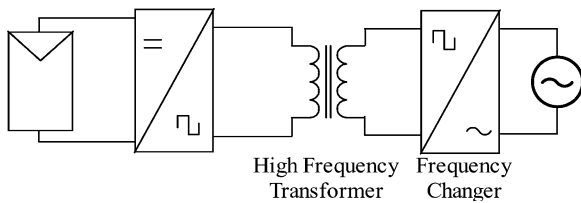


Fig. 31. MIC without a dc link.

The topology shown in Fig. 34 is based on the two-inductor boost converter [102]. The two-inductor boost converter first transforms the dc voltage to the high frequency ac current. A frequency changer made up of three bidirectional switches then converts the ac current of the high frequency to the ac voltage of the grid frequency. Another attractive feature of this converter is the nonpolarised capacitor as a second phase in the load, which provides the power balance and removes the need of the electrolytic capacitor normally required at the converter input to handle the current ripple at twice the line frequency common to the single phase inverter applications. However, a diode is required to be series connected with the primary side MOSFET in the practical implementation as negative drain source voltages exist due to bidirectional power flow.

Several key parameters of the above MIC systems with power ratings less than 500 W are summarized in Table IV.

In the three topologies listed in Table IV, matrix converter technology is employed. As a result, the topology is greatly simplified in this MIC arrangement but this arrangement generally faces both hardware and software challenges—the bidirectional switches and the complicated matrix converter control strategies.

Two other topologies with a frequency changer have been proposed for the PV inverters with power ratings in the kilowatt range and they are shown in Figs. 35 and 36 [103], [104]. They both include two stages—a full bridge inverter followed by a forced-commutated cycloconverter. Theoretically, these topologies can be also applied to the MIC implementations, where the standard power rating is less than 500 W.

## VI. DISCUSSION ON THE MIC TOPOLOGIES

In this paper, MIC topologies are categorised into three different arrangements. This section will discuss the important fea-

tures for the individual arrangements, which will form a useful reference for future applications.

### A. MIC With a DC Link

In the MIC with a dc link, the power conversion process can be easily divided into two separate stages—dc–dc and dc–ac conversions. In this case, the dc–dc converter may be controlled to track the maximum power point of the PV module and the dc–ac converter may be controlled to produce ac power of the unity power factor [4], [105]. However, two major drawbacks do exist in this arrangement.

- 1) The dc–ac converter generally requires PWM control in order to meet the harmonic requirements by the grid however this control technique is relatively complex to implement. The control circuitry can be greatly simplified by the modern microcontroller technology but complications do exist in the gate driver design in order to produce fast turn-on and turn-off transients under high frequencies.
- 2) If only the hard-switching topologies are used, the switching loss tends to be high as the semiconductors in both conversion stages switch under high frequencies. Power loss in the gate driving circuit can also be significant with the conventional totem-pole arrangement and this will further deteriorate the converter overall efficiency.

To minimize the drawback of this arrangement, soft-switching technique can be utilized in both conversion stages. However, the tradeoff could be a higher component count therefore a higher cost and a lower reliability.

Like other single phase converters, the MICs have the inherent power balance issue and require an energy storage element, more often an electrolytic capacitor, to deal with the 100-Hz power ripple.

In this first MIC arrangement, the power balancing capacitor is preferably to be placed at the dc link. As the dc link voltage is of the grid level, the energy stored by the capacitor per unit volume is high and this assists in achieving an overall compact design.

### B. MIC With a Pseudo DC Link

Amongst the three possible MIC arrangements, the MIC with a pseudo dc link has received the greatest interest and a large number of the reviewed topologies employ this arrangement. In the multiple-stage inverters, other than the simple controller design as in the MIC with a dc link, the major advantage is that the dc–ac conversion stage operates at the line frequency. Simple square-wave control can be employed and high switching losses can be avoided even with the hard-switched design. However, more challenging control techniques may be required in the dc–dc conversion stage due to the modulation need.

It is worth mentioning that many transformerless or even single-stage inverters have been proposed under this arrangement. Although they are more compact and efficient due to a smaller component count and lower power loss [106], these topologies do suffer from the following drawbacks.

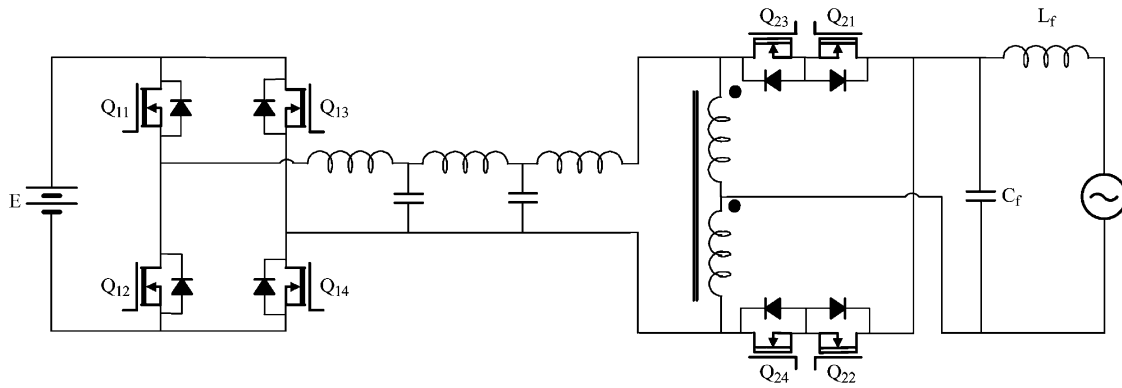


Fig. 32. Topology proposed in [100].

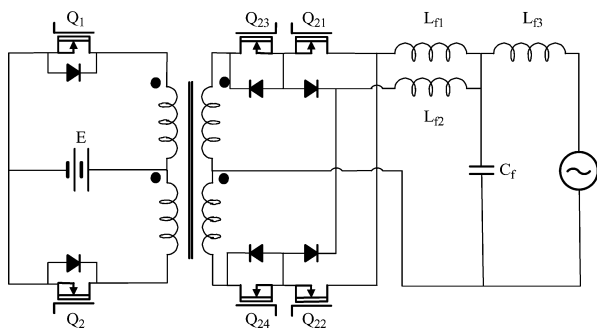


Fig. 33. Topology proposed in [101].

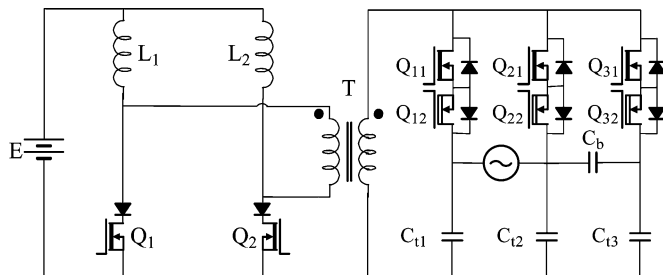


Fig. 34. Topology proposed in [102].

- 1) The transformerless inverters have limited ac peak voltages that are less than dc bus voltages.
- 2) The dual grounding becomes a difficult issue in the transformerless inverters [4].
- 3) The dc voltage range in single-stage inverters is more limited than that in multiple-stage inverters [107].

In this MIC arrangement, the power balancing capacitor is normally placed at the converter input as the dc link needs to provide a wide voltage control range and be free of any large capacitors. Compared with the capacitive energy storage at the dc link, this solution has an obvious disadvantage of lower energy storage per unit volume.

### C. MIC Without a DC Link

The third MIC arrangement completely removes the dc link in the power conversion process. The major advantage of the frequency-changer-based MIC is the reduction of the total power

conversion stages to two. With the current technology, the construction of the bidirectional switches remains a challenge and this greatly hinders the development of the MIC topologies with frequency changers. However, this arrangement does open the possibility of lower component count and higher overall efficiency along with the technology advancement. An obvious tradeoff in this arrangement is the requirement of more sophisticated and higher bandwidth controls as no intermediate energy storage stage is present and the power conversion can no longer be identified as independent dc–dc and dc–ac conversion stages.

In this MIC arrangement, the power balancing capacitor normally needs to be placed at the converter input as no intermediate dc link is available. Some improvement can be made if a second phase output can be provided in addition to the load as shown in Fig. 34. In this case the second independently controlled phase adjusts the capacitor voltage to cancel the 100-Hz power ripple. As the capacitor experiences an ac voltage, the capacitor can be easily implemented by a small nonpolarized capacitor and the volume and the lifetime issues of the large electrolytic capacitors can be avoided. The obvious advantage is that the MTBF and the lifetime of the inverter can be significantly extended [108].

### D. Summary

The main features of the three MIC arrangements are compared in Table V.

The authors hold strong beliefs that the third MIC topology where no dc link exists may become the trend for the development of the next generation MIC with the recent upswing of the research interest in matrix converters and a better semiconductor technology.

Finally, a commercial inverter which has a dc input of 110 V, an ac output of 240 V and a power rating of 300 W has been studied in the laboratory to illustrate the waveforms at different power stages. The circuit diagram of the inverter is shown in Fig. 37 and it is classified as the one with a dc link. The inverter employs the isolated hard-switched full bridge dc–dc converter to produce a higher dc voltage on the dc bus and then a PWM inverter to generate the sinusoidal waveform. The voltage waveforms at power conversion different stages are shown in Figs. 37

TABLE IV  
COMPARISONS OF MIC WITHOUT A DC LINK

MIC	Power Rating (W)	Minimum Component Count			
		Active Switch	Diode	Magnetic Core	Copper Winding
Fig. 32, [100]	30	8	0	4	5
Fig. 33, [101]	300	6	0	1	4
Fig. 34, [102]	100	8	2	1	2

TABLE V  
COMPARISONS OF THREE MIC ARRANGMENTS

DC Link		Yes	Pseudo	No
Control Strategy	DC-DC Conversion	Fixed duty ratio control	Duty ratio modulation control	Matrix converter control
	DC-AC Conversion	PWM control	Square wave control	
Major Advantages		Independent control for two separate conversion stages	Independent control for two separate conversion stages, low power loss in dc-ac conversion stages	Potentially small component count and converter size
Major Challenges		High power loss in dc-ac conversion stage	DC-DC converter modulation control	Bidirectional switch, matrix converter control
Power Balancing Capacitor	Location	DC link	Converter input	Converter input or output
	Type	Electrolytic	Electrolytic	Electrolytic or non-polarized
	Power Density	Medium	Small	Small (electrolytic), high (non-polarized)

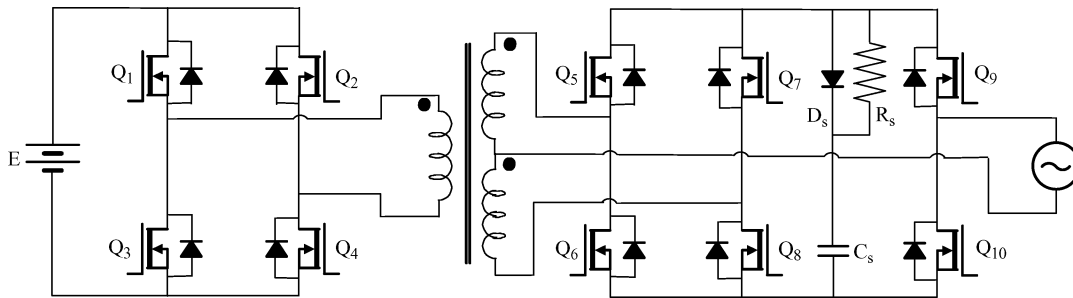


Fig. 35. Topology proposed in [103].

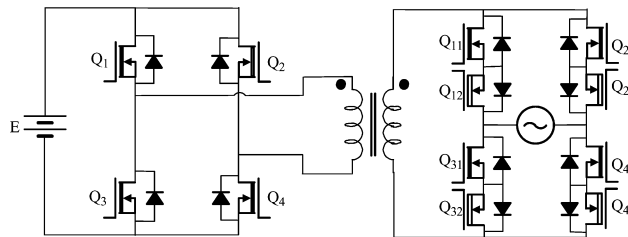


Fig. 36. Topology proposed in [104].

and 38. From top to bottom, Fig. 37, respectively, shows the waveforms of the MOSFETs  $Q_2$  and  $Q_4$  gate voltages and the transformer secondary winding voltage. From top to bottom, Fig. 38 respectively show the waveforms of the dc bus voltage, the inverter output voltages before and after the filter. It can be seen that the hard-switched full bridge converter is operating at 25-kHz switching frequency and produces an average dc bus voltage of 370 V with around 20-V peak to peak voltage oscillations. A 10-kHz PWM control is applied to the dc-ac conversion stage to produce the high frequency modulated waveform. A lowpass filter is then employed to remove the harmonics and generate the line frequency sinusoidal voltage.

## VII. CONCLUSION

PV energy is one of the favourable renewable energy resources for the mankind and MIC has been proved to be one of the important enabling technologies in PV utilization. A variety of topologies which have been proposed in the recent publications for the MICs with ratings up to 500 W are reviewed in this paper. Different MIC topologies are categorised into three arrangements based on the dc link configurations. Finally, the important advantages and disadvantages of the individual MIC arrangements are also discussed in detail. Among three different MIC arrangements, the MIC with a line frequency dc-ac converter currently seems to be the best topology and

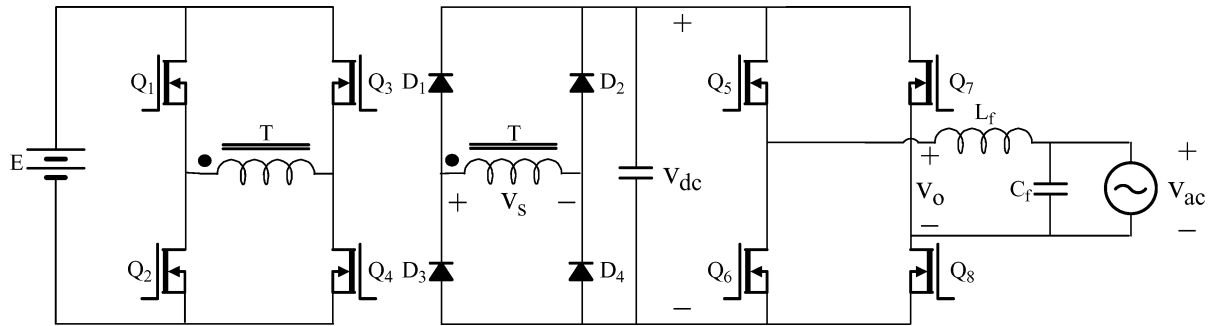


Fig. 37. Circuit diagram of the commercial inverter.

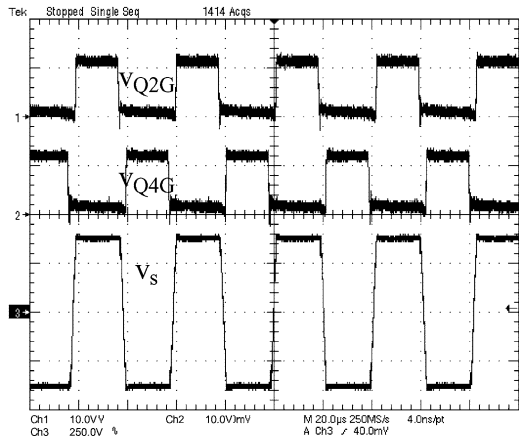


Fig. 38. High-frequency bridge gate and transformer secondary voltage waveforms for the commercial inverter.

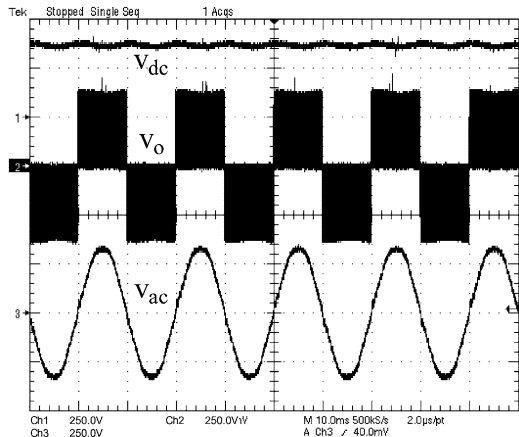


Fig. 39. DC bus, inverter output, and filtered output voltage waveforms for the commercial inverter.

the frequency-changer-based MIC may be a better candidate for the next generation MIC designs. The thorough discussion of the MIC topologies will form a clear guideline and a useful foundation for future MIC development considerations.

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**Quan Li** (M'06) received the B.Eng. degree in electrical engineering from Tsinghua University, Beijing, China, in 1997, and the M.Eng. and Ph.D. degrees from Central Queensland University, Rockhampton, Australia, in 2002 and 2006, respectively.

He is currently a Research Officer at the Faculty of Sciences, Engineering and Health, Central Queensland University, Rockhampton, Australia. His research interests include dc-dc conversion, high-frequency converters, magnetic designs, and renewable energy applications.

Dr. Li is a member of the Institution of Engineers Australia.



**Peter Wolfs** (M'80–SM'99) was born in Rockhampton, Australia, in 1959. He received the B.Eng. degree from the Capricornia Institute of Advanced Education, Rockhampton, in 1980, the M.Eng. degree from the Philips International Institute, Eindhoven, The Netherlands, in 1981, and the Ph.D. degree from the University of Queensland, Australia, in 1992.

He is the Associate Dean (Research) at the Faculty of Sciences, Engineering and Health at Central Queensland University, Rockhampton, Australia. His

special fields of interest include rural and renewable energy supply, electric, solar and hybrid electric vehicles and intelligent systems applications in railways.

Prof. Wolfs is a Fellow of Engineers Australia, a Registered Professional Engineer in the State of Queensland, and a member of the Railway Technical Society of Australia.