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Power Sharing and Management in a Utility Connected DC Microgrid

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***Abstract*— This paper introduces a control technique for proportional load sharing in a DC microgrid during both islanded and utility connected modes. The DC microgrid is connected to a utility system through an interlinking voltage source converter and a unidirectional DC-DC converter. The DC-DC converter draws the desired amount of power from the utility, while the interlinking converter holds the DC bus voltage. The DERs in the DC microgrid are operated under droop sharing using DC-DC converters. Each DC-DC converter is equipped with a state feedback with integral controller that can regulate its output voltage for a wide range of input voltage fluctuation and load variation. Simulation studies are conducted on PSCAD/EMTDC to validate the proposal.**

***Index Terms*—DC microgrid, VSC, state feedback, integral control, DC-DC converter.**

I. INTRODUCTION

MANY of the loads in low voltage, such as computers, efficient lighting systems, battery chargers etc., use DC power. Thus these devices require AC-DC conversion stages. This has led to a renewed worldwide interests in DC distribution systems, especially in DC microgrids. A microgrid is cluster of distributed generators (DGs) and loads [1]. It can be operated in either grid-tied or islanded modes. The grid tied mode is also as vital as the islanded mode for bringing resilience in the electricity network. In the grid connected mode, usually DGs and batteries in a MG supply pre-specified amount of power up-to their capacity and the extra demand can be supplied by the utility, if possible. Also, it is important to achieve flexibility in the microgrid operation so that the DGs, irrespective of their power ratings, can be easily connected to or disconnected from the system [2].

A DC microgrid consists of DC sources and loads and it is connected with the utility through an interlinking converter (IC) [3]. Usually droop characteristic is employed in DC microgrids that regulates the DG output voltage depending on current or power [4], [5]. Several ways to improve current sharing accuracy is explored in [6-8], while [9] proposes a proportional droop index (PDI) controller. For autonomous and independent operation of DC microgrid, it is required to establish a well-designed control system which can provide back up from the utility at any instance, while allowing proportional load sharing amongst the DGs.

There are many control methods for operating DC-DC converters such as LQR, genetic algorithm, Tabu search etc. [10-18]. However a simpler method has been employed in this paper. Even though it is a perturbation based method [19], it is still very robust and tolerates a wide variation in the input voltage and loads. A state feedback controller with integral control is designed that forces the output error to zero asymptotically.

The rest of the paper is organized as follows: Section II presents the system structure, interlinking VSC structure and control and DC microgrid droop control. Section III presents the DC-DC converter modeling and control. Simulation studies perform in PSCAD are presented in Section IV and the paper concludes in Section V.

II. SYSTEM STRUCTURE

The system structure considered in this study is shown in Fig. 1 (a). The DC microgrid (DCMG) is connected to the utility through an interlinking converter (IC) and a DC-DC power flow controller (PFC). On the AC side of the IC a LC filter (L_f and C_f) is used to bypass high frequency switching harmonics. The IC is essentially a voltage source converter (VSC) and it holds the DC capacitor voltage V_{dc1} across C_{dc1} to a constant magnitude. For this study a buck converter has been used as PFC. Given that V_{dc1} is constant, the PFC modulates the voltage V_{dc2} across C_{dc2} to facilitate power flow to the DCMG from the utility in a controlled manner.

The DCMG structure, shown in Fig. 1 (b), contains two boost converters and a buck converter. The boost converters are connected with the two DGs to step up the voltage to a distribution level, while the buck converter steps down the voltage for supplying power to the DC loads. All these DC-DC converters are designed in a way such that it can hold the desired output voltage even during the disturbances in the DGs. The resistances R_1 and R_2 are the line resistances, while the inductors are damping inductors. The PFC is connected to the DC distribution line through a resistor R_3 and the power flow from the AC utility is denoted by $P_{link.}$ The power flow from DG_1 and DG_2 respectively are P_{DC1} and P_{DC2}.

A. Interlinking Converter

The schematic diagram of the interlinking converter is shown in Fig. 2, where a storage capacitor (C_{dc}) is connected

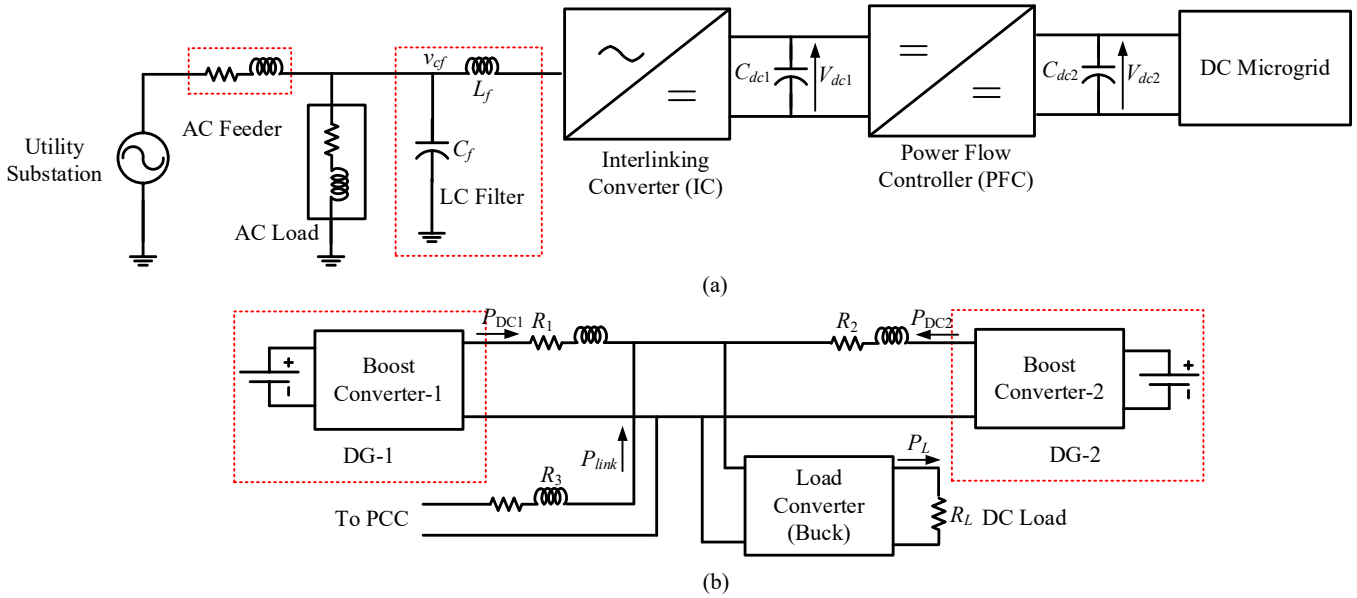

Fig. 1. a) The overall system structure and (b) the structure of the DC microgrid.

to hold the input voltage of the PFC to a constant. The resistance R_f represents the converter losses. The IC is connected to the utility feeder through a transformer. Each phase of the VSC is controlled individually with a state feedback controller and the switching signals are generated using PWM. Let the reference voltage for phase-*a* be given by

$$v_{pa}^{*} = |V|\sin(2\pi f t + \delta) \tag{1}$$

where $|V|$ is a pre-specified voltage magnitude and δ is the desired angle. The references for the other two phases are obtained by phase shifting the above waveform by 120°. The angle δ in (1) should be chosen such that the sum of the power required by the DCMG and converter losses should flow from the utility through the PCC. This can only be achieved if the dc capacitor voltage is held constant. From this logic, the following proportional plus integral (PI) controller is used.

$$\delta = K_{P\delta}\left(V_{dc}^{*} - \langle V_{dc}(t)\rangle\right) + K_{I\delta}\int\left(V_{dc}^{*} - \langle V_{dc}(t)\rangle\right)dt \tag{2}$$

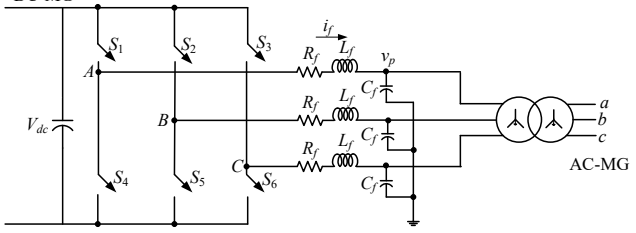

Fig. 2. Schematic diagram of the interlinking converter.

A discrete-time linear quadratic regulator is employed to generate the control input u_c. For generating the switching signal, a triangular carrier waveform (v_{tri}) which varies from – 1 to + 1 with a duty ratio of 0.5 is used. The control output u_c is sampled twice in each cycle of the carrier waveform and is held by a zero-order hold (ZOH). The switching signal for phase-a is generated by the crossing of the carrier waveform and the control signal as

$$\begin{aligned} &u_c(k) > v_{tri}(k), \text{ turn } S_1 \text{ is ON and } S_4 \text{ is OFF} \\ &u_c(k) \le v_{tri}(k), \text{ turn } S_4 \text{ is ON and } S_1 \text{ is OFF} \end{aligned} \tag{3}$$

Similar logic is used for the other two phases as well.

B. Droop Control for DCMG

The two DGs in the DCMG are controlled by droop equations, given by

$$\begin{aligned} V_1 &= V_{ref} - n_1 P_{DC1} \\ V_2 &= V_{ref} - n_2 P_{DC2} \end{aligned} \tag{4}$$

where n_1 and n_2 are the droop gains of DG-1 and DG-2 respectively. However, a microgrid, in an islanded mode, will only be able to supply up to its maximum capacity. Based on this, the droop gains are calculated in such a way that that the DGs share power according to their ratings.

Let us consider DG-1 first. It has a maximum rating of P_{1max}. The droop gains are so chosen that the maximum voltage drop along the DC feeder is restricted. Let us assume that the maximum voltage drop for each DG is ΔV_{max}. Noting that the maximum voltage drop occurs when the DG is supplying its maximum power, we get from (4)

$$\Delta V_{\max} = n_1 \times P_{1\max} \tag{5}$$

Therefore the droop gain is calculated as

$$n_1 = \frac{\Delta V_{\max}}{P_{1\max}} \tag{6}$$

In a similar way, the droop gain of DG-2 is calculated as

$$n_2 = \frac{\Delta V_{\max}}{P_{2\max}} \tag{7}$$

Therefore ΔV_{max} is the product of the droop gain and maximum power of each DG, i.e.,

$$\begin{aligned}&\Delta V_{\max} = n_1 \times P_{1\max} = n_2 \times P_{2\max} \\ &\Rightarrow P_{1\max} \big/ P_{2\max} = n_2 \big/ n_1\end{aligned} \tag{8}$$

This implies that for the DGs to share power according to their ratings, the droop gains must be reciprocal to their ratings.

III. DC-DC CONVERTER CONTROL

The DCMG and PFC contains either buck or boost converters. Their control laws can be constructed in a similar fashion. In this section, the control law of only the buck converter is explained. The schematic diagram of a buck converter is shown in Fig. 3 (a). It contains a switch *S* that is periodically switched on and off in a duty ratio control, a diode, which allows the current to flow in only one direction, and three passive elements. The converter is said to be in continuous conduction mode (CCM) if the inductor current does not need to be blocked by the diode; otherwise it is said to be in discontinuous conduction mode (DCM). We shall design the controller assuming only CCM mode of operation.

A. Buck Converter Model

If the switching frequency converter is *f*, then the time period between two successive switching is $T = 1/f$. The switch *S* is periodically turned on and off as shown in Fig. 3 (b). We then define the following

$$t_2 - t_0 = T, \quad t_1 - t_0 = DT, \quad t_2 - t_1 = (1-D)T \tag{9}$$

where D, $0 \le D \le 1$, is called the duty ratio.

The equivalent circuit when the switch is closed is shown in Fig. 3 (c) and when the switch is open is shown in Fig. 3 (d). Let us the state vector as $x = [V_0 \;\; i_L]^T$. Then the state space equation when the switch is closed is

$$\dot{x} = A_1 x + B_1 V_{dc} \tag{10}$$

and when the switch is open is

$$\dot{x} = A_1 x \tag{11}$$

where

$$A_1 = \begin{bmatrix} -1/RC & 1/C \\ -1/L & 0 \end{bmatrix}, \; B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix}$$

The output equation for both these cases is given by

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} x = Cx \tag{12}$$

Since V_{dc} is constant, using the relations (9), the solution of the state equations (10) and (11) are given by

$$\begin{aligned} x(t_1) &= e^{A_1 DT} x(t_0) + \left\{ \int_0^{DT} e^{A_1 (DT-\tau)} d\tau \right\} B_1 V_{dc} \\ &= e^{A_1 DT} x(t_0) - A_1^{-1} \left(I - e^{A_1 DT} \right) B_1 V_{dc} \end{aligned} \tag{13}$$

$$x(t_2) = e^{A_1 (1-D)T} x(t_1) \tag{14}$$

Substituting (13) in (14), we get

$$x(t_2) = e^{A_1 (1-D)T} e^{A_1 DT} x(t_0) - e^{A_1 (1-D)T} A_1^{-1} \left[I - e^{A_1 DT} \right] B_1 V_{dc} \tag{15}$$

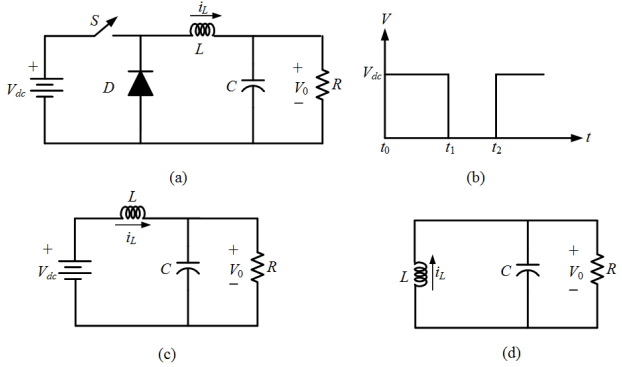

Fig. 3. (a) Schematic diagram of a buck converter; (b) its switching sequence; equivalent circuit when the switch (c) is closed and (d) is open.

B. Linearized model

In this section, we shall derive a linearized model that relates two successive swathing instants, i.e., t_0 and t_2. For linearization, we define the following state and input variables

$$x = x_0 + \Delta x, \quad D = D_o + \Delta D \tag{16}$$

where the subscript '0' denotes the steady state values around which the linearization takes place and Δ denotes its perturbation. In the steady state, the values of the state variables remain the same at the end of each switching cycle, i.e., $x(t_2) = x(t_0)$. Linearizing (15) with respect to x and D, we get

$$\Delta x(t_2) = F \Delta x(t_0) + G \Delta D(t_0) \tag{17}$$

where

$$F = e^{A_1 T}$$

$$G = A_1 T e^{A_1 (1-D_0)T} A_1^{-1} \left[I - e^{A_1 D_0 T} \right] B_1 V_{dc} + e^{A_1 (1-D_0)T} e^{A_1 D_0 T} B_1 V_{dc}$$

Defining switching instant t_2 as $k + 1$ and instant t_0 as k, we can write (18) as

$$\Delta x(k+1) = F \Delta x(k) + G \Delta D(k) \tag{18}$$

The output equation is obtained from (12) as

$$\Delta y(k) = C \Delta x(k) \tag{19}$$

C. State Feedback with Integral Control

For the control of the buck converter, a state feedback with an integral control action is proposed. The discrete-time equivalent of the integral controller is given by

$$\begin{aligned} e(k) &= \Delta y(k) - \Delta y_{ref}(k) \\ z(k) &= z(k-1) + K_I e(k) \end{aligned} \tag{20}$$

where y_{ref} is the reference voltage. Substituting (19) into (20), we get

$$z(k+1) = z(k) + K_I C\Delta x(k) - K_I \Delta y_{ref}(k) \quad (21)$$

An extended state vector is now defined as

$$x_e = \begin{bmatrix} \Delta x \\ z \end{bmatrix}$$

Then from (18) and (21), the extended state space description of the system can be written as

$$x_e(k+1) = \begin{bmatrix} F & 0 \\ K_I C & 1 \end{bmatrix} x_e(k) + \begin{bmatrix} G \\ 0 \end{bmatrix} \Delta D(k) - \begin{bmatrix} 0 \\ K_I \end{bmatrix} \Delta y_{ref}(k) \quad (22)$$

A state feedback controller is then designed that is of the form

$$\Delta D(k) = -K x_e(k) \quad (23)$$

which will force the output error $e(k)$ to zero asymptotically. The gain matrix K is obtained using a discrete-time linear quadratic regulator.

D. PFC Operation

The circuit diagram of Fig. 1 contains 4 DC-DC converters, all of which control their output voltages as per (23). The boost converters track the voltages obtained from the droop equation (4). The load buck converter holds the load voltage constant irrespective of its input voltage or load. The power flow controller (PFC) has to regulate the voltage V_{dc2} across this capacitor C_{dc2}. Therefore it needs a reference voltage V_{dc2}^* that it needs to track. There are two modes of operation. In one mode, the power flow from the utility side is predefined (it can be zero as well). In the second mode, the entire power has to come from the utility when both the DGs are down. The voltage reference generation scheme for the PFC is shown in Fig. 4.

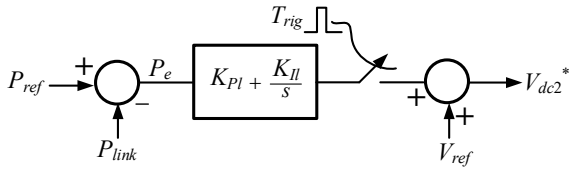

Fig. 4. PFC output voltage reference generation scheme.

The reference of the power that needs to flow through the link is denoted by P_{ref}. This is then compared with the power though the link. The error is passed through a PI controller. The output of the PI controller is added with DC voltage reference of the DCMG to obtain V_{dc2}^* as

$$P_e = P_{ref} - P_{link}$$
$$V_{dc2}^* = V_{ref} + K_{Pl} P_e + K_{Il} \int P_e \, dt \quad \text{.....(24)}$$

When both the DGs are down, a signal T_{rig} is generated. Then the PI controller is bypassed and the PFC hold the DC voltage to V_{ref}. The power required by the load then flows from the utility side.

IV. Simulation Studies

In this section at first the performance of the buck converter with the proposed control algorithm is presented. Followed by this, three case studies for the microgrid operation are presented. The system parameters used in these studies are listed in Table I.

TABLE I: System Parameters

Quantities		Parameters
AC side	Operating frequency Voltage L-L RMS	50Hz 11kV
DC side	DG-1 rating DG-1 rating Voltage reference (V_{ref}) Maximum voltage deviation Droop gain for DG-1 Droop gain for DG-1	0.2MW 0.1MW 1kV 100V 0.5 1
IC	Transformer DC capacitor Filter capacitor Filter inductor Switching frequency Reference DC voltage	11/1.72kV 5000μF 50μF 33mH 15kHz 2.5 kV
Load buck converter	Inductor Capacitor Output voltage	4mH 250μF 500 V
PFC buck converter	Inductor Capacitor	4mH 250μF

In the first case study it is assumed that the microgrid is operating in islanded mode. During this scenario no power is required to be transmitted through the PFC and hence its reference is chosen as zero. In the next case study, a constant amount of power is supplied to the DCMG from the utility. Output voltage reference of the PCC is changed accordingly so that it can facilitate requested amount of power from the utility. In the last case study, it is considered that the DGs in the DCMG are inactive. Subsequently, the utility has to supply power to all the DC loads. While all the simulation studies are performed in PSCAD, the control parameters for the converters are calculated using MATLAB.

A. DC-DC Converter Operation

For the performance study of the DC-DC converters with the proposed control algorithm the parameters stated in Table I are chosen. The output is nominally assumed as 1 Ω. It is to be noted that for a buck converter, the output voltage is duty ratio times the input voltage. The results are shown in Fig. 5.

At the beginning, the duty is set to 0.2. This, for the input voltage of 2.5 kV, indicates that the output voltage will be 500 V and the output power will be $500^2/1 = 250$ kW. At 0.3 s, the output voltage reference is increased to 600V. To perform the voltage tracking, the duty increases to 0.24 and the output power increases to 360 kW. At 0.6 s, the input voltage is changed to 2 kV. Since the proposed controller can hold the output voltage irrespective of any input voltage variations, after a small transient, the output voltage settles to 600V. However the duty ratio is changed to 0.3 as expected. Finally at 1 s, the load resistance is changed to 0.5 Ω, thereby doubling the load power. It can be seen from Fig. 4 that even

though the load changes to 720 kW, the output voltage and the duty ratio remain the same.

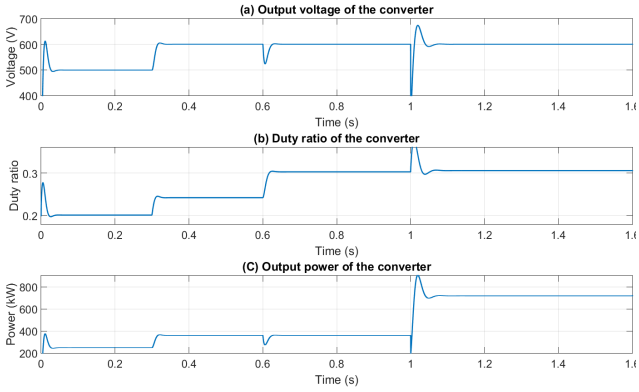

Fig. 5. Buck converter performance when the output voltage reference, input voltage and load are changed.

B. Islanded Mode of DCMG Operation

For this case it has been assumed that the DCMG operates in an isolated mode and no power gets transferred from the utility side. Therefore the power reference (P_{ref}) for the PFC is set as zero. The results for a cold start are shown in Figs. 6 and 7.

Fig. 6 (a) shows the power generated (P_s) and the power supplied to the utility local load (P_{LAC}), where P_s is around 565 kW. The DC side voltage of the IC is shown in Fig. 6 (b). It can be seen that it settles to the desired value of 2.5 kV. The PFC output voltage is shown in Fig. 6 (c). It settles to around 1 kV, as expected.

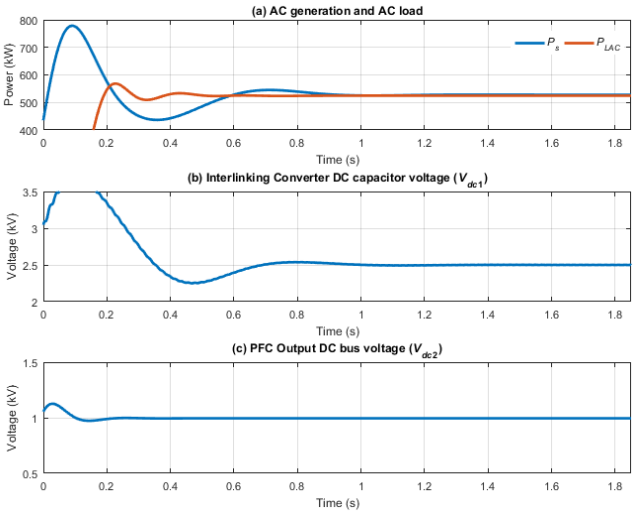

Fig. 6. Islanded mode of operation: (a) AC generation and AC Load, (b) IC DC capacitor voltage and (c) PFC output DC voltage.

From Fig. 7 shows the performance of the DCMG, where the dc load (P_L) is 180 kW. It is shared in the ratio 2:1 by the two DGs (120:60 kW) as can be seen from Fig. 7 (a). The link power remains zero (Fig. 7 b). The DG output voltages settle to around 940 V (Fig. 7 c) as per the droop equation (4).

C. Pre-Specified Power Flow from Utility

With the DCMG operating in standalone mode, the power reference (P_{ref}) is changed to 100 kW at 0.15 s. The results are shown in Figs. 8 and 9. It can be seen from Fig. 8 (a) that the utility power increases by 100 kW to meet the increased power demand from DCMG. The IC DC capacitor voltage however remains at 2.5 kV barring an initial transient (Fig. 8 b). The DGMG powers are shown in Fig. 9 (a). It can be seen that the DG powers drop, but the load power remains constant. The link power is 100 kW, as expected. The remaining 80 kW

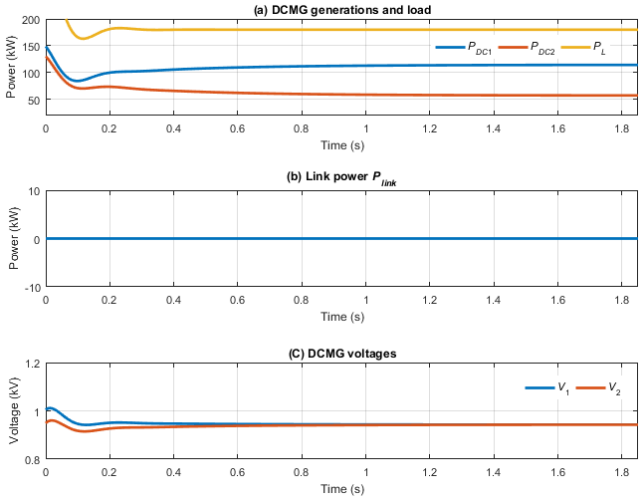

Fig. 7. Islanded mode of operation: (a) DCMG generations and load, (b) link power and (c) DCMG voltages.

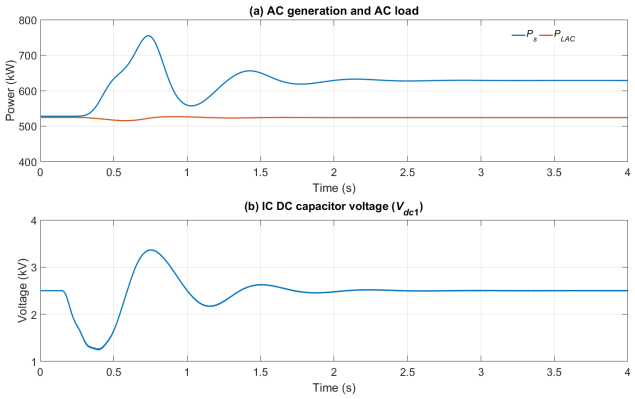

Fig. 8. Constant power flow: (a) AC generation and load and (b) IC DC capacitor voltage.

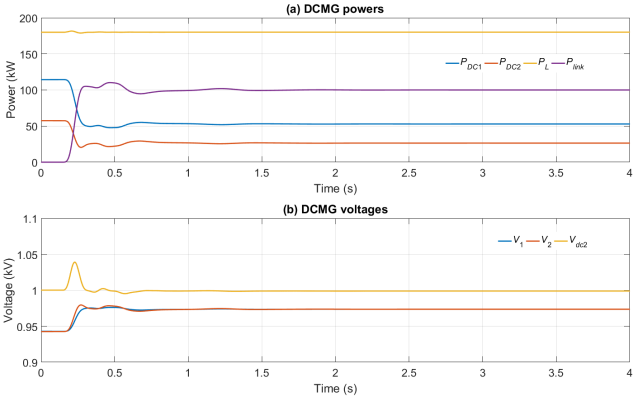

Fig. 9. Constant power flow: (a) DC generations, load and link power and (b) DCMG voltages.

are shared by the DGs according to their rating. Since the power generated by the DGs have dropped, the DGs voltage rise, as can be seen from Fig. 9 (b).

D. Inactive DCMG Generators

With the system operating in the steady state, the DGs in the DCMG get disconnected at 0.2 s. When this is detected, the trigger signal T_{rig} is activated and the PI controller of Fig. 4 is bypassed. The dc load is assumed to be 100 kW. The AC power supply then increases by 100 kW to cater to the DC load as shown in Fig. 10 (a). The DCMG powers are shown in Fig. 10 (b). It can be seen the DG power outputs become zero and the link power becomes equal to the DC load power.

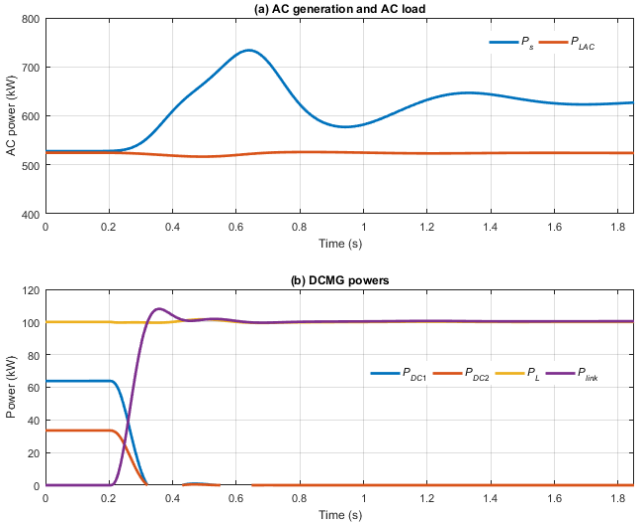

Fig. 10. DCMG DGs get disconnected: (a) AC generation and AC load and (b) DC generations, load and link power.

V. CONCLUSION

In this paper, the operation of a utility connected DC microgrid is studied. The AC side is connected to the DCMG though an interlinking VSC. Also a DC-DC buck converter is connected at the output of the IC for the voltage compatibility with the DCMG and for controlled power flow. It has been assumed that the DGs are connected to the DCMG through DC-DC boost converters, while the DC loads are supplied by a DC-DC buck converter. All these DC-DC converters are controlled by a state feedback with integral controller based on DLQR. Even though this method is based on a perturbation method, it is very robust as has been illustrate in this paper. All the DGs in the DCMG operate in V-P droop control regime, a simple method of droop gain selection based on the voltage drop is proposed.

A two mode power flow control scheme is proposed. In one of the modes, a fixed amount of power is transferred from the utility to the DCMG, which can be zeros as well. The DGs in the DCMG then share the balance power requirement according to their ratings. The other mode is invoked when all the DGs in the DCMG are disconnected, in which case the entire DCMG load is supported by the utility. Extensive simulation studies in PSCAD are performed to verify the efficacy of the proposed scheme.

VI. ACKNOWLEDGEMENT

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