Impact of DC-Link Fault on the Dynamic Performance of DFIG

A. M. Shiddiq Yunus, *Student Member IEEE,* A. Abu-Siada, *Member IEEE*
and Mohammad A. S. Masoum, *Senior Member IEEE*

***Abstract*— The number of doubly fed induction generators (DFIG) connected to the existing network has increased significantly worldwide during the last two decades. This triggers off manufactures to improve the performance of DFIG through robust and reliable design. The stator in DFIG is directly connected to the grid whereas the rotor is interfaced to the grid through two voltage source converters; rotor side converter (RSC) and grid side converter (GSC), which are considered as the crux of the DFIG system. The converter stations determine the ability of wind turbine to operate optimally during wind speed fluctuation and it can provide reactive power support to the grid during grid disturbance events. The DC capacitor link between the two converters allows optimum and smooth power exchange between DFIG and the grid. Therefore, any faults within the DC link will affect the overall performance of the DFIG. This paper investigates the impact of open circuit and short circuit faults in the DC link capacitor on the dynamic performance of the DFIG. The compliance of the wind energy conversion (WEC) system with different grid codes such as those of Denmark, Spain, Nordic and Sweden under such faults is also investigated.**

***Index Terms*—DFIG, Grid side converter, Rotor side converter, Fault ride through**

I. Introduction

WIND energy is one of the most promising renewable energy resources in the world. The global wind energy installed capacity has been increased from 2 GW at the end of year 1990 to 94 GW by the end of year 2007. In 2008, electricity generation using wind power has reached to 1% of the global electricity generation and by the year 2020, it is expected that wind power to supply about 10% of the global electricity [1]. Doubly fed induction generator (DFIG) is one of the popular variable speed wind turbine generators, where about 46.8% of the global installed wind turbines in 2002 were of this type [2]. The popularity of DFIG is based on its several advantages over the fixed speed wind turbine. These advantages include, more optimal power capture, improved power quality, reduced mechanical stress imposed on the turbine during wind fluctuation and decoupled control of active and reactive power. The DFIG is more economic than wind turbine equipped with full scale converter [2, 3]. DFIG stator winding is directly connected to a transformer low voltage side while its rotor winding is connected to a bidirectional back to back IGBT voltage source converter as shown in Fig. 1. The converter helps in decoupling the mechanical and electrical frequencies and making variable speed operation possible. Because of the fact that DFIG is equipped with partial scale converter, the turbine cannot operate in full range from zero to the rated speed, however the speed range is quite sufficient [4]. The detailed system under study (Fig. 1) along with the DFIG model used in this paper is given in [5].

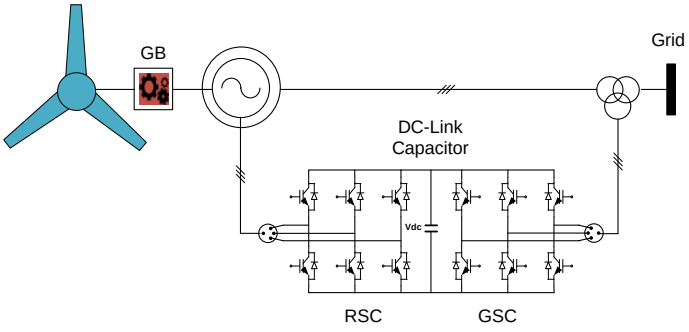


Fig. 1. Typical configuration of DFIG

Most of literatures studies about DFIG considered its performance during various grid disturbances [6-9]. Although, there are few studies in the literatures about the effect of converter station faults on the overall performance of HVDC systems [10-12], no attention was given to the performance of the DFIG and its compliance to the grid code during possible converter station faults. This paper investigates the impact of open circuit (OC) and short circuit (SC) of the DC link capacitor on the dynamic performance of the DFIG. The DFIG fault ride through (FRT) compliance with some international grid codes such as Denmark, Spain, Sweden and Nordic (interconnected system of Denmark, Sweden, Norway and Finland) is also investigated. The simulation is carried out using Matlab / Simulink software and the results will be useful for designing appropriate DC link converter protection of DFIG.

II. Fault Ride Through of International Grid Codes

Increasing wind power penetration into existing power systems has led to the development of grid technical

A. M. Shiddiq Yunus is with the Department of Mechanical Engineering, Energy Conversion Study Program, State Polytechnic of Ujung Pandang, Perintis Kemerdekaan KM. 10 Makassar 90215, Indonesia (e-mail: a.yunus@postgrad.curtin.edu.au).

A. Abu-Siada and M. A. S. Masoum are with the Department of Electrical and Computer Engineering, Curtin University, Perth, WA 6845 Australi (e-mail: a.abusiada@curtin.edu.au and m.masoum@curtin.edu.au).

requirement codes. These grid codes require the wind turbine generators (WTGs) to support the grid during various grid disturbances. One parameter that has been given special attention in most of the worldwide grid codes is the voltage profile at the point of common coupling (PCC) where the wind turbine is required to withstand certain level of voltage sag for certain duration during grid disturbance events. This requirement is known as fault ride through (FRT) or low voltage ride through (LVRT). The typical FRT of some countries is shown in Fig. 2

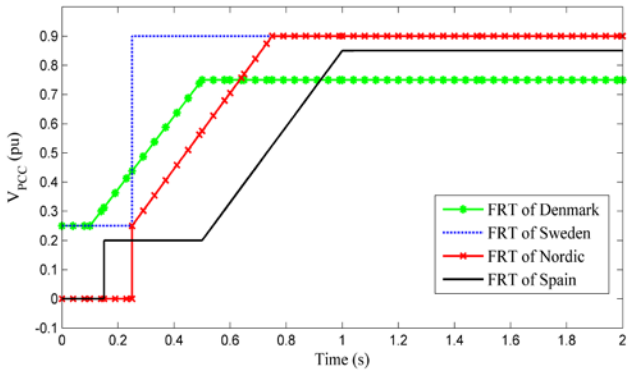


Fig. 2. Various FRT of recent grid codes [13, 14]

The voltage level at the point of common coupling that fall below the lines shown in Fig. 2 will cause a disconnection of the wind turbine from the grid to avoid any damages that may occur to the WTG. Upon a grid disturbance, the minimum voltage drop allowed in the FRT code of Denmark is 0.25 pu for a duration of 0.1 s and the minimum voltage recovery level is 0.75 pu after 0.5 s from the fault occurrence. The same minimum voltage level of 0.25 pu is allowed for Sweden FRT grid code however, it can last for a duration of 0.25 s after which the voltage must be recovered to a level not less than 0.9 pu. On the other hand, WTGs are remaining connected to the PCC during voltage drop to zero for duration of 0.15 s and 0.25 s in the Nordic and Spain FRT grid codes respectively. Nordic FRT grid code requires the voltage to be recovered to 0.9 pu after 0.7 s of fault occurrence. However, FRT of Spain allows the voltage level of 0.2 pu for a duration of 0.35 s after which it should be recovered to a minimum level of 0.85 pu in 1 s of the fault occurrence. These grid codes are summarized in Table I.

TABLE I
LVRT REQUIREMENTS OF SOME INTERNATIONAL GRID CODES

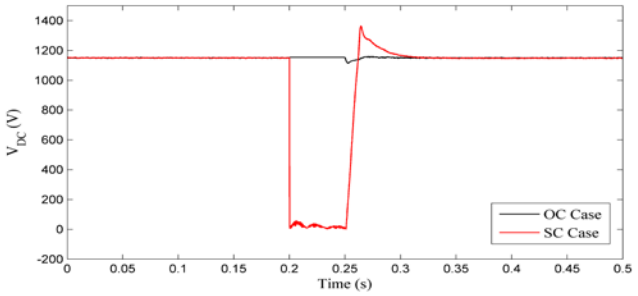
Country	LVRT			
	During Fault		Fault Clearance	
	V_{min} (pu)	T_{max} (s)	V_{min} (pu)	T_{max} (s)
Denmark	0.25	0.1	0.75	0.5
Sweden	0.25	0.25	0.9	0.25
Nordic	0	0.25	0.9	0.7
Spain	0	0.15	0.85	1

III. SIMULATION RESULTS

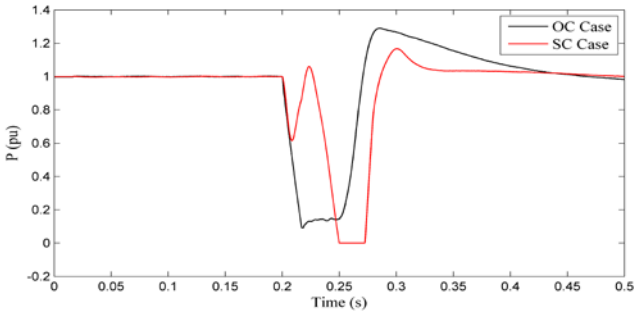
The dynamic performance of the DFIG under the DC link capacitor open and short circuit faults is examined. For both faults, two scenarios are assumed; the first scenario assumes that the fault starts at 0.2 s and cleared out at 0.25 s while in the second scenario, the fault is assumed to start at 0.2 s and is failed to be cleared out.

A. Open and Short circuit faults with successful clearance

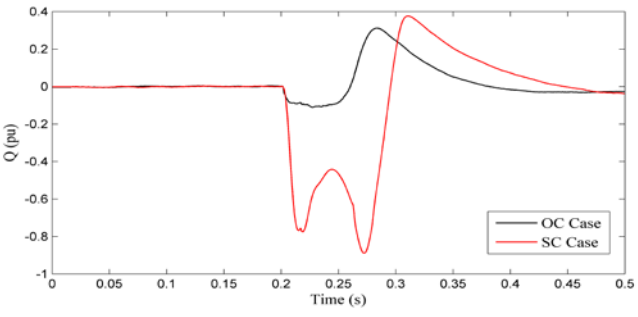
In this fault, the DC capacitor is assumed to experience open circuit and short circuit faults at 0.2 s and the fault is cleared out after two and half cycles (0.05 s) as can be shown in Fig. 3 (a). Figs. 3 (b), (c) shows the active and reactive power of the DFIG. During normal operating conditions, the active and reactive powers delivered to the grid are respectively 1 pu and 0 pu. Upon the occurrence of OC and SC capacitor faults, the generated active power will significantly reduced and the DFIG will absorb reactive power from the grid which is more significant in case of SC fault as can be shown in Fig. 3 (b). After clearing the fault at 0.25 s, power restoration will take place in about 0.05 s. it is worth to notice that active and reactive power will experience some transient fluctuations before settling down in both types of faults.



(a)



(b)



(c)

Fig. 3. (a) Capacitor voltage, (b) DFIG active power and (c) Reactive power

The DC capacitor voltage safety margin is set up by the manufacturer. In [15], this margin is set between 0.25 pu and 1.25 pu. If this requirement is applied, the converter protection will be energized for SC case as the voltage across the DC capacitor will drop to 0 V of the nominal value.

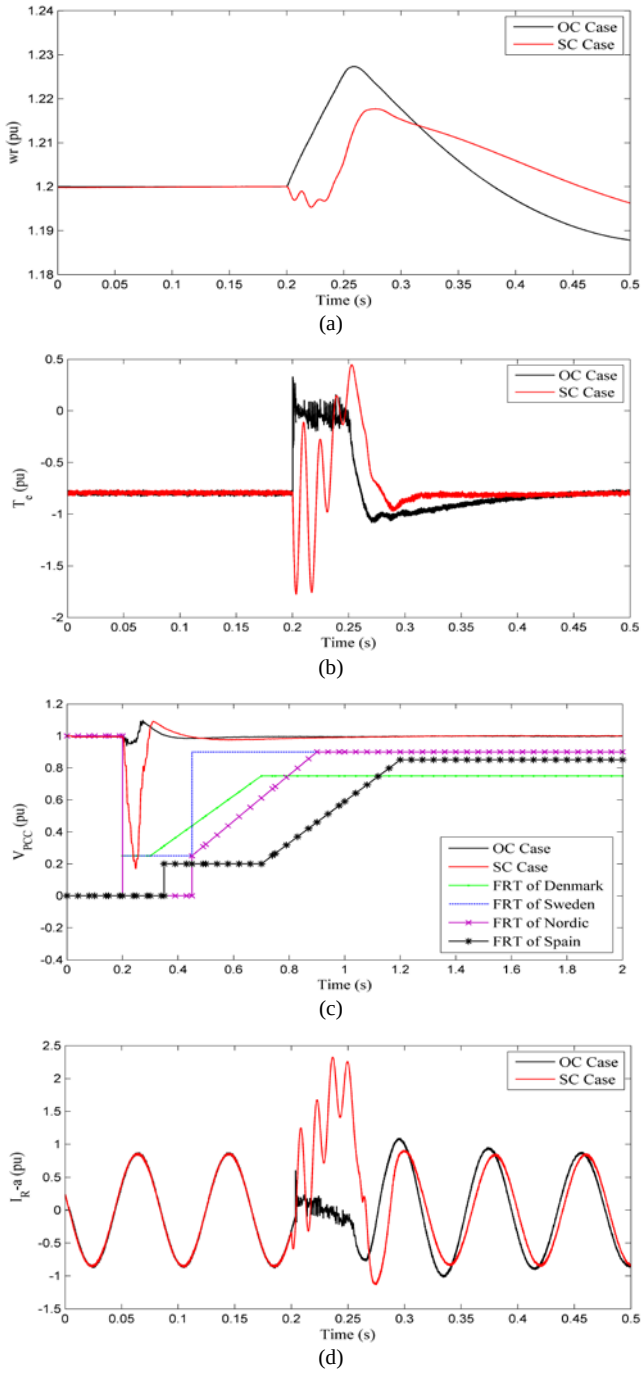


Fig. 4. Impact of capacitor OC and SC on (a) Shaft speed (b) electromagnetic torque (c) Voltage at PCC and (d) Rotor current at phase-a

Due to the power reduction during capacitor OC and SC faults, the rotor shaft will accelerate and the electromagnetic torque will be reduced as can be shown in Figs. 4 (a), (b) respectively. The pitch control will not be able to stabilize the shaft speed as in most of grid disturbance and in some occasions this may lead to rotor instability. The voltage at the PCC will drop to 0.2 pu in case of capacitor SC fault while the drop in the voltage due to capacitor OC fault is insignificant. When compared with different grid codes, the voltage at the PCC in case of capacitor SC fault will violate the LVRT code of both Denmark and Sweden however; it will be in the safe margin boundary of Nordic and Spain grid codes as shown in Fig. 4 (c). The rotor current (Fig 4(d)) will drop to a level close zero during capacitor OC fault while it reaches a crest value of 2.4 pu in case of capacitor SC fault.

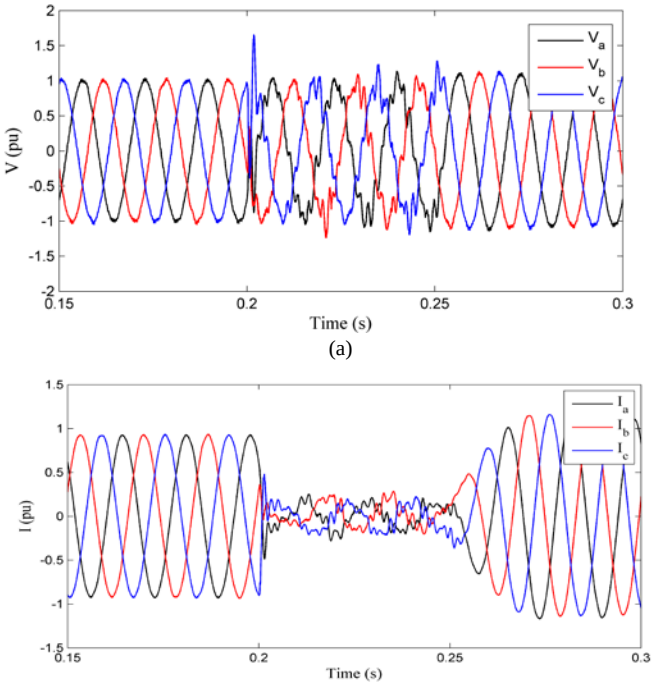


Fig. 5. Impact of capacitor OC fault on (a) Stator voltages (b) Stator currents

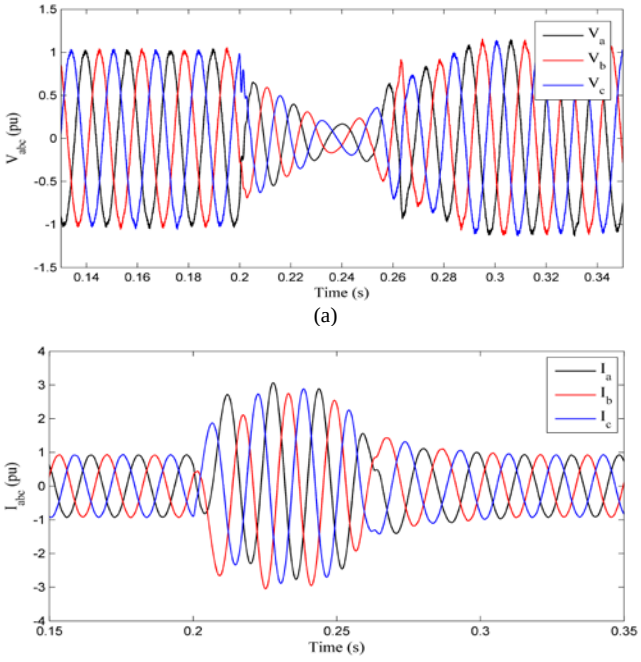


Fig. 6. Impact of capacitor SC fault on (a) Stator voltages (b) Stator currents

Fig. 5 and Fig. 6 show the impact of capacitor OC and SC faults on the stator 3-phase voltages and currents respectively. In case of capacitor OC fault, the stator voltages will experience some spikes during the fault and normal operation voltage waveform will be restored once the fault is cleared. On the other side, the stator 3-phase currents will drop to almost zero level during the fault as is shown in Fig. 5. Fig. 6 shows that during capacitor SC fault, the stator voltages will significantly reduced while the stator currents will increase to a significant level of 3. It can be noticed that capacitor short circuit fault will introduce more transient oscillations in all the parameters mentioned above.

B. Open and Short circuit faults with unsuccessful clearance

In this fault, the DC capacitor is assumed to experience open circuit and short circuit faults at 0.2 s and the fault is sustained because unsuccessful clearance as can be observed in the capacitor DC voltage (Fig. 7 (a)) which shows that the DC voltage drops to zero at the instant of fault occurrence in case of SC fault while the OC fault has no impact on the DC voltage.

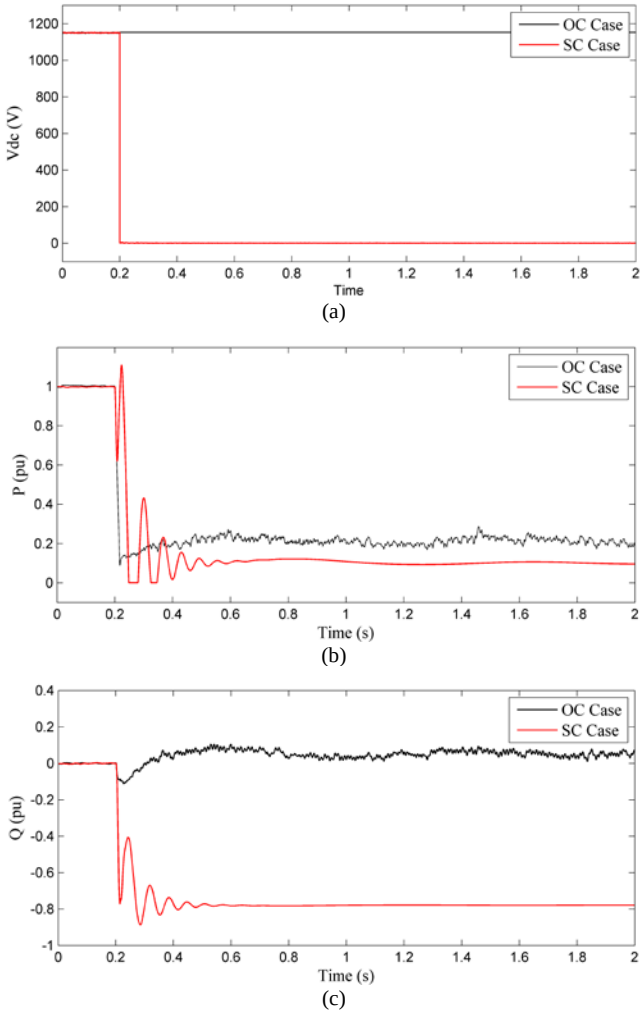


Fig. 7. (a) Capacitor voltage, (b) DFIG active power and (c) Reactive power

Similar to the successful clearance scenario, the DFIG generated active power (Figs. 7 (b)) will significantly reduced with more reduction in case of SC fault. However, as the fault is not cleared in this case, power restoration is not possible. The reactive power is slightly affected at the instant of applying OC fault however, the DFIG will require a significant reactive power from the grid in case of SC fault (Fig. 7 (c)).

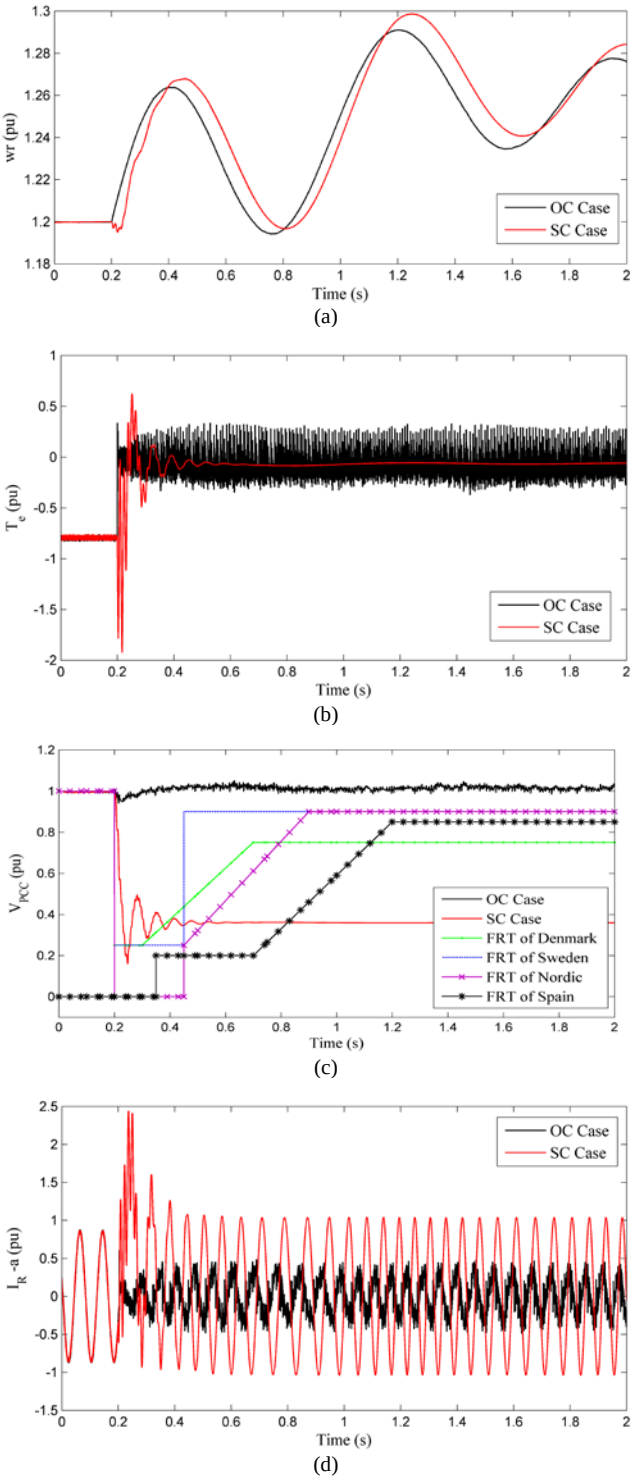
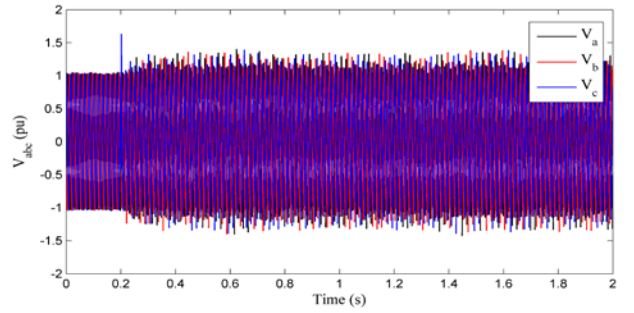


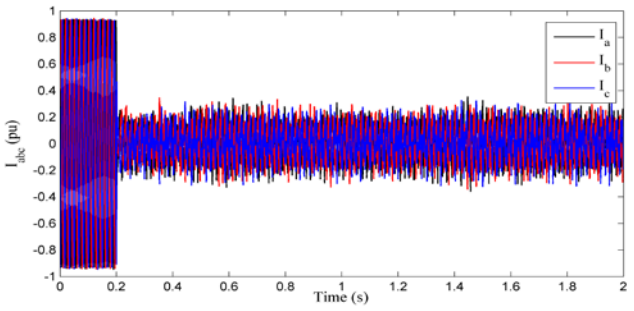
Fig. 8. Impact of sustained capacitor OC and SC on (a) Shaft speed (b) electromagnetic torque (c) Voltage at PCC and (d) Rotor current at phase-a

As mentioned in the previous case study, the shaft speed (Fig. 8 (a)) will accelerate due to the reduction in output power however, because fault is not cleared, the shaft speed will increase without limitation and will lead to rotor instability and other severe shaft damages if not controlled. The

electromagnetic torque will be reduced and maintained at zero level as shown in8. 9(b). When compared with LVRT grid codes of Denmark, Sweden, Spain and Nordic, the voltage at the PCC will violate all safety boundaries in case of SC fault as it will be maintained at 0.4 pu and will not be recovered (Fig. 8 (c)). This will lead to the disconnection of the wind turbine from the grid to avoid any damages. Fig. 8 (d) shows that the rotor current will drop to zero in case of OC fault while it will experience a maximum overshooting of 2.5 pu at the instant of fault occurrence in case of SC fault.

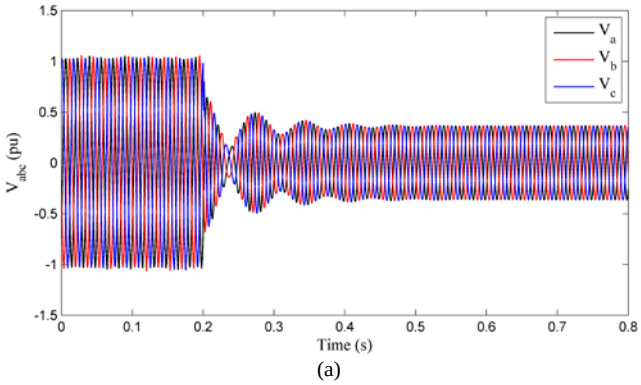


(a)

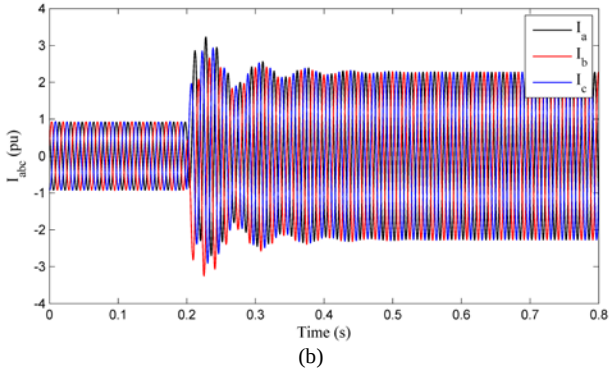


(b)

Fig. 10. Impact of capacitor OC fault on (a) Stator voltages (b) Stator currents



(a)



(b)

Fig. 11. Impact of capacitor SC fault on (a) Stator voltages (b) Stator currents

The stator 3-phase voltages and currents during OC and SC faults are respectively shown in Fig. 10 and Fig. 11. The same parameters trend as the previous case study of successful fault clearance can be observed here however, non of these parameters will be recovered to the nominal values as far as the fault is sustained.

IV. Conclusion

This paper investigates the impact of open circuit and short circuit faults of the DC capacitor link on the dynamic performance of DFIG. Two fault scenarios (successful and unsuccessful fault clearance) were simulated and investigated. In both scenarios, the impact of short circuit fault is more pronounced and the LVRT compliance with different grid codes is failed. Results of this study will open the door for further developments of protection systems for wind energy converter stations to avoid any damages to the wind turbine during such faults.

V. Acknowledgment

The first author would like to thank the Higher Education Ministry of Indonesia (DIKTI) and the State Polytechnic of Ujung Pandang for providing him with a PhD scholarship at Curtin University, Australia.

VI. References

[1] P. Musgrove, Wind Power, New York: Cambridge University Press, pp. 221-222.2010

[2] T. Ackermann, Wind Power in Power System, West Sussex: John Wiley and Sons Ltd, pp. 65.2005

[3] R. Pena, J. C. Clare, and G. M. Asher, "Doubly fed induction generator using back-to-back PWM converters and its application to variable-speed wind-energy generation", *Electric Power Applications, IEE Proceedings* -, vol. 143, pp. 231-241.1996

[4] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey", *IEEE Transactions on Industrial Electronics*, vol. 53, pp. 1002-1016.2006

[5] N. W. Miller, J. J. Sanchez-Gasca, W. W. Price, and R. W. Delmerico, "Dynamic modeling of GE 1.5 and 3.6 MW wind turbine-generators for stability simulations," in *Power Engineering Society General Meeting, 2003, IEEE*, pp. 1977-1983 Vol. 3.2003

[6] R. K. Behera and G. Wenzhong, "Low voltage ride-through and performance improvement of a grid connected DFIG system," in *International Conference on Power Systems, 2009. ICPS '09.* pp. 1-6.2009

[7] A. M. Shiddiq-Yunus, A. Abu-Siada, and M. A. S. Masoum, "Improvement of LVRT Capability of Variable Speed Wind Turbine Generators Using SMES Unit," in *Innovative Smart Grid Technologies (ISGT) Asia, IEEE PES*, Perth, Western Australia.2011

[8] A. M. Shiddiq-Yunus, A. Abu-Siada, and M. A. S. Masoum, "Application of SMES Unit to Improve the High-Voltage-Ride-Through Capability of DFIG-Grid Connected During Voltage Swell," in *Innovative Smart Grid Technologies (ISGT) Asia, IEEE PES*, Perth, Western Australia.2011

[9] A. M. Shiddiq-Yunus, A. Abu-Siada, and M. A. S. Masoum, "Application of SMES Unit to Improve The Voltage Profile of The System With DFIG During Grid Dip and Swell", *International Journal of Advances in Engineering & Technology*, vol. 1, pp. 1-13.2011

[10] A. Abu-Siada and S. Islam, "Application of SMES Unit in Improving the Performance of an AC/DC Power System", *IEEE Transactions on Sustainable Energy*, , vol. 2, pp. 109-121, 2011

[11] H. A. Darwish, A. M. I. Taalab, and M. A. Rahman, "Performance of HVDC converter protection during internal faults," in *Power Engineering Society General Meeting, 2006. IEEE*, p. 7 pp.2006
[12] S. O. Faried and A. M. El-Serafi, "Effect of HVDC converter station faults on turbine-generator shaft torsional torques", *IEEE Transactions on Power Systems*, vol. 12, pp. 875-881.1997
[13] Alt, x, M. n, Go, O. ksu, R. Teodorescu, P. Rodriguez, B. B. Jensen, and L. Helle, "Overview of recent grid codes for wind power integration," in *12th International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)*, pp. 1152-1160, 2010
[14] M. Tsili and S. Papathanassiou, "A review of grid code technical requirements for wind farms", *Renewable Power Generation, IET*, vol. 3, pp. 308-332.2009
[15] V. Akhmatov, "Analysis of Dynamic Behaviour of Electric Power System with Large Amount of Wind Power," in *Electrical Power Engineering* Lyngby: Technical University of Denmark, 2003.

VII. BIOGRAPHIES

A. M. Shiddiq Yunus (S'11) was born in Makassar, Indonesia. He received his B.Sc from Hasanuddin University, Indonesia in 2000 and his M.Eng.Sc from Queensland University of Technology, Australia in 2006 both in Electrical Engineering. He is currently towards his PhD study at Curtin University, WA, Australia. His employment experience include lecturer in the Department of Mechanical Engineering, Energy Conversion Study Program, State Polytechnic of Ujung Pandang since 2001. He is also a member of assessor institution of Indonesia in electrical engineering since 2007. His special fields of interest included superconducting magnetic energy storage (SMES), smart grid and renewable energy.

A. Abu-Siada (M'07) received his B.Sc. and M.Sc. degrees from Ain Shams University, Egypt and the PhD degree from Curtin University of Technology, Australia, All in Electrical Engineering. Currently, he is a lecturer in the Department of Electrical and Computer Engineering at Curtin University. His research interests include power system stability, Condition monitoring, Power Electronics, Power Quality, Energy Technology and System Simulation. He is a regular reviewer for the IEEE Transaction on Power Electronics, IEEE Transaction on Dielectrics and Electrical Insulations, and the Qatar National Research Fund (QNRF).

Mohammad A. S. Masoum (S'88–M'91–SM'05) received his B.S., M.S. and Ph.D. degrees in Electrical and Computer Engineering in 1983, 1985, and 1991, respectively, from the University of Colorado, USA. Dr. Masoum's research interests include optimization, power quality and stability of power systems/electric machines and distributed generation. He is the co-author of *Power Quality in Power Systems and Electrical Machines* (New York: Academic Press, Elsevier, 2008). Currently, he is an Associate Professor and the discipline leader for electrical power engineering at the Electrical and Computer Engineering Department, Curtin University, Perth, Australia and a senior member of IEEE.