School of Electrical Engineering Computing and Mathematical Sciences

Operation and Control of DC Microgrid

Amit Jyoti Datta

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Declaration

To the best of my knowledge and belief this thesis contains no material previously published by any other person except where due acknowledgment has been made.
This thesis contains no material which has been accepted for the award of any other degree or diploma in any university.

Signature:

Date: 01/09/2019

To my Family

Abstract

Power harnessing technology from the renewable energy resources has been developed over the past two decades. This technology enabled us to integrate renewable energy based power generation to the conventional electric power grid. The approach of coupling the renewable energy based power generations with power distribution system is referred as distributed generation. In a microgrid (MG), locally produced electric power is supplied to the local loads, while a backup of electric power grid or battery is used during insufficient power generation from the renewables. The distributed generators control the power sharing in an autonomous microgrid. This study aims to improve the dynamic response and the load regulation using improved control strategies of the dc converters. Dc converters switch between two configurations: (i) switch on state and (ii) switch off state. Even though all the circuit elements of a dc converter are linear and the above mentioned configurations have linear behaviour, the overall behaviour of the circuit is nonlinear. For the control design, two different linearization procedures are presented. Both these methods are used for deriving state feedback with integral control for regulating the output voltage. Additionally, a proportional-plus-integral (PI) is controller is also used and a method for stable gain selection has been presented.

A significant amount of research is carried out about dc microgrids as the dc network has certain advantages over ac network. However, enough developments have not yet been made to form a generalized model of the dc microgrid. For any control algorithm, we analyse the network stability at varied conditions. Subsequently, we develop a generalized homogeneous model of an autonomous dc microgrid. To evaluate the susceptibility of droop gain and load variations in a dc microgrid, the adapted control laws are implemented while maintaining stable dc bus voltage and power sharing. The stability of the dc microgrid is further analysed using a detailed eigenvalue analysis in which the trajectory of the eigenvalues is identified.

One of the aims of this thesis is to investigate the power sharing between multiple dc microgrids. Power sharing between utility/ac microgrid and dc microgrid is also discussed. Dc microgrid is connected to the utility/ac microgrid through an interlinking converter. To enable power flow in bidirectional mode, we require to define droop for the interlinking converter. The challenge of defining the droop gains is the mismatch of the droop coefficients on either side of the interlinking converter. To overcome this challenge, three approaches are proposed that do not require droop gain selection of the interlinking converter to enable bidirectional

power flow. In these approaches a dc converter is used to enable power flow from ac to dc microgrid and, bidirectional switch and dual active bridge (DAB) is used to enable bidirectional power flow. A linearized model for the DAB has been developed. A small signal model of the DAB has been derived based on state transition equation, where the continuity of the state variables during the switching operation has been retained.

In practice, power sharing in between microgrids will not only depend on available power. It will also depend on other factors, including power generation cost and electricity market situation. To incorporate these factors in the analysis of the fair allocation of surplus power, ideas such as the "Shapely Value" from the field of cooperative game theory is adopted. When it is not a cooperative system, e.g. in the monopoly or duopoly, competition is introduced between multiple players. In these competitive scenarios, the power transfer from one MG to other MG is solved using the "Price leadership" and "Stackleberg Duopoly" methods, adopted again from the field of game theory:

All the developed models for this thesis are tested through simulation studies. Performance of a dc microgrid is evaluated with hardware prototypes. The power hardware-in-the-loop (PHIL) concept is used in this thesis to test the coupling of a ac microgrid (ACMG) and a dc microgrid (DCMG). In PHIL, the ACMG side with an interlinking voltage source converter is simulated and is interfaced with the hardware of the DCMG through a suitable converter, termed as the power flow converter (PFC). It is expected that this research work will significantly contribute to the knowledge of operation of integrated AC/DC systems.

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Contents

CHAPTER 1

INTRODUCTION

Fossil energy sources have been the major source for electric power generation for over a hundred years. However to reduce the carbon emission from these fossil fuel based power generators and at the same time to ensure a reliable and flexible energy source, renewable energy based power generation are currently gaining much attention. In this regard, distributed generation (DG) based on renewable sources, which are located near the distribution network or connected directly to the customer site of the meter, are getting connected to power distribution networks [1, 2]. Also a microgrid (MG) containing several DGs can provide a better control flexibility to maintain a stable operation for a cluster of loads and paralleled DG systems [3-6].

According to Navigant Research [7], 1,869 projects have been under development as of 4th quarter of 2017. These have a total capacity of 20.7 GW, spanning 123 countries. This is more 4 GW compared to 16 GW identified in the 2nd quarter of 2016. Asia-Pacific regions leads in the microgrid deployment with 8.4 GW of total capacity. North American deployment is second with 6.97 GW. Surprisingly the whole of Europe with a deployment figure of 1.8 GW.

In a dc microgrid (DCMG) all the generations and loads are connected to a common dc bus. In a utility connected dc microgrid and also in an interconnected ac and dc microgrid, ac and dc sides are linked together through an interlinking ac/dc converter, which can facilitate a bi-directional power flow. There is a difference between the grid connected operation of ac and dc microgrids. In a grid connected ac microgrid, the frequency of the DGs is set by the utility and the DGs control their local bus voltages through reactive power. In an islanded mode, an ac microgrid operates in droop control, which has several variations depending on system structure. Since a dc microgrid is separated from a utility grid through power electronic converters, its DGs can always operate in V-P or V-I droop control.

A large majority of electrical loads, such as LED-lighting, adjustable speed motors, electric vehicles, computing and communication equipment need dc supply. At the same time, many DERs like PV, batteries, fuel cell produce power at dc voltage

level, which is then converted in ac for grid connection. Moreover, there is potential to directly connect a wind turbine or microturbine to a dc grid. Increasingly a large number of researchers are proposing the use of dc grid at the distribution level as this reduces conversion losses significantly. Voltage transformation from one level to another in a dc grid can be achieved through dc-dc converters, which have around 95% efficiency [8]. However, when ac loads coexist with dc loads, an interconnected system can be considered [8-11].

Usually, the DGs in a MG are scattered in a region which makes it inconvenient to establish a power sharing via a communication link with wires. Subsequently, the droop control method has been adapted by many researchers to determine the electric power contribution of each DGs for load demand sharing [8-11]. This power sharing is achieved in the proportion to the power ratings of the DGs [9]. Power sharing in the ac side of a ac-dc interconnected microgrid could be controlled by regulating the frequency to a desired range, whereas the dc side power distribution is voltage dependent. Subsequently, during coupling of the ac microgrid and the dc microgrid, the major challenge for controlling the power sharing is the mismatch of the droop coefficients of the interlinking converter [11]. Normalization of the droop equations [11] and a technique considering ac side frequency and dc side voltage as a common signal to generate droop coefficients for the inter-linking converter has been proposed to date [12].

Traditionally, during a transient in an ac system, the inertia of the synchronous machines determines the stability of the system. A sudden change in load or fault can cause a change in frequency and the kinetic energy stored in the rotor of synchronous generators vary accordingly to alleviate the immediate impact of a transient. Unfortunately inertia cannot be used in dc systems. It increases the possibility of unstable conditions in the aftermath of a load change. Moreover, in a hybrid ac-dc microgrid, there will be several converters which are expected to hold the voltage and frequency to an optimum level so that the power sharing in between the microgrids is achieved. All these converters are usually designed with feedback controllers to regulate the voltage or the current. The overall system stability has to be carefully examined by testing it for different probable penetration.

1.1. MICROGRID CONCEPT AND ARCHITECTURE

Microgrid is a concept where local loads are fed from the local generation and together they can operate in either grid connected or isolated modes. Microgrid has gained enormous popularity with the development of electrical power harnessing from photovoltaic, wind, fuel cells etc. Rapid advancement in the battery storage technology are also occurring to cope up with the intermittency of renewable energy based power generation. A schematic diagram of a microgrid is shown in Fig. 1.1.

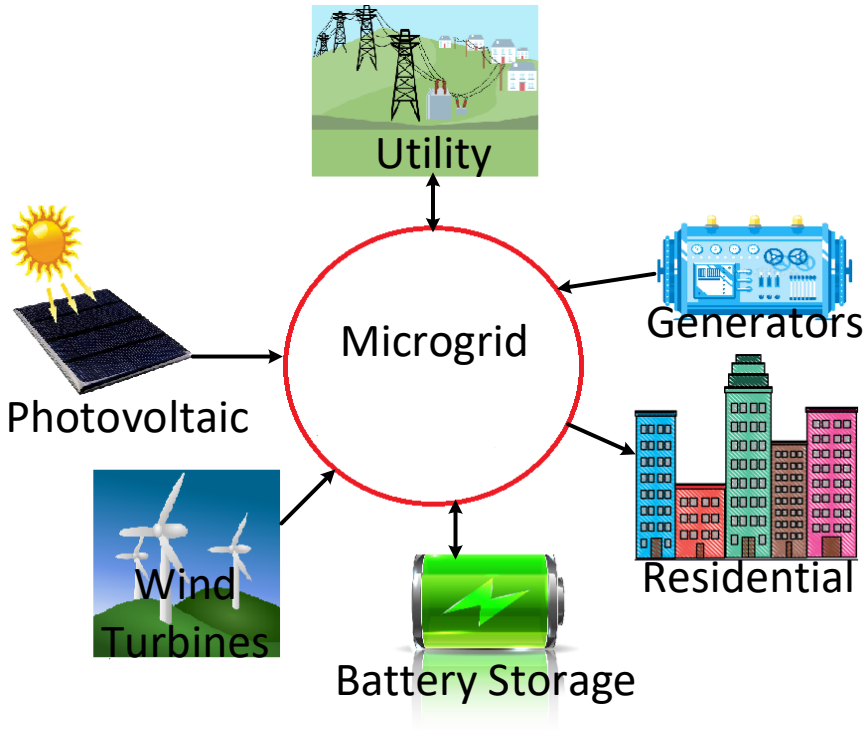

Fig. 1.1 Basic architecture of a microgrid

Microgrid concept is introduced to connect the renewable energy sources (RES) to the existing utility grid [4, 13-15]. Microgrid will not require expansion of existing utility grid to accommodate new RES based electric power generation. Subsequently, integrating RES in the power network is expected to provide green power at a reduced cost. It also makes the electric power network resilient and secure by dispersing the generation sources as well.

In a microgrid, photovoltaics arrays (PVs), fuel cell, battery energy storage devices and wind turbines are connect to a low to medium voltage electric power grid. A microgrid can be either ac or dc. Based on the type of connection, they will be called

AC Microgrid (ACMG) or DC Microgrid (DCMG). However, irrespective of the types, microgrids are usually connected to the utility grid. An ACMG can be connected to the utility grid through an isolating switch (a circuit breaker). However for the connection of a DCMG with an ac system, a power electronic dc/ac converter is required. Microgrids are designed in such a way that they can operate in grid connected or islanded modes [5, 16]. In the grid connected mode, the microgrid local generators can supply the local in its entirety or some amount of power can be imported from the grid. Also it is likely that the microgrid can supply power to the grid. On the other hand, in the islanded mode, all the microgrid generators and it's the energy storage systems must support its local loads, failing which, load shedding will be required. There could be communication channels to make these power control decisions [17-19].

1.1.1. ACMG

ACMG is the most commonly adopted microgrid architecture for obvious reasons [20-33]. However most of the RES based power generations are connected to the existing utility grid or microgrid through power electronic interfaces. For example, micro-wind turbines require back to back converters to be connected to the ac utility grid since the synchronous generators here rotate at low rpm [34-43]. Photovoltaics (PV) based power generations require inverter to be connected to the ac utility grid. ACMG architecture can also have batteries to store the surplus power generated from the RES. The dc loads can be connected via rectifiers, while the ac loads can be directly connected. Although most of the recent microgrids designed and installed are ACMGs, DCMGs are expected to emerge in some niche applications and also due to their inherent benefits over ACMGs. A schematic diagram of an ac microgrid is shown in Fig. 1.2.

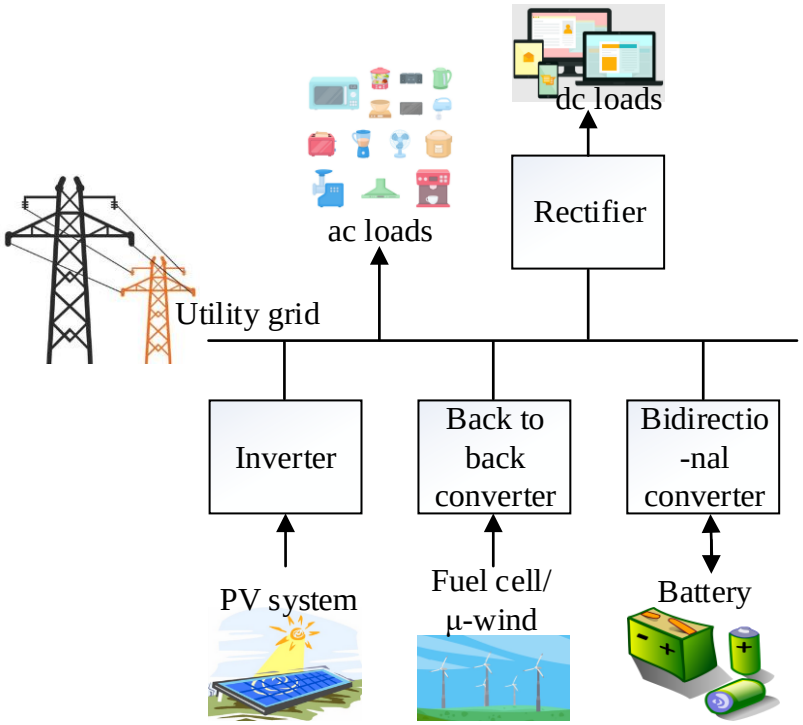

Fig. 1.2 Basic architecture of an ACMG

1.1.2. DCMG

A dc microgrid is considered as a power network consisted of dc sources and loads. It can be connected with a utility grid or an ACMG through an interlinking converter (IC) [44]. DCMG is gaining increasing popularity because of its numerous advantages. Most of the electrical appliances (e.g., smartphones, computers, ballasted fluorescent ceiling lights and etc.) that we use regularly, information technology system, brushless dc motors, variable speed motor drives and many other equipment run on dc power [7,45,46]. A dc microgrid enables all these appliances to be connected without multiple conversion stages. A simple buck converter can be used to step down the dc grid voltage to the dc load voltage to connect all these appliances directly to the dc grid. AC loads can also be connected to the dc grid through an inverter. Usually, RES based power generations are connected to the dc grid through multiple boost converters [45, 46]. A schematic diagram of a dc microgrid is shown in Fig. 1.3.

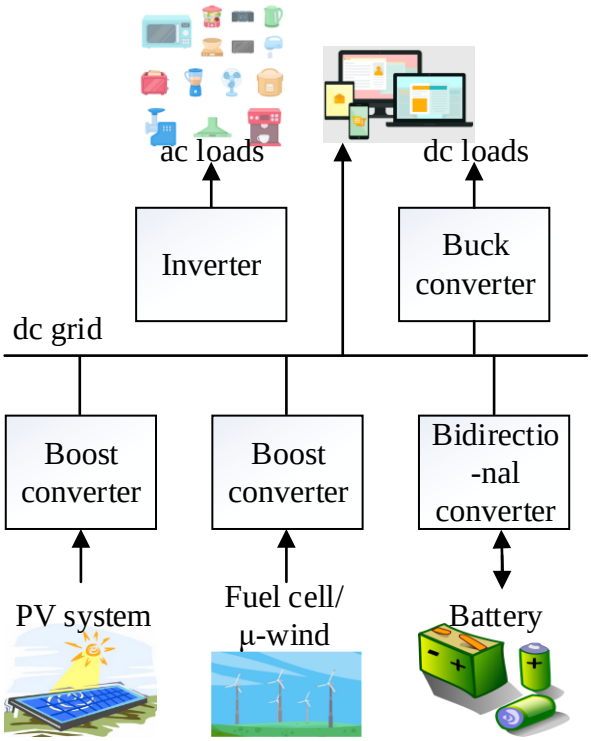

Fig. 1.3 Basic architecture of a DCMG

Apart from connecting the dc loads to utility grid without going through multiple conversion stages, there are other certain advantages of DCMG. DC system is less prone to transmission losses as it offers skin effect free power transmission. In dc transmission, current flows through the entire cable unlike only through the peripherals in the ac system. This phenomena effectively reduces cable size and length [13]. Moreover, dc grid does not require synchronization thus reducing system complexity and increasing stability. However, there are some limitations in such systems. Protection system and grounding are more complicated than ac distribution system.

1.1.3 MICROGRID OPERATING MODE

Based on the load and RES location different microgrid interconnection approach is adopted. Microgrids can be operated independently or with a support from the utility. Several microgrids can also be interconnected to enhance the reliability and also enable power sharing.

Islanded mode:

Microgrids can be operated in islanded mode. In islanded mode of operation microgrids supply power to their local loads without the utility grid [6, 18, 21]. In ac microgrid the ac loads can be directly connected to the ac bus and the dc loads require a rectifier to convert ac to dc power. Similarly, in dc microgrid, dc loads can be connected directly to the dc bus. Often buck converters are used to step down the voltage if the dc bus voltage is higher than the dc load voltage.

Grid connected mode:

In grid connected mode of operation, microgrids are connected to the utility. It can be also designed to supply the load power from utility while RES can be used to charge the battery. Depending on the microgrids' generation capacity and amounts of loads connected the system is designed accordingly [47]. An ac microgrid can be connected to the utility grid through back to back converters to allow specified amount of power flow or power flow from the grid when the DGs are overloaded [29, 30]. A dc microgrid can be connected to the ac utility through an inverter and a transformer on the ac side of the inverter.

AC/DC interconnected mode:

AC and dc microgrid can be interconnected with an interlinking converter [8-11, 48]. In this mode, it can be designed to connect the ac loads to the ac microgrid and the dc loads to the dc microgrid. This approach will reduce the conversion losses in the power distribution system by decreasing the number of power electronic conversion devices. Electric power can be shared among the microgrids in case of power shortfall in either side of the IC. A schematic diagram of ac/dc interconnected microgrid is shown in Fig. 1.4

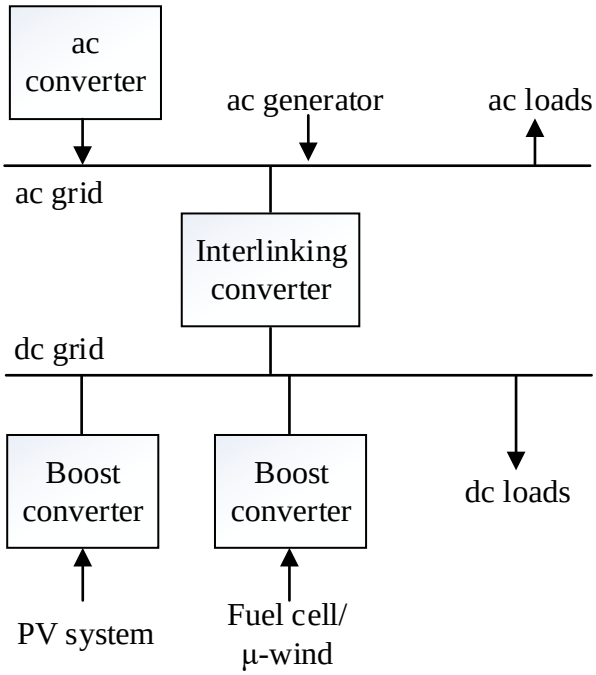

Fig. 1.4 A schematic diagram of ac/dc interconnected microgrid

1.2. POWER ELECTRONICS ELEMENTS IN MICROGRID

Power electronics devices are used to controllably extract power from the RES [49]. One aim of the research is to provide the best performance of these power electronic devices for maximizing power harnessing from RES and use it in the microgrid application. And the other aim is to operate these devices to interconnect the utility grid or even multiple microgrids to share power among themselves. In this section, the topology of the different power electronic devices used in a microgrid and their control mechanism are discussed. As this thesis is focused on the dc microgrid, the control topology and strategies of dc converters are studied. Also, operation of interlinking converter is studied.

1.2.1 DC CONVERTERS

Dc converters can be of several types. In this thesis, buck, boost, buck-boost and dual active bridge are discussed. Among these converters, first three converters are used to allow unidirectional dc power flow. Dual active bridge can be used to enable bidirectional dc power flow.

The basic converter configuration is adopted in this thesis. The dc converters switch between multiple states during its switching operation. But the final state of a switching cycle is the same as the initial state of the next switching cycle for all these converters.

Over the time, researchers have proposed different control techniques to regulate the output quantity of the dc converters. It ranges from fuzzy logic [50] to linear quadratic regulator (LQR) [51-53]. Researchers have also proposed non-linear control techniques [54-56] as well. In LQR the discrete time model of the converter is linearized around an operating point and in non-linear control technique an averaged model of the converter is used to design the controller. All these methods involve in simplifying the dynamic behaviour of the dc converter.

Among all the controllers, PI controller is the most widely used controller for controlling the output voltage or current of the dc converters [57-66]. The output quantity regulation with a PI controller can be achieved by measuring a single state variable [67]. For more precise output voltage/current regulation, state space modelling and averaging technique is introduced. Middlebrrok and Cuk introduced a unified method incorporating the advantages of state space modelling and averaging technique [67]. It has the following advantages:

- designing a controller in state-space domain is simple
- it reduces the output voltage ripple
- it provides an easier analysing tool when multiple dc converters are connected to a system.

The dc converters can be designed using a discrete time model or using a continuous time model. In the discrete time model, the state evolution over a switching cycle is defined and is then linearized [68, 69]. This method is called as the corner point method. The corner point model is a discrete-time model and therefore depends on the switching frequency. The corner point method is best suited for the case when the converter's switching frequency is close to the open loop system bandwidth. But since this method is switching frequency dependent, this method is not suitable for system dynamic analysis for a system with multiple dc converters. Whereas, state space averaging based method can be adapted to design a continuous time model

irrespective of switching frequency. A comparative study of three of these control techniques are presented in the next chapter.

1.2.2 MICROGRID INTERCONNECTION

An ACMG can be connected to the ac utility grid through a back to back (BTB) converter [70-71]. Even multiple ACMGs can be interconnected with BTB converters [72]. For an interconnected ac/dc microgrid or a grid connected dc microgrid, the interconnection is not straight forward. Depending on the power flow direction, the interface between the ac and dc side should be selected. Ideally, it should be designed to enable bidirectional power flow. To connect a dc microgrid with a utility or an ac microgrid, a voltage source converter (VSC) is required for ac/dc power conversion [9, 10, 13, 73]. Diode and controlled rectifier circuitry are sufficient to enable power flow from the ac grid to the dc grid only. Some special topologies are also adapted to enable unidirectional power flow in an ac/dc interconnected system.

For a unidirectional power flow (ac to dc) single phase or three phase rectifier circuits are used. The rectifiers are controlled to hold the dc voltage level and enable power flow from the ac side [74-77]. For bipolar dc system often voltage balancer is used to balance positive and negative voltage. However, with rectifiers in the system, it experiences lower order harmonic distortion in the line current mostly below 2 kHz [13]. The techniques to mitigate the harmonics in the line current can be classified into passive techniques, multi-pulse rectifier techniques and active harmonic cancellation technique [78]. A special topology like single phase diode rectifier circuit with dc converter on its dc side is one of the most common topology to improve the line current quality. It is called “a single phase with power factor correction”. Using similar principle, electronic inductor (EI) topology is developed for a three phase system [79], [80].

Few of the common voltage source converter topology is two level VSC, three level neutral point clamped VSC, three level flying capacitor VSC and four level flying capacitor VSC [81-85]. All these topologies have certain advantages and disadvantages for specific applications. Since the two level VSC offers wider flexibility in design and operation, it is utilized to develop the microgrid models in this

research. Blasko et al. [86] developed a simple mathematical model of VSC. The method of technical optimum and the method of symmetrical optimum is utilized by them to calculate the time constants and gain of the voltage and current regulators. But it is observed that a small ripple in the dc bus voltage increased total harmonic distortion (THD) [86]. Even the improper selection of the passive elements of the ac and dc side of the VSC can lead to an unstable operation [87], [88]. Researchers have introduced different order LCL filter to the ac side of the VSC to decrease the harmonics contents and improve the dynamic performance of the overall system [89-91].

1.3. POWER SHARING IN A MICROGRID

Power sharing in an interconnected ac/dc microgrid in a controlled manner has remained a challenge with the growth of power generation from the RES. Rodriguez et al proposed a system with optimized use of battery storage and reduced dependency on utility grid to support the required amount of power in an interconnected ac/dc microgrid [73]. In [9], [10], autonomous control of interconnected ac/dc microgrid is discussed based on normalizing the droop coefficients. But Qi et al [92] pointed out that large frequency variation leads to poor performance of the microgrid system in the aforementioned method. Xia et al [93] mentioned that most of the methods to date are only applicable if multiple microgrids have similar power ratings and to address this issue, a distributed coordination power control strategy is adapted. In their research, a battery storage supports the ac side voltage and the IC is designed to provide voltage support to the dc side of IC. In [48], a bidirectional switch has been used to control the power flow between the two sides of the interconnected ac/dc microgrid.

In the following section, power sharing during an islanded mode of operation is described. During an islanded mode of operation, the DGs inside an ACMG or a DCMG generate power according to their droop gains. Proportional DG generation and load sharing is achieved within the microgrid.

1.3.1. DCMG DROOP CONTROL

Usually DCMG operates in voltage droop [47]. The output voltage of distributed generations (DG) in a microgrid is regulated depending on current or power [44], [94]. Khorsandi et al estimated the line resistances to design and tune the droop gains to improve current sharing accuracy [95]. Tah et al proposed an enhanced droop control method taking the line resistances into account, while [96] proposes a coordinated control algorithm to control the power flow in islanded and grid connected mode.

1.3.2 ACMG DROOP CONTROL

The real power sharing in the ACMG is controlled by regulating the frequency of the DGs to a desired range at its point of connection [47]. The reactive power flow is controlled by the voltage magnitude of the DGs in the ACMG. This method shows a slow transient response [5], [97]. During transients, an ACMG can become unstable if it has some converter interface in between the DGs and the ac bus. Integral droop line method can be utilized in this type of scenario to improve power sharing accuracy [30].

The real power distribution in an ACMG can also be controlled by regulating the voltage angle. The angle droop control is best suited for an ACMG where all the DGs are connected to the ac bus with a converter interface [19]. Similar to the frequency droop control, angle droop control method does not require any communication channel. However, this method is dependent on the output inductance of the DGs. An improved droop controller is proposed by the researchers [99-100] which are robust irrespective of system parameters and disturbances.

1.4 STABILITY OF MICROGRID

With more RES getting connected to the existing grid, it is required to ensure a stable operation of the microgrids at utility grid connected mode and islanded mode [101]. Researchers have investigated the stability of ACMG and DCMG with their associated droop principles [102], [103]. Marwali et al. considered a system with paralleled DGs operating in phase and voltage angle droop to analyse the stability [102]. Majumder et al. conducted an eigenvalue analysis for an autonomous microgrid

which is valid for complex network with multiple DGs and loads [103]. In their analysis, all the DGs are connected to the ac grid with VSCs which are modelled in state space domain. Droop sharing is adapted and designed in state space domain as well.

Researchers have reported the stability analysis of a DCMG with a DG feeding a single load in [104-110]. Root locus plot for the adapted controllers and power sharing algorithm is shown. Aroudi et al. and Giaouris et al. extended this method for single-source multiple-load systems [111], [112]. All these studies only considered a voltage source to represent the DGs and did not consider the interfacing dc converters in the stability analysis. As the operation of the dc converter is comprised of multiple configurations in a specific switching cycle, the network is designed including the converters incorporating their different switching configurations. Subsequently, the converters' controller design and droop sharing are incorporated in the DCMG model for stability analysis.

Different methods of mathematical approaches has been utilized by the researchers for stability analysis [102], [113], [114]. Aroudi et al extended the approach of dynamic controller with a feedback compensator [111]. Giaouris et al. utilized Filippov's method for analysing stability of dc converters in continuous conduction mode (CCM) [112]. In this research, all the dc-dc converters are modelled and combined together with droop equations and the network description for stability analysis.

1.5. POWER TRADING IN INTERCONNECTED SYSTEM

In an electrical network with different types of DGs, power generation and distribution do not depend only on the generation capacity and load at any specific time. It also depends on other factors such as electricity market condition and price of electricity. In general, the aim should be to maximize the generation from the most efficient DGs and to minimize the cost of electricity for the consumers. In addition, fair allocation of the surplus power is required. However, both market condition and price of the electricity can change due to the competition from the new entrants in the market. Fair allocation and competition are not considered in most of the researches.

Nunna et al. [115] introduced an agent-based energy management system which uses demand response and the load profile to formulate power trading in between microgrids. Shi et al. [116] have taken uncertainty of power generation and load into account in their research. Chen et al. [117] proposed microgrid operation optimization based on the market policy.

Samadi et al. [118] used game theoretic approach to utilize the excess generation capacity. However, different market conditions like fair allocation, monopoly and duopoly/oligopoly market are not taken into consideration in their research. Basu et al. [119] and Sinha et al. [120] identified microgrid market as oligopolistic [121] and included different market conditions to formulate electricity pricing in a microgrid system. In our research we have considered a fair allocation of surplus power to the other microgrids. We have also formulated the surplus power distribution at a competitive price at monopoly and duopoly situation using game theoretic approach.

1.6. POWER HARDWARE IN THE LOOP

In the past few years, microgrid concept has seen a significant shift from research stage to the installation and operational phases. Increasing number of distributed energy resources (DERs) are getting connected to the low voltage grid. AS 4777 is also released to incorporate all these new generations to the existing electrical grid in an industry standard way [122]. The standard requires a control over the power flow to and from the electrical grid. Therefore, the existing researches require extensive hardware testing. To address this issue, testing facilities like Power hardware in the loop (PHIL) approach has gained much attention.

There are different methods to implement the new methodologies on a hardware platform. When it comes to a big system like a microgrid where there will be a lots of power electronic converters, it might be a bit complicated to arrange such a big setup even in a small scale. On top of that it will be expensive as well. To alleviate the above mentioned issues, PHIL concept is introduced where a part of the circuit is simulated and the rest is implemented on a hardware platform. The new methodologies are usually implemented on the hardware platform and the rest of the system is

simulated as a virtual circuit. The PHIL concept is an extension of the Hardware in the loop (HIL) concept [123-125]. In PHIL hardware under test (HuT) is implemented on a hardware platform and the rest of the circuit is simulated using a real time simulator. The virtual circuit generates a current or voltage signal of certain magnitude which is later translated as the input from the virtual circuit to the HuT.

Many researchers have demonstrated PHIL setup for microgrid [126-128]. It combines hardware prototype and the virtual circuit in a closed-loop simulation. The control software is executed in the virtual circuit and also to the HuT in co-ordination to assess the practicality of any system under test and to find features to improve before developing the product itself. Huerta et al. presented a PHIL simulation of ACMG comprising of wind turbines and used a voltage source converter as the interface of virtual circuit and HuT [126]. Merabet et al. also integrated batteries and PVs in his HuT to test the PHIL test of a microgrid [128]. As this thesis focuses mostly to the dc side of the microgrid, subsequently a DCMG is used as HuT in this thesis. Kakigano introduced a method to run PHIL test for a DCMG [129]. Weaver et al. presented an approach tying up the dc sources to a common dc bus through dc-dc converters (boost) which also allows to test a hybrid system [130]. In this thesis, a detailed modelling of the interface is presented. Then a hybrid microgrid with the proposed controllers is developed on PHIL architecture and tested to validate the simulation results obtained.

In PHIL the entire network is torn in two segments. This often causes numerical stability problem. Moreover, an improper interface in between the HuT and virtual circuit might introduce some delay in the control system [131]. Ideally, the interface should have unity gain with no time delay but in practical situation the closed loop will add some delay to the system. These issues cause a difference in between the physical system and the PHIL system. However, Kron et al. proposed a method of tearing the network into two or more segments which offers possibilities [132-135]. A schematic diagram of PHIL setup is shown in Fig. 1.5

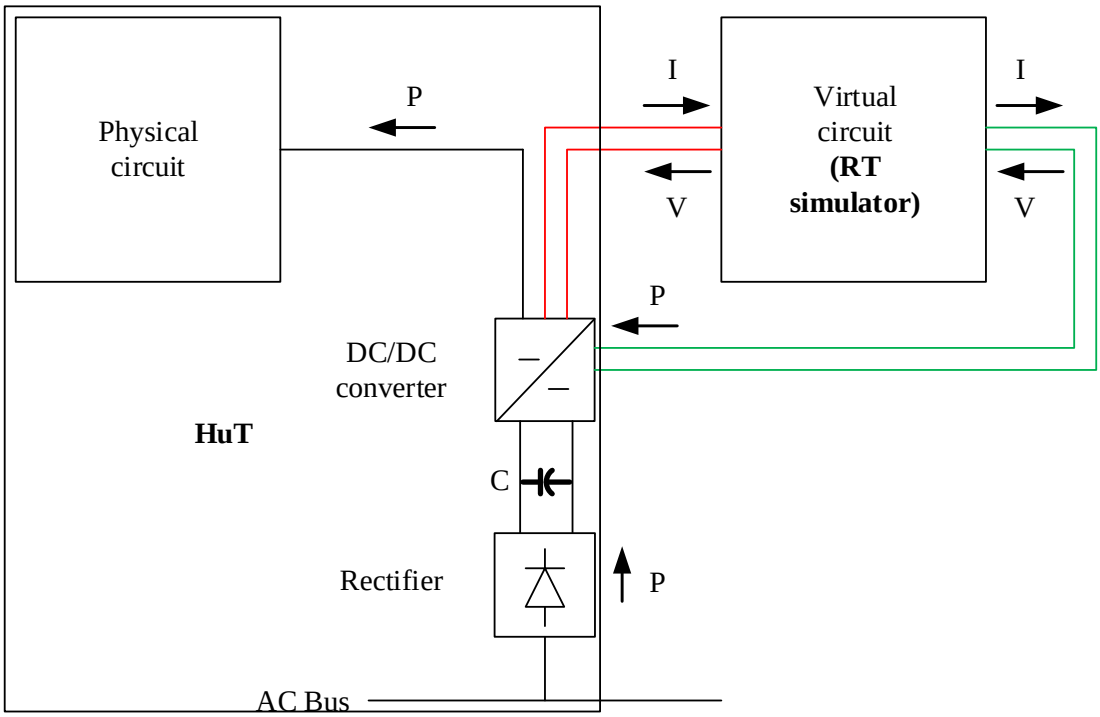

Fig. 1.5 A schematic diagram of PHIL for Unidirectional power flow

1.7 Objectives of the Thesis and Specific Contribution

In this section the objectives of the thesis are discussed. It is followed by the specific contribution of the thesis and an overview of how the thesis is organized over six chapters.

1.7.1. Objectives of the Thesis

The objectives of the thesis is given below:

1. Investigate the different control strategies of the dc-dc converters (buck and boost).
2. Evaluate the stability boundary of a *P-V* and *V-I* droop control of a dc microgrid through eigenvalue analysis.
3. Modelling and control of dual active bridge (DAB) for bidirectional power flow
4. Proposal of operation of interconnected ac-dc system
5. Application of Game theoretic approach for power sharing in microgrid clusters

1.7.2. SPECIFIC CONTRIBUTION OF THE THESIS

The specific contribution of the thesis is discussed below:

1. Dc-dc converter performance is evaluated using discrete-time small signal model (corner point method).
2. Dc-dc converter performance is evaluated using continuous-time small signal model (state space averaging method).
3. A brief analysis to tune PI controller is presented in this thesis
4. Two different linearization procedures and three different controllers are presented and utilized to evaluate dc-dc converter performance during nominal operation, load and input voltage change.
5. The stability of a DCMG operation is investigated through small-signal modelling. The converters in the DCMG are modelled using state space averaging technique. Combining the converter and the network models, a homogeneous model of an autonomous DCMG is developed. The trajectory of the eigenvalues is identified with a detailed eigenvalue analysis. The effect of droop control parameters and the load variations on the system stability is investigated.
6. Three control techniques for proportional load sharing in a utility-connected dc microgrid are discussed. The dc microgrid is connected to a utility system through an interlinking voltage source converter. On the dc side of the IC, a power flow controller (PFC) is connected. Three different PFCs are considered. In the first case, a dc-dc converter is connected at the dc side of the IC to facilitate unidirectional power flow from the utility to the DCMG. In the second case, a bidirectional switch is employed to facilitate bidirectional power flow from the utility to DCMG or the other way around. Finally a dual active bridge (DAB) is employed for bidirectional power flow.
7. A detailed analysis and control design for a DAB are also presented. A new power flow control strategy for the DAB is proposed based on discrete-time state feedback with integral control. For this, a linearized model of the DAB has been designed based on the nominal power transfer condition. The veracity of the scheme is verified through both simulation and experimental results.

8. The operation and control of an ac/dc interconnected microgrid are discussed. The ac microgrid is connected to the dc microgrid through an interlinking converter. On the dc side of the interlinking converter a bidirectional switch or a DAB are used to control the power flow in between the microgrids. In the proposed system operation, either of the microgrids draws the exact amount of power that is required for preventing a system collapse. It is to be note here that it has been assumed that the ACMG is able to supply power to the DCMG during its power shortfall and vice versa.
9. Power sharing for a system configuration where an ACMG is connected to multiple DCMGs through an IC and multiple DABs is presented in this thesis. This model eliminates the effect of circulating current in an interconnected microgrid cluster.
10. Multiple approaches for power reference selection at different market condition for an interconnected microgrids are also discussed in this thesis. Perfect market condition and also monopoly and duopoly market condition are considered to analyse the amount of power to be delivered in between the microgrids.
11. The power hardware-in-the-loop (PHIL) concept is used to test a coupled AC-DC microgrid.

1.7.3. THESIS ORGANIZATION

The contents of this thesis are organized into eight chapters. In the first chapter, the topics covered in this thesis are introduced and an overall picture of the whole thesis is presented. Three research articles have been already published. These are as follows:

[a] Datta, Amit Jyoti, Arindam Ghosh, Firuz Zare, and Sumedha Rajakaruna. "Bidirectional Power Sharing in an AC/DC system with a Dual Active Bridge Converter." IET Generation, Transmission & Distribution (2018).

[b] Datta, Amit Jyoti, Arindam Ghosh, and Sumedha Rajakaruna. "Power sharing in a hybrid microgrid with bidirectional switch." In Power & Energy Society General Meeting, 2017 IEEE, pp. 1-5. IEEE, 2017.

[c] Datta, Amit Jyoti, Arindam Ghosh, and Sumedha Rajakaruna. "Power sharing and management in a utility connected DC microgrid." In Australasian Universities Power Engineering Conference (AUPEC), 2017, pp. 1-6. IEEE, 2017..

In Chapter 2, the structure of dc-dc converters and different control strategies are depicted. A small signal model of the dc-dc converters is developed in discrete time domain and continuous time domain. It is followed by the design of proportional-integral controller, state feedback controller in corner point method and state space averaging based method. This chapter is concluded with simulation results and a numerical study of dc-dc converter parameter selection process. Corner point method is used in [a-c]

In Chapter 3, the operation of DCMG is discussed followed by stability analysis. The conventional *P*-*V* and *I*-*V* droop control theories are explored. The impact of droop gain selection in power sharing is also discussed. Since, the state space averaging method allows to design each converters in the DCMG in the continuous time domain based on its average over one cycle, it is used to develop a state space model of a two converter DCMG. The control law and the homogenous equation is derived for an eigenvalue analysis using both *P*-*V* droop method and *I*-*V* droop method.

Three control techniques for proportional load sharing in a utility-connected dc microgrid are discussed in Chapter 4 On the dc side of the IC, a power flow controller (PFC) is connected to control the power flow in the utility connected DCMG. Three different PFCs are considered. In the first case, a dc-dc converter is connected at the dc side of the IC to facilitate unidirectional power flow from the utility to the DCMG. In the second case, a bidirectional switch is employed to facilitate bidirectional power flow from the utility to DCMG or the other way around. Followed by these, a detailed analysis and control design for a DAB are also presented. A new power flow control strategy for the DAB is proposed based on discrete-time state feedback with integral control. Finally a dual active bridge (DAB) is used as PFC to facilitate bidirectional power flow. All these analysis are verified through simulation studies. The operation of DAB is verified with a hardware setup. DAB modelling and its performance is published as [a]. The use of bidirectional switch as PFC is published as [b] and dc converter as PFC is published as [c].

ACMG operation through frequency droop control is explored in Chapter 5. The nominal operation, power shortfall in ACMG and DCMG in an ac/dc microgrid with bidirectional switch is discussed with associated simulation studies. This study is followed by an analysis of power management in an ac/dc microgrid with a DAB.

In Chapter 6, the performance of multiple dc sub-grids tied up to the ACMG/utility grid is investigated. All four possible cases for the interconnected system is assessed. Ac to dc power supply and vice versa are explored with extensive simulation studies. These studies are followed by the case study of power supply to a DCMG from the ACMG and the other DCMG. Power supply to a DCMG and ACMG from the other DCMG is also verified with the newly proposed system architecture. Finally, a game theoretic approach is discussed for the proposed system architecture at different market condition. Power transfer reference is selected by optimizing the power generation cost. Shapely value is utilized to formulate the power flow from the ACMG to DCMGs. Price leadership model is utilized to control the power flow from the DCMGs to the ACMG at monopoly market situation and Stackleberg model adopted at duopoly market situation.

The hardware results of an interconnected DCMG are presented in Chapter 7. Hardware test setup for islanded mode of operation is presented and the proposed control algorithms are verified through the set up. Followed by this, constant power supply to the DCMG is verified by using a PFC. Proposed PFC control is implemented in the dc converter. Finally a PHIL concept is utilized to analyse the performance of an interconnected ac-dc microgrid.

Finally, the thesis is concludes in Chapter 8 with concluding remarks and potential future works in continuation to this thesis.

CHAPTER 2

DC-DC CONVERTER STRUCTURE AND CONTROL

Dc-Dc converters play a vital role in the interface of the dc energy sources to ac and/or dc grids. These converters receive electric power from the dc energy sources and deliver that power at a defined voltage level. For this, the output voltage of a dc-dc converter has to be regulated around the desired voltage. In this chapter, two different types of dc-dc converters are considered and their three different control strategies are discussed. It is to be noted that all the discussed control strategies can be applied in the same fashion to either buck, boost or buck-boost converters. However the control techniques are explained with a buck and a boost converter in this chapter since these two are used subsequently in dc microgrid applications. The control of buck-boost converters are discussed in Appendix 9.1.

The three control methods presented in this chapter are designed with (a) state feedback with integral controller and (b) proportional plus integral (PI) controller. For the state feedback controller design, a linearized model of the converter is required. Two different methods are employed here. They are (a) discrete-time model based on state transition equation and (b) a continuous time state space averaged model. In the former method, the state evolution over a switching cycle is defined and is then linearized [66, 69]. Since this defines the switching behaviour at the start of a switching cycle, it is termed as the corner point method. It will be shown that both the state feedback controllers can perform in a wide operating range and can hold the output voltage to a constant magnitude irrespective of the input or load fluctuations These features are really advantageous in the utility applications since the renewable energy are often intermittent in nature. First a method for obtaining the steady state condition is discussed. This will be followed by the discussion state feedback and PI controllers.

2.1. DISCRETE-TIME SMALL SIGNAL MODEL (CORNER POINT)

In this section a procedure to calculate the steady state value of a dc-dc converter is discussed. Steady state values of buck, boost and buck-boost converter

can be calculated following this procedure. The steady state calculation procedure for only the buck converter is discussed below.

The schematic diagram of a dc-dc buck converter is shown in Fig. 2.1 (a). It contains a switch *S* that is periodically switched on and off in duty ratio control, a diode, which allows the current to flow in only one direction, and three passive elements. The converter is said to be in continuous conduction mode (CCM) if the inductor current does not need to be blocked by the diode; otherwise it is said to be in discontinuous conduction mode (DCM) [67]. In this analysis, only CCM mode of operation is considered.

The operation of the switch *S* is shown in Fig. 2.1 (b). If the switching frequency is *f*, then the time period between two successive switching is $T = 1/f$. From Fig. 2.1 (b), following equations can be written

$$\begin{aligned} t_2 - t_0 &= T \\ t_1 - t_0 &= dT \\ t_2 - t_1 &= (1-d)T \end{aligned} \tag{2.1}$$

where d, $0 \le d \le 1$, is called the duty ratio.

The equivalent circuit when the switch is closed is shown in Fig. 2.1 (c) and when the switch is open is shown in Fig. 2.1 (d). Let the system state vector be defined as $x = [V_0 \;\; i_L]^T$. Then the state space equation when the switch is closed given by

$$\dot{x} = A_1 x + B_1 V_{dc} \tag{2.2}$$

and when the switch is open is given by

$$\dot{x} = A_2 x + B_2 V_{dc} \tag{2.3}$$

where

$$A_1 = A_2 = \begin{bmatrix} -1/RC & 1/C \\ -1/L & 0 \end{bmatrix}, \quad B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

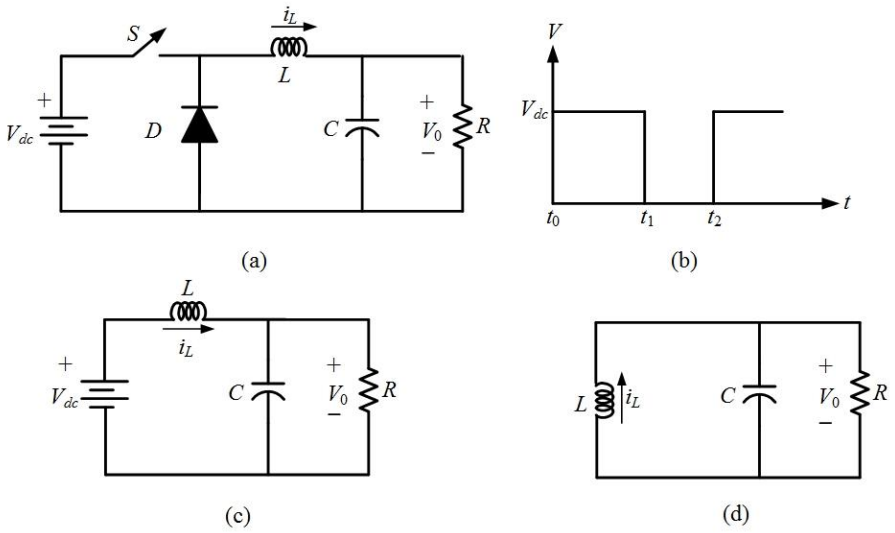

Fig. 2.1. (a) Schematic diagram of a buck converter; (b) its switching sequence; equivalent circuit when the switch (c) is closed and (d) is open.

Since the capacitor voltage is desirable output, the output equation for both these cases is

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} x = C_1 x \tag{2.4}$$

Since V_{dc} is constant, the solution of the state equation (2.2) is given by

$$x(t_1) = e^{A_1(t_1 - t_0)} x(t_0) + \left\{ \int_{t_0}^{t_1} e^{A_1(t_1 - \tau)} d\tau \right\} B_1 V_{dc} \tag{2.5}$$

Substituting (2.1) in the above equation, we get

$$x(t_1) = e^{A_1 dT} x(t_0) + \left\{ \int_{0}^{dT} e^{A_1(dT - \tau)} d\tau \right\} B_1 V_{dc} \tag{2.6}$$

Since A_1 is non-singular, the solution of (2.5) is given as

$$\begin{aligned} x(t_1) &= e^{A_1 dT} x(t_0) - A_1^{-1} \left(e^{A_1(dT - \tau)} \right) \Big|_0^{dT} B_1 V_{dc} \\ &= e^{A_1 dT} x(t_0) - A_1^{-1} \left(I - e^{A_1 dT} \right) B_1 V_{dc} \\ &= e^{A_1 dT} x(t_0) - A_1^{-1} B_1 V_{dc} + A_1^{-1} e^{A_1 dT} B_1 V_{dc} \end{aligned} \tag{2.7}$$

Similarly, the solution of (2.3) is

$$x(t_2) = e^{A_1(t_2-t_1)}x(t_1) = e^{A_1(1-d)T}x(t_1) \tag{2.8}$$

Substituting (2.7) in (2.8), we get

$$\begin{aligned} x(t_2) &= e^{A_1(1-d)T}x(t_1) \\ &= e^{A_1(1-d)T}\left[e^{A_1 dT}x(t_0) - A_1^{-1}B_1V_{dc} + A_1^{-1}e^{A_1 dT}B_1V_{dc}\right] \\ &= e^{A_1(1-d)T}e^{A_1 dT}x(t_0) + e^{A_1(1-d)T}\left[-A_1^{-1} + A_1^{-1}e^{A_1 dT}\right]B_1V_{dc} \\ &= e^{A_1 T}x(t_0) + \left[-e^{A_1(1-d)T}A_1^{-1} + A_1^{-1}e^{A_1 T}\right]B_1V_{dc} \end{aligned} \tag{2.9}$$

Defining the instant $t_0 = k$ and $t_2 = k + 1$, the above equation can be written in a discrete-time state space form as

$$x(k+1) = e^{A_1 T}x(k) + \left[-e^{A_1(1-d)T}A_1^{-1} + A_1^{-1}e^{A_1 T}\right]B_1V_{dc} \tag{2.10}$$

2.1.1. STEADY STATE CALCULATION

For a fixed duty ratio $d = d_0$, in the steady state, $x(k + 1) = x(k)$. Therefore, from (2.10), the steady state space vector is given by

$$\begin{aligned} x_0 &= x(k+1) = x(k) \\ &= \left(I - e^{A_1 T}\right)\left[-e^{A_1(1-d_0)T}A_1^{-1} + A_1^{-1}e^{A_1 T}\right]B_1V_{dc} \end{aligned} \tag{2.11}$$

In a dc-dc converter, both the capacitor voltage and the inductor current go through periodic charging and discharging due to switching action. Therefore the steady state values obtained before is only valid at the corner points. However, if the capacitor size is relatively large and the switching frequency is high, the ripple can be assumed to be negligible. In that case, the values obtained from (2.11) can be safely assumed to be steady state average values for small signal derivation when dealing with state space averaging. The corner point method needs these values any way. A method for a more accurate average calculation is outlined in [66].

2.1.2. SMALL SIGNAL CORNER POINT MODEL

In this sub-section, a discrete-time linearized model for the system described by equation (2.10) is derived. For this, the steady state and perturbed values are defined as

$$x = x_0 + \Delta x, \quad d = d_0 + \Delta d \tag{2.12}$$

where the subscript 0 denotes the steady state values around which the linearization takes place and Δ denotes its perturbation. The following state space description is obtained by linearizing (2.11) with respect to x and d.

$$\Delta x(k+1) = e^{A_1 T}\Delta x(k) + (G_1 B_1 V_{dc})\Delta d(k) \tag{2.13}$$

where

$$G_1 = A_1 T e^{(1-d_0)TA_1} A_1^{-1}$$

The output equation is then given by

$$\Delta y(k) = C_1 \Delta x(k) \tag{2.14}$$

The corner point model derivation for the boost and buck-boost converters are discussed in Appendix A.

2.2. CONTINUOUS-TIME STATE SPACE AVERAGE SMALL SIGNAL MODEL

State space averaging technique is introduced by R. D. Middlebrook and S. Cuk [67]. For a boost converter, the two switching intervals and the equivalent circuits for these two intervals are shown in Fig. 2.2.

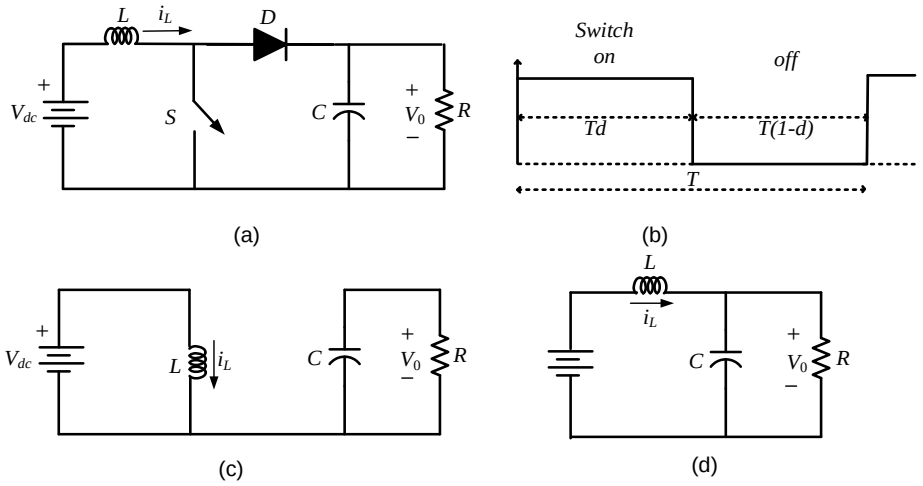

Fig. 2.2 (a) Schematic diagram of a boost converter; (b) Switching sequence for the state space averaging model derivation (c) is closed and (d) is open.

The state space equation for the time interval when the switch is closed ($0 \le t < dT$) is given by the following equation:

$$\dot{x} = A_1 x + B_1 V_{dc} \tag{2.15}$$

and when the switch is open ($dT \le t < T$) is given by

$$\dot{x} = A_2 x + B_2 V_{dc} \tag{2.16}$$

where

$$A_1 = \begin{bmatrix} -1/RC & 0 \\ 0 & 0 \end{bmatrix}, \quad A_2 = \begin{bmatrix} -1/RC & 1/C \\ -1/L & 0 \end{bmatrix}, \quad B_1 = B_2 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix}$$

Let us now assume that the boost converter has a duty ratio of d and the switching time of T. Then the state space average of the boost converter, noting that $B_1 = B_2$, is

$$\begin{aligned} \dot{x} &= \left[A_1 d + A_2 (1-d) \right] x + \left[B_1 d + B_2 (1-d) \right] V_{dc} \\ &= \left[A_1 d + A_2 (1-d) \right] x + B_1 V_{dc} \end{aligned} \tag{2.17}$$

Now (2.17) is linearized around the operating point x_0 and d_0 to obtain

$$\Delta \dot{x} = A \Delta x + B \Delta d \tag{2.18}$$

where

$$A = A_1 d_0 + A_2 (1 - d_0)$$
$$B = [A_1 - A_2] x_0$$

The output equation is

$$\Delta y = [1 \quad 0] \Delta x = C_1 \Delta x \tag{2.19}$$

2.3. PROPORTIONAL-INTEGRAL CONTROL

Proportional-integral control is widely used for constant output voltage regulation of dc converters [67]. This can be achieved by only measuring one state variable. This control action leads to decoupling of input current and output voltage dynamics [67]. This control method is realized for the calculation simplicity it offers. PI controller can be used to set the output voltage to a desired value during fluctuations or transient in the input voltage of the converters. Let us consider an open-loop transfer function of the form

$$G(s) = \frac{(s + z_1)(s + z_2) \cdots (s + z_m)}{(s + p_1)(s + p_2) \cdots (s + p_n)}, \; n \geq m \tag{2.20}$$

With only a proportional (P) controller, the closed-loop transfer function of the system is

$$\frac{Y(s)}{Y_r(s)} = \frac{K_P (s + z_1)(s + z_2) \cdots (s + z_m)}{(s + p_1)(s + p_2) \cdots (s + p_n) + K_P (s + z_1)(s + z_2) \cdots (s + z_m)} \tag{2.21}$$

The steady state output with a unit step response (dc gain) will then be

$$y_{ss} = \frac{K_P \times z_1 \times z_2 \times \cdots \times z_m}{p_1 \times p_2 \times \cdots \times p_n + K_P \times z_1 \times z_2 \times \cdots \times z_m} \tag{2.22}$$

It can be seen from (2.22) that the steady state output can be brought closer to 1 if a large value of K_P is used. However, a large gain may also cause instability by moving the closed-loop poles to the right half *s*-plane.

Alternatively, we may use a PI controller of the form [57, 58, 65, 136, 137]

$$G_C(s) = K_P + \frac{K_I}{s} = \frac{sK_P + K_I}{s}$$

The closed-loop transfer function of the system is then

$$\frac{Y(s)}{Y_r(s)} = \frac{(sK_P + K_I)(s+z_1)(s+z_2)\cdots(s+z_m)}{s(s+p_1)(s+p_2)\cdots(s+p_n)+(sK_P + K_I)(s+z_1)(s+z_2)\cdots(s+z_m)} \tag{2.23}$$

The steady state output with a unit step response will then be

$$y_{ss} = \lim_{s\to 0} \frac{(sK_P + K_I)(s+z_1)(s+z_2)\cdots(s+z_m)}{(sK_P + K_I)(s+z_1)(s+z_2)\cdots(s+z_m)} = 1 \tag{2.24}$$

This implies that the system will not have any steady state error, which is the most desirable attribute of a PI controller. This form of controller is widely used in this thesis not only for the control of dc-dc converters, but also for other power flow controllers.

2.3.1. PI GAIN SELECTION

In this section, a method of PI gain selection is described. The PI gains have to be selected such that the system stays stable. For this analysis a dc-dc converter model is considered, the continuous-time linearized state space model of which is

$$\Delta\dot{x} = A\Delta x + B\Delta d \tag{2.25}$$

The output equation is

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} \Delta x = C_1 \Delta x$$

The transfer function of the system is given by

$$\frac{Y(s)}{\Delta d(s)} = C_1 (sI - A)^{-1} B = G(s) \tag{2.26}$$

The PI controller is considered of the form

$$\Delta d = K_P\left(1+\frac{K}{s}\right)e(s) = K_P\left(\frac{s+K}{s}\right) = G_C(s)e(s) \tag{2.27}$$

The closed-loop transfer function is

$$\begin{aligned}\frac{Y(s)}{Y_{ref}(s)} &= \frac{G_C(s)G(s)}{1+G_C(s)G(s)} = \frac{K_P\left(\frac{s+K}{s}\right)G(s)}{1+K_P\left(\frac{s+K}{s}\right)G(s)} \\ &= \frac{K_P(s+K)G(s)}{s+K_P(s+K)G(s)}\end{aligned} \tag{2.28}$$

From (2.28), the characteristic equation of the system can be written as

$$s+K_P(s+K)G(s)=0 \tag{2.29}$$

Now a simple dc-dc converter has an order of 2. Let us define the open-loop transfer function of the system as

$$G(s) = \frac{b_0 s + b_1}{s^2 + a_1 s + a_2} \tag{2.30}$$

Then the characteristic equation can be expanded as

$$\begin{aligned}&s+K_P(s+K)G(s)=0 \\ &\Rightarrow s\left(s^2+a_1s+a_2\right)+K_P(s+K)\left(b_0s+b_1\right)=0 \\ &\Rightarrow s^3+\left(a_1+K_Pb_0\right)s^2+\left(a_2+K_Pb_1+K_PKb_0\right)s+K_PKb_1=0\end{aligned} \tag{2.31}$$

From (2.31), the following Routh-Hurwitz's table [138] is formed.

$$\begin{array}{lll} s^3 & 1 & \left(a_2+K_Pb_1+K_PKb_0\right) \\ s^2 & \left(a_1+K_Pb_0\right) & K_PKb_1 \\ s^1 & \alpha & \\ s^0 & K_PKb_1 & \end{array} \tag{2.32}$$

where

$$\alpha = \frac{\left(a_1+K_Pb_0\right)\times\left(a_2+K_Pb_1+K_PKb_0\right)-K_PKb_1}{\left(a_1+K_Pb_0\right)} \tag{2.33}$$

For absolute stability, all the elements of the first row of (2.32) must be positive. For positive values of K_P, K and b_1, we have the following conditions

$$\begin{aligned} &a_1 + K_P b_0 > 0 \text{ and} \\ &\left(a_1 + K_P b_0\right) \times \left(a_2 + K_P b_1 + K_P K b_0\right) - K_P K b_1 > 0 \\ &\Rightarrow K_P^2 \left(b_0 b_1 + K b_0^2\right) + K_P \left(a_1 b_1 + a_1 K b_0 + b_0 a_2 - K b_1\right) + a_1 a_2 > 0 \end{aligned} \tag{2.34}$$

Table 2.1: DC-DC boost converter parameters for stability analysis of PI controller

Parameters	**Values**
Input Voltage, V_{dc}	250 V
Inductor, L	4 mH
Capacitor, C	5000 μF
Switching frequency, f	10 kHz
Load resistance, R_L	2.0808 Ω

Let us now consider a boost converter with the system parameters given in Table 2.1. With these values and for K = 10, the following parameters are obtained

$$\begin{aligned} b_0 &= -8 \times 10^4 \\ b_1 &= 1.25 \times 10^7 \\ a_1 &= 96.12 \\ a_2 &= 1.5 \times 10^4 \end{aligned}$$

Therefore from the limiting condition of (2.34), the following limits are obtained

$$\begin{aligned} &96.12 > 8 \times 10^4 K_P \\ &\Rightarrow K_P < 0.0012 \end{aligned}$$

$$\begin{aligned} &-10 \times 10^{11} K_P^2 - 2.019 \times 10^8 K_P + 1.4437 \times 10^6 > 0 \\ &\Rightarrow \left(K_P + 0.0013\right)\left(K_P - 0.0011\right) > 0 \end{aligned}$$

From the above two condition, we find that K_P is bounded in a very small region, given by

$$0.0011 < K_P < 0.0012$$

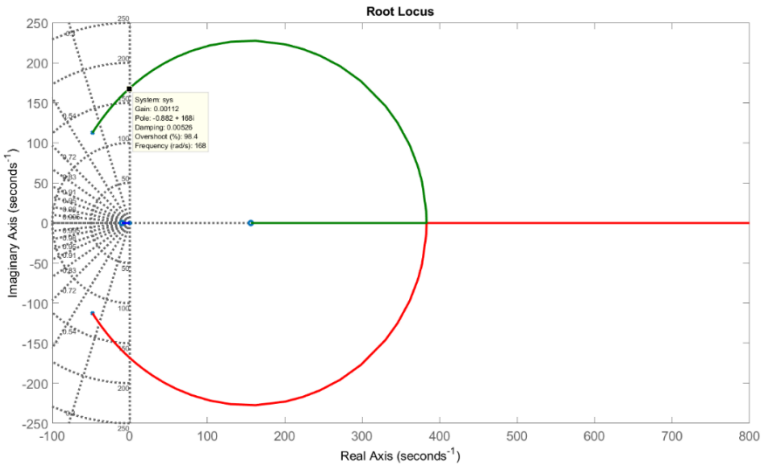

Fig. 2.3. Root locus plot for the boost converter P gain selection.

The root locus plot is shown in Fig. 2.3. From the Routh-Hurwitz condition it can be seen that K_P has to be selected in between a small range of 0.0011 and 0.0012. An approximate value can also be selected from the crossing of the imaginary axis from this figure by clicking at the imaginary axis crossing point. As can be seen from Fig. 2.3, for a proportional gain (K_P) of 0.00112, one of the pole is located at – 0.882 + j168. The closed-loop is still stable, but is on the verge of instability. This agrees with the stability condition obtained before.

Now the characteristic equation (2.31) can be rewritten as

$$\begin{aligned} & s^3 + \left(a_1 + K_P b_0\right) s^2 + \left(a_2 + K_P b_1 + K_P K b_0\right) s + K_P K b_1 = 0 \\ & \Rightarrow 1 + K \frac{K_P b_0 s + K_P b_1}{s^3 + \left(a_1 + K_P b_0\right) s^2 + \left(a_2 + K_P b_1\right) s} = 0 \end{aligned} \tag{2.35}$$

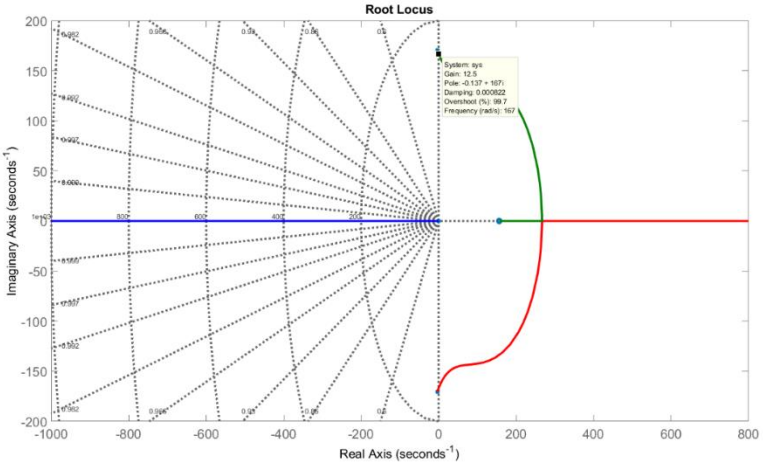

Fig. 2.4. Root locus plot for the boost converter I gain selection.

With K_P = 0.00112, the integral gain K is now varied. The root locus plot is shown in Fig. 2.4. From this plot it can be seen that for K around 13, the poles cross over to the imaginary axis. The system is more stable for a lower value of K. However, this will impact the settling time.

2.4. STATE FEEDBACK CONTROL DESIGN

In this section, two state feedback control laws with integral control are designed. One of these is a discrete-time controller for the corner point method, while the other is a continuous-time controller for the state space average method.

2.4.1. CORNER POINT METHOD

Consider the discrete-time model of (2.13) and (2.14). The purpose of the integral control is to track a reference for the output voltage. For this, the discrete-time equivalent of the integral controller is chosen which is given by

$$\begin{aligned} e(k) &= \Delta y(k) - \Delta y_{ref}(k) \\ z(k) &= z(k-1) + K_I e(k) \end{aligned} \tag{2.36}$$

where y_{ref} is the reference voltage. Equation (2.36) is expanded as

$$\begin{aligned} z(k+1) &= z(k) + K_I\left[\Delta y(k) - \Delta y_{ref}(k)\right] \\ &= z(k) + K_I C_1 \Delta x(k) - \Delta y_{ref}(k) K_I \end{aligned} \tag{2.37}$$

An extended state vector is now defined as

$$x_e(k) = \begin{bmatrix} \Delta x(k) \\ z(k) \end{bmatrix}$$

Combining (2.37) with (2.13), the following extended state space model is obtained

$$x_e(k+1) = \begin{bmatrix} e^{A_1 T} & 0 \\ K_I C_1 & 1 \end{bmatrix} x_e(k) + \begin{bmatrix} G_1 B_1 V_{dc} \\ 0 \end{bmatrix} \Delta d(k) - \begin{bmatrix} 0 \\ K_I \end{bmatrix} \Delta y_{ref}(k) \tag{2.38}$$

A state feedback controller [5] is then designed that is of the form

$$\Delta d(k) = -K x_e(k) \tag{2.39}$$

which will force the output error $e(k)$ to zero asymptotically.

2.4.2. STATE-SPACE AVERAGING BASED CONTROL

A state feedback with integral control will now be developed for the linearized state space equation with state space averaging. The block diagram of the scheme is shown in Fig. 2.5. At first a state feedback controller of the following form is designed

$$\Delta d = -K\Delta x \tag{2.40}$$

To eliminate the steady state error, an integral controller of the following form is introduced

$$z = \int \left(\Delta y_r - \Delta y\right) dt \Rightarrow \dot{z} = \Delta y_r - \Delta y \tag{2.41}$$

The control law is then modified to include this integral action as per

$$\Delta d = -K\Delta x + K_I z \tag{2.42}$$

where K_I is the integral gain.

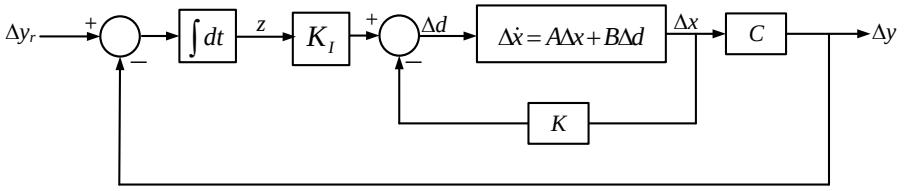

Fig. 2.5. Block diagram of state feedback with integral control.

Let us now define and extended state vector as $x_e = [\Delta x \quad z]^T$. Then combining (2.42) with (2.18) and (2.19), we get the extended state space equation of the following form

$$\dot{x}_e = \begin{bmatrix} A - BK & K_I B \\ -C_1 & 0 \end{bmatrix} x_e + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} \Delta y_r = F x_e + G \Delta y_r \tag{2.43}$$

2.5. SIMULATION RESULTS

2.5.1. CONVERTER PERFORMANCE WITH STATE SPACE AVERAGING METHOD

Let us consider a boost converter with the following parameters:

V_{dc} = 250 V, L = 4 mH, C = 5000 μF, R = 2.08 Ω and f = 10,000 Hz.

The steady state duty ratio is chosen as d_0 = 0.4519. The steady state output voltage and inductor current are respectively computed as 456.12 V and 400.12 A. A linear quadratic regulator (LQR) [12-15] state feedback controller is now designed with the following parameters

$$Q = \begin{bmatrix} 10 & 0 \\ 0 & 1 \end{bmatrix}, \quad r = 0.1$$

The resultant gain matrix is given by K = [–0.9275 7.0466]. The closed-loop transfer function is then given by

$$\frac{\Delta Y(s)}{\Delta Y_r(s)} = \frac{-1.6 \times 10^7 s + 2.5 \times 10^9}{s^3 + 8.8 \times 10^5 s^2 + 1.27 \times 10^8 s + 2.5 \times 10^9}$$

It is obvious that the dc gain is 1. And the eigenvalues (poles) of the system are located at -8.77×10^{5}, -121.11 and -23.52.

With the system operating in the steady state at the nominal operating point, the reference voltage is changed to 600 V at 0.1 s. These results are shown in Fig. 2.6. It can be seen that the system settles within about 0.15 s. The results of Fig. 2.7 is for the case when the load resistance is halved at 0.1 s with the output voltage being regulated at 456. 12 V. This means that the load current and hence the inductor current will be doubled from its nominal value. From Fig. 2.7, it is evident that both the duty ratio and the output voltage come back to their steady state values, while the inductor current nearly doubles. These results prove that the controller is very robust and can reject disturbances in load and can track the voltage change reference accurately.

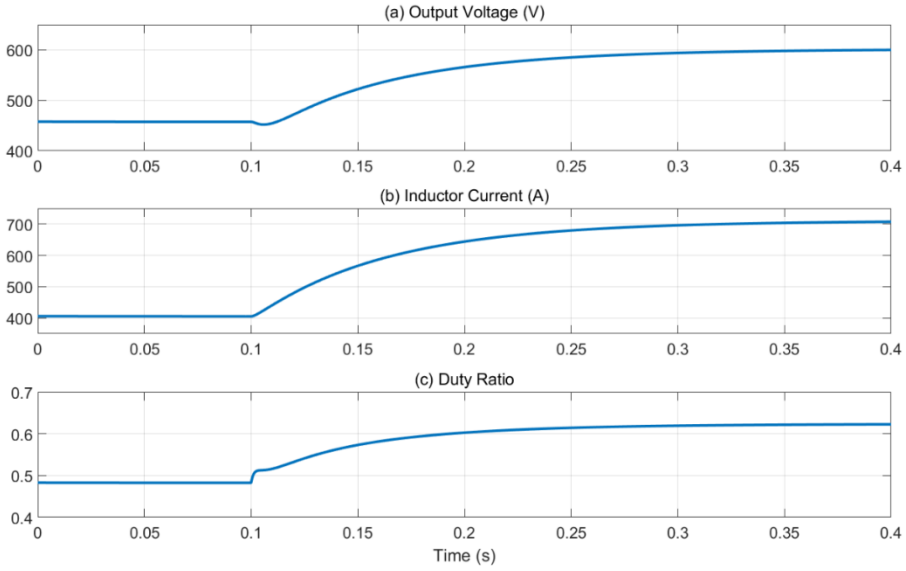

Fig. 2.6. Response for a step change in reference voltage.

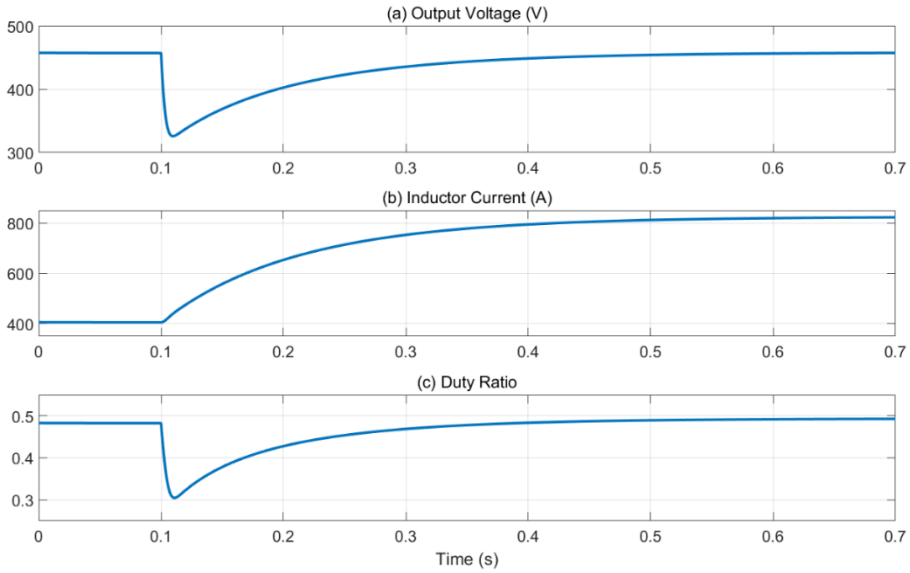

Fig. 2.7. Response for a step change in load.

2.5.2. CONVERTER PERFORMANCE WITH CORNER POINT METHOD

This this case, a buck converter selected with the following parameters:

V_{dc} = 2500 V, L = 4 mH, C = 250 μF, R = 1 Ω and f = 10,000 Hz.

It is to be noted that for a buck converter, the output voltage is duty ratio times the input voltage.

At the beginning, the duty is set to 0.2. This, for the input voltage of 2.5 kV, indicates that the output voltage will be 500 V and the output power will be $500^2/1$ = 250 kW. At 0.3 s, the output voltage reference is increased to 600V. To perform the voltage tracking, the duty increases to 0.24 and the output power increases to 360 kW. At 0.6 s, the input voltage is changed to 2 kV. Since the proposed controller can hold the output voltage irrespective of any input voltage variations, after a small transient, the output voltage settles to 600V. However the duty ratio is changed to 0.3 as expected. Finally at 1 s, the load resistance is changed to 0.5 Ω, thereby doubling the load power. It can be seen from Fig. 2.8 that even though the load changes to 720 kW, the output voltage and the duty ratio remain the same.

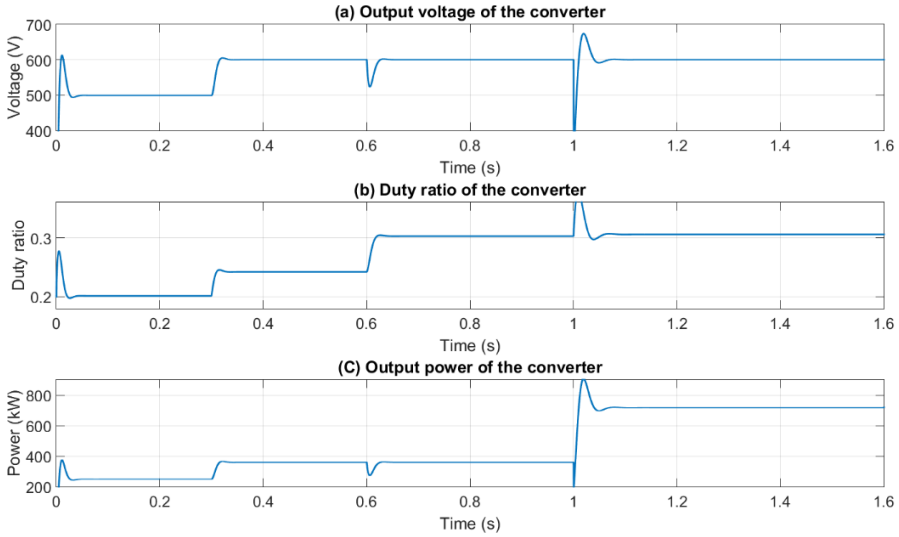

Fig. 2.8. Buck converter performance when the output voltage reference, input voltage and load are changed.

2.5.3. CONVERTER PERFORMANCE WITH PI CONTROLLER

For the performance study of the dc-dc converters with PI controller, the boost converter of the Sub-section 2.5.2 is chosen. The proportional gain K_P is chosen as 0.00112 and the integral gain (K) is chosen as 10, as per Sub-section 2.3.1. The results are shown in Fig. 2.9.

At the beginning, the duty is set to 0.5. This, for the input voltage of 250 V, indicates that the output voltage will be 500 V and the output power will be $500^2/1$ = 250 kW. At 2 s, the output voltage reference is increased to 600V. To perform the voltage tracking, the duty increases to 0.58 and the output power increases to 360 kW. At 3 s, the input voltage is changed to 300V. After a small transient, the output voltage settles to 600V. However the duty ratio is changed to 0.5 as expected. Finally at 4 s, the load resistance is changed to 0.5Ω, thereby doubling the load power. It can be seen from Fig. 2.9 that even though the load changes to 720 kW, the output voltage and the duty ratio remains the same. It can be observed from the Fig. 2.9 that the converter output voltage and power with PI controller have more ripple than Fig. 2.8.

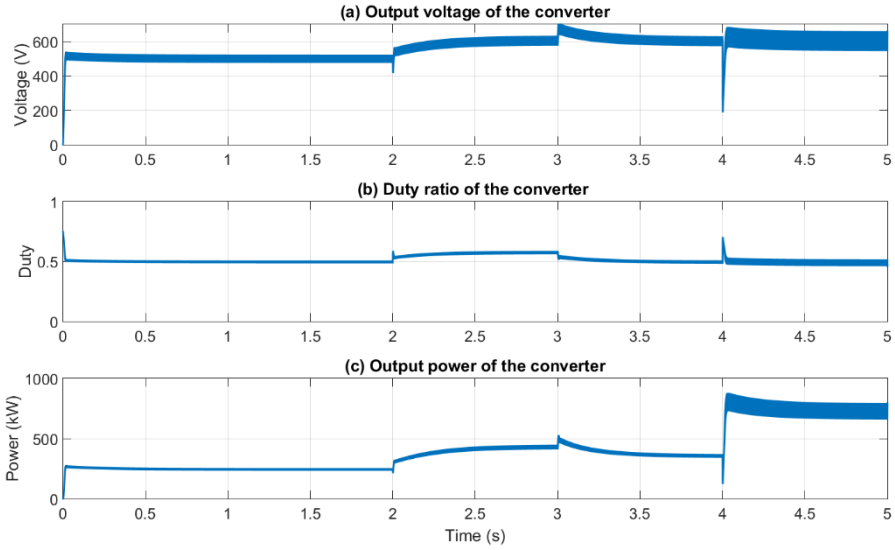

Fig. 2.9. Boost converter performance when the output voltage reference, input voltage and load are changed.

2.6. PARAMETER SELECTION PROCESS

The main idea is to operate the any dc-dc converter in a CCM. Below a simple method is discussed, which guarantees this. Consider the following system parameters for a buck converter.

$$L = 4 \text{ mH},\ C = 250\ \mu\text{F},\ R = 10\ \Omega,\ V_{dc} = 500 \text{ V},\ f = 10 \text{ kHz},\ T = 1/f$$

The nominal duty ratio (d_0) is chosen as 0.5. This gives the following steady state quantities

$$x_0 = \begin{bmatrix} 249.9995 \text{ V} \\ 23.4372 \text{ A} \end{bmatrix}$$

The steady state response for the buck converter is shown in Fig. 2.10.

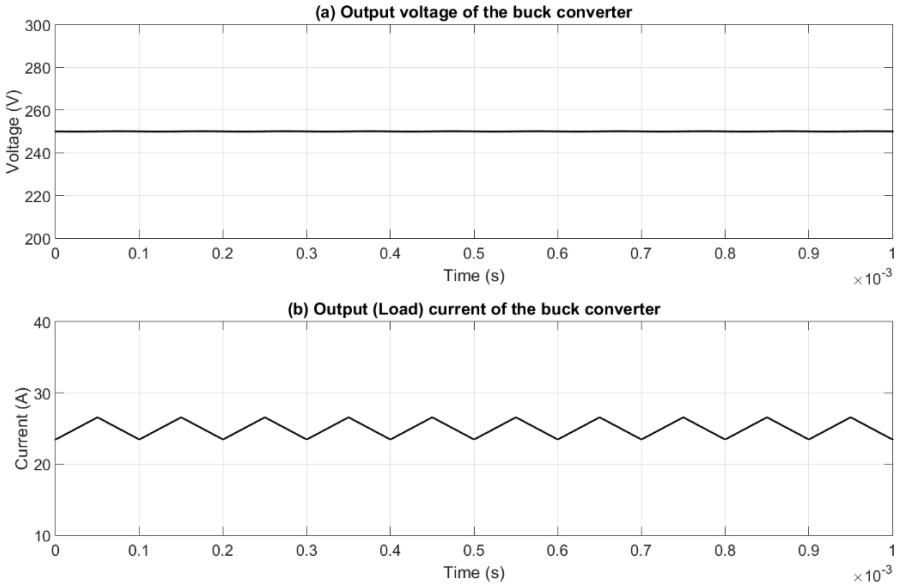

Fig. 2.10. Buck converter performance when L= 4mH.

To evaluate the performance of the buck converter, the inductor L is decreased to 0.4 mH. This gives a nominal state vector of

$$x_0 = \begin{bmatrix} 249.9948\ \text{V} \\ 9.3424\ \text{A} \end{bmatrix}$$

As the inductor value is reduced, the current ripple increases significantly, as shown in Fig. 2.11.

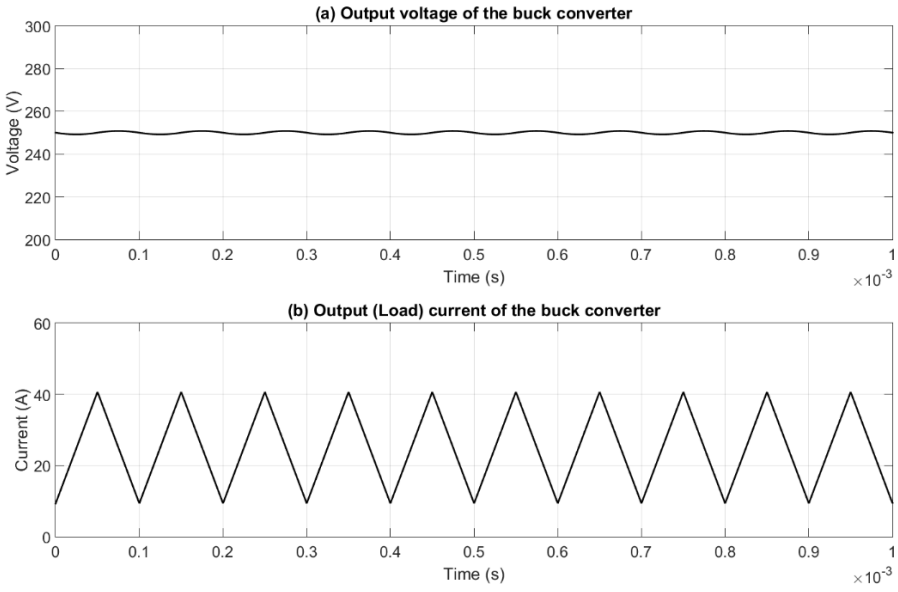

Fig. 2.11. Buck converter performance when L= 0.4 mH.

Finally, when the inductor value is decreased to 0.26 mH, the buck converter no longer operates in CCM. The steady state value for this case is given by

$$x_0 = \begin{bmatrix} 249.9916 \text{ V} \\ -0.0837 \text{ A} \end{bmatrix}$$

Since the inductor current is negative, it shows that the solution is not feasible under the formulation presented before. Therefore, following this procedure, both the inductor and capacitor values can be chosen such that the ripples remain within acceptable ranges.

2.7. CONCLUSION

In this chapter, two different linearization procedures and three different controllers are presented. It has been shown that the state feedback controllers are more robust that the PI controller. The PI controller lacks in tracking accuracy, error minimization and mostly sensitive to any input transients. However it is easier to implement in a hardware set up.

The corner point model is a discrete-time model and therefore depends on the switching frequency. This can be problematic for system dynamic analysis for a system, where several dc-dc converters are connected. This can be performed assuming that all the converters have the same switching frequency and also the triangular PWM waveforms are synchronized. The assumptions are unrealistic.

The advantage of state space averaging method, which presents a continuous-time model, calculates the average between two successive switching instants. Therefore this method is independent of switching frequency is hence is extremely suitable for dynamic analysis. This method will be used for eigenvalue analysis of a dc microgrid in the next chapter.

CHAPTER 3

DCMG OPERATION AND STABILITY ANALYSIS

In order to achieve a reliable, extendable and maintainable microgrid system, the DGs, irrespective of power ratings, can be easily connected to or disconnected from the dc grid and should be able to share power with less complexity [139]. The droop control method fulfils the above conditions by providing a decentralized (wireless) power sharing approach, where the power is shared among the DGs in proportion to their power ratings [140, 141]. It is to be noted that a microgrid, whether dc or ac, will only be able to supply the maximum power that its DGs can generate. Therefore the droop gain of each DG needs to reflect its power capacity. In this chapter the theories of droop gain selection for dc microgrids are discussed. Two types of droop control are considered – power versus voltage (P-V) and current versus voltage (I-V). These are discussed first, where the droop gain calculations reflect the power capacity of each DG.

In the later part of this chapter, the stability of a DCMG operation is investigated through small-signal modelling [102, 103, 107, 111, 112, 142-146]. The converters in the DCMG are modelled using state space averaging technique. It is assumed that each converter is equipped with a state feedback with integral control. Combining the converter and the network models, a homogeneous model of an autonomous DCMG is developed. The trajectory of the eigenvalues is identified with a detailed eigenvalue analysis. The effect of droop control parameters and the load variations on the system stability is investigated. The eigenvalue analysis results are verified through simulation studies using PSCAD/EMTDC.

3.1. DC MICROGRID DROOP CONTROL

One of the simplest method of controlling the power sharing among multiple DGs in a microgrid is the droop sharing method. In a DCMG with multiple converters, droop can be defined from their power or current contribution to the loads.

3.1.2. P-V DROOP CONTROL

Let us consider the circuit shown in Fig. 3.1. It contains two dc sources with voltages of V_1 and V_2. These two sources are supplying a resistive load R_L. The resistances R_1 and R_2 denote the feeder resistances. Let us denote the power supplied by dc power source 1 and 2 by P_{dc1} and P_{dc2} respectively.

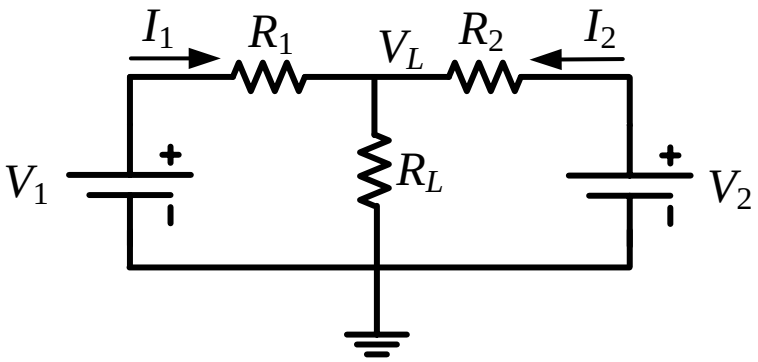

Fig. 3.1. Schematic diagram of a dc microgrid containing two sources.

Two DGs in the DCMG controlled by P-V droop equations is given by

$$\begin{aligned} V_1 &= V_{ref} - n_1 P_{dc1} \\ V_2 &= V_{ref} - n_2 P_{dc2} \end{aligned} \tag{3.1}$$

where V_{ref} is the reference voltage and n_1 and n_2 are the droop gains of DG-1 and DG-2 respectively. It is to be noted from (3.1) that the unit of droop gains is V/kW. The droop gains are calculated in such a way that that the DGs share power according to their ratings.

Let us consider DG-1 first. It has a maximum rating of P_{1max}. The droop gains are so chosen that the maximum voltage drop along the dc feeder is restricted. Let us assume that the maximum voltage drop for each DG is the same and is denoted by ΔV_{max}. Noting that the maximum voltage drop occurs when the DG is supplying its maximum power, we get from (3.1)

$$V_{ref} - V_1 = \Delta V_{\max} = n_1 \times P_{1\max} \tag{3.2}$$

Therefore the droop gain is calculated as

$$n_1 = \frac{\Delta V_{\max}}{P_{1\max}} \tag{3.3}$$

In a similar way, the droop gain of DG-2 is calculated as

$$n_2 = \frac{\Delta V_{\max}}{P_{2\max}} \tag{3.4}$$

From (3.3) and (3.4) it can surmised that ΔV_{max} is the product of the droop gain and maximum power of each DG, i.e.,

$$\begin{aligned} &\Delta V_{\max} = n_1 \times P_{1\max} = n_2 \times P_{2\max} \\ &\Rightarrow P_{1\max} \big/ P_{2\max} = n_2 \big/ n_1 \end{aligned} \tag{3.5}$$

This implies that for the DGs to share power according to their ratings, the droop gains must be reciprocal to their maximum power.

3.1.1. I-V DROOP CONTROL

From Fig. 3.1 the droop equations for a dc microgrid can be written as follows

$$\begin{aligned} V_1 &= V_{ref} - n_1 I_1 \\ V_2 &= V_{ref} - n_2 I_2 \end{aligned} \tag{3.6}$$

From (3.6), it is obvious that the unit of droop gains is Ω. Now from Fig. 3.1, we get

$$V_L = V_1 - R_1 I_1 = V_2 - R_2 I_2 \tag{3.7}$$

Combining (3.6) and (3.7), the following equation is obtained

$$\begin{aligned} &V_{ref} - (n_1 + R_1) I_1 = V_{ref} - (n_2 + R_2) I_2 \\ &\Rightarrow \frac{I_1}{I_2} = \frac{(n_2 + R_2)}{(n_1 + R_1)} \end{aligned} \tag{3.8}$$

Now the power generated by the two sources is given by

$$\begin{aligned} P_1 &= V_1 I_1 \\ P_2 &= V_2 I_2 \end{aligned}$$

Therefore the power ratio is given by

$$\frac{P_1}{P_2} = \frac{V_1 I_1}{V_2 I_2} \tag{3.9}$$

Let us now assume that

$$V_{ref} \approx V_1 \approx V_2$$

Then (3.9) can be written as

$$\frac{P_1}{P_2} \approx \frac{I_1}{I_2} \tag{3.10}$$

Substituting (3.8) in (3.10), we get

$$\frac{P_1}{P_2} = \frac{n_2 + R_2}{n_1 + R_1} \tag{3.11}$$

Now if $n_1 >> R_1$ and $n_2 >> R_2$, the power sharing will be governed by the droop gains, i.e.,

$$\frac{P_1}{P_2} \approx \frac{n_1}{n_2}$$

On the other hand, if $n_1 << R_1$ and $n_2 << R_2$, the power sharing will be governed by the line resistances, i.e.,

$$\frac{P_1}{P_2} \approx \frac{R_1}{R_2}$$

The droop gains are selected much higher than the line resistance. This makes the power generation to be the function of the droop gains. This is illustrated below.

Let us assume that the DGs in a microgrid together will supply a maximum of P_{max} power to its load. Also note that a large voltage drop in the sources is not permitted as this may result in an underutilization of the available power in a dc circuit. Therefore a limit of ΔV_{max} is set for the maximum allowable voltage drop. From Fig. 3.1 the following equation could be written:

$$V_1 = V_L + I_1 R_1$$

Utilizing the equation (3.6) it could be written

$$V_{ref} - n_1 I_1 = V_L + R_1 I_1$$
$$V_{ref} - I_1(n_1 + R_1) = V_L$$

Assuming that for an efficient power sharing the line resistance to be kept negligible to the droop gains, which is $R_1 \approx 0$

$$V_{ref} - n_1 I_1 = V_L$$

Now since $I_1 = P_1/V_1$, the above equation could be written as

$$V_{ref} - \frac{P_1}{V_1} n_1 = V_L$$
$$\Rightarrow V_{ref} - V_L = \Delta V = \frac{P_1}{V_1} n_1 \quad (3.12)$$
$$\Rightarrow n_1 = \frac{V_1 \times \Delta V}{P_1}$$

In a similar way, the droop gain for DG-2 can be written as

$$n_2 = \frac{V_2 \times \Delta V}{P_2} \quad (3.13)$$

Note that if there are N DGs in a microgrid system, the products of droop gains and power ratings follow the following identity irrespective of the droop controller selected (i.e., P-V or I-V)

$$n_1 P_1 = n_2 P_2 = \cdots = n_N P_N \quad (3.14)$$

3.2. EFFECT OF DROOP GAIN SELECTION

Some simple case studies are presented in this section to illustrate the impact of droop gain selection for a network.

Example 3.1. (High I-V Droop Gains): Let us consider the network of Fig. 3.1 with R_1 = 0.01 Ω, R_2 = 0.06 Ω and R_L = 10 Ω. The droop gains are selected as n_1 =

2 Ω and n_2 = 4 Ω, which imply that P_1 should be twice of P_2. The reference voltage V_{ref} is chosen as 2.5 kV. The simulation results are shown in Fig. 3.2.

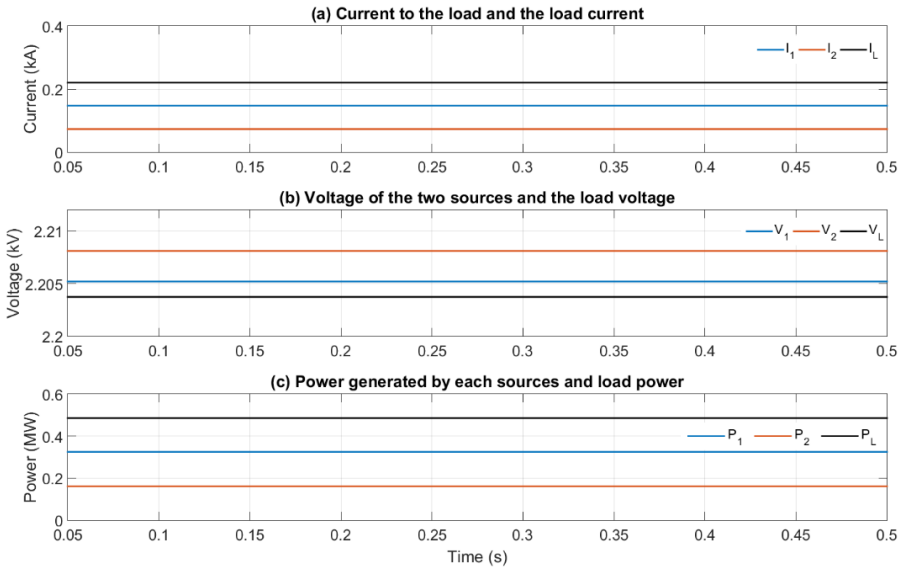

Fig. 3.2. Power sharing with high droop gains.

The total load power demand is 485 kW, P_1 is 325 kW while P_2 is 161 kW. This means that P_1:P_2 = 2:1 (nearly). The currents are I_1 = 147 A and I_2 = 73 A. The voltages V_1 and V_2 are nearly equal to 2.2 kV. This implies that the droop gains dominate the power sharing.

Example 2 (Low I-V Droop Gains): This is a continuation of Example 3.1, where the droop gains are chosen as n_1 = 0.002 Ω and n_2 = 0.004 Ω. It can be seen that $R_1 > n_1$ and $R_2 > n_2$. The simulation results are shown in Fig. 3.3. The total load power demand is 624 kW, P_1 is 525 kW while P_2 is 99 kW. The currents are I_1 = 210 A and I_2 = 40 A. The voltages V_1 and V_2 are nearly equal to 2.5 kV. This gives P_1:P_2 = 5.3:1. This implies that the droop gains have no effect on the power sharing and it is mainly dominated by the line resistances with a ratio of R_1:R_2 = 1:6.

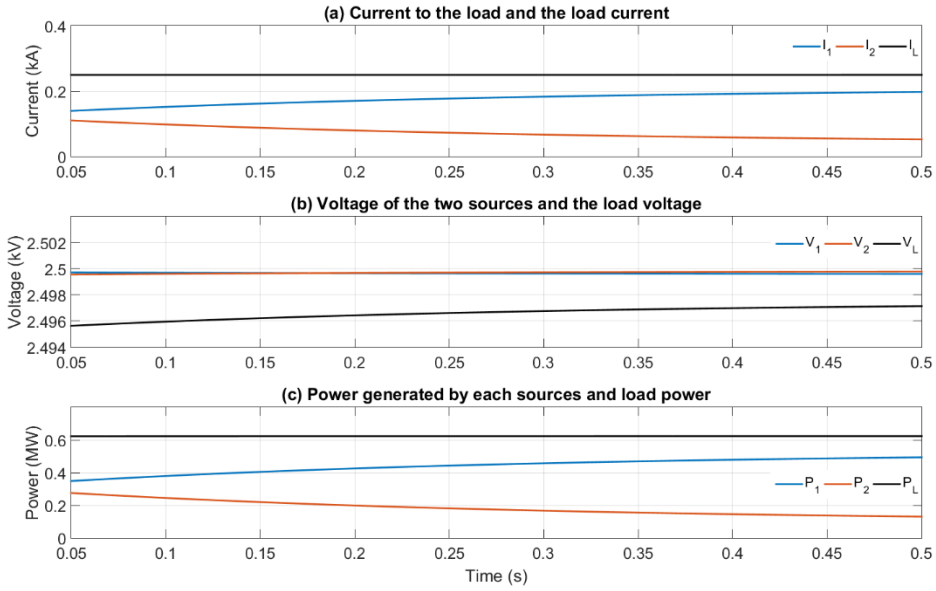

Fig. 3.3. Power sharing with low droop gains.

The above two examples show an interesting behaviour. If the droop gains are much higher than the line resistances, the power sharing is more accurate. However they also cause voltage drop in the system. On the other hand, when the droop gains are lower, the power sharing is dictated by the line resistances. Therefore, we have to make a compromising choice of the droop gains. Consider the system of Examples 3.1 and 3.2. Let us try to restrict the voltage drop by 100 V. Then the load power roughly is $(2.4)^2 \div 10 = 576$ kW. Of this, source 1 should supply 2/3rd, i.e., 384 kW, while source 2 should supply 1/3rd, i.e., 192 kW. This implies that $I_1 = 384 \div 2.4 = 160$ A., then from (3.1), we get

$$V_1 - V_{ref} = -n_1 I_1 \Rightarrow 100 = n_1 \times 160 \Rightarrow n_1 = \frac{100}{160} = 0.625\Omega$$
$$n_2 = 1.25\Omega$$

The voltages are shown in Fig. 3.4. It can be seen that they remain within the stipulated boundary of 2.4 kV. The load power is 574.8 kW, of which P_1 is 387.4 kW while P_2 is 188 kW. Therefore the power sharing is fairly and is acceptable.

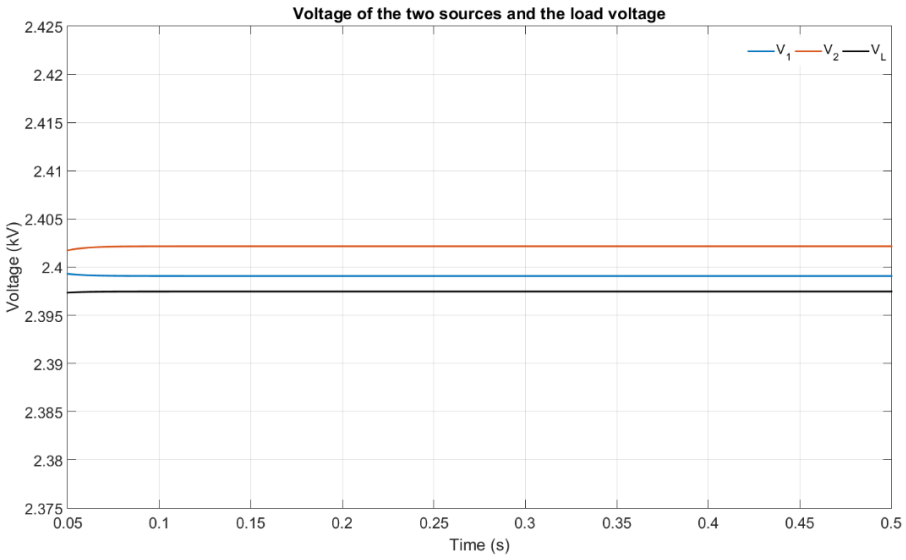

Fig. 3.4. Voltages with voltage restricting droop gains.

Using (3.6), the droop gains for the two boost converters designed to operate at the maximum powers of 20 kW and 30 kW are varied. This is shown in Fig. 3.5. From this figure it can be seen that the maximum voltage drop is 250 V. The droop gains at this voltage are n_1 = 3.125 Ω, n_2 = 2.0833 Ω. It can also be observed that for larger values of droop gains value the system will become unstable. We can therefore define the values n_1 = 3.125 Ω, n_2 = 2.0833 Ω to be critical values.

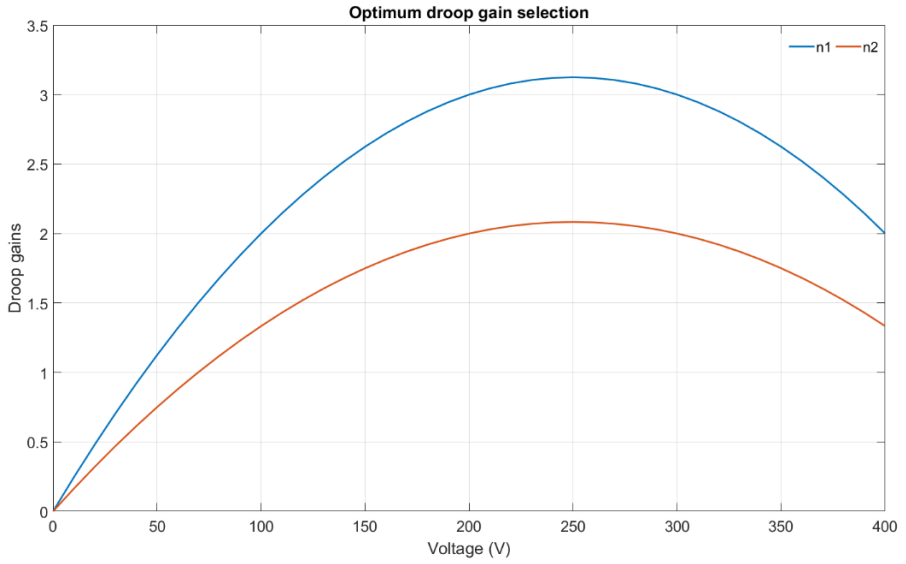

Fig. 3.5. Maximum permissible droop gain for different voltage drop.

3.3. DC GRID STABILITY ANALYSIS

In this section, the stability studies of a DCMG are performed through eigenvalue analysis. There are two possible ways to determining the overall system model – (1) a discrete-time model and (2) a continuous-time model. In these studies, the latter is chosen where state space averaging technique has been employed. The rational for this is explained below.

Let us first consider the discrete-time model with only two converters. These converters may have different switching frequencies and their sawtooth waveforms may not be synchronized. Consider the timing diagram of Fig. 3.6 (a). In this, it has been assumed that both the converters have the same switching frequency of *f* and their sawtooth waveforms are synchronized. In that case, using the corner point models, the overall system state space equation can be easily obtained.

Now consider the timing diagram of Fig. 3.6 (b), in which it has been assumed that both the converters operate at the same switching frequency of *f*. However the sawtooth waveform of one of the converters starts with a delay of τ s from the other. Now consider the timing diagram of Fig. 3.6 (c). Here the converters do not switch at the same frequency and their sawtooth waveforms are not synchronized.

For the switching diagram of Fig. 3.6 (b), it is possible to determine the overall state space model using multi-rate sampling method [147-152], where a multi-rate controller can be designed to compensate an error-sampled feedback system [148]. However this is possible only when two converters are considered. The system becomes more complicated with more than two converters. For the system of Fig. 3.6 (c), it is almost impossible to design a state space model since the converters operate at different switching frequencies such that the starting time of the second converter shifts continuously with respect to that of the first one.

Based on the above arguments, discrete-time eigenvalue analysis has not been preferred. The advantage of state space averaging is that a continuous time model of each converter is derived based on its average over one cycle. Therefore the switching frequency and the time shifts become irrelevant.

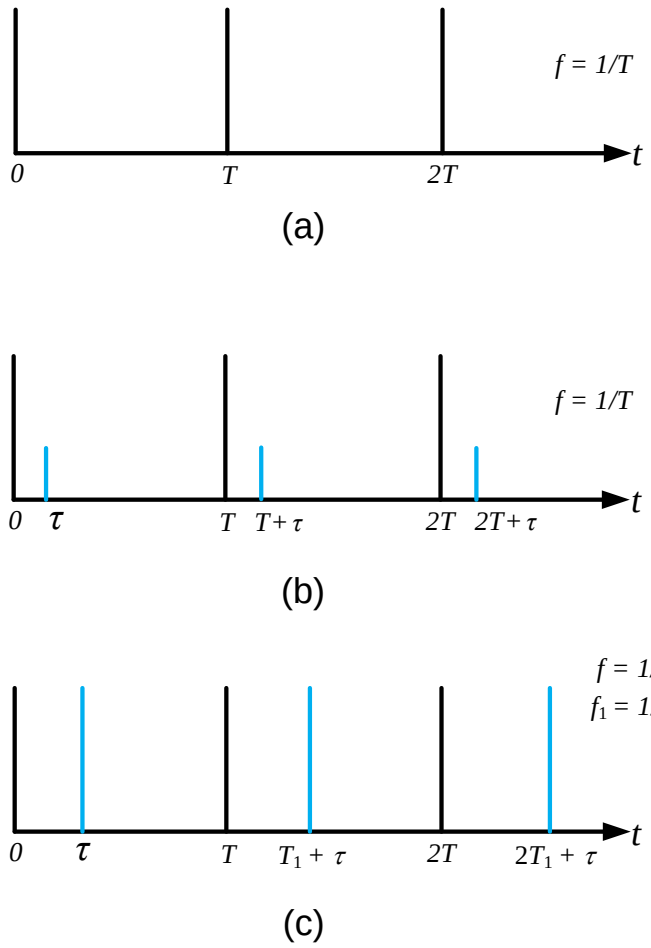

Fig. 3.6: Different sampling approaches of the two converters.

3.3.1. State Space Model of a Two Converter DCMG

The DCMG circuit with two boost converters are shown in Fig. 3.7 (a). At first, the voltage current relations of the dc grid are determined. These are given by

$$\begin{aligned} V_1 &= \left(R_1 + R_L\right) i_1 + R_L i_2 \\ V_2 &= \left(R_2 + R_L\right) i_2 + R_L i_1 \end{aligned} \tag{3.15}$$

The currents can then be expressed in terms of voltages as

$$\begin{aligned} i_1 &= m_{11} V_1 + m_{12} V_2 \\ i_2 &= m_{21} V_1 + m_{22} V_2 \\ M &= \begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{bmatrix} = \begin{bmatrix} R_1 + R_L & R_L \\ R_L & R_2 + R_L \end{bmatrix}^{-1} \end{aligned} \tag{3.16}$$

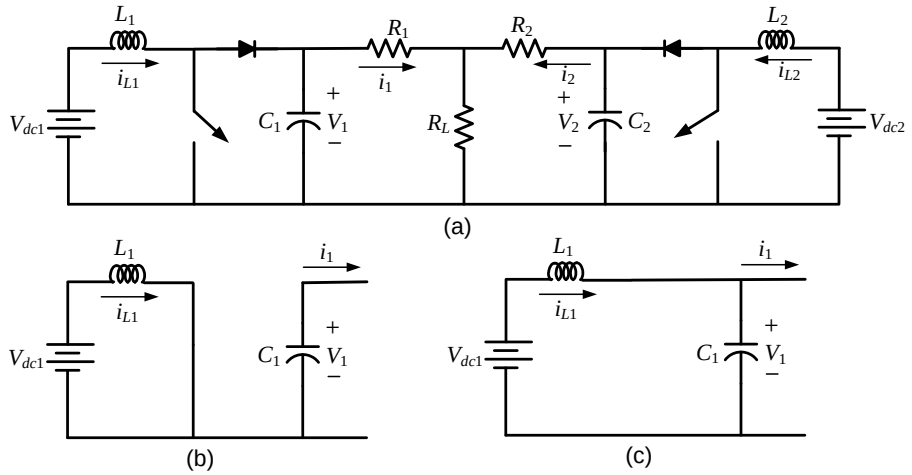

Fig. 3.7. (a) DCMG with boost converters and Equivalent circuit of a boost converter when (b) the switch is closed and (c) the switch is open.

Now let us consider only converter-1. We define the state vector as $x_1 = [V_1\ i_{L1}]$. Then when the switch is closed, the equivalent circuit is shown in Fig. 3.7 (b). From this we get

$$\dot{x}_1 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} x_1 + \begin{bmatrix} 0 \\ 1/L_1 \end{bmatrix} V_{dc1} + \begin{bmatrix} -1/C_1 \\ 0 \end{bmatrix} i_1 \tag{3.17}$$

Substituting (3.16) in (3.17), we get

$$\begin{aligned} \dot{x}_1 &= \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} x_1 + \begin{bmatrix} 0 \\ 1/L_1 \end{bmatrix} V_{dc1} + \begin{bmatrix} -1/C_1 \\ 0 \end{bmatrix} \left(m_{11} V_1 + m_{12} V_2 \right) \\ &= \begin{bmatrix} -m_{11}/C_1 & 0 \\ 0 & 0 \end{bmatrix} x_1 + \begin{bmatrix} 0 \\ 1/L_1 \end{bmatrix} V_{dc1} + \begin{bmatrix} -m_{12}/C_1 \\ 0 \end{bmatrix} V_2 \\ &= A_{11} x_1 + B_{11} V_{dc1} + H_{11} V_2 \end{aligned} \tag{3.18}$$

where

$$A_{11} = \begin{bmatrix} -m_{11}/C_1 & 0 \\ 0 & 0 \end{bmatrix}, \quad B_{11} = \begin{bmatrix} 0 \\ 1/L_1 \end{bmatrix}, \quad H_{11} = \begin{bmatrix} -m_{12}/C_1 \\ 0 \end{bmatrix}$$

When the switch is opened, the equivalent circuit is shown in Fig. 3.7 (c). From this we get

$$\begin{aligned}\dot{x}_1 &= \begin{bmatrix} 0 & 1/C_1 \\ -1/L_1 & 0 \end{bmatrix} x_1 + \begin{bmatrix} 0 \\ 1/L_1 \end{bmatrix} V_{dc1} + \begin{bmatrix} -1/C_1 \\ 0 \end{bmatrix} i_1 \\ &= \begin{bmatrix} 0 & 1/C_1 \\ -1/L_1 & 0 \end{bmatrix} x_1 + \begin{bmatrix} 0 \\ 1/L_1 \end{bmatrix} V_{dc1} + \begin{bmatrix} -1/C_1 \\ 0 \end{bmatrix} \left(m_{11} V_1 + m_{12} V_2 \right) \\ &= A_{12} x_1 + B_{12} V_{dc1} + H_{12} V_2 \end{aligned} \tag{3.19}$$

Substituting (3.15) in (3.19), we have

$$\dot{x}_1 = A_{12} x_1 + B_{12} V_{dc1} + H_{12} V_{ref} \tag{3.20}$$

$$A_{12} = \begin{bmatrix} -m_{11}/C_1 & 1/C_1 \\ -1/L_1 & 0 \end{bmatrix}, \quad B_{12} = B_{11} = \begin{bmatrix} 0 \\ 1/L_1 \end{bmatrix}, \quad H_{12} = H_{11} = \begin{bmatrix} -m_{12}/C_1 \\ 0 \end{bmatrix}$$

Let the duty ratio of converter-1 be denoted by d_1. Then the state space average of converter-1 is

$$\begin{aligned}\dot{x}_1 &= \left[A_{11} d_1 + A_2 \left(1 - d_1\right) \right] x_1 + \left[B_{11} d_1 + B_{12} \left(1 - d_1\right) \right] V_{dc1} \\ &\qquad + \left[H_{11} d_1 + H_{12} \left(1 - d_1\right) \right] V_2 \\ &= \left[A_{11} d_1 + A_2 \left(1 - d_1\right) \right] x_1 + B_{11} V_{dc1} + H_{11} V_2 \end{aligned} \tag{3.21}$$

Equation (3.21) is linearized around the operating point x_{10}, V_2 and d_{10}. This gives

$$\Delta \dot{x}_1 = A_1 \Delta x_1 + B_1 \Delta d_1 + H_1 \Delta V_2 \tag{3.22}$$

where

$$\begin{aligned} A_1 &= A_{11} d_{10} + A_{12} \left(1 - d_{10}\right) \\ B_1 &= \left[A_{11} - A_{12} \right] x_{10} \\ H_1 &= H_{11} \end{aligned}$$

The output equation is

$$\Delta y_1 = \begin{bmatrix} 1 & 0 \end{bmatrix} \Delta x_1 = C \Delta x_1 \tag{3.23}$$

In a similar way, linearizing converter-2 around the operating point of x_{20}, V_1 and d_{20}, we have

$$\Delta \dot{x}_2 = A_2 \Delta x_2 + B_2 \Delta d_2 + H_2 \Delta V_1 \tag{3.24}$$

and the output equation is given by

$$\Delta y_2 = \begin{bmatrix} 1 & 0 \end{bmatrix} \Delta x_2 = C \Delta x_2 \tag{3.25}$$

3.3.2. P-V DROOP EQUATIONS

As per the discussions in Chapter 2, the P-V droop equations are given by

$$\begin{aligned} y_{r1} &= V_{ref} - n_1 P_1 = V_{ref} - n_1 V_1 i_1 \\ y_{r2} &= V_{ref} - n_2 P_2 = V_{ref} - n_2 V_2 i_2 \end{aligned} \tag{3.26}$$

For a boost converter, the output current can be written in terms of the inductor current as $i = (1 - d) \times i_L$. Therefore (3.26) can be modified as

$$\begin{aligned} y_{r1} &= V_{ref} - n_1 V_1 (1 - d_1) i_{L1} \\ y_{r2} &= V_{ref} - n_2 V_2 (1 - d_2) i_{L2} \end{aligned} \tag{3.27}$$

In the linearized form, the droop equation for converter-1 is given by

$$\begin{aligned} \Delta y_{r1} &= -n_1 (1 - d_{10}) i_{L10} \Delta V_1 - n_1 (1 - d_{10}) V_{10} \Delta i_{L1} + n_1 V_{10} i_{L10} \Delta d_1 \\ &= D_1 \Delta x_1 + n_1 V_{10} i_{L10} \Delta d_1 \end{aligned} \tag{3.28}$$

where

$$D_1 = \begin{bmatrix} -n_1 (1 - d_{10}) i_{L10} & -n_1 (1 - d_{10}) V_{10} \end{bmatrix}$$

In a similar way, the linearized equation for converter-2 can be written as

$$\Delta y_{r2} = D_2 \Delta x_2 + n_2 V_{20} i_{L20} \Delta d_2 \tag{3.29}$$

where

$$D_2 = \begin{bmatrix} -n_2 (1 - d_{20}) i_{L20} & -n_2 (1 - d_{20}) V_{20} \end{bmatrix}$$

3.3.3. CONTROL LAW AND HOMOGENOUS EQUATION

Both the converters now use the predesigned control of (2.17), i.e., for converter-1, we have

$$\Delta d_1 = -K_1 \Delta x_1 + K_{I1} z_1 \tag{3.30}$$

where

$$\dot{z}_1 = \Delta y_{r1} - \Delta y_1 \tag{3.31}$$

Substituting (3.28) in (3.31) we have

$$\begin{aligned} \dot{z}_1 &= D_1 \Delta x_1 + n_1 V_{10} i_{L10} \Delta d_1 - \Delta y_1 \\ &= (D_1 - C) \Delta x_1 + n_1 V_{10} i_{L10} \Delta d_1 \end{aligned} \tag{3.32}$$

Now substituting (3.30) into (3.31), we have

$$\dot{z}_1 = (D_1 - C - K_1 n_1 V_{10} i_{L10}) \Delta x_1 + n_1 K_{I1} V_{10} i_{L10} z_1 \tag{3.33}$$

Again substituting (3.30) in (3.22), we have

$$\Delta \dot{x}_1 = (A_1 - B_1 K_1) \Delta x_1 + B_1 K_{I1} z_1 + H_1 \Delta V_2 \tag{3.34}$$

Defining an extended state vector for converter-1 as $x_{e1} = [\Delta x_1 \quad z_1]^T$ and combining (3.33) and (3.34), we have

$$\begin{aligned} \dot{x}_{e1} &= \begin{bmatrix} A_1 - B_1 K_1 & K_{I1} B_1 \\ (D_1 - C - K_1 n_1 V_{10} i_{L10}) & n_1 K_{I1} V_{10} i_{L10} \end{bmatrix} x_{e1} + \begin{bmatrix} H_1 \\ 0 \end{bmatrix} \Delta V_2 \\ &= F_1 x_{e1} + L_1 C \Delta x_2 \end{aligned} \tag{3.35}$$

In a similar way, for converter-2, we have

$$\Delta d_2 = -K_2 \Delta x_2 + K_{I2} z_2 \tag{3.36}$$

$$\dot{z}_2 = \Delta y_{r2} - \Delta y_2 \tag{3.37}$$

$$\begin{aligned} \dot{x}_{e2} &= \begin{bmatrix} A_2 - B_2 K_2 & K_{I2} B_2 \\ \left(D_2 - C - K_2 n_2 V_{20} i_{L20}\right) & n_2 K_{I2} V_{20} i_{L20} \end{bmatrix} x_{e2} + \begin{bmatrix} H_2 \\ 0 \end{bmatrix} \Delta V_1 \\ &= F_2 x_{e2} + L_2 C \Delta x_1 \end{aligned} \tag{3.38}$$

We now define a combined state vector as

$$\Delta x_c = \begin{bmatrix} \Delta x_{e1} \\ \Delta x_{e2} \end{bmatrix}$$

Then the homogeneous state space description of the system can be written from (3.35) and (3.38) as

$$\dot{x}_c = \begin{bmatrix} F_1 & L_1 C \\ L_2 C & F_2 \end{bmatrix} x_c \tag{3.39}$$

3.3.4. P-V DROOP EIGENVALUE ANALYSIS

Let us first consider the P-V droop equations and perform the eigenvalue analysis. For this we assume that converter-1 is rated 200 kW and converter-2 is rated 100 kW. The controller is designed around the half rated power, i.e., 100 kW for converter-1 and 50 kW for converter-2.

Fig. 3.8 shows the eigenvalue trajectories as the load of the DCMG is changed. For this study, the droop coefficients are considered constant. It can be seen that, as the load resistance is increased beyond R_L =4.95 Ω, the eigenvalues start becoming complex conjugate. For a very high value of R_L =50 Ω (i.e., when the load becomes almost negligible), the complex conjugate pair still do not reach the imaginary axis indicating a high system stability. For low R_L also, the system stays stable. It can be said that the system is not sensitive to the load changes. Overall, this system response indicates a stable operation.

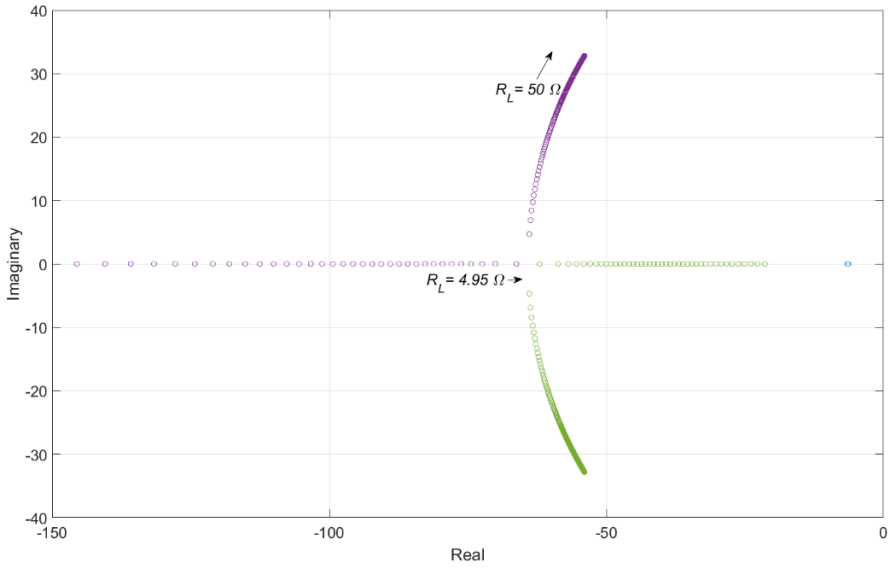

Fig. 3.8. Eigenvalue trajectories with the change of the load.

Fig. 3.9 shows the corresponding eigenvalue trajectory of the DCMG as a function of droop gains. In this case, the load is considered constant (R_L=5 Ω) and the droop gains are denoted by $m = n_1 = 0.5*n_2$. It can be seen that for a very high value of m (14.85×10^{-3}), a complex conjugate pair the eigenvalues almost reaches the imaginary axis indicating a low system stability. If the droop gain is further increased then it crosses the imaginary axis. For $m = 15\times10^{-5}$, the eigenvalues cross the imaginary axis. This behavior indicates an unstable operation. Therefore the droop gains have to be selected in a proper range for a stable operation of the DCMG.

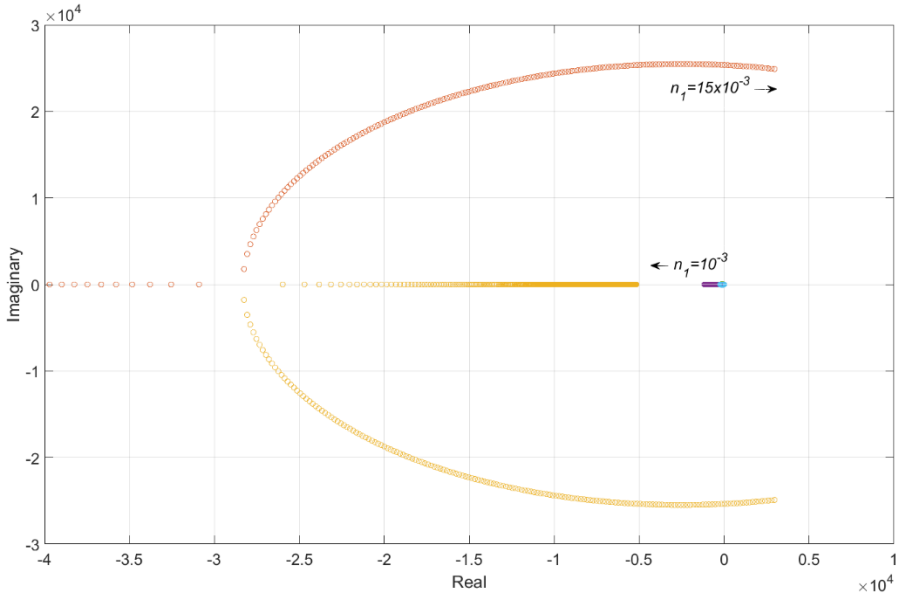

Fig. 3.9. Eigenvalue trajectories with the change of the droop gain.

The DCMG model shown in Fig. 3.6 is simulated in PSCAD to verify the above mentioned analysis. Both the converters are droop controlled and designed with a state feedback with integral control action. In the Fig. 3.10, P_1 and P_2 represents the power supplied by the boost converter 1 and 2. The droop gains are selected assuming that boost converter 2 has half the power rating of the boost converter 1. In this simulation, the maximum allowable voltage drop is assumed to be 100 V. The droop gains at 100 V voltage drop will be n_1=0.5e^{-3} and n_2=1e^{-3}. From the simulation results it can be noticed that P_1, P_2 are contributing 34 kW, 17 kW. After 1 seconds when the load is increased to 270 kW boost converter 1 and 2 are supplying 180 kW and 90 kW respectively. The voltage across the load also changes accordingly. Before 1 second it is 484 V and after the load change it further dropped to 415 V.

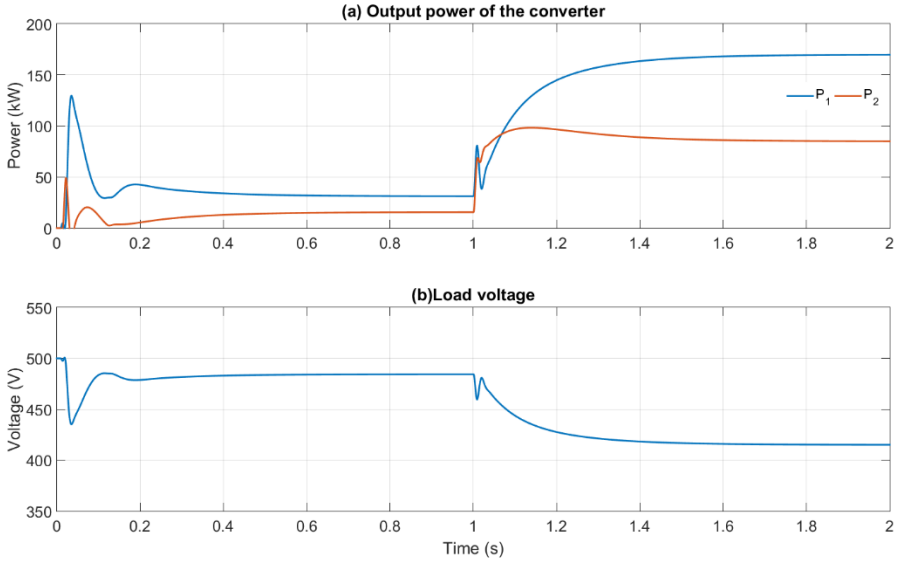

Fig. 3.10. DCMG performance when the load is changed.

Now, the droop gains are selected as following: n_1=15e^{-3}, n_2=30e^{-3} and R_L=0.75 Ω. From Fig. 3.11 it can be noticed that P_1, P_2 are contributing 56 kW, 32 kW. It can be noticed that the power sharing accuracy is decreased. Also since the voltage across the load is negative, it can be termed as an unstable behaviour.

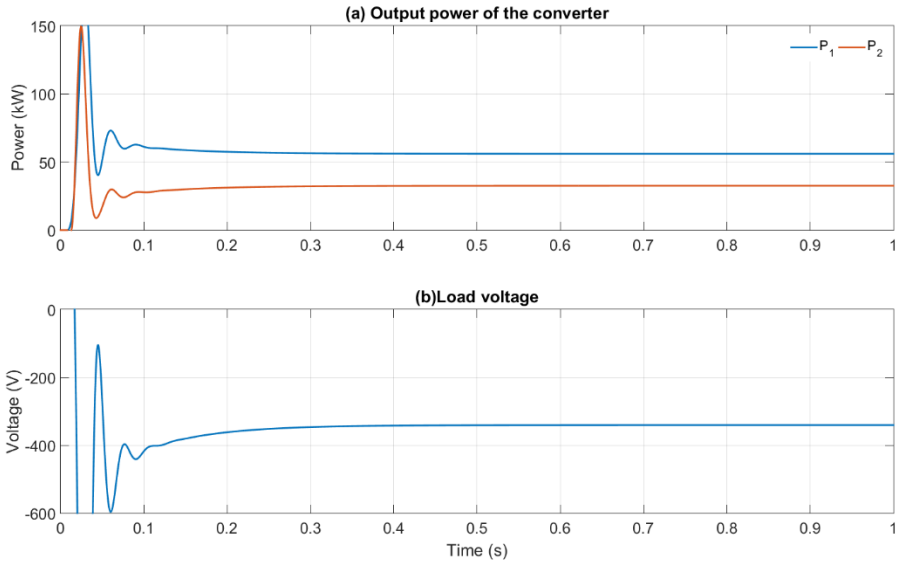

Fig. 3.11. DCMG performance when $n_1=15e^{-3}$.

For this case, the droop gains are selected as following: $n_1=2e^{-3}$, $n_2=4e^{-3}$ and the load is kept unchanged (R_L=0.75 Ω.). From Fig. 3.12 it can be seen that P_1, P_2 are contributing 88 kW, 44 kW. It can be noticed that the power sharing accuracy is little bit improved. But the reference voltage V_{ref} has dropped even beyond the allowable droop voltage indicating poor performance of the DCMG.

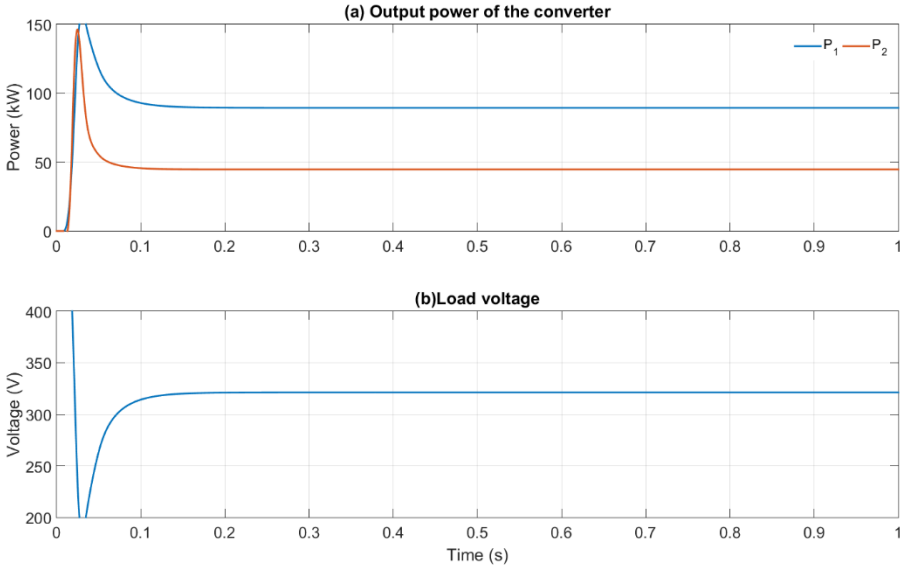

Fig. 3.12. DCMG performance when $n_1=2e^{-3}$.

Finally, the droop gain is selected as follows: $n_1=1e^{-3}$, $n_2=2e^{-3}$and R_L=0.75 Ω. These droop gain selection results in perfect power sharing, where the load voltage is

kept within the specified limit. This ensures a stable operation. Boost converter 1 and 2 is supplying 150 kW and 75 kW. The reference voltage settles to 425 V.

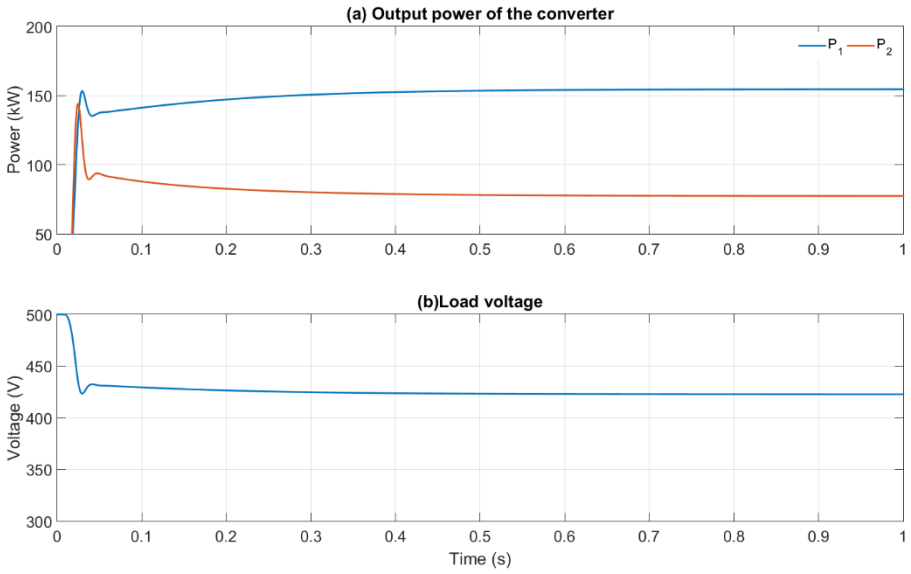

Fig. 3.13. DCMG performance when n_1=1e^{-3}.

Table. 2. 1. Excitation system model parameters.

DCMG parameters	
Voltage reference (V_{ref})	500V
Maximum voltage drop (ΔV)	100V
DG rating	DG-1: 200 kW, DG-2: 100 kW
Droop gains (for fixed droop gain analysis)	n_1 = 0.5, n_2 = 1
Line resistances	R_1 = 0.03 Ω, R_2 = 0.06 Ω,

3.3.5. I-V DROOP EQUATIONS

The I-V droop equations are given by

$$\begin{aligned} y_{r1} &= V_{ref} - n_1 I_1 \\ y_{r2} &= V_{ref} - n_2 I_2 \end{aligned} \tag{3.40}$$

The above equations can be written in terms of inductor currents as

$$\begin{aligned} y_{r1} &= V_{ref} - n_1 (1-d_1) i_{L1} \\ y_{r2} &= V_{ref} - n_2 (1-d_2) i_{L2} \end{aligned} \tag{3.41}$$

In the linearized form, the droop equation for converter-1 is given by

$$\begin{aligned}\Delta y_{r1} &= -n_1\left(1-d_{10}\right)V_{10}\Delta i_{L1} + n_1 i_{L10}\Delta d_1 \\ &= D_1\Delta x_1 + n_1 i_{L10}\Delta d_1\end{aligned} \tag{3.42}$$

where

$$D_1 = \begin{bmatrix} 0 & -n_1\left(1-d_{10}\right)\end{bmatrix}$$

In a similar way, the linearized equation for converter-2 can be written as

$$\Delta y_{r2} = D_2\Delta x_2 + n_2 i_{L20}\Delta d_2 \tag{3.43}$$

where

$$D_2 = \begin{bmatrix} 0 & -n_2\left(1-d_{20}\right)\end{bmatrix}$$

The control laws are the same as those given in the previous section. Therefore only the F will be altered as

$$\begin{aligned}F_1 &= \begin{bmatrix} A_1 - B_1K_1 & K_{I1}B_1 \\ \left(D_1 - C - K_1 n_1 i_{L10}\right) & n_1 K_{I1} i_{L10}\end{bmatrix} \\ F_2 &= \begin{bmatrix} A_2 - B_2K_2 & K_{I2}B_2 \\ \left(D_2 - C - K_2 n_2 i_{L20}\right) & n_2 K_{I2} i_{L20}\end{bmatrix}\end{aligned} \tag{3.44}$$

The homogeneous state space description of the system remains the same as that given by (3.37).

3.3.5. I-V DROOP EIGENVALUE ANALYSIS

Now, let us consider the I-V droop equations and perform the eigenvalue analysis. For this one also we assume that converter-1 is rated 200 kW and converter-2 is rated 100 kW. The controller is designed around the half rated power, i.e., 100 kW for converter-1 and 50 kW for converter-2.

Fig. 3.14 shows the eigenvalue trajectories as the load of the DCMG is changed. Similar studies as section 3.3.4 are carried out in this section. For this study,

the droop coefficients are considered constant. It can be seen that, as the load resistance is increased beyond R_L =7.7 Ω, the eigenvalues start becoming complex conjugate. For a very high value of R_L =50Ω (small load), the complex conjugate pair still do not reach the imaginary axis indicating a high system stability. For low R_L also the system stays stable. It can be said that the system is not sensitive to the load changes. Overall, this system response indicates a stable operation.

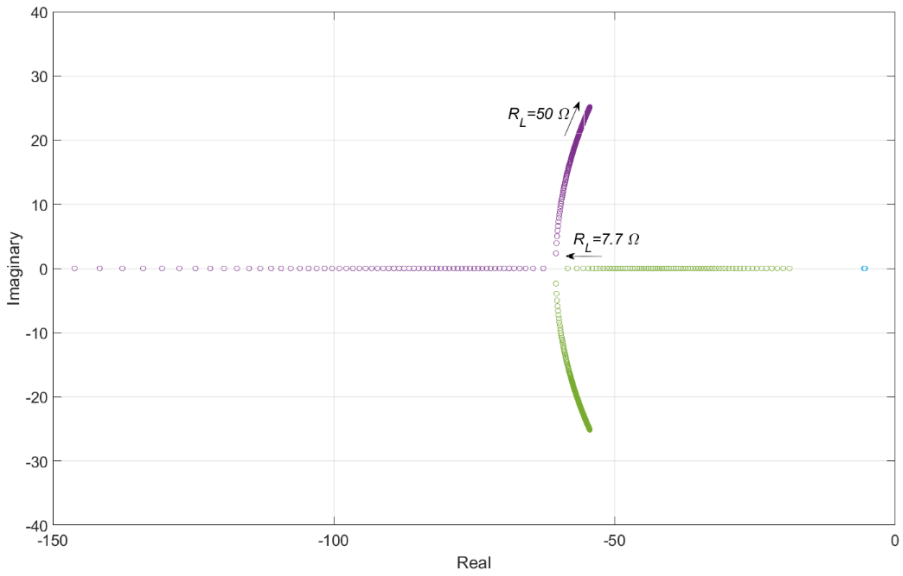

Fig. 3.14. Eigenvalue trajectories with the change of the load for I-V droop method.

Fig. 3.15 shows the corresponding eigenvalue trajectory of the DCMG as a function of droop gains. In this case, the load is considered constant (R_L=5Ω). It can be seen that at m =5.98 (m = n_1 = 0.5*n_2), a complex conjugate pair the eigenvalues almost reaches the imaginary axis indicating a low system stability. If the droop gain is further increased then it crosses the imaginary axis. For m = 6.8, the eigenvalues cross the imaginary axis. This behavior indicates an unstable operation. Subsequently the droop gains has to be selected in a proper range for a stable operation of the DCMG. It can be seen that the system becomes unstable with a small change of the droop gains.

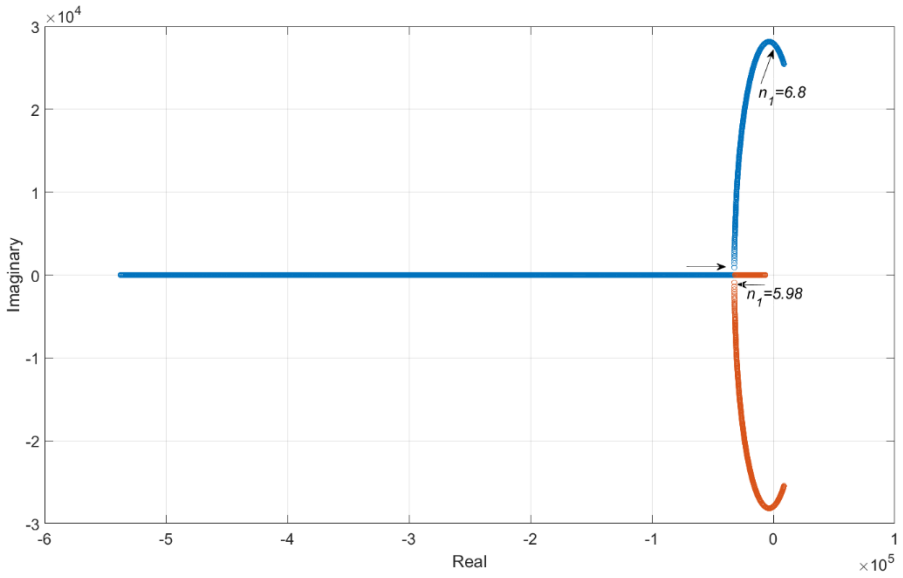

Fig. 3.15. Eigenvalue trajectories with the change of droop gains for I-V droop method.

The DCMG model shown in Fig. 3.6 is simulated in PSCAD to verify the above mentioned analysis. Both the converters are droop controlled and designed with a state feedback with integral control action. In the Fig. 3.16, P_1 and P_2 represents the power supplied by the boost converter 1 and 2. The droop gains are selected assuming that boost converter 2 has half the power rating of the boost converter 1. However, in this simulation the maximum allowable voltage drop is assumed to be 100 V. The droop gains at 100 V voltage drop will be n_1=0.2, n_2=0.4. From the simulation results it can be noticed that P_1, P_2 are contributing 32 kW, 16 kW. After 1 seconds when the load is increased to 250kW boost converter 1 and 2 are supplying 170 kW and 85 kW respectively. The voltage across the load also changes accordingly. Before 1 second it is 486 V and after the load change it further dropped to 415 V.

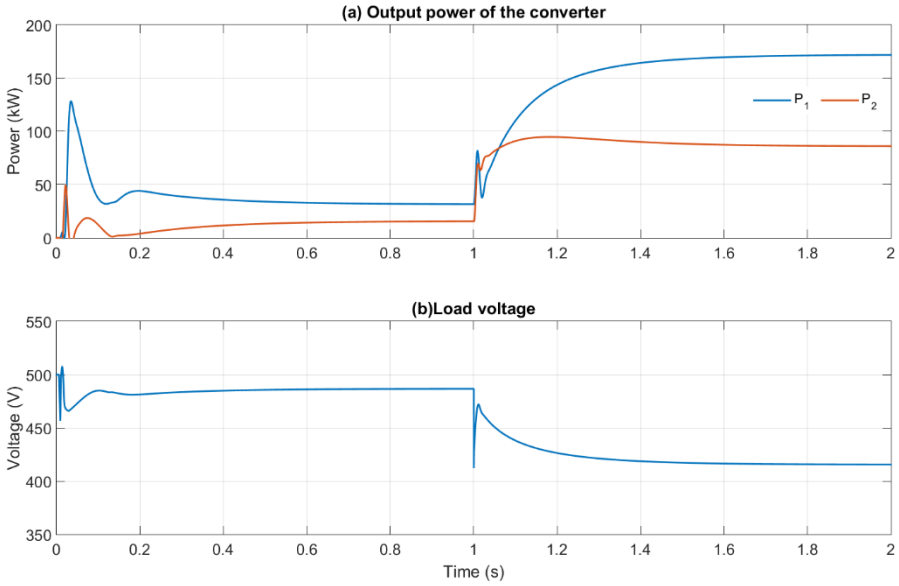

Fig. 3.16. DCMG performance when the load is changed for I-V droop method.

Now, the droop gains are selected as following: n_1=7, n_2=14 and R_L=0.75Ω. From Fig. 3.17 it can be noticed that P_1, P_2 are contributing 56 kW, 32 kW. It can be noticed that the power sharing accuracy is decreased. Since the load voltage is negative, the system operation can be considered as unstable.

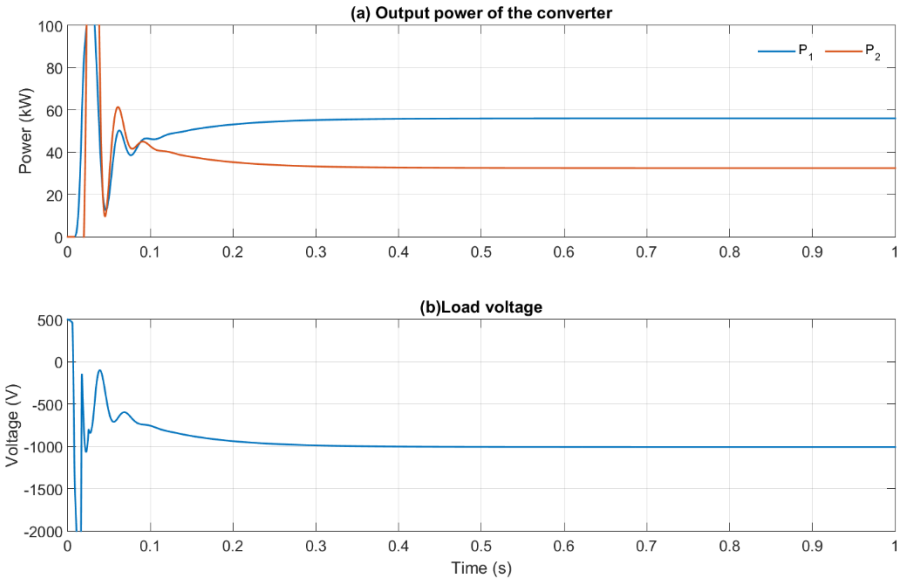

Fig. 3.17. DCMG performance when n_1=7 for I-V droop method.

For this case, the droop gains are selected as following: n_1=1, n_2=2 and the load is kept unchanged (R_L=0.75Ω.). From Fig. 3.18 it can be seen that P_1, P_2 are

contributing 62 kW, 31 kW. It can be noticed that the power sharing accuracy is little bit improved. But the load voltage V_{ref} has dropped to 267 V which is even beyond the allowable droop voltage indicating poor performance of the DCMG.

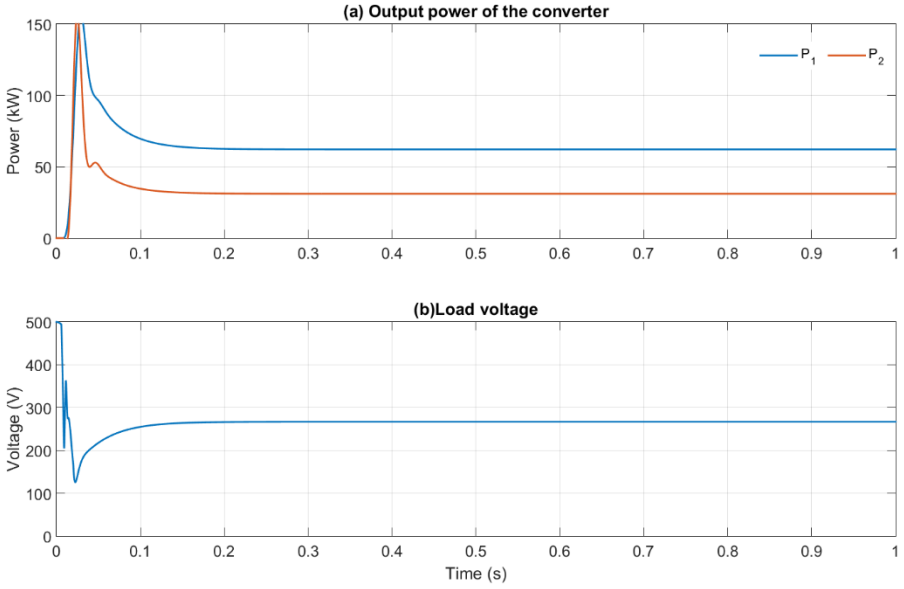

Fig. 3.18. DCMG performance when n_1=1 for I-V droop method.

Finally, the droop gain is selected as follows: n_1=0.2, n_2=0.4and R_L=0.75. These droop gain selection results in perfect power sharing. This ensures a stable operation. Boost converter 1 and 2 is supplying 157 kW and 78 kW. The load voltage settles to 424 V.

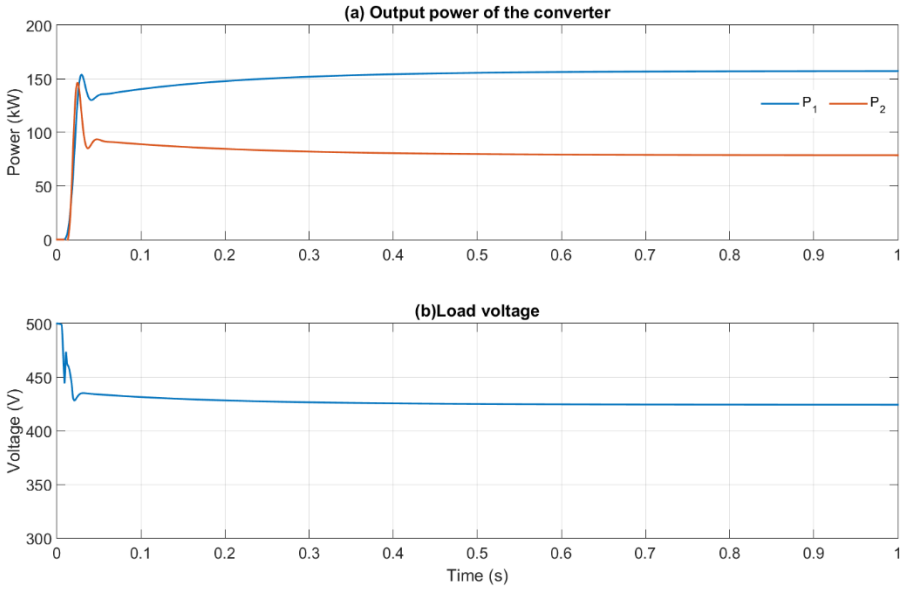

Fig. 3.19. DCMG performance when n_1=0.2 for I-V droop method.

3.4. CONCLUSION

The theories of P-V droop mechanism and I-V droop principle are explained in this chapter. A linearized state space model of an autonomous DCMG is developed. For this study two converters and a load is used to represent the network. But the proposed generalized model is valid even for a network with multiple converters and loads. Eigenvalue analysis around a nominal operating point is carried out to analyse the stability of the system. It has been shown that the power sharing is affected by the change of the droop coefficients, while it is not sensitive with the variation of the load. This implies that the state feedback controller designed is very robust. Droop coefficients are defined using both P-V droop and I-V droop method. Extensive simulation studies are carried out to validate the results of the eigenvalue analysis. Finally, with the proposed control method, it is shown that proper load sharing is possible while keeping the voltage drop of this system in the defined droop range. Moreover, the control of the system is based on local measurements only. Overall, the eigenvalue analysis predicts stability boundary accurately.

CHAPTER 4

POWER MANAGEMENT IN A UTILITY CONNECTED DC MICROGRID

Many of the loads in low voltage, such as computers, efficient lighting systems, battery chargers etc., use dc power. Thus these devices require AC-DC conversion stages. This has led to a renewed worldwide interests in dc distribution systems, especially in dc microgrids. A microgrid (MG) can be operated in either grid-tied or islanded modes. The grid tied mode is as vital as the islanded mode since many of the applications both DCMG and utility or ACMG are tied together. In the grid connected mode, usually pre-specified amount of power is supplied by the utility, while the DGs and the batteries in the DCMG supply the rest, up-to their maximum capacity. In any event, it is important to provide flexibility in the DCMG operation such that the DGs irrespective of power rating can be easily connected to or disconnected from the system [13, 30].

A dc microgrid consists of dc sources and loads and it is connected with the utility through an interlinking converter (IC) [142]. Usually droop characteristics is employed in dc microgrids that regulate the DG output voltage depending on current or power [153, 154]. Several ways to improve current sharing accuracy is explored in [94, 95], while [57] proposes a proportional droop index (PDI) controller. For autonomous and independent operation of dc microgrid, it is required to establish a well-designed control system which can provide back up from the utility at any instance, while allowing proportional load sharing amongst the DGs.

In this chapter, three control techniques for proportional load sharing in a utility-connected dc microgrid are discussed. The dc microgrid is connected to a utility system through an interlinking voltage source converter. On the dc side of the IC, a power flow controller (PFC) is connected. Three different PFCs are considered. In the first case, a dc-dc converter is connected at the dc side of the IC to facilitate unidirectional power flow from the utility to the DCMG. The power flow controller and the dc converters in the DCMG are designed with the control technique described in Chapter 2 and chapter 3. In the second case, a bidirectional switch is employed to

facilitate bidirectional power flow from the utility to DCMG or the other way around. Finally a dual active bridge (DAB) is employed for bidirectional power flow. A detailed analysis and control design for a DAB are also presented. The DERs in the DCMG are operated under droop sharing using dc-dc converters. Each dc-dc converter is equipped with a state feedback with integral controller that can regulate its output voltage for a wide range of input voltage fluctuation and load variation. Simulation studies are conducted on PSCAD/EMTDC to validate the proposals.

4.1. POWER MANAGEMENT WITH DC-DC CONVERTER BASED PFC

Since a unidirectional dc-dc converter is chosen as PFC, a desired amount of power flows from the utility to the DCMG, while the interlinking converter (IC) holds the DC bus voltage constant.

4.1.1. SYSTEM STRUCTURE

The system structure considered in this study is shown in Fig. 4.1 (a). The dc microgrid (DCMG) is connected to the utility through an interlinking converter (IC) and a DC-DC power flow controller (PFC). On the ac side of the IC an LC filter (L_f and C_f) is used to bypass high frequency switching harmonics. The IC is essentially a voltage source converter (VSC) and it holds the dc capacitor voltage V_{dc1} across C_{dc1} to a constant magnitude. For this study a buck converter has been used as PFC. Given that V_{dc1} is constant, the PFC modulates the voltage V_{dc2} across C_{dc2} to facilitate power flow to the DCMG from the utility in a controlled manner.

The DCMG structure, shown in Fig. 4.1 (b), contains two boost converters and a buck converter. The boost converters are connected with the two DGs to step up the voltage to a distribution level, while the buck converter steps down the voltage for supplying power to the dc loads. The boost converters track the voltages obtained from the droop equation (3.1). The load buck converter holds the load voltage constant irrespective of its input voltage or load. All these dc-dc converters are designed in a way such that they can hold the desired output voltage even during the disturbances in the DCMG. The resistances R_1 and R_2 are the line resistances, while the inductors are used as damping inductors. The PFC is connected to the dc distribution line through a resistor R_3 and the power flow from the ac utility is denoted by $P_{link.}$ The power flow from DG_1 and DG_2 respectively are P_{DC1} and P_{DC2}.

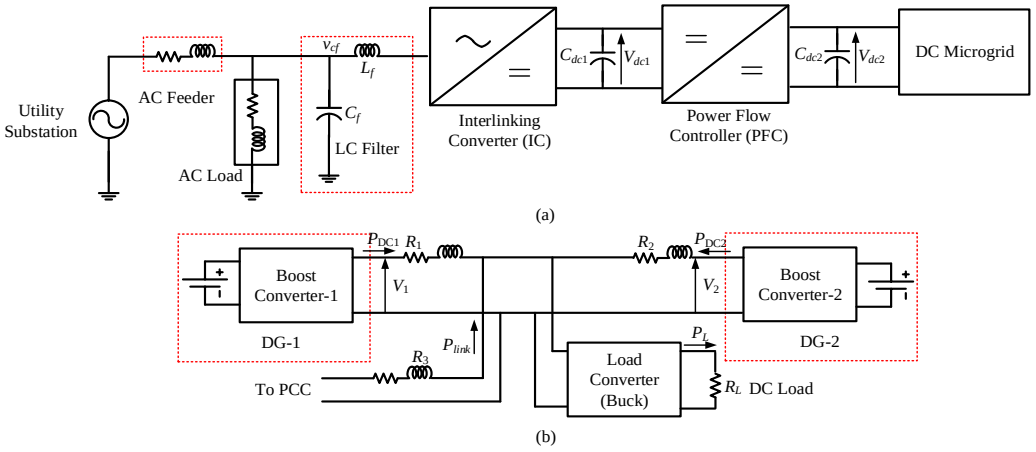

Fig. 4.1: a) The overall system structure and (b) the structure of the DC microgrid.

4.1.2. INTERLINKING CONVERTER OPERATION

The IC is a transformer-less three-phase, three-leg VSC, the schematic diagram of which is shown in Fig. 4.2. In this figure, each switch represents an insulated gate bipolar transistor (IGBT) along with a snubber circuit and an anti-parallel diode. The dc link of the IC is connected to the PFC. An LC filter (L_f-C_f) is connected at the ac side of the IC to suppress the high frequency switching harmonics. The resistance R_f represents the converter losses. The purpose of the IC is to convert ac voltage into dc. To do this it must regulate to the voltage v_{cf} across the filter capacitor C_f (See Fig. 4.1) and hold the dc side voltage V_{dc1} constant [13]. The instantaneous ac voltage references for the PCC voltage v_p are given by

$$\begin{aligned} v_{pa}^{*} &= |V|\sin\left(2\pi f t + \delta\right) \\ v_{pb}^{*} &= |V|\sin\left(2\pi f t + \delta - 120^{\circ}\right) \\ v_{pc}^{*} &= |V|\sin\left(2\pi f t + \delta + 120^{\circ}\right) \end{aligned} \tag{4.1}$$

where $|V|$ is a pre-specified voltage magnitude and δ is the desired angle. Note that the reference quantities are denoted by '*'. The angle δ in (4.1) should be chosen such that the sum of the power required by the DCMG should flow towards it. In any VSC, the dc link voltage should roughly be around 1.5 times the line-to-line ac voltage to be synthesized. Therefore, once the dc capacitors are charged, the dc link voltage will remain constant if no power is drawn from the capacitors. This means that the converter losses, in addition to the power to the DCMG, must be supplied by the utility grid. This mean that the angle δ in (4.1) should be chosen such that the sum total of

the power required by the load and converter losses should flow from the source to the PCC. This can only be achieved if the dc capacitor voltage is held constant. From this logic, the following proportional plus integral (PI) controller is used to control the dc voltage.

$$\delta = K_{P\delta}\left(V_{dc}^{*} - \langle V_{dc}(t)\rangle\right) + K_{I\delta}\int\left(V_{dc}^{*} - \langle V_{dc}(t)\rangle\right)dt \tag{4.2}$$

where $\langle V_{dc}(t)\rangle$ is the average of the dc capacitor voltage that is usually obtained by the passing the measurement through a lowpass filter with a low cutoff frequency.

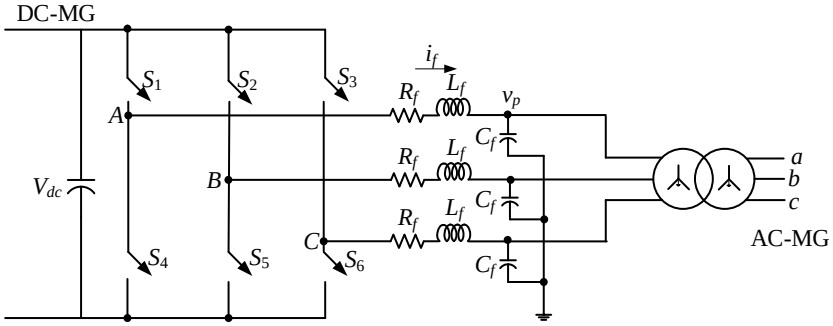

Fig. 4.2: Schematic diagram of the interlinking converter.

A linear quadratic regulator is employed to generate the control input u_c [10]. For generating the switching signal, a triangular carrier waveform (v_{tri}) which varies from – 1 to + 1 with a duty ratio of 0.5 is used. The control output u_c is sampled twice in each cycle of the carrier waveform and is held by a zero-order hold (ZOH). The switching signal for phase-a is generated by the crossing of the carrier waveform and the control signal as

$$\begin{aligned} &u_c(k) > v_{tri}(k), \text{ turn } S_1 \text{ is ON and } S_4 \text{ is OFF} \\ &u_c(k) \le v_{tri}(k), \text{ turn } S_4 \text{ is ON and } S_1 \text{ is OFF} \end{aligned} \tag{4.3}$$

Similar logic is used for the other two phases as well.

4.1.3. DC-DC CONVERTER BASED PFC OPERATION

The power flow controller (PFC) regulates the voltage V_{dc2} across the capacitor C_{dc2}. Therefore it needs a reference voltage V_{dc2}^{*} that it needs to track. There are two modes of operation. In one mode, the power flow from the utility side is predefined (it can be zero as well). In the second mode, the entire power has to come from the utility

when both the DGs are down. The voltage reference generation scheme for the PFC is shown in Fig. 4.3.

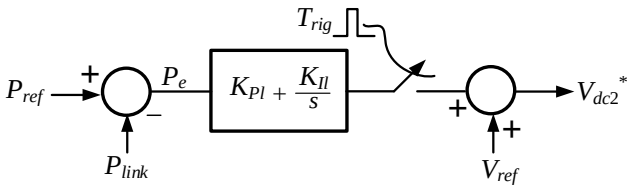

Fig. 4.3. PFC output voltage reference generation scheme.

The reference of the power that needs to be supplied through the link is denoted by P_{ref}. This is then compared with the power though the link. The error is passed through a PI controller. The output of the PI controller is added with dc voltage reference of the DCMG to obtain V_{dc2}^* as

$$\begin{aligned} P_e &= P_{ref} - P_{link} \\ V_{dc2}^* &= V_{ref} + K_{Pl} P_e + K_{Il} \int P_e \, dt \end{aligned} \tag{4.4}$$

When both the DGs are down, a signal T_{rig} is generated. Then the PI controller is bypassed and the PFC hold the DC voltage to V_{ref}. The power required by the load then flows from the utility side.

4.1.4. SIMULATION RESULTS WITH DC-DC CONVERTER BASED PFC

The system parameters used in these studies are listed in Table 4.1. In this section, three case studies for the microgrid operation are presented.

Table 4.1: System parameters

Quantities		Parameters
ac side	Operating frequency Voltage L-L RMS	50Hz 11kV
dc side	DG-1 rating DG-1 rating Voltage reference (V_{ref}) Maximum voltage deviation Droop gain for DG-1 Droop gain for DG-1	0.2MW 0.1MW 1kV 100V 0.5 1
IC	Transformer dc capacitor Filter capacitor Filter inductor Switching frequency Reference dc voltage	11/1.72kV 5000μF 50μF 33mH 15kHz 2.5 kV
Load buck converter	Inductor Capacitor Output voltage	4mH 250μF 500 V
PFC buck converter	Inductor Capacitor	4mH 250μF

In the first case study it is assumed that the microgrid is operating in islanded mode. During this scenario no power is required to be transmitted through the PFC and hence its reference is chosen as zero. In the next study, a constant amount of power is supplied to the DCMG from the utility. Output voltage reference of the point of common coupling (PCC) is changed accordingly so that it can facilitate requested amount of power from the utility. In the last study, it is considered that the DGs in the DCMG are inactive. Subsequently, the utility has to supply power to all the DC loads. While all the simulation studies are performed in PSCAD, the control parameters for the converters are calculated using MATLAB.

A. Islanded Mode of DCMG Operation

For this case it has been assumed that the DCMG operates in an isolated mode and no power gets transferred from the utility side. Therefore the power reference (P_{ref}) for the PFC is set as zero. The results for a cold start are shown in Figs. 4.4 and 4.5.

Fig. 4.4 (a) shows the power generated (P_s) and the power supplied to the utility local load (P_{LAC}), where P_s is around 565 kW. The dc side voltage of the IC is shown

in Fig. 4.4 (b). It can be seen that it settles to the desired value of 2.5 kV. The PFC output voltage is shown in Fig. 4.4 (c). It settles to around 1 kV, as expected.

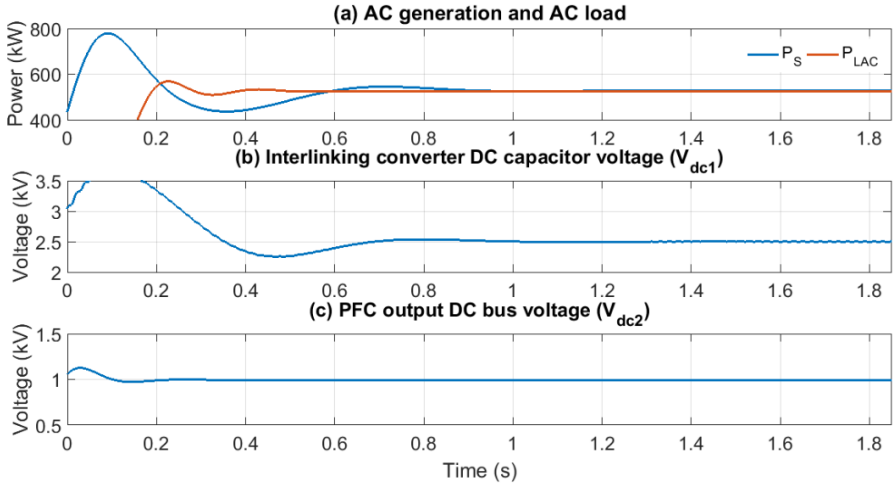

Fig. 4.4. Islanded mode of operation: (a) AC generation and AC Load, (b) IC DC capacitor voltage and (c) PFC output DC voltage.

Fig. 4.5 shows the performance of the DCMG, where the dc load (P_L) is 180 kW. It is shared in the ratio 2:1 by the two DGs (120:60 kW) as can be seen from Fig. 4.5 (a). The link power remains zero (Fig. 4.5 b). The DG output voltages settle to around 940 V (Fig. 4.5 c) as per the droop equation.

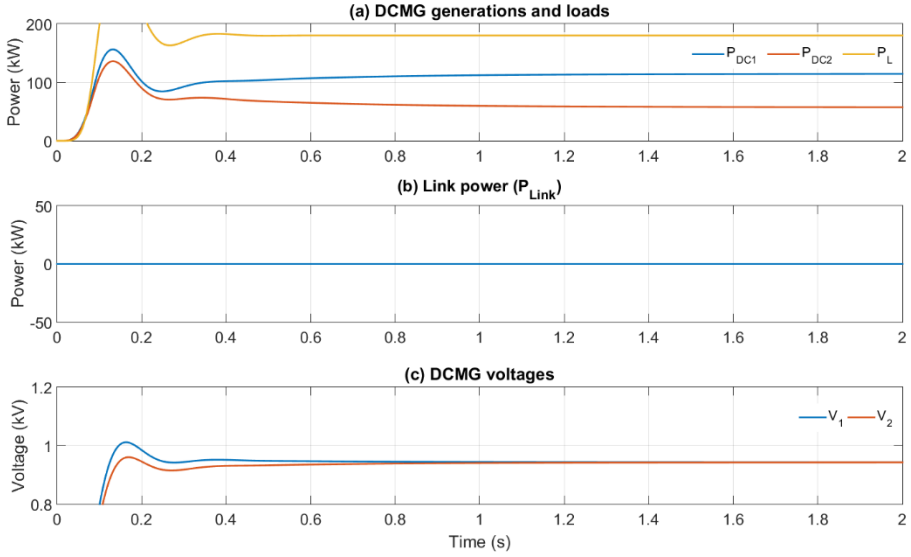

Fig. 4.5. Islanded mode of operation: (a) DCMG generations and load, (b) link power and (c) DCMG voltages.

B. Pre-Specified Power Flow from Utility

With the DCMG operating in the standalone mode, the power reference (P_{ref}) is changed to 100 kW at 0.15 s. The results are shown in Figs. 4.6 and 4.7. It can be seen from Fig. 4.6 (a) that the utility power increases by 100 kW to meet the increased power demand from DCMG. The IC dc capacitor voltage however remains at 2.5 kV barring an initial transient (Fig. 4.6 b). The PFC dc bus voltage is shown in Fig. 4.6 (c). The DGMG powers are shown in Fig. 4.7 (a). It can be seen that the DG powers drop, but the load power remains constant. The link power is 100 kW, as expected. The remaining 80 kW are shared by the DGs according to their rating. Since the power generated by the DGs have dropped, the DGs' voltage rise, as can be seen from Fig. 4.7 (c).

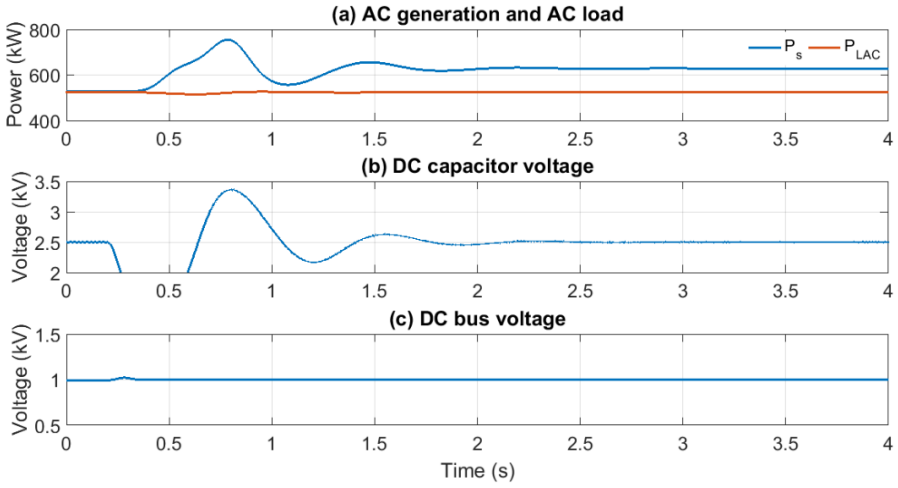

Fig. 4.6. Constant power flow: (a) AC generation and load and (b) IC DC capacitor voltage and (c)dc bus voltage.

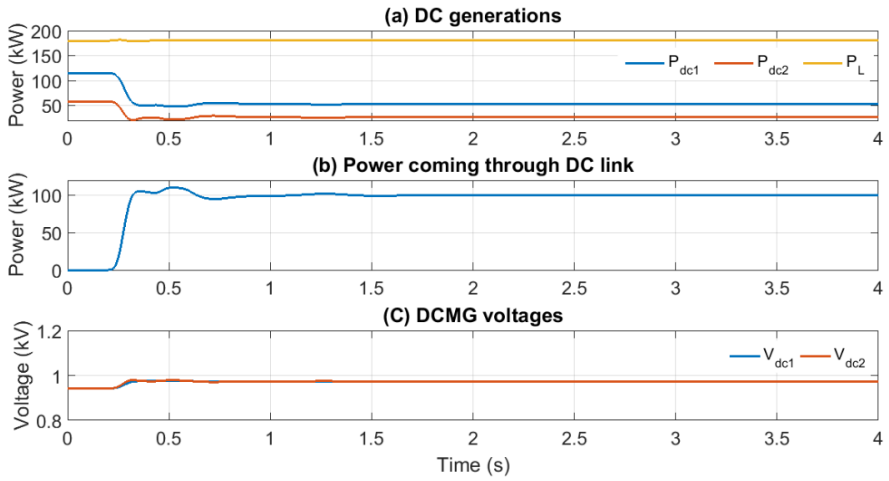

Fig. 4.7. Constant power flow: (a) DC generations, load and link power and (b) DCMG voltages and (c) DCMG voltages.

C. Disconnection of DCMG Generators

With the system operating in the steady state, the DGs in the DCMG get disconnected at 0.2 s. When this is detected, the trigger signal T_{rig} is activated and the PI controller of Fig. 4.3 is bypassed. The dc load is assumed to be 100 kW. The AC power supply then increases by 100 kW to cater to the dc load as shown in Fig. 4.8 (a). The DCMG powers are shown in Fig. 4.8 (b). It can be seen the DG power outputs become zero and the link power becomes equal to the dc load power.

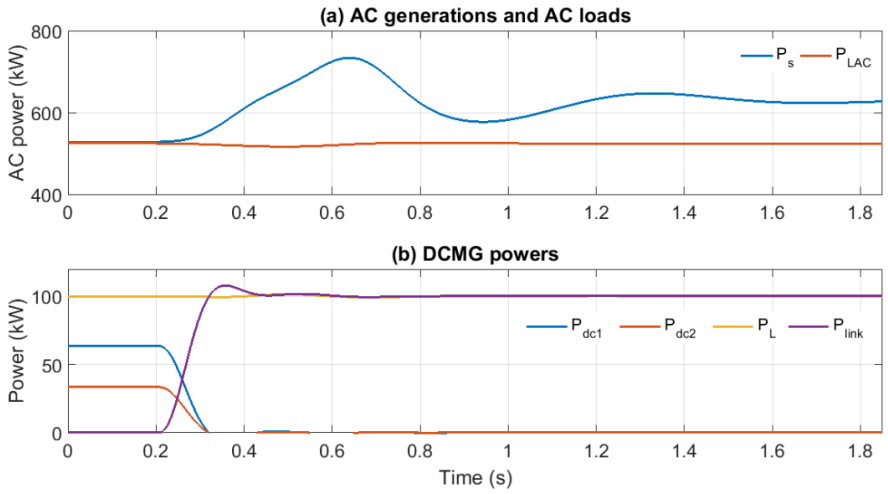

Fig. 4.8. DCMG DGs get disconnected: (a) AC generation and AC load and (b) DC generations, load and link power.

4.2. POWER MANAGEMENT WITH BIDIRECTIONAL SWITCH

In this section, dc-dc converter based PFC is replaced with a bidirectional switch. The bidirectional switch will allow the DCMG to receive power from the utility or send power to it.

4.2.1. SYSTEM STRUCTURE WITH BIDIRECTIONAL SWITCH

The system structure considered in this study is shown in Fig. 4.9. Even though the DCMG is capable to transfer power to the utility, only a special case is discussed here in which the utility supplies power to the DCMG when its DGs get saturated, i.e., are supplying their maximum power. In this case, only that amount power that cannot be supplied by the DGs in the DCMG will be supplied by the utility.

The IC regulates the voltage across the dc capacitor C_{dc} according to the power flow requirement. The switch pairs Sw_1 and Sw_2 are normally open. One of them closes to facilitate power transfer in the required direction only when a command is issued. For example, when the utility needs to supply power to the DCMG, Sw_1 closes. Alternatively Sw_2 closes when the DCMG supplies power to the ACMG. Former case is discussed in this chapter and the latter case is discussed in the next chapter.

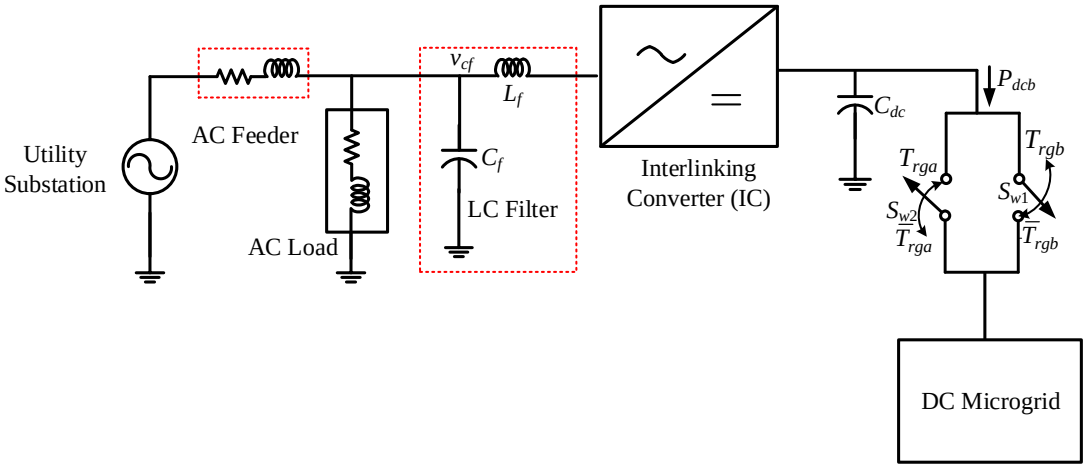

Fig.4.9: A compact representation of the proposed system with bidirectional switches.

4.2.2. OPERATING MODES

Two different operating modes are discussed in this section.

A. Mode-1: Isolated Mode of Operation

In this mode, it is assumed that the DGS in DCMG has sufficient power to supply its loads. Since no power is required from the utility, the interlinking converter holds the dc voltage across C_{dc} to a pre-specified value and the switches S_1 and S_2 remain open. Following condition is satisfied during this mode of operation.

$$\text{DC-MG: } \sum_{k=1}^{N_{DC}} P_k^* \geq \sum_{k=1}^{M_{DC}} P_{Lk} + P_{Loss} \tag{4.5}$$

where N_{DC} is the total number of DGs in an MG and M_{DC} is total number loads and P_{Loss} is the line loss in the dc circuit.

B. Mode-2: Power Shortfall in DC-MG

In this mode, it is assumed that condition (4.5) is violated which represents an overloaded condition in the DCMG. As has been discussed in Chapter 3, the maximum possible voltage drop in a DG in the DC microgrid is ΔV. Therefore this quantity will be used for overload detection in the DCMG.

The voltage drop in the DC-MG is measured for only one particular DG in the network, say DG-*i*. Once the voltage drops below the minimum level, a trigger signal (T_{rgb}) is generated, which is then used to close the switch Sw_1. Thereafter another PI

controller is used that holds the voltage of that DG (V_{dci}) at the minimum level by drawing the exact amount of power (P_{dcb}^{*}) from the utility to prevent a collapse in the MG. The PI controller is given by

$$\begin{aligned} e_v &= V_{ref} - \Delta V - V_{dci} \\ P_{dcb}^{*} &= K_{Pv}\, e_f + K_{Iv} \int e_v\, dt \end{aligned} \tag{4.6}$$

The control structure is shown in Fig. 4.10. The reset signal is used when the power shortfall is removed.

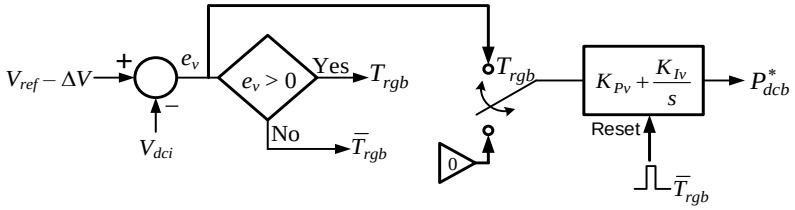

Fig. 4.10. Schematic diagram of overload prevention in DC-MG.

4.2.4. DC CAPACITOR VOLTAGE REFERENCE FOR IC

Once the reference power P_{dcb}^{*} is computed from (4.6), the voltage across the capacitor C_{dc} (see Fig. 4.9) is changed to facilitate this amount of power flow from the utility. The schematic diagram for the capacitor voltage reference generation scheme is shown in Fig. 4.11. In this, the direction of power flowing from the utility to the DCMG is taken as positive and this power is denoted by P_{dc}. A 2-by-1 multiplexer is used for selecting the correct power reference, as shown in Fig. 4.11. For example, when s1s0 = 01 (i.e., only T_{rga} is 1), P_{dca}^{*} is selected as the reference power. On the other hand, when s1s0 = 00 no power will be supplied from the utility. The reference is then compared with the power flowing out of the dc capacitor and is passed through a third PI controller to generate the dc capacitor voltage reference V_{dcref}. This PI controller is given by

$$\begin{aligned} e_P &= P_{dc}^{*} - P_{dc} \\ V_{DCref} &= V_{ref} - K_{PP}\, e_P - K_{IP} \int e_P\, dt \end{aligned} \tag{4.7}$$

The PI controller is reset when either T_{rgb} becomes zero.

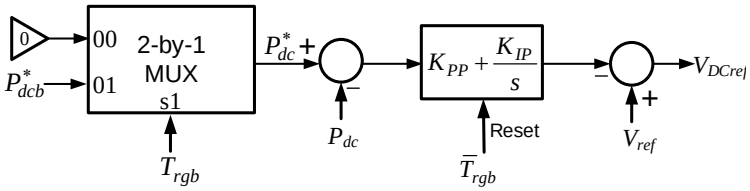

Fig. 4.11. DC capacitor voltage reference generation scheme.

4.2.5. SIMULATION RESULTS

In this section, the simulation studies, performed using PSCAD, are discussed. The system parameters used in the studies are listed in Table I. There are two DGs in the DC-MG rated 500 kW and 250 kW.

Table 4.2: System parameters.

Quantities		Parameters
AC Side:	DG power rating	1 MW
	Frequency (f_r)	50 Hz
	Voltage L-L RMS	11 kV
	Maximum frequency Deviation (Δf)	0.5 Hz
	Droop Gain (n)	0.5 Hz/MW
DC Side:	DG-1 rating	0.5 MW
	DG-2 rating	0.25 MW
	Voltage reference (V_{ref})	2.5 kV
	Maximum frequency Deviation (ΔV)	100 V
	Droop gain for DG-1 (d_1)	0.48 Ω
	Droop gain for DG-2 (d_2)	0.96 Ω
Interlinking converter	Transformer	11/1.72 kV
	DC capacitor (C_{dc})	5000 μF
	Filter capacitor (C_f)	50 μF
	Filter inductor (L_f)	33 mH
	Switching frequency	15 kHz

A. Mode-1: Nominal Operation

In this example, it is assumed that the utility is supplying 575 kW to its local load. This is shown in Fig. 4.12, along with the generated power. The load in the DC side is 562 kW. This plus the losses in the DC lines are shared by the two DGs (almost) in a ratio of 2:1, as shown in Fig. 4.13. The voltages of the DGs in the DCMG are shown in Fig. 4.13 (b). It can be seen that both these voltages are above the lowest rated voltage of 2.4 kV. Also voltage V_1 is lower than V_2 since DG-1 is supplying more power than DG-2.

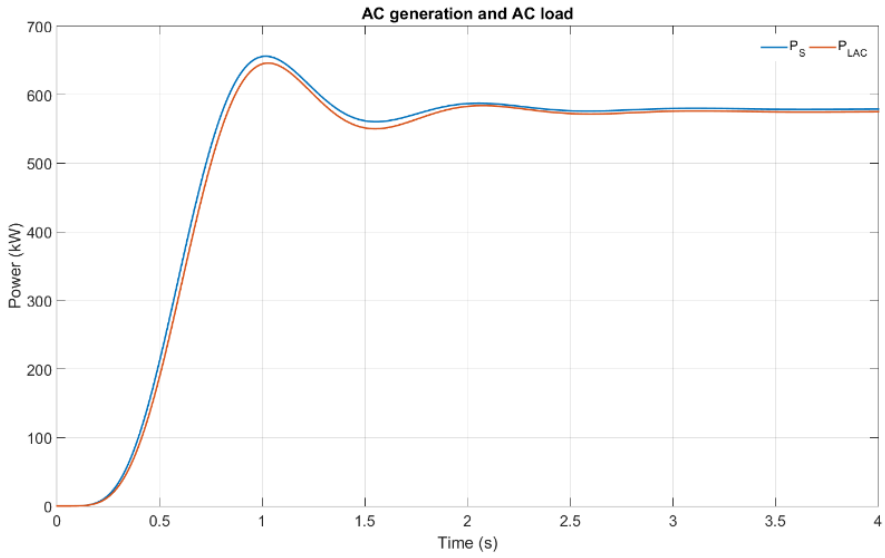

Fig. 4.12. AC generation and load when bidirectional switch is placed at nominal operation mode

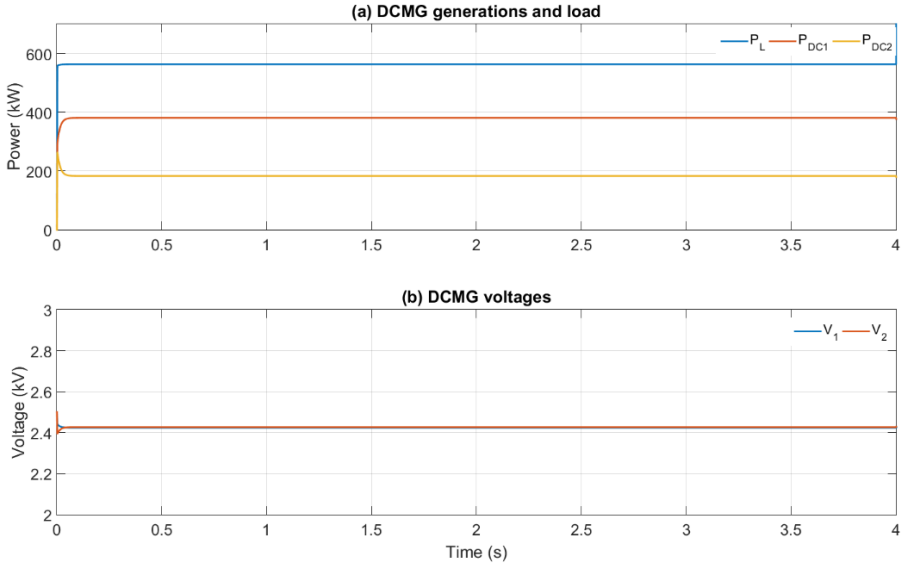

Fig. 4.13.(a) DCMG generations and load and (b) DCMG voltages for mode-1

B. Mode-2: Power Shortfall in DC-MG

In this example, it has been assumed that the utility is supplying 575 kW to the load such that its generation is 578.5 kW. The DCMG is supplying 586 kW power to

the load, when at 1 s, its load demand increases to 821 kW. Since the total capacity of the DGs in the DCMG is 750 kW, the excess power has to be drawn from the utility. The power flow in the ac and dc sides is shown in Fig. 4.14 (a) and (b) respectively. It can be seen that the utility side load power remains constant, while its generated power increases to 661 kW (Fig. 4.14 a). The DGs in the DCMG supplies their maximum rated power, as can be seen in Fig. 4.14 (b).

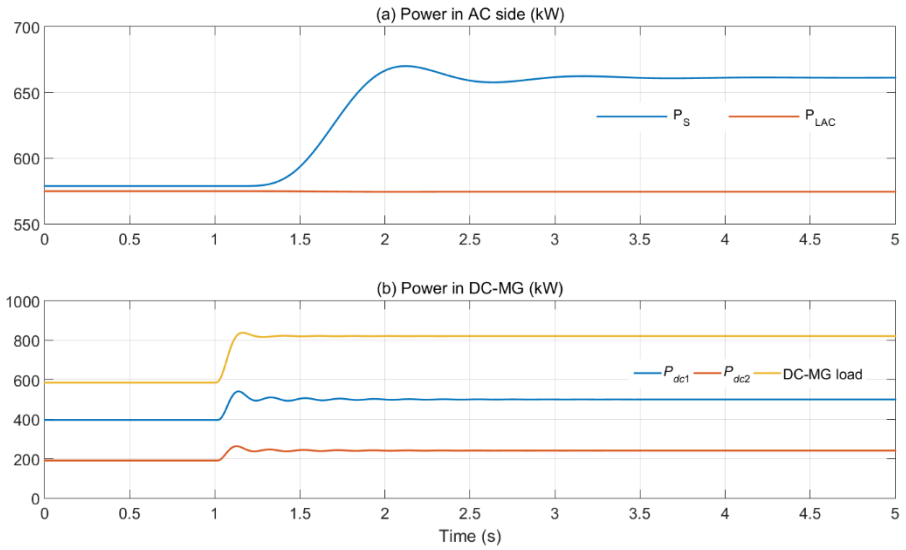

Fig. 4.14. Power flow through the hybrid for Mode-2.

The voltages in the DCMG are shown in Fig. 4.15 (a). Since DG-1 is used for lower voltage regulation, its voltage is held constant at 2.4 kV. The DG-2 voltage is also very close to this value. The dc capacitor voltage reference is shown in Fig. 4.15 (b). The reference power that has to be drawn from the utility to the DCMG is shown in Fig. 4.16.

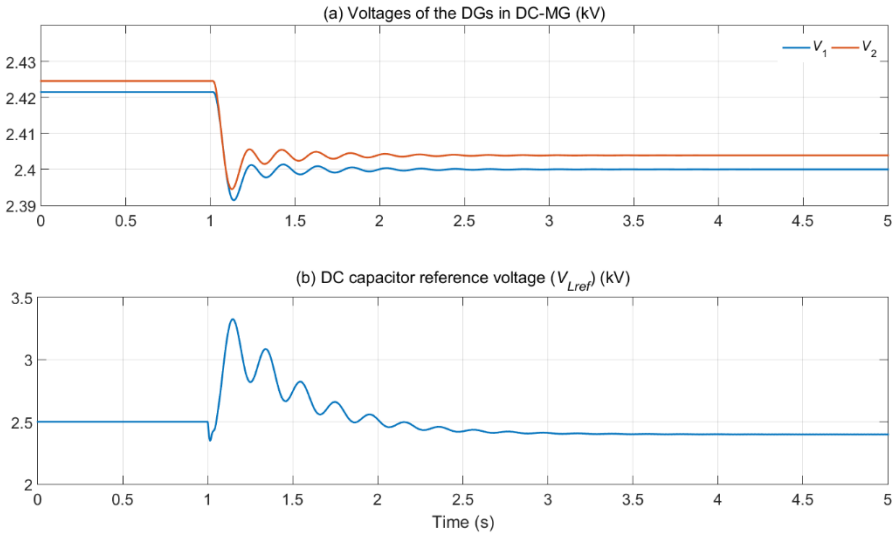

Fig. 4.15. DC-MG voltages, and DC capacitor voltage reference for Mode-2.

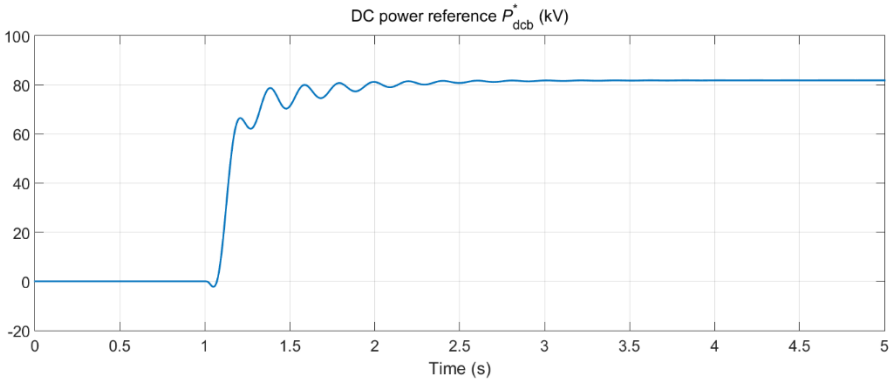

Fig. 4.16. DC power reference for Mode-2.

4.3. POWER MANAGEMENT WITH A DAB

In this section, a DAB is coupled with the interlinking converter (IC) to facilitate bidirectional power flow. A DAB contains two H-bridges that are connected together through a high frequency transformer. When a DCMG is connected to an ac system, it is expected that the ac voltage will be high. The voltage can be brought to the level of DCMG by a transformer at the input of the IC. However, for medium voltage systems, only a VSC is sufficient. In this case the DAB transformer can provide the required isolation. In Fig. 4.17 (a), the IC holds the dc voltage (V_{dc1}). Therefore it cannot enable power flow control since it might adversely affect the power

control in the DCMG. With the inclusion of the DAB, the separation between the voltages V_{dc1} and V_{dc2} is achieved. Now V_{dc2} can be controlled for power flow. In fact, this configuration has also been suggest in [13].

4.3.1. System Structure with DAB

The overall system structure is shown in Fig. 4.17 (a). The DCMG is connected to the utility system through an interlinking converter (IC) and a dual active bridge (DAB). The IC holds the dc voltage V_{dc1} across the capacitor C_{dc1} constant and has an ac side LC filter (L_f and C_f). Given that V_{dc1} is held constant by the IC, the DAB modulates the voltage V_{dc2} across C_{dc2} to facilitate the bidirectional power flow.

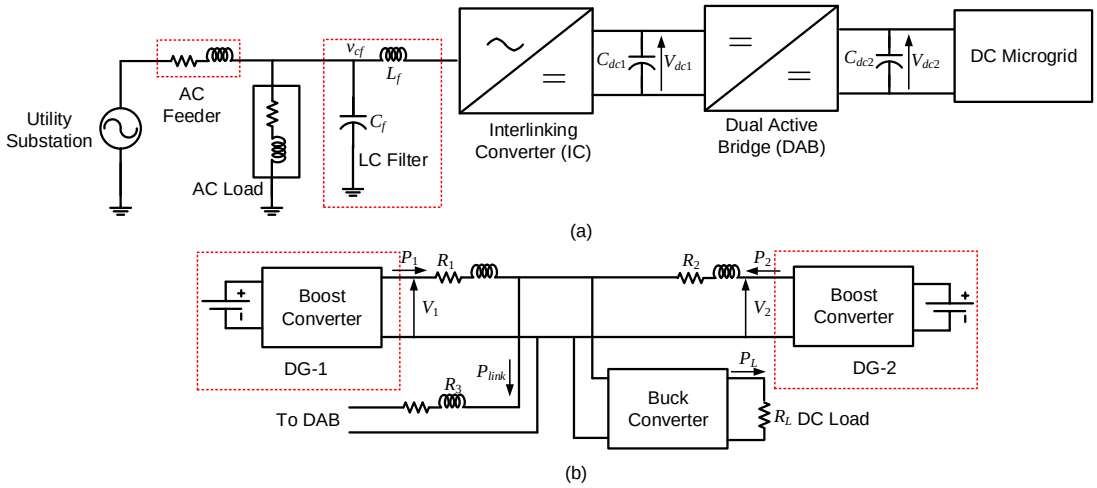

Fig. 4.17. (a) The overall system structure, and (b) the structure of the dc microgrid.

4.3.2. Dual Active Bridge Modelling and Control

The schematic diagram of a dual active bridge bi-directional dc-dc converter is shown in Fig. 4.18 (a). It contains two H-bridges that are connected together through a high frequency transformer. Here L is the leakage inductance of the transformer and any added inductance, while R represents the losses.

There are different control strategies of DAB such as single phase shift (SPS) control, extended phase shift control, dual phase shift control and triple phase shift control [155]. In the SPS control, the cross connected switches of the H-bridge are provided same rectangular pulse and the other two switches are provided a complementary phase shifted rectangular pulse. In the other H-bridge the switching pulses are phase shifted from the first one. By controlling the phase shift, the output voltage and the power flow in the desired direction can be achieved. In this research

work, the SPS control method is selected. In the SPS control, the cross connected switches of the H-bridge are provided same rectangular pulse and the other two switches

Since the DAB contains two H-bridge converters, this has four possible switching states, given by

$$v_p = \begin{cases} V_{dc} & \text{when } S_1 \text{ is ON and } S_2 \text{ is OFF} \\ -V_{dc} & \text{when } S_2 \text{ is ON and } S_1 \text{ is OFF} \end{cases}$$
$$v_s = \begin{cases} V_0 & \text{when } S_3 \text{ is ON and } S_4 \text{ is OFF} \\ -V_0 & \text{when } S_4 \text{ is ON and } S_3 \text{ is OFF} \end{cases} \quad (4.8)$$

It is assumed that both the H-bridges are operated at 50% duty ratio. However their switching is shifted by an instant ϕ as shown in Fig. 4.18 (b). The phase shift ϕ is the control variable.

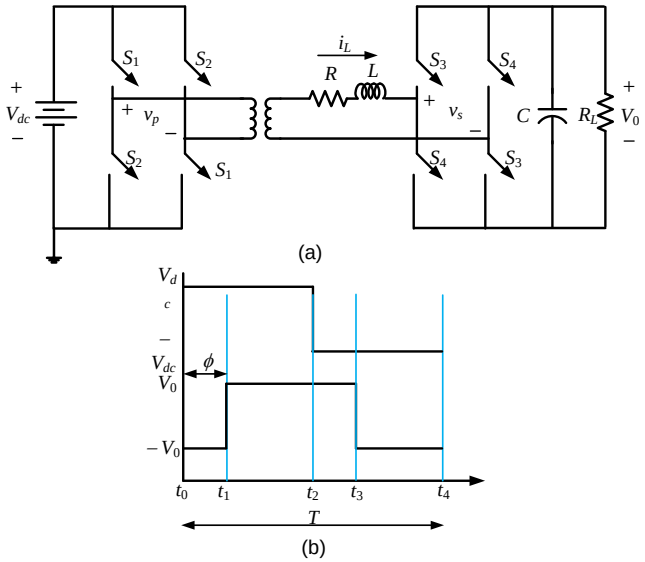

Fig. 4.18. (a) Schematic diagram of a DAB and (b) its switching states.

A sequence of 4 state space equations can be written to represent the behaviour of the DAB over one switching cycle:

$$\dot{x} = \begin{cases} A_1 x + B_1 V_{dc} & \text{for } t_0 \le t < t_1 \\ A_2 x + B_2 V_{dc} & \text{for } t_1 \le t < t_2 \\ A_3 x + B_3 V_{dc} & \text{for } t_2 \le t < t_3 \\ A_4 x + B_4 V_{dc} & \text{for } t_3 \le t < t_4 \end{cases} \tag{4.9}$$

where

$$A_1 = A_4 = \begin{bmatrix} -1/R_L C & -1/C \\ 1/L & -R/L \end{bmatrix}, A_2 = A_3 = \begin{bmatrix} -1/R_L C & 1/C \\ -1/L & -R/L \end{bmatrix}$$
$$B_1 = B_2 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix}, B_3 = B_4 = \begin{bmatrix} 0 \\ -1/L \end{bmatrix}$$

We note from Fig. 4.18 (b) that $t_1 - t_0 = \phi$, $t_2 - t_1 = T/2 - \phi$, $t_3 - t_2 = \phi$ and $t_4 - t_3 = T/2 - \phi$. Also since all the A matrices are non-singular, the solutions of the four state equations are given by

$$x(t_1) = e^{A_1 \phi} x(t_0) - A_1^{-1}\left[I - e^{A_1 \phi}\right] B_1 V_{dc} \tag{4.10}$$

$$x(t_2) = e^{A_2 (T/2-\phi)} x(t_1) - A_2^{-1}\left[I - e^{A_2 (T/2-\phi)}\right] B_2 V_{dc} \tag{4.11}$$

$$x(t_3) = e^{A_3 \varphi} x(t_2) - A_3^{-1}\left[I - e^{A_3 \varphi}\right] B_3 V_{dc} \tag{4.12}$$

$$x(t_4) = e^{A_4 (T/2-\phi)} x(t_3) - A_4^{-1}\left[I - e^{A_4 (T/2-\phi)}\right] B_4 V_{dc} \tag{4.13}$$

Since all the A matrices are non-singular, the solutions of (4.10-4.13) are given as

$$\begin{aligned} x(t_1) &= e^{A_1 \phi} x(t_0) + \left\{ \int_0^{\phi} e^{A_1 (\phi - \tau)} d\tau \right\} B_1 V_{dc} \\ &= e^{A_1 \phi} x(t_0) - A_1^{-1}\left[e^{A_1 (\phi - \tau)} \Big|_0^{\phi} \right] B_1 V_{dc} \\ &= e^{A_1 \phi} x(t_0) - A_1^{-1}\left[I - e^{A_1 \phi}\right] B_1 V_{dc} \end{aligned} \tag{4.14}$$

$$
\begin{aligned}
x(t_2) &= e^{A_2(T/2-\phi)}x(t_1)+\left\{\int_0^{T/2-\phi} e^{A_2(T/2-\phi-\tau)}d\tau\right\}B_2V_{dc} \\
&= e^{A_2(T/2-\phi)}x(t_1)-A_2^{-1}\left[e^{A_2(T/2-\phi-\tau)}\Big|_0^{T/2-\phi}\right]B_2V_{dc} \\
&= e^{A_2(T/2-\phi)}x(t_1)-A_2^{-1}\left[I-e^{A_2(T/2-\phi)}\right]B_2V_{dc}
\end{aligned} \tag{4.15}
$$

$$
x(t_3) = e^{A_3\phi}x(t_2)-A_3^{-1}\left[I-e^{A_3\phi}\right]B_3V_{dc} \tag{4.16}
$$

$$
x(t_4) = e^{A_4(T/2-\phi)}x(t_3)-A_4^{-1}\left[I-e^{A_4(T/2-\phi)}\right]B_4V_{dc} \tag{4.17}
$$

Combining (4.14-4.17), we have

$$
x(t_4) = Fx(t_0)+GV_{dc} \tag{4.18}
$$

where

$$
F = e^{A_4(T/2-\phi)}e^{A_3\phi}e^{A_2(T/2-\phi)}e^{A_1\phi}
$$

$$
\begin{aligned}
G &= -e^{A_4(T/2-\phi)}e^{A_3\phi}e^{A_2(T/2-\phi)}A_1^{-1}\left[I-e^{A_1\phi}\right]B_1-e^{A_4(T/2-\phi)}e^{A_3\phi}A_2^{-1}\left[I-e^{A_2(T/2-\phi)}\right]B_2 \\
&\quad -e^{A_4(T/2-\phi)}A_3^{-1}\left[I-e^{A_3\phi}\right]B_3-A_4^{-1}\left[I-e^{A_4(T/2-\phi)}\right]B_4 \\
&= -e^{A_4(T/2-\phi)}e^{A_3\phi}e^{A_2(T/2-\phi)}A_1^{-1}B_1+e^{A_4(T/2-\phi)}e^{A_3\phi}e^{A_2(T/2-\phi)}A_1^{-1}e^{A_1\phi}B_1 \\
&\quad -e^{A_4(T/2-\phi)}e^{A_3\phi}A_2^{-1}B_2+e^{A_4(T/2-\phi)}e^{A_3\phi}A_2^{-1}e^{A_2(T/2-\phi)}B_2 \\
&\quad -e^{A_4(T/2-\phi)}A_3^{-1}B_3+e^{A_4(T/2-\phi)}A_3^{-1}e^{A_3\phi}B_3-A_4^{-1}B_4+A_4^{-1}e^{A_4(T/2-\phi)}B_4
\end{aligned}
$$

Therefore

$$
\begin{aligned}
\frac{\partial F}{\partial \phi} &= e^{A_4(T/2-\phi)}e^{A_3\phi}e^{A_2(T/2-\phi)}e^{A_1\phi} \\
&= -A_4e^{A_4(T/2-\phi)}e^{A_3\phi}e^{A_2(T/2-\phi)}e^{A_1\phi}+e^{A_4(T/2-\phi)}A_3e^{A_3\phi}e^{A_2(T/2-\phi)}e^{A_1\phi} \\
&\quad -e^{A_4(T/2-\phi)}e^{A_3\phi}A_2e^{A_2(T/2-\phi)}e^{A_1\phi}+e^{A_4(T/2-\phi)}e^{A_3\phi}e^{A_2(T/2-\phi)}A_1e^{A_1\phi}
\end{aligned} \tag{4.19}
$$

$$\frac{\partial G}{\partial \phi} = A_4 e^{A_4(T/2-\phi)} e^{A_3\phi} e^{A_2(T/2-\phi)} A_1^{-1} B_1 - e^{A_4(T/2-\phi)} A_3 e^{A_3\phi} e^{A_2(T/2-\phi)} A_1^{-1} B_1$$
$$+ e^{A_4(T/2-\phi)} e^{A_3\phi} A_2 e^{A_2(T/2-\phi)} A_1^{-1} B_1$$
$$- A_4 e^{A_4(T/2-\phi)} e^{A_3\phi} e^{A_2(T/2-\phi)} A_1^{-1} e^{A_1\phi} B_1 + e^{A_4(T/2-\phi)} A_3 e^{A_3\phi} e^{A_2(T/2-\phi)} A_1^{-1} e^{A_1\phi} B_1$$
$$- e^{A_4(T/2-\phi)} e^{A_3\phi} A_2 e^{A_2(T/2-\phi)} A_1^{-1} e^{A_1\phi} B_1 + e^{A_4(T/2-\phi)} e^{A_3\phi} e^{A_2(T/2-\phi)} e^{A_1\phi} B_1$$
$$+ A_4 e^{A_4(T/2-\phi)} e^{A_3\phi} A_2^{-1} B_2 - e^{A_4(T/2-\phi)} A_3 e^{A_3\phi} A_2^{-1} B_2 - A_4 e^{A_4(T/2-\phi)} e^{A_3\phi} A_2^{-1} e^{A_2(T/2-\phi)} B_2$$
$$+ e^{A_4(T/2-\phi)} A_3 e^{A_3\phi} A_2^{-1} e^{A_2(T/2-\phi)} B_2 - e^{A_4(T/2-\phi)} e^{A_3\phi} e^{A_2(T/2-\phi)} B_2$$
$$+ A_4 e^{A_4(T/2-\phi)} A_3^{-1} B_3 - A_4 e^{A_4(T/2-\phi)} A_3^{-1} e^{A_3\phi} B_3 + e^{A_4(T/2-\phi)} e^{A_3\phi} B_3 - e^{A_4(T/2-\phi)} B_4 \tag{4.20}$$

We now shall derive a linearized model over a switching cycle, i.e., between t_0 and t_4. For linearization, we define the following state and input variables

$$x = x_0 + \tilde{x}, \quad \phi = \phi_o + \tilde{\phi} \tag{4.21}$$

where the subscript 0 denotes the steady state values around which the linearization takes place and Δ denotes its perturbation. In the steady state, the values of the state variables remain the same at the end of each switching cycle, i.e., $x(t_4) = x(t_0)$. We assume these as two successive sampling instants, i.e., $k + 1$ and k and in the steady state $x(t_0) = x_0$. Then the linearized equation from (4.18) is given as

$$\tilde{x}(k+1) = F_0 \tilde{x}(k) + \left(\frac{\partial F}{\partial \phi} x_0 + \frac{\partial G}{\partial \phi} V_{dc} \right) \tilde{\phi} = A\tilde{x}(k) + B\tilde{\phi} \tag{4.22}$$

$$\tilde{y}(k) = C_1 \tilde{x}(k) \tag{4.23}$$

A state feedback with an integral control action is now proposed. The discrete-time equivalent of the integral controller is given by

$$\begin{aligned} e(k) &= \tilde{y}(k) - \tilde{y}_{ref}(k) \\ z(k) &= z(k-1) + K_I e(k) \end{aligned} \tag{4.24}$$

where y_{ref} is the reference voltage. Substituting (4.23) into (4.24), we get

$$z(k+1) = z(k) + K_I C_1 \tilde{x}(k) - K_I \tilde{y}_{ref}(k) \tag{4.25}$$

An extended state vector is now defined as

$$x_e(k) = \begin{bmatrix} \tilde{x}(k) \\ z(k) \end{bmatrix}$$

Then from (4.22) and (4.25), the extended state space description of the system can be written as

$$x_e(k+1)=\begin{bmatrix} A & 0 \\ K_I C_1 & 1 \end{bmatrix} x_e(k)+\begin{bmatrix} B \\ 0 \end{bmatrix}\tilde{\phi}(k)-\begin{bmatrix} 0 \\ K_I \end{bmatrix}\tilde{y}_{ref}(k) \tag{4.26}$$

A state feedback controller is then designed that is of the form

$$\tilde{\phi}(k)=-Kx_e(k) \tag{4.27}$$

which will force the output error $e(k)$ to zero asymptotically.

4.3.3. CALCULATION OF STEADY STATE

If the converter is assumed to be lossless, the power transfer relationship is given by [156, 157]

$$P_1 = P_2 = \frac{V_{dc} V_0 \phi(\pi-\phi)}{2\pi^2 fL} \tag{4.28}$$

Therefore the power transfer is zero either when $\phi = 0$ or when $\phi = \pi$ and the maximum power is transferred when $\phi = \pi/2$. For the state feedback control of (4.27), a linearized model of the system is required. From (4.28), it can be seen for constant V_{dc}, P_2 and ϕ, the output voltage V_0 will change with the output resistance.

The first step in the linearization process is to decide a nominal value of the output power P_{20}. Given the input voltage V_{dc}, a desired nominal output voltage $V_0 = V_{00}$ is chosen. Therefore the load resistance is then be given by $R_L = (V_0)^2/P_{20}$. The matrices A_1, A_2, A_3 and A_4 are now calculated based on this value of R_L.

Now (4.28) can be rewritten as

$$\phi^2 - \pi\phi \frac{2\pi^2 fL}{V_{dc} V_{00}} P_{20} = 0 \tag{4.29}$$

Solving the quadratic equation and choosing the lesser of the two values, the nominal value of the phase shift ϕ_0 is obtained. Therefore, with these values, the steady state values of the state vector is computed from (4.18) as

$$x_{ss} = \left(I - F\right)^{-1} G V_{dc} \tag{4.30}$$

These are now used for linearized model and control derivation.

4.3.4. POWER FLOW CONTROL

Comparing Fig. 4.18 (a) with Fig. 4.17 (a), it is obvious that input voltage V_{dc} is V_{dc1} and the output voltage V_0 is V_{dc2}. While the former is controlled by the interlinking converter (Section 4.1), the reference for latter is determined by the desired link power transfer. Let us denote the desired link power by P_{link}^*. Then the reference voltage for the DAB is obtained though the following proportional plus integral (PI) controller of the form

$$\begin{aligned} e_l &= P_{link}^* - P_{link} \\ V_{dc2,ref} &= V_{ref} - K_{Pl} e_l - K_{Il} \int e_l dt \end{aligned} \tag{4.31}$$

4.3.5. EFFICIENCY OF DAB

The copper loss is dependent on the ac resistance of the inductor, ac resistance of the HV and LV winding of the transformer. A negligible magnetizing current is assumed and the current harmonics of the high frequency transformer is ignored for the lossless model of DAB. [158]. Kolar et al. reported an efficiency of 90.6% with their optimal modulation scheme.

Fig. 4.19 (b) shows that 3kW power is lost in primary to secondary. Power in the primary side of the high frequency transformer is 28 kW and in the secondary side is 25kW. 10% power loss can be seen in this simulation. 0.0001 p.u. leakage reactance,

air-core reactance of 0.2 p.u., magnetizing current of 0.4% is defined for the high frequency transformer to reflect practical situation in the simulation studies.

4.3.6. SIMULATION RESULTS

Simulation studies are carried out in PSCAD, with the system data given in Table 4.3. The control parameters for the DAB, three dc-dc converters and the VSC are calculated in MATLAB and then are used to run simulations in PSCAD.

Performance of a DAB with a load is shown in Fig. 4.19. DC voltage of the DAB is 2500V and the load voltage is designed to be 500V. Fig 4.19 (a) shows that primary voltage of the DAB is 2500V and the secondary voltage is 500V with a phase shift from the primary voltage. According to equation 4.8 primary voltage of the high frequency transformer should equal V_{dc} and secondary voltage should equal the load voltage. Fig. 4.19 (a) also shows that the H-bridges are operated at 50% duty ratio and their switching is shifted in every switching cycle. Phase shift is defined as a function of the duty cycle. Fig. 19 (b) shows the power output at primary and secondary side of the high frequency transformer. Fig. 19 (c) shows that phase shift changes with the change in power.

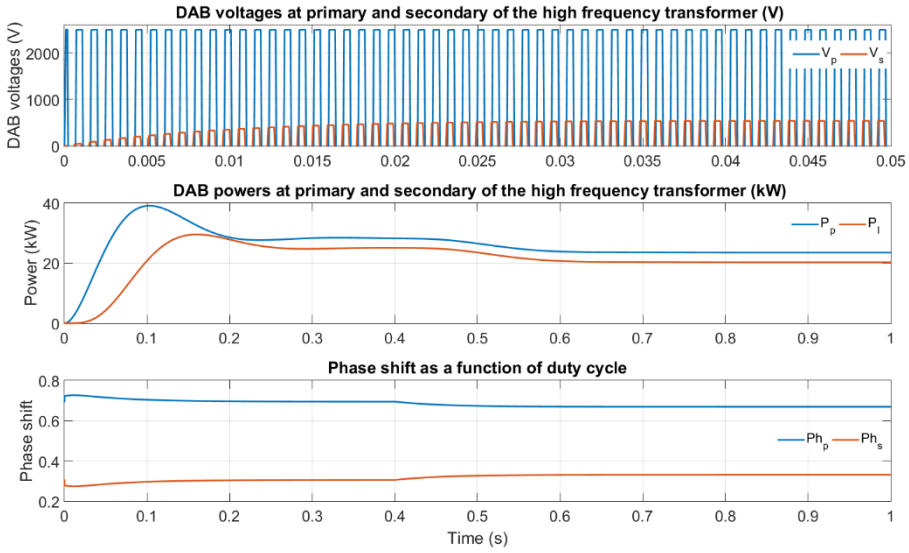

Fig. 4.19 Performance of DAB: (a) voltages (b) power and (c) phase shifts at primary and secondary of the high frequency transformer, (b) dc link voltage and (c) voltage angle.

Two case studies are performed. These are discussed below.

A. Case 1: Nominal Operation

In this case, it is assumed that no power flows through the DAB and the utility side and the DCMG perform operate in isolated fashion. The nominal phase shift in the DAB is calculated as per (4.28), for an input voltage of 15 kV and an output voltage of 500 V. The total load in the DCMG is 78.5 kW and the power generated by the two DGs are 48.7 kW and 24.6 kW. For this power level, the voltages V_1 and V_2 will be roughly around 475 V. Also the power supplied by the utility to supply its local loads and the converter losses is 565 kW.

With the system remaining in the steady state, the DCMG load is changed to 148.5 kW at 0.3 s. The results are shown in Figs. 4.20-4.22. Fig. 4.20 shows the performance of the utility and IC, where it can be seen that, barring a transient during the load change, the utility power, dc capacitor voltage V_{dc1} and voltage angle δ maintain their pre-load change values. The performance of the DCMG is depicted in Fig. 4.21. It can be seen that the power supplied by the DGs rises to 101 kW and 51 kW to cater to the load change. The voltages V_1 and V_2 drop to around 449.5 V in sympathy with the load change.

Table 4.3: System parameters

Quantities	Values
AC Side	
AC source voltage	11 kV (L-L)
System frequency	50 Hz
AC feeder impedance	Inductance: 38.6 mH and resistance: 1.21 Ω
Filter parameters	L_f = 33 mH, C_f = 50 μF
Interlinking Converter	
dc Capacitor (C_{dc1})	5000 μF
Voltage Magnitude (V_m)	9 kV (peak)
Carrier waveform	15 kHz
Sampling frequency	30 kHz
dc voltage reference (V_{dc}^*)	15 kV
PI controller	$K_{P\delta}$ = – 0.1, $K_{I\delta}$ = – 0.5
DAB	
Transformer	2.5 kV/2.5 kV
Inductance	L = 0.4 mH
Switching frequency	10 kHz
PI controller	K_{Pl} = 2, K_{Il} = 100
dc Capacitor (C_{dc2})	5000 μF
DCMG	
Voltage reference (V_{ref})	500 V
Maximum voltage drop (ΔV)	100 V
DG rating	DG-1: 200 kW, DG-2: 100 kW
Droop gains	n_1 = 0.5, n_2 = 1.0
Line resistances	R_1 = 0.01 Ω, R_2 = 0.06 Ω, R_3 = 0.001 Ω

The performance of the DAB is shown in Fig. 4.22. It can be seen that the phase shift and hence the power flow through the link (P_{link}) remain zero as no power between the ac and dc systems are desired. This figure also shows the dc voltage V_{dc2} and its reference. It can be seen the voltage tracking by the DAB is perfect. Also these voltages drop after the load change to maintain zero power flow since V_1 and V_2 have dropped.

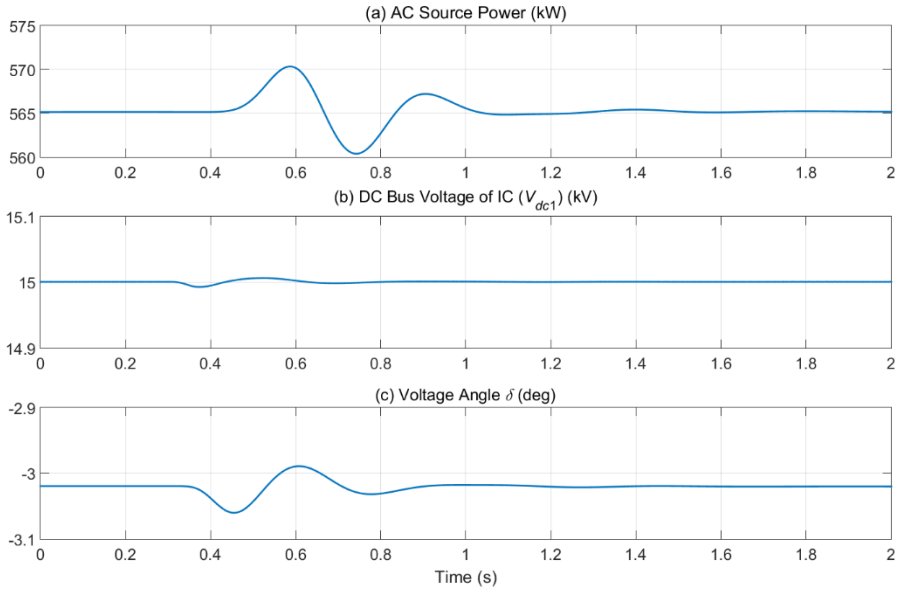

Fig. 4.20 Performance of utility and IC for Case 1: (a) source power, (b) dc link voltage and (c) voltage angle.

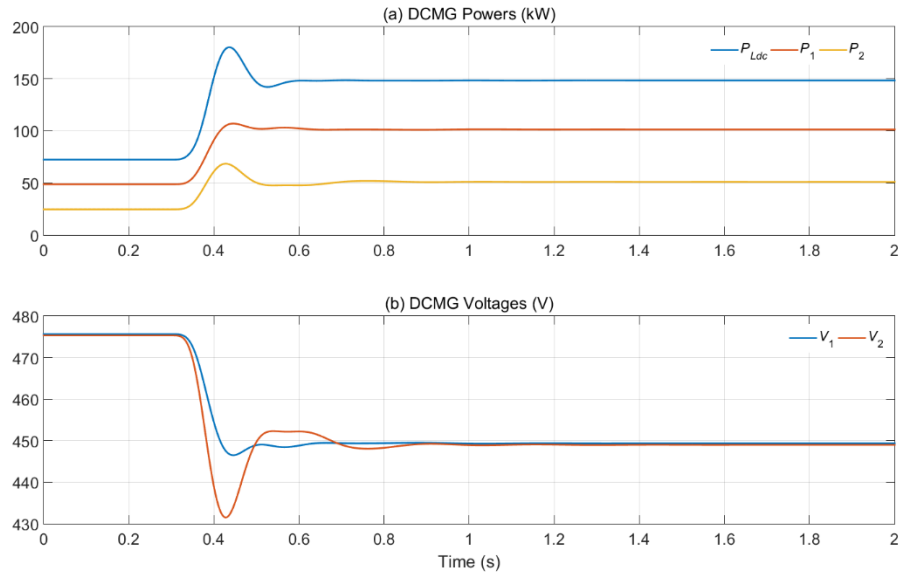

Fig. 4.21 Performance of DCMG for Case 1: (a) power flow and (b) voltages.

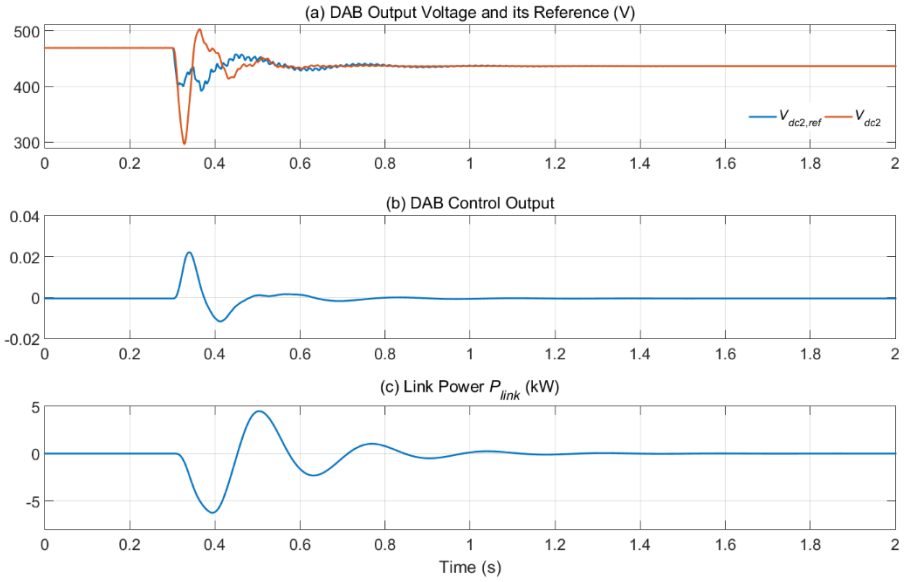

Fig. 4.22 Performance of DAB for Case 1: (a) voltage V_{dc2} and its reference, (b) phase shift and (c) power flow through the link.

B. Case 2: Power flow from AC Grid to DCMG

In this case, it is assumed that the utility grid starts supply 100 kW of power to the DCMG at 0.3 s when the systems are in the steady state and operating in isolated fashion. The total load in the DCMG is 202 kW and the power generated by the two

DGs are 140 kW and 70 kW. The voltages V_1 and V_2 are roughly around 430 V. The power supplied by the utility s is 565 kW. The results are shown in Figs. 4.23 and 4.24.

Fig. 4.23 shows that the power supplied by the utility increases to 665 kW. The capacitor voltage V_{dc1} is maintained at 15 kV and the voltage angle decreases to accommodate increased power flow from the utility. The results for the DCMG side are shown in Fig. 4.24. As evident from this figure, the power consumed by the dc load remains constant, however the DGs now supply less amount of power of 70 kW and 35 kW. The link power settles is – 100 kW. Due to the decrease in the power supplied by the DGs, the voltages rise to 465 V. Note that the power flow from the DCMG to the ac side is discussed in the next chapter.

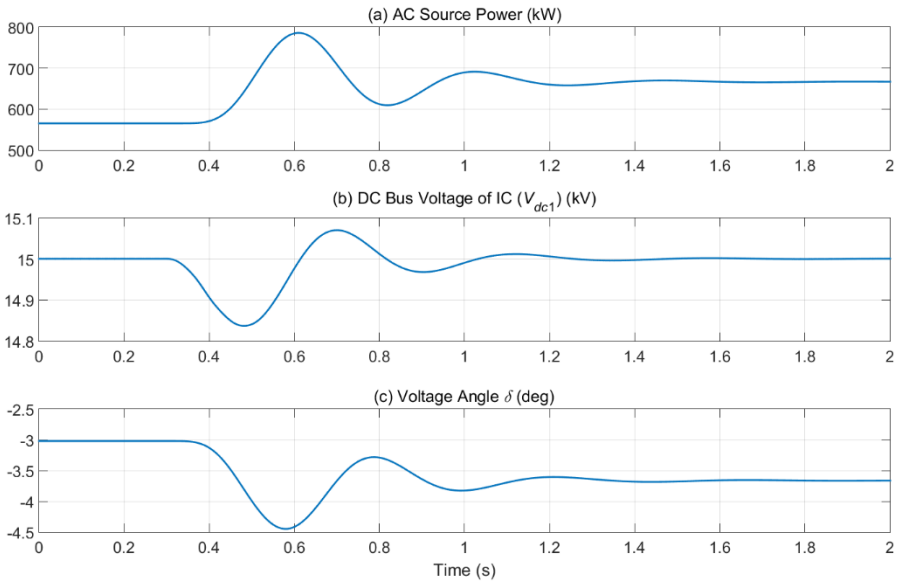

Fig. 4.23 Performance of utility and IC for Case 2: (a) source power, (b) dc link voltage and (c) voltage angle.

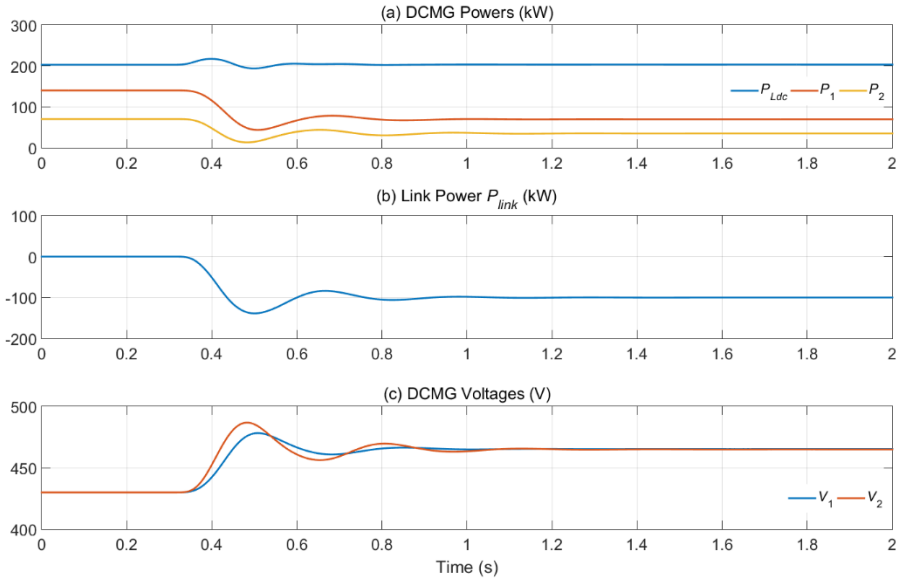

Fig. 4.24. Performance of DCMG for Case 2: (a) power flow, (b) link power and (c) voltages.

4.3.7. EXPERIMENTAL RESULTS

Hardware test results of nominal operation and power flow from AC grid to DCMG are reported in this section. A scaled prototype of the DCMG with a DAB is implemented for experimental verification of the proposed control scheme. Simulation results of the same hardware prototype is also presented in this section. DSPACE-1104 is used to measure the control parameters and then to implement the proposed control scheme. The experimental system is also simulated in PSCAD. A photograph of the hardware setup is shown in Fig. 4.25 and the system parameters of the hardware prototype is presented in Table 4.4.

Table 4.4: Hardware prototype parameters

DAB	
Inductance	L = 2.2 mH
Switching frequency	2 kHz
dc Capacitor (C_{dc2})	1100 μF
DCMG	
Voltage reference (V_{ref})	15 V
Maximum voltage drop (ΔV)	5 V
DG rating	DG-1: 30 W, DG-2: 15 W
Droop gains	n_1 = 0.5, n_2 = 1.0
Line resistances	R_1 = 1.1 Ω, R_2 = 1.3 Ω, R_3 = 1.2 Ω

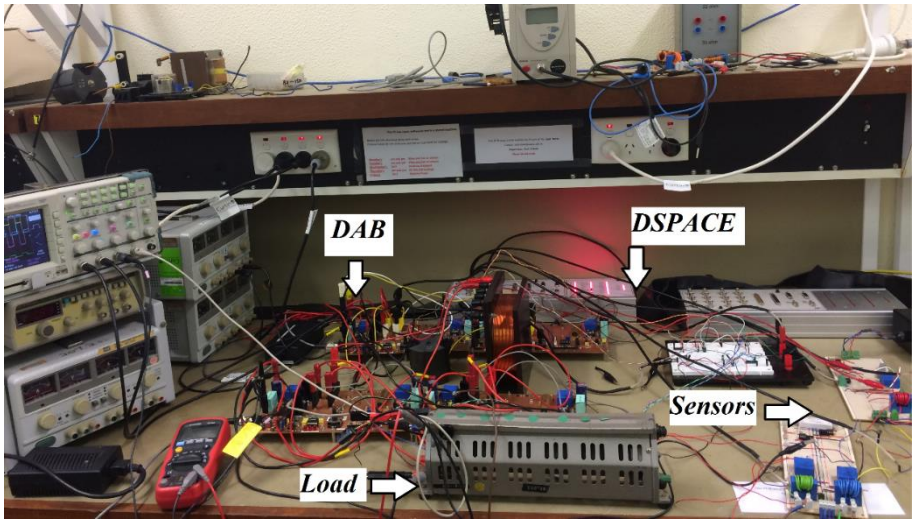

Fig. 4.25. Hardware prototype of the system

The hardware prototype of DAB is operated at a frequency of 2 kHz. The switching pulses of S_1, S_2, S_3 and S_4 are shown in Fig. 4.26. It is evident that the switches operate with 50% duty ratio. The phase shift is also evident in this figure.

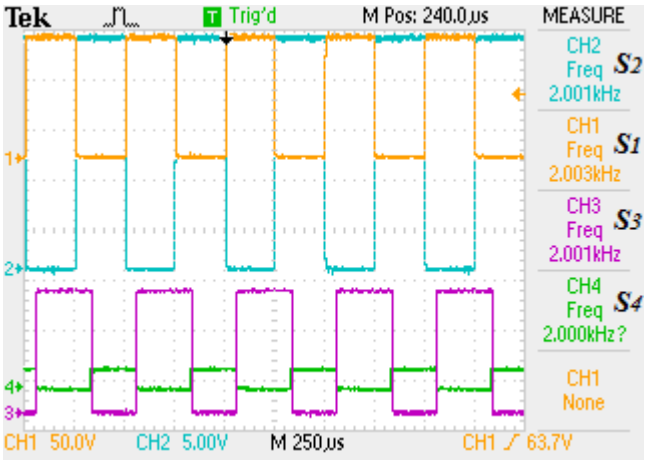

Fig. 4.26. Firing pulses of the DAB switches.

During Nominal operation, DCMG is self-sufficient and hence no power needs to be supplied by the utility through the DAB. It has been assumed that the rating of the two DGs have a ratio of 2:1 and together they have a maximum rating of 0.6 p.u. The power supplied by the DGs is shown in Fig. 4.27 (simulation) and Fig. 4.28 (hardware) when the load is 0.6 p.u. The DG voltages and currents are also shown in these figures.

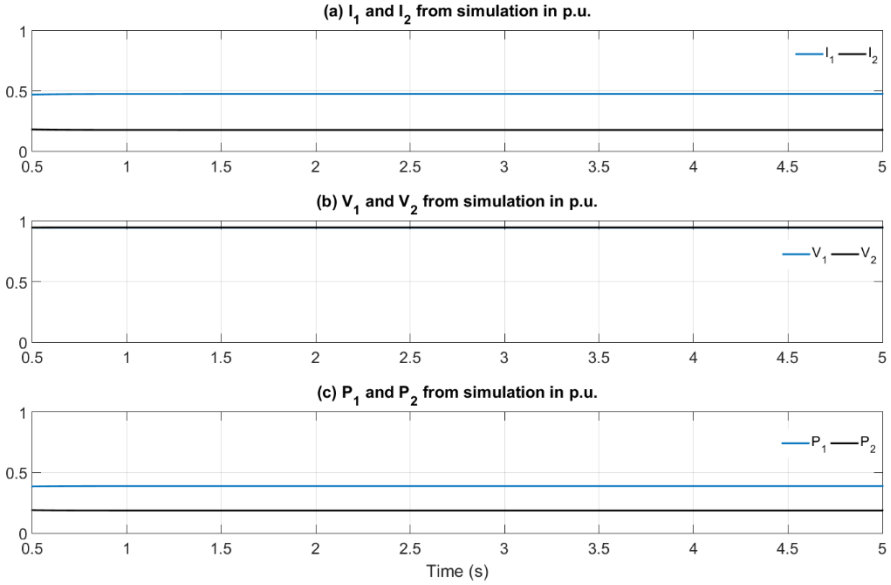

Fig. 4.27. Simulation results of the DCMG at Nominal operation

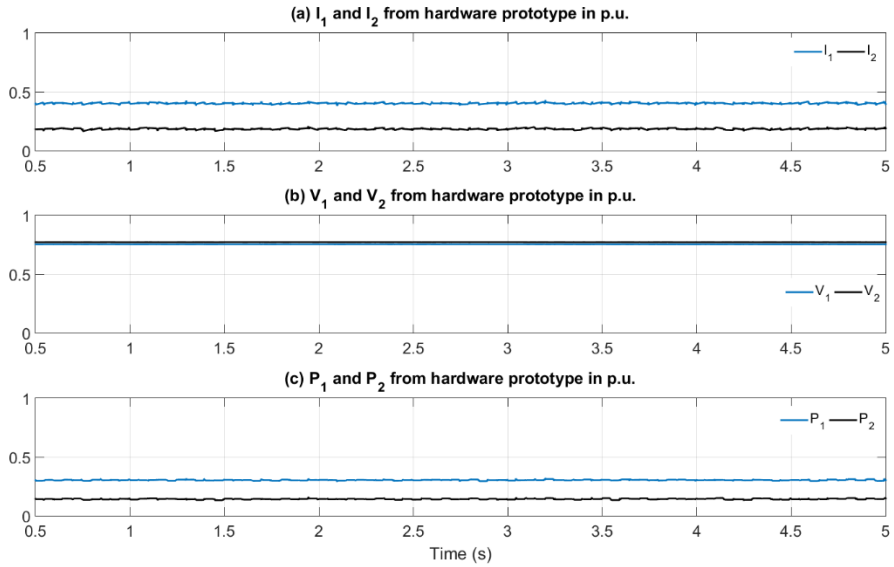

Fig. 4.28. Hardware results of the DCMG at Nominal operation

Figs 4.29 and 4.30 show the DAB output voltage, current and power when the utility supplies power to the DCMG, when the load is increased to 0.77 p.u.. It is evident that the additional power is supplied to the load through DAB. When the load is load is increased to 0.8 p.u, power through the DAB becomes 0.2 p.u, as evident from Fig. 4.31 and 4.32. For this case, the flow from the DAB increases and its output voltage drops. It can be noticed from this studies that the hardware results has some ripples, which not present in simulations, as expected.

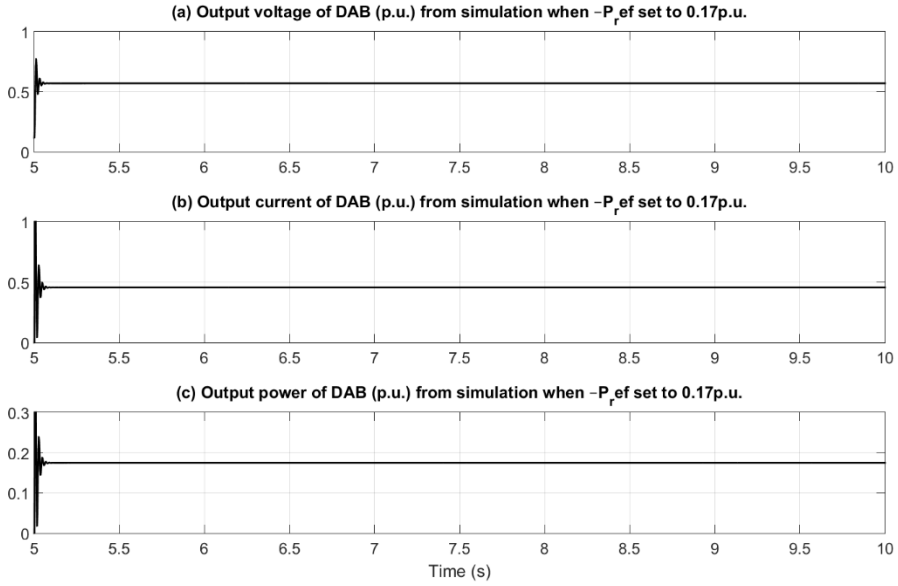

Fig. 4.29 Simulation of the Performance of the DAB at -P_{ref} set to 0.17 p.u.

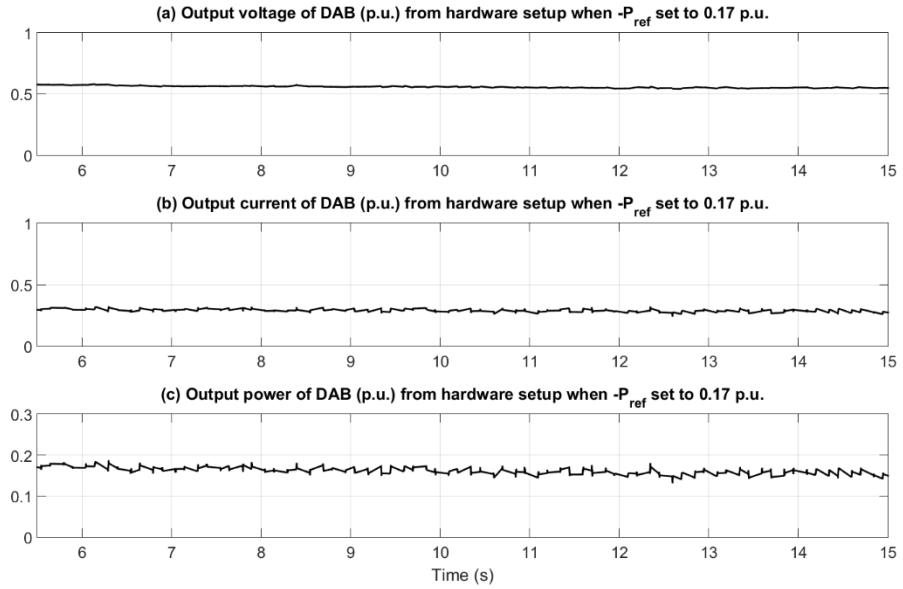

Fig. 4.30 Hardware test results of the Performance of the DAB at -P_{ref} set to 0.17 p.u.

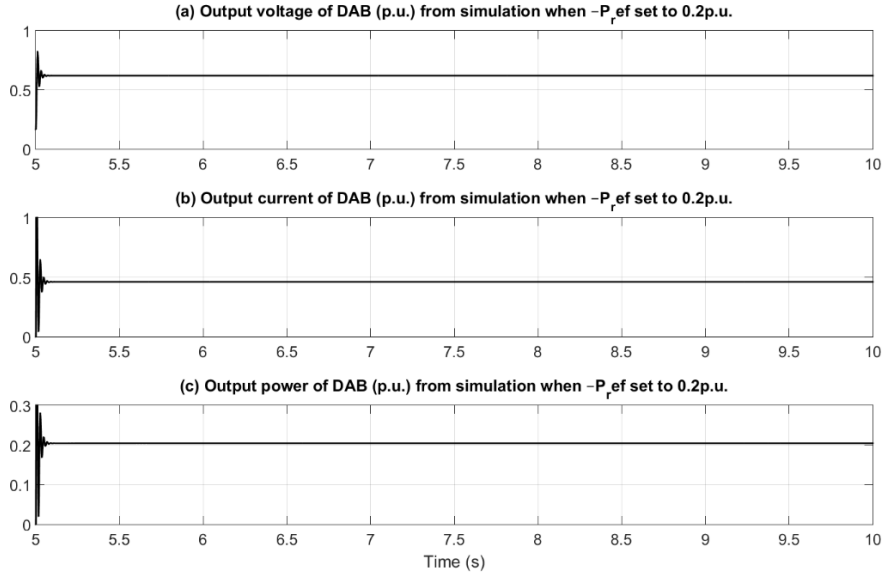

Fig. 4.31 Simulation of the Performance of the DAB at -P_{ref} set to 0.20 p.u.

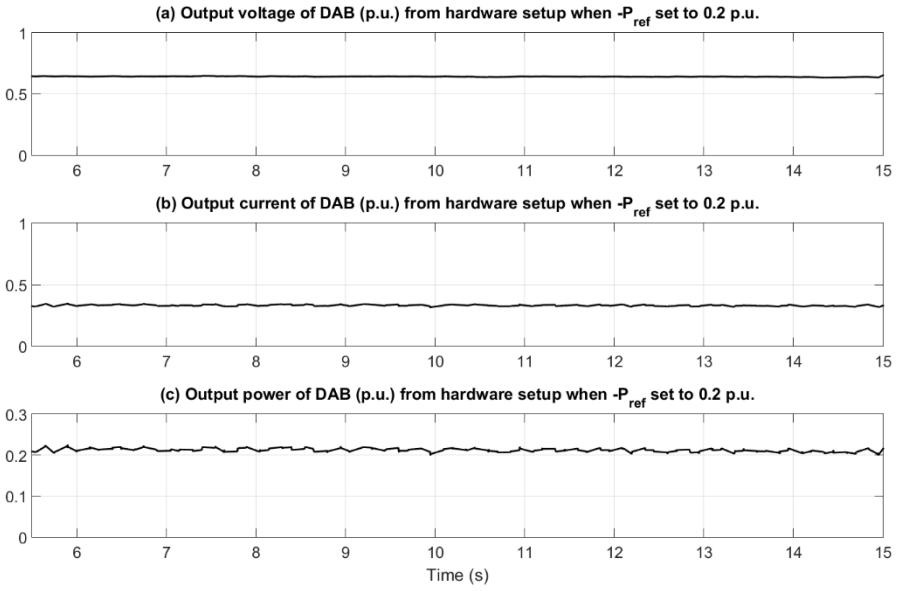

Fig. 4.32 Hardware test results of the Performance of the DAB at -P_{ref} set to 0.20 p.u.

4.4 CONCLUSIONS

In this chapter, a PFC is designed to manage a controlled power flow from an ac side to a DCMG. Three different topologies are discussed, in each of which, The PFC draws a predefined amount of power from the utility. In all these methods, IC regulates the ac side voltage through dc capacitor control. Since the dc side of the interlinking converter is isolated from the DCMG, it does not participate in droop sharing in the DCMG. Through this, the mismatch between units of the droop coefficients between the two sides of the IC has been avoided.

Out of the three topologies presented in this chapter, only one restricts the power flow from the ac side to the dc side. Bidirectional power flow is possible through the other two methods. Out of the last two methods, the topology using DAB is more versatile as it can facilitate smooth power flow in either direction and no switching is necessary. For this, a new power flow control strategy for the DAB is proposed based on discrete-time state feedback with integral control. For this, a linearized model of the DAB has been designed based on the nominal power transfer condition. The veracity of the scheme is verified through both simulation and experimental results.

CHAPTER 5

POWER SHARING IN AN INTERCONNECTED AC/DC MICROGRID

In the last chapter, a DCMG connection to an ac utility has been discussed. In this chapter, the connection of DCMG with an ac microgrid (ACMG) is discussed. As will be illustrated in this chapter, this type of interconnection increases the system reliability. Through this, either of the microgrids can support the other during power deficiency. As presented in the last chapter, the ac and dc sub-systems can be tied together by interlinking converter (VSC) to allow bidirectional power flow though different configurations. However of the configurations discussed in the last chapter, the use of dc-dc converter is not suitable for bidirectional power flow and is not considered in this chapter.

In this chapter, only bidirectional switch and DAB are considered for power sharing between an ACMG and a DCMG. The main aim of the interconnection is to supply power to either of the MGs during its power shortfall. Only the amount of power required to maintain the stability of either of the MGs will be drawn for the other MG. This will avoid unnecessary load shedding, provided that the MG supplying power has sufficient reserve. The proposals presented in this chapter are verified through extensive simulation results using EMTDC/PSCAD.

5.1. ACMG OPERATION THROUGH FREQUENCY DROOP

The DGs in the ACMG are controlled in a decentralized manner through real power –frequency (*P-f*) and reactive power-voltage (*Q-V*) droop, given by

$$f = f_r + m \times \left(0.5P^* - P\right) \tag{5.1}$$

$$V = V_r + n \times (Q^* - Q) \tag{5.2}$$

where f_r and f are the rated and instantaneous frequency of the system respectively. The rated and actual real power are denoted by P^* and P respectively; Q^* and Q are the

rated and actual reactive power respectively. The droop coefficients are denoted by *m* and *n*.

The droop gain is such chosen that the frequency deviation is restricted to ± Δ*f* from the reference frequency f_r, which is taken as 50 Hz. For example, when the DGs are supplying their maximum rated power, the frequency will be 50 – Δ*f* Hz, and when they are not supplying any power, the frequency will be 50 + Δ*f* Hz. For the latter case, the droop gain of the i^{th} DG is given by [72].

$$\begin{aligned} & f_r + \Delta f = f_r + m_i \times 0.5 P_i^* \\ & \Rightarrow m_i = \frac{\Delta f}{0.5 P_i^*} \end{aligned} \tag{5.3}$$

It is to be note that all the DGs in an ACMG must operate at the same frequency. Therefore the droop gains of all the DGs must obey (5.3). Assume that there are a total number of *N* DGs in a microgrid. Then the product of the droop gain and the power rating of the DGs will be given by [72]

$$m_1 \times P_1^* = m_2 \times P_2^* = \cdots = m_N \times P_N^* = 2\Delta f \tag{5.4}$$

5.1.1. POWER SHORTFALL MANAGEMENT IN ACMG

As mentioned earlier, the MG must draw the exact amount of power that is required to meet its power shortfall. Let there be a total number N_{AC} of DGs in the ACMG and M_{AC} is its total number loads. Then for the stable operation of the MG, the following condition must be true

$$\sum_{k=1}^{N_{AC}} P_k^* \geq \sum_{k=1}^{M_{AC}} P_{Lk} + P_{Loss}^{AC} \tag{5.5}$$

where P_{Loss}^{AC} is the line loss in the ac circuit.

Let us now define the following power shortfall quantity

$$P_{SF}^{AC} = \sum_{k=1}^{M_{AC}} P_{Lk} + P_{Loss}^{AC} - \sum_{k=1}^{N_{AC}} P_k^* \tag{5.6}$$

If $P_{SF}^{AC} > 0,$ the frequency will drop below *f* – Δ*f* Hz. The basic aim is to bring the frequency back to *f* – Δ*f* Hz and hold it there till the overload condition has been

removed. Based on this argument, a proportional plus integral (PI) controller is designed that set the reference P_{dca}^{*} for the amount of power to be drawn from the DCMG as

$$e_f = f_r - \Delta f - \hat{f}$$
$$P_{dca}^{*} = K_{Pf}\, e_f + K_{If} \int e_f \, dt \tag{5.8}$$

where $\hat{f}$ is the measured or estimated microgrid frequency. The block diagram of the overload prevention scheme is shown in Fig. 5.1. The estimated frequency $\hat{f}$ is compared with a fixed number of $f_r - \Delta f$. If this is greater than 0, then a trigger signal (T_{rga}) is activated. Otherwise the trigger signal remains zero. If T_{rga} = 1, the input to the PI controller is e_f as in (5.8). When the T_{rga} changes from 1 to 0, a one shot Schmitt trigger is used to generate a pulse that will reset the integrator. The input to the PI controller is then changed to 0 such that P_{dca}^{*} is zero as no power is required from the DC-MG.

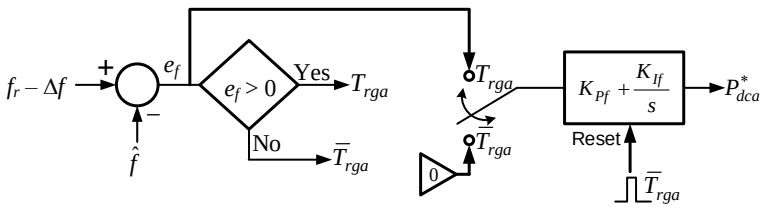

Fig. 5.1. Schematic diagram of overload prevention in AC-MG.

It is to be noted that the power shortfall prevention in DCMG has already been discussed in Sub-section 4.2.2 of the previous chapter.

5.2. POWER MANAGEMENT IN AN AC/DC MICROGRID WITH BIDIRECTIONAL SWITCH

The system structure considered in this study is shown in Fig. 5.2. The IC regulates the voltage across the dc capacitor C_{dc} according to the power flow requirement. The switch pairs S_{w1} and S_{w2} are normally open. One of them closes to facilitate power transfer in the required direction only when a command is issued. For example, when the ACMG needs to supply power to the DCMG, S_{w1} closes.

Alternatively S_{w2} closes when the DCMG supplies power to the ACMG. Former case was discussed in the previous chapter and the latter case is discussed in this chapter.

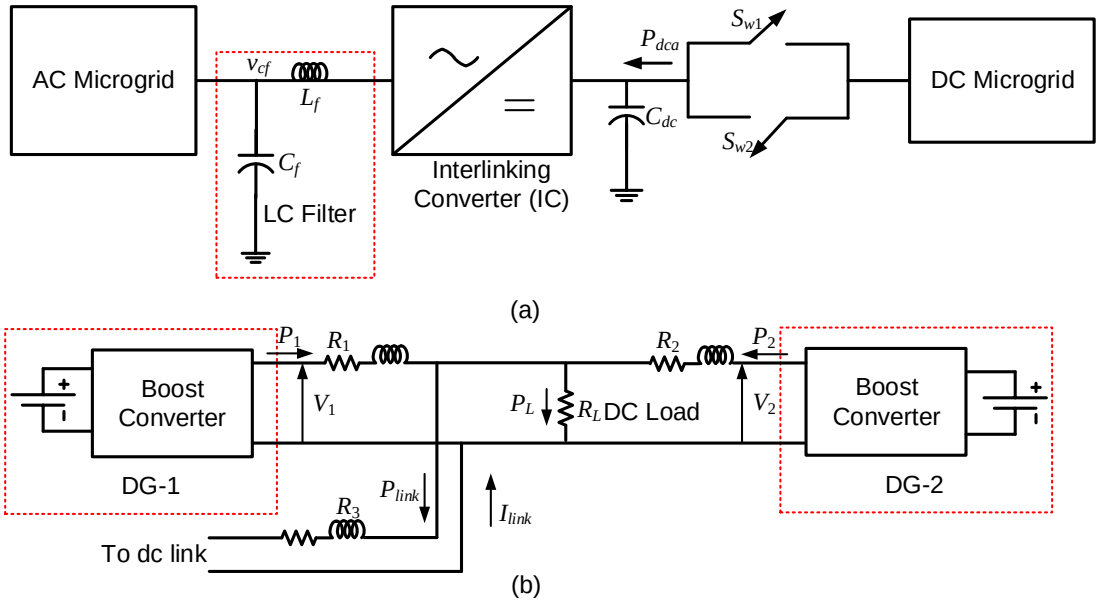

Fig 5.2. (a) Schematic diagram of an interconnected ac/dc system and (b) the structure of the dc microgrid.

To manage the power shortfall in the ACMG, the reference power P_{dca}^* is computed from (5.8). Thereafter, the voltage across the capacitor C_{dc} is changed to facilitate this amount of power flow from the DCMG. The schematic diagram for the capacitor voltage reference generation scheme is shown in Fig. 5.3. In this, the direction of power flowing from the DCMG to the ACMG is taken as positive and this power is denoted by P_{dc}. A 2-by-1 multiplexer is used for selecting the correct power reference, as shown in Fig. 5.3. For example, when $s1s0 = 01$ (i.e., only T_{rga} is 1), P_{dca}^* is selected as the reference power. On the other hand, when $s1s0 = 00$ no power will be supplied from the DCMG, i.e., ACMG will run in an islanded mode. The reference is then compared with the power flowing out of the dc capacitor and is passed through a third PI controller to generate the capacitor voltage reference V_{Lref}. This PI controller is realized, as given in (4.7) of Chapter 4.

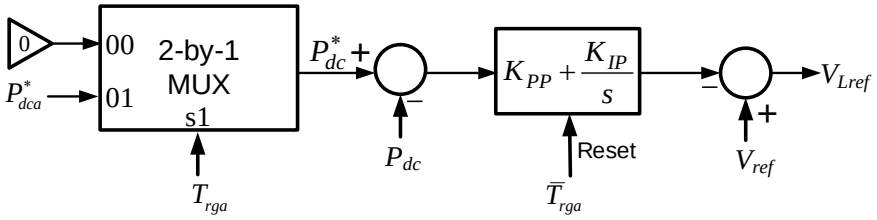

Fig. 5.3. Voltage reference generation schematic diagram.

5.2.1. SIMULATION RESULTS

In this section, the simulation results with the bidirectional switch are discussed. The system parameters are given in Table 5.1

Table 5.1: System parameters.

Quantities		Parameters
ACMG	Total power rating of DGs	1 MW
	Frequency (f_r)	50 Hz
	Voltage L-L RMS	11 kV
	Maximum frequency Deviation (Δf)	0.5 Hz
DCMG	DG-1 rating	0.5 MW
	DG-2 rating	0.25 MW
	Voltage reference (V_{ref})	2.5 kV
	Maximum frequency Deviation (ΔV)	100 V
	Droop gain for DG-1 (d_1)	0.48 Ω
	Droop gain for DG-2 (d_2)	0.96 Ω
Interlinking converter	Transformer	11/1.72 kV
	DC capacitor (C_{dc})	5000 μF
	Filter capacitor (C_f)	50 μF
	Filter inductor (L_f)	33 mH
	Switching frequency	15 kHz

A. Mode-1: Nominal Operation

In this example, it has been assumed that the AC-MG is supplying 575 kW to its local load. This is shown in Fig. 5.4 (a), along with the MGAC generated power. The frequency is slightly below 50 Hz (49.92 Hz) since the DG is supplying just above its half rated power (shown in Fig. 5.4 b). The output of the angle controller is shown in Fig. 5.4 (c). This angle is negative to make the power flow from the DGs to the load.

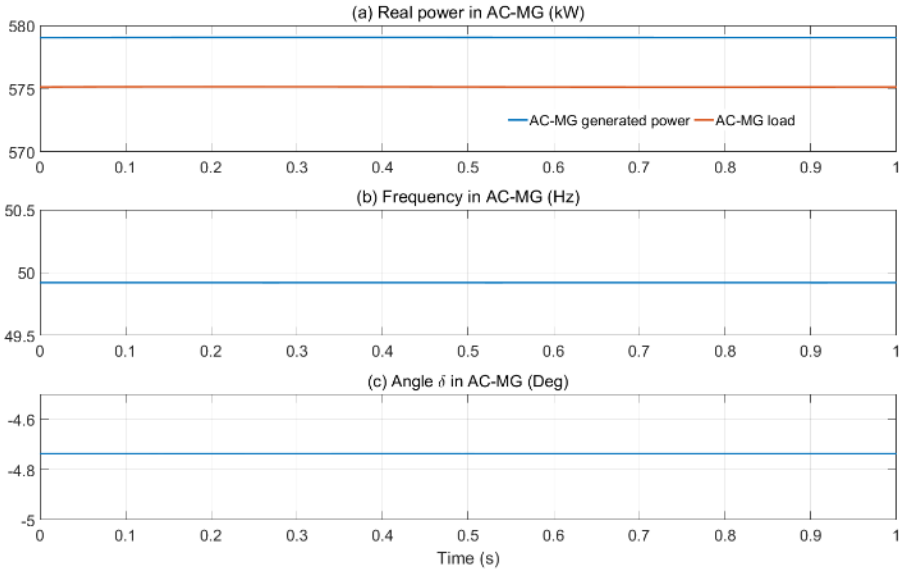

Fig. 5.4. System quantities in AC-MG for nominal operation.

The load in the DC side is 562 kW. This plus the losses in the DC lines are shared by the two DGs (almost) in a ratio of 2:1, as shown in Fig. 5.5 (a). The voltages of the DGs in the DC-MG are shown in Fig. 5.5 (b). It can be seen that both these voltages are above the lowest rated voltage of 2.4 kV. Also voltage V_1 is lower than V_2 since DG-1 is supplying more power than DG-2.

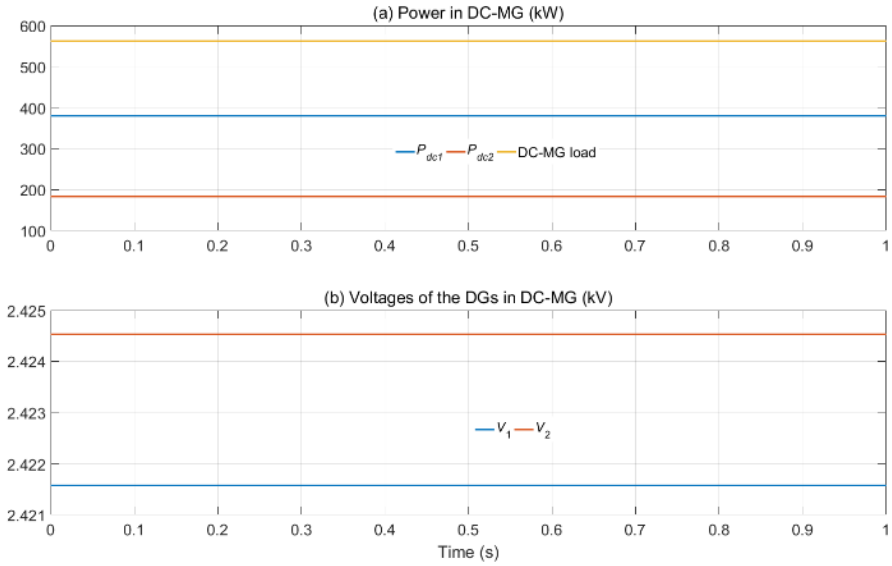

Fig. 5.5. System quantities in DC-MG for nominal operation.

B. Power Shortfall in the ACMG

In this example, it has been assumed that the DGs in the ACMG are supplying 833 kW to the load. At 1 s, the load demand in the ACMG increases to 1118 kW. Since this ACMG has a generation limit of 1 MW, this power has to flow from the DCMG.

Before 1 s, the local load in the DCMG is 300 kW, which is shared by the DGs in the specified ratio of 2:1. After 1 s, the load in the DCMG remains constant. However the generation by the two DGs increases to 288 kW and 140 kW to meet the shortfall in the ACMG. The generated and consumed power in the two sides of the hybrid MG are shown in Fig. 5.6.

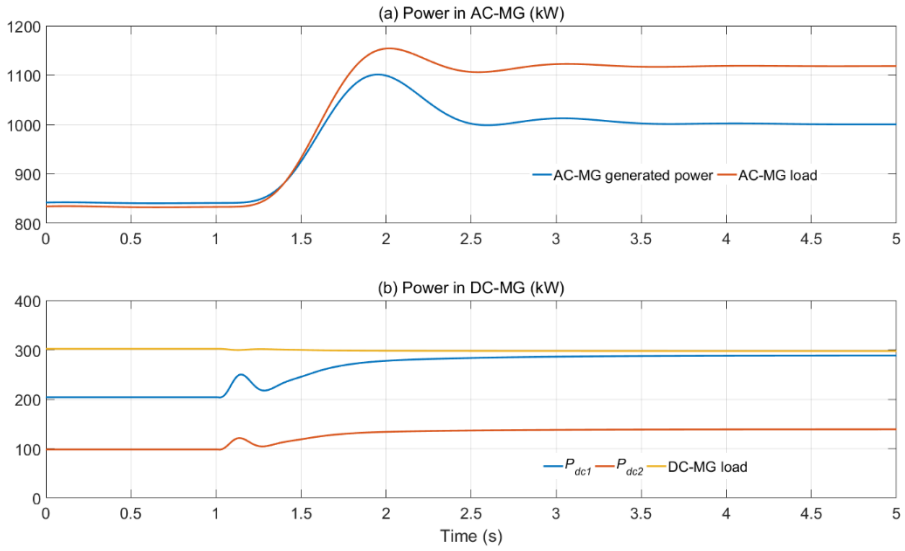

Fig. 5.6. Power flow in an interconnected AC/DC microgrid- (a) Power in ACMG and (b) Power in DCMG.

The voltages in the DC-MG are shown in Fig. 5.7 (a). They remain above the lower limit of 2.4 kV. The ACMG frequency is shown in Fig. 5.7 (b). It can be seen that it saturates at 49.5 Hz, as expected. The DC capacitor voltage reference is shown in Fig. 5.7 (c). It can be noted that it drops a bit from 2.5 kV to facilitate power transfer from DCMG.

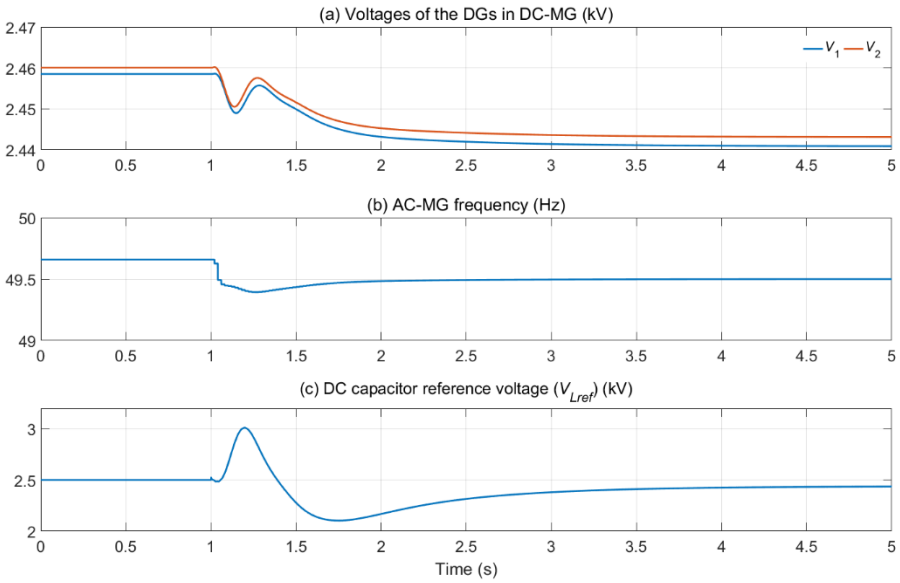

Fig. 5.7. (a) DCMG voltages, (b) ACMG frequency and (c) dc capacitor voltage reference

C. Mode-3: Power Shortfall in DCMG

In this example, it has been assumed that the ACMG is supplying 575 kW to the load such that its generation is 578.5 kW. The DCMG is supplying 586 kW power to the load, when at 1 s, its load demand increases to 821 kW. Since the total capacity of the DGs in the DCMG is 750 kW, the excess power has to be drawn from the ACMG. The power flow in the AC and DC sides is shown in Fig. 5.8 (a) and (b) respectively. It can be seen that the ACMG load power remains constant, while its generated power increases to 661 kW (Fig. 5.8 a). The DGs in the DCMG supplies their maximum rated power, as can be seen in Fig. 5.8 (b).

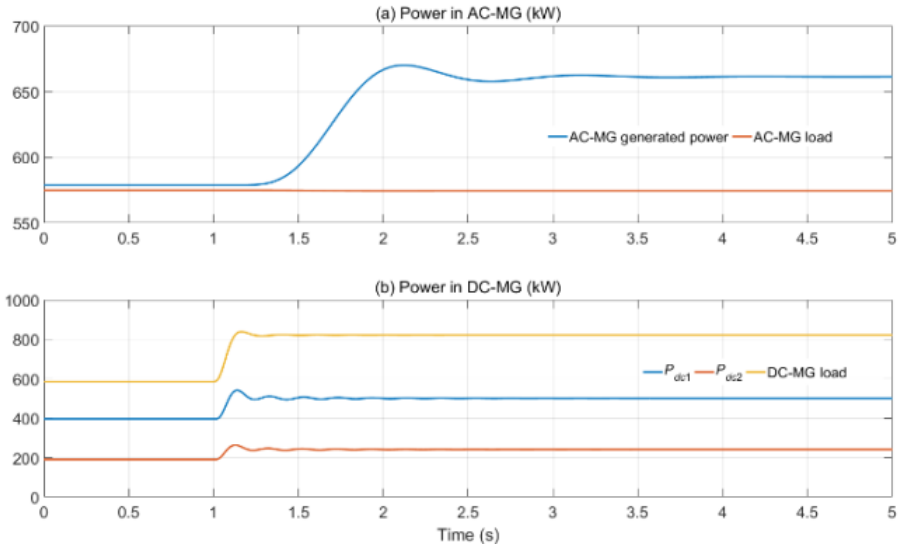

Fig. 5.8. Power flow through the hybrid for Mode-3.

The voltages in the DC-MG are shown in Fig. 5.9 (a). Since DG-1 is used for lower voltage regulation as per (4.6), its voltage is held constant at 2.4 kV. The DG-2 voltage is also very close to this value. The ACMG frequency is shown in Fig. 5.9 (b). It can be seen that it reduces from its nominal value to accommodate for increased power generation by the ACMG. The DC capacitor voltage reference is shown in Fig. 5.9 (c). The reference power that has to be drawn from the AC-MG to the DC-MG is shown in Fig. 5.10 (a), while the output of the angle controller is shown in Fig. 5.10 (b). It can be seen that the angle retards to extract more power from the AC-MG.

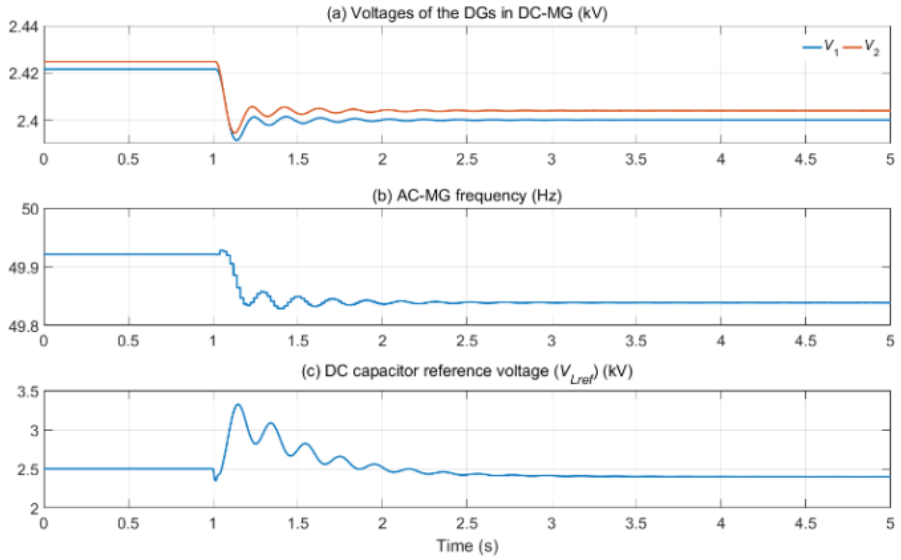

Fig. 5.9. DC-MG voltages, AC-MG frequency and DC capacitor voltage reference for Mode-3.

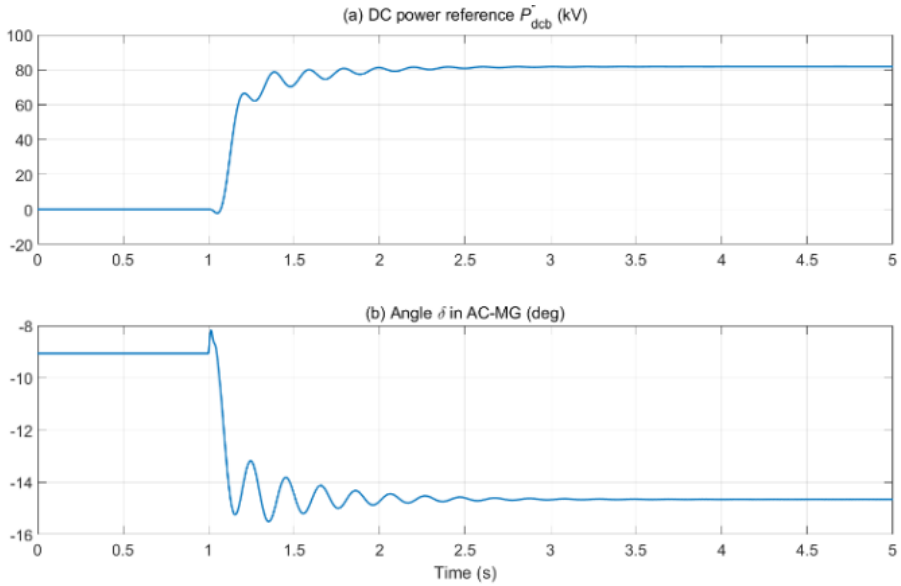

Fig. 5.10. DC power reference and angle controller output for Mode-3.

5.3 Power Management in a AC/DC Microgrid with DAB

The ACMG is connected to the DCMG through ac/dc conversion stages. Therefore the overall system structure is shown in Fig. 5.11. The DCMG is connected to the ACMG through an interlinking converter (IC) and a dual active bridge (DAB). The IC holds the dc voltage V_{dc1} across the capacitor C_{dc1} constant. The IC has an ac side LC filter (L_f and C_f). Given that V_{dc1} is held constant by the IC, the DAB modulates the voltage V_{dc2} across C_{dc2} to facilitate the bidirectional power flow.

In this case, the power shortfall in the ac side is defined by the frequency. The power reference for the DAB is then set as per (5.8). The DAB then facilitates the power transfer using (4.31). On the other hand, when a power shortfall occurs in the dc side, the exact amount of power that needs to be drawn is discussed in Sub-section 4.2.2. From (4.6), the power that needs to be drawn from the ACMG is determined.

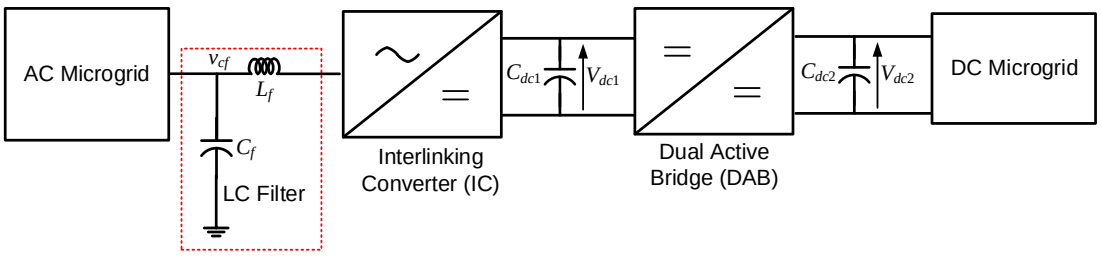

Fig. 5.11. Schematic diagram of an interconnected ac/dc system with DAB.

5.3.1. SIMULATION RESULTS

The dual active bridge bi-directional dc-dc converter contains two H-bridges that are connected together through a high frequency transformer. It is assumed that both the H-bridges are operated at 50% duty ratio. However their switching is shifted by an instant ϕ as shown in Fig. 4.18 (b). The phase shift ϕ is the control variable. A state feedback with integral control law is designed for the DAB. The gain matrices for the controller are chosen using discrete-time linear quadratic regulator, which will force the output error $e(k)$ to zero asymptotically.

The dc side voltage of the interlinking converter is controlled by the interlinking converter (Section 4.1). The reference for the DAB is determined by the desired link power transfer (P_{link}^{*}). The parameters chosen for the study are listed in Table 5.2.

A. Nominal operation

In this case, it is assumed that no power flows through the DAB and the ACMG and the DCMG operate in isolated fashion. The nominal phase shift in the DAB is calculated as per (4.29), for an input voltage of 15 kV and an output voltage of 400 V. The total load in the DCMG is 280 kW and the power generated by the two DGs are 185 kW and 95 kW. For this power level, the voltages V_1 and V_2 will be roughly around 320 V. Also the power supplied by the ACMG to supply its local loads and the converter losses is 565 kW.

Table 5.2: System parameters

Quantities	Values
ACMG	
AC sub-grid voltage	11 kV (L-L)
System frequency	50 Hz
AC feeder impedance	Inductance: 38.6 mH and resistance: 1.21 Ω
Filter parameters	L_f = 33 mH, C_f = 50 μF
Interlinking Converter	
dc Capacitor (C_{dc1})	5000 μF
Voltage Magnitude (V_m)	9 kV (peak)
Carrier waveform	15 kHz
Sampling frequency	30 kHz
DC voltage reference (V_{dc}^*)	15 kV
PI controller	$K_{P\delta}$ = – 0.1, $K_{I\delta}$ = – 0.5
DAB	
Transformer	2.5 kV/2.5 kV
Inductance	L = 0.4 mH
Switching frequency	10 kHz
PI controller	K_{Pl} = 2, K_{Il} = 100
DC Capacitor (C_{dc2})	5000 μF
DCMG	
Voltage reference (V_{ref})	400 V
Maximum voltage drop (ΔV)	100 V
DG rating	DG-1: 240 kW, DG-2: 120 kW
Droop gains	n_1 = 0.5, n_2 = 1.0
Line resistances	R_1 = 0.01 Ω, R_2 = 0.06 Ω, R_3 = 0.001 Ω

The results are shown in Figs. 5.12 and 5.13. Fig. 5.12 shows the performance of the ACMG operating in *P-f* droop. It can be seen that, barring a transient during the start, the ACMG power, ACMG frequency and voltage angle δ are constant. The performance of the DCMG is depicted in Fig. 5.13. It can be seen that the power sharing is accurate according to the defined droop gains. The voltages V_1 and V_2 drop to around 320 V in sympathy with the load connected to the DCMG.

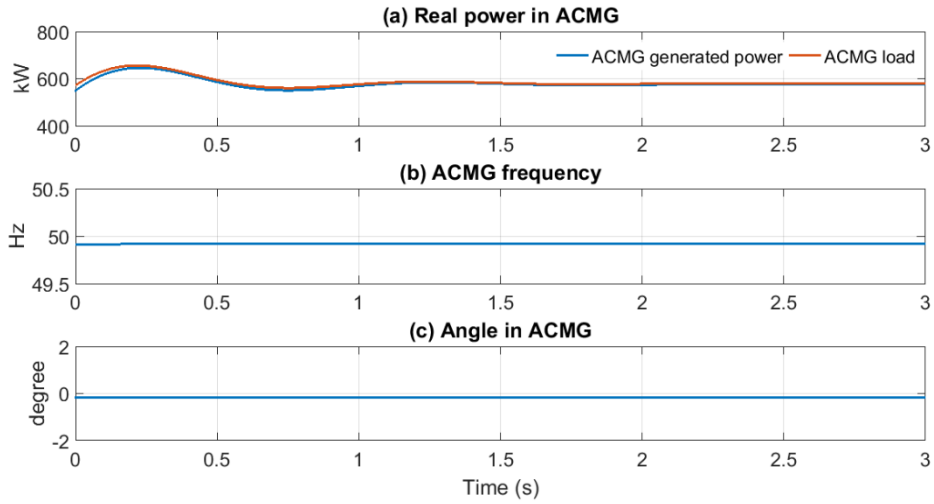

Fig. 5.12. Performance of ACMG for nominal operation: (a) source power, (b) ACMG frequency and (c) voltage angle.

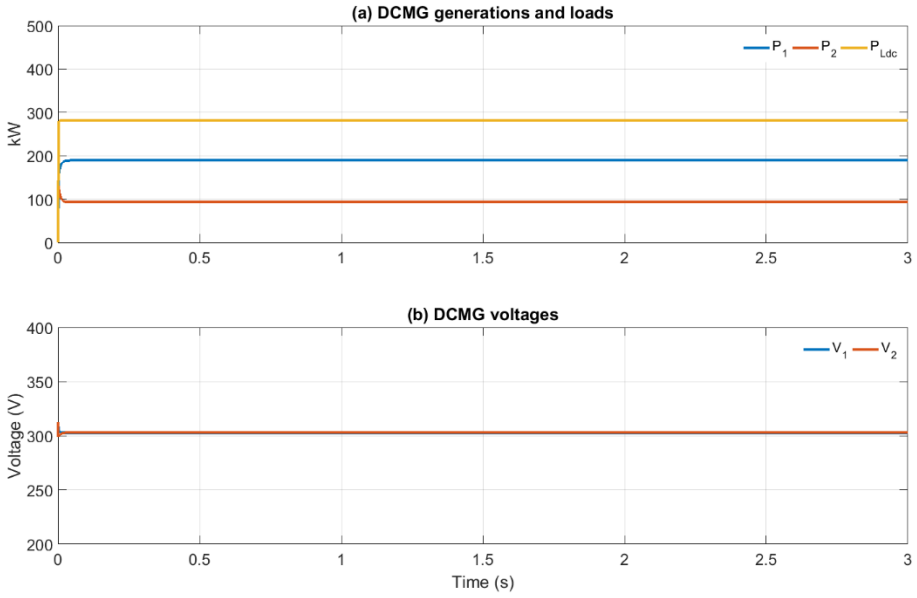

Fig. 5.13. Performance of DCMG for nominal operation: (a) power flow and (b) voltages.

B. Power shortfall in ACMG

At the beginning of this case, it is assumed that no power flows through the DAB. The total load in the DCMG is 210 kW and the power generated by the two DGs are 140 kW and 70 kW. The voltages V_1 and V_2 are roughly around 340 V. The power supplied by the ACMG s is 565 kW. With the system operating in the steady state, the ACMG load is changed to 1090 kW at 1 second. The results are shown in Figs. 5.14 and 5.15.

Fig. 5.15 (a) shows that the ACMG is supplying around 1000 kW power as expected. The ACMG frequency drops to 49.5 as shown in Fig. 5.14 (b). The voltage angle (δ) is shown in Fig. 5.14 (c). From Fig. 5.15 (a), it can be seen that the power consumed by the dc load remains constant at 210 kW. However due to the extra amount of power supplied to the ac side, the DGs now supply 200 kW and 100 kW. The link power settles to 90 kW. Due to the increase in the power supply by the DCMG, the voltages drop to 315 V.

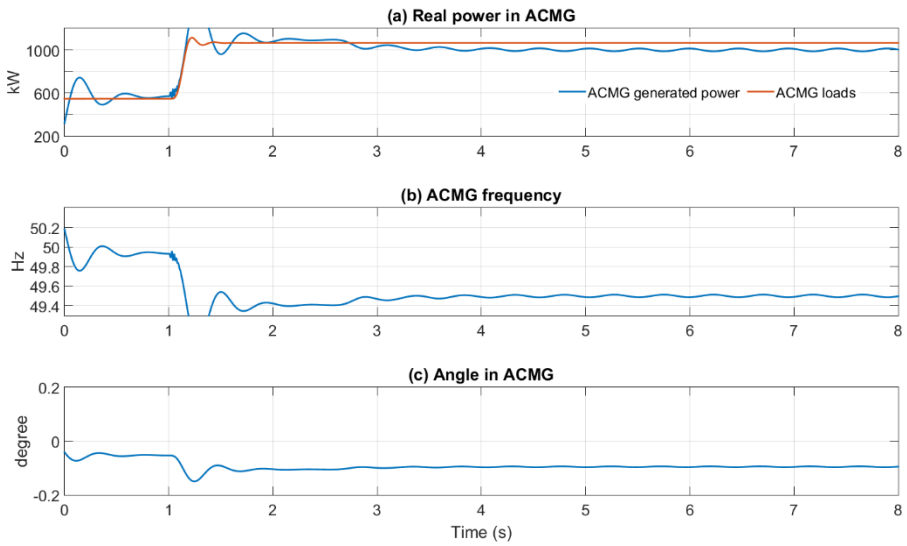

Fig. 5.14 Performance of ACMG during power shortfall in ACMG (a) source power, (b) dc link voltage and (c) voltage angle.

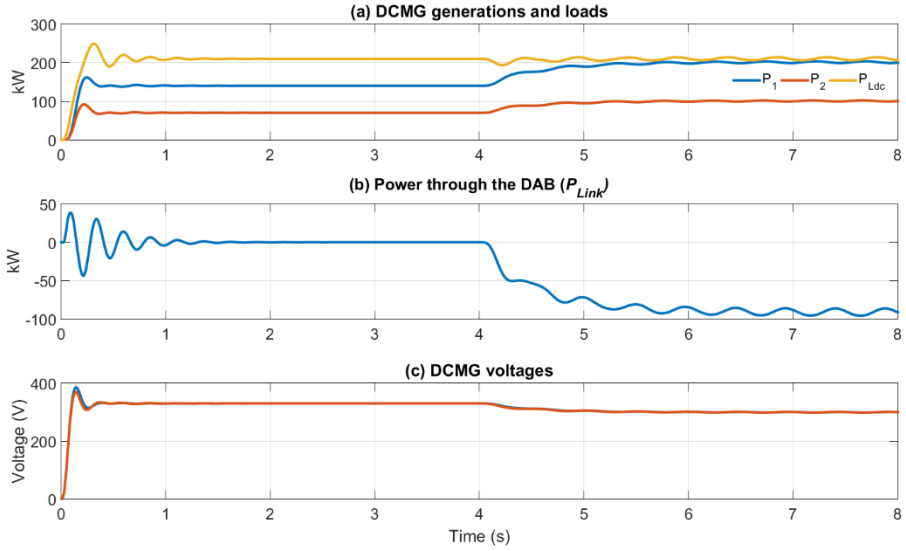

Fig. 5.15. Performance of DCMG during power shortfall in ACMG: (a) power flow, (b) link power and (c) voltages.

C. Power shortfall in DCMG

In this case, it is assumed that the ACMG supplies the power deficit in DCMG when the loads in the DCMG is increased. Till 4 seconds, the microgrids operate in isolated fashion. The total load in the DCMG is 280 kW and the power generated by the two DGs are 185 kW and 95 kW. The voltages V_1 and V_2 are roughly around 320 V. The power supplied by the ACMG s is 565 kW. At 4 s, the DCMG load increases by 100 kW. The results are shown in Figs. 5.17 and 5.18.

Fig. 5.16 shows that the power supplied by the ACMG increases to 665 kW to cater extra 100 kW load in DCMG. The capacitor voltage V_{dc1} is maintained at 15 kV and the voltage angle decreases to accommodate increased power flow from the ACMG. The results for the DCMG side are shown in Fig. 5.17. As evident from this figure, the power consumed by the dc load remains constant, however the DGs now supply their maximum rated power 240 kW and 120 kW respectively. The link power settles is – 100 kW. Due to maximum amount of power supply by the DGs to the local loads, the voltages reach to 300 V.

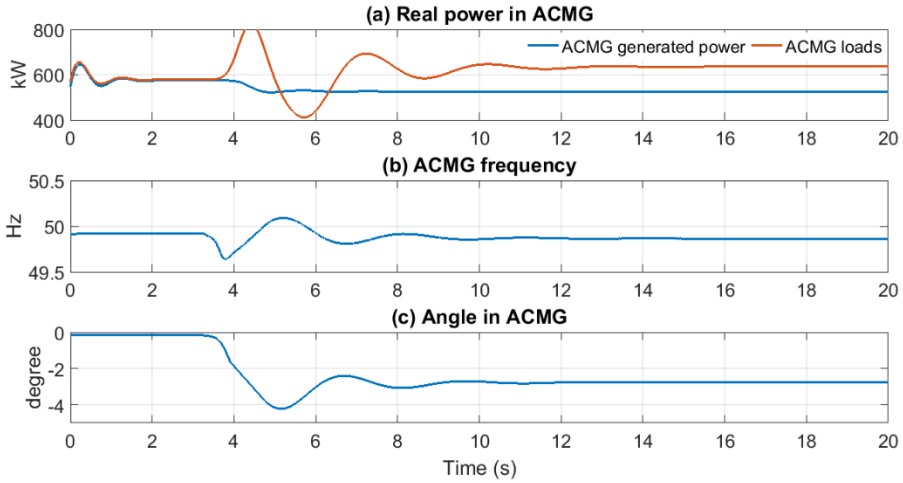

Fig. 5.16. Performance of ACMG during power shortfall in DCMG: (a) source power, (b) ACMG frequency and (c) voltage angle.

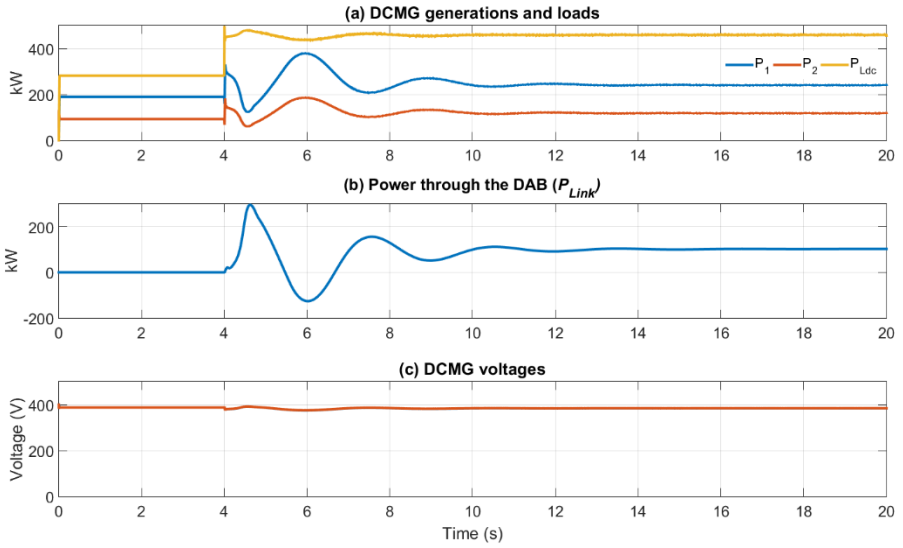

Fig. 5.17. Performance of DCMG during power shortfall in DCMG: (a) power flow, (b) Power through the DAB and (c) voltages.

5.4. CONCLUSIONS

In this chapter, the operation and control of an ac/dc interconnected microgrid are discussed. The ac microgrid is connected to the dc microgrid through an interlinking converter. On the dc side of the interlinking converter a bidirectional switch or a DAB are used to control the power flow in between the microgrids. In the

proposed system operation, either of the microgrids draws the exact amount of power that is required for preventing a system collapse. However due to the presence of the bi-directional switch or the DAB, these two sides operate autonomously.

It is to be note here that it has been assumed that the ACMG is able to supply power to the DCMG during its power shortfall and vice versa. However it might so happen that they may not have sufficient power surplus when to support the other during its contingency. In this event, load shedding has to be implemented in the microgrid having a shortfall. A load shedding scheme has not been considered in this thesis.

CHAPTER 6

POWER SHARING IN A AC/DC MICROGRID WITH MULTIPLE DC SUB-GRIDS

One of the major challenges of connecting multiple dc sub-grids tied up to the ACMG/utility grid is the circulating current. The existing topologies are designed to reduce this circulating current to a minimum value. Multiple rectifiers or multiple interlinking converters are usually connected to the ACMG/utility grid to connect multiple dc-sub-grids. However, these topologies require a passive filter connected to any side of the IC to reduce line current harmonics [13]. Researchers have attempted to use rectifiers/IC of different ratings and different dc link filter configuration to mitigate these issues. But these methods are susceptible to any network disturbances. In the case of the diode rectifiers turned on and off at different time can generate circulating current. Even connecting multiple ICs to integrate the dc sub-grids to the ac utility results in a circulating current. It can be reduced to some extent by controlling the PWM patterns [159] and changing the switching frequency [160]. In this chapter, a system configuration is chosen in which an ACMG is connected to two DCMGs through an IC and two DABs.

The proposed system architecture does not require droop gain selection for the interlinking converter to share power to any DGs of the network irrespective of its location. The DCMGs are connected to the dc side of the interlinking converter through DABs that can operate at different dc voltage levels. All possible cases are discussed to assess the system performance for these cases. Dual active bridge converters are designed according to the control approach described in Chapter 4. The DABs are tuned to enable power supply at the designed dc voltage levels of each DCMG. Detailed PSCAD simulations are presented to show the system operation.

At the beginning of this chapter, the electrical system simulation studies are presented to show how a coupled system containing more than one microgrids are connected. It has been shown how bidirectional power transfer can take place between an ac and two dc microgrids. However, even though the electrical quantities can be controlled in a desired manner, the power transfer relations must be set up as a pre-

condition. Note that the ACMG and DCMGs do not share power according to a unified droop equation as has been discussed in [10] since these microgrids can have different ratings and cost of generations. Therefore there is a need to develop energy trading policies between them considering their utility functions. These can be a fair allocation, a monopoly policy or a duopoly policy.

Therefore game theoretic approaches are applied for power sharing amongst the microgrids. Two different cases are considered. These are:

1. The first approach considers that the ACMG, which has a lower generation cost, supplies power to the DCMGs, which have higher generation costs. Instead of a competition, the DCMGs form a coalition. To ensure fairness of power distribution to the coalition, Shapely Value has been used [161]. The power transfer here is not on the basis of cost. However the overall cost of the MGs is highlighted.
2. In the second approach, it has been assumed that the DCMGs have excess available power, especially during the day time on weekdays when the sun shines. Therefore they can supply power at lower cost to the ACMG. This case introduces a competition in the market when both the DCMGs will try to maximize their profit by selling their reserve power to the ACMG. The "price leadership model" and the "Stackleberg Duopoly model" are used to determine a fair electric power supply to the ACMG [162, 163]. In an unfair market condition, the least expensive power producer captures the market and the other cannot sell anything. Using the Stackleberg duopoly model DCMGs can simultaneously decide how much electricity to generate and the price at which the electric power is sold is determined by the total amount generated [162].

6.1. SYSTEM STRUCTURE

The system structure is presented in Fig. 6.1. An ACMG and two DCMGs are connected through an interlinking converter. The DCMGs are connected to the dc side of the IC through a DAB. From the figure 6.1 it can be seen that the IC holds the dc voltage V_{dc1} across the capacitor C_{dc1} constant. The IC has an ac side LC filter (L_f and C_f). Given that V_{dc1} is held constant by the IC, the DAB modulates the voltage V_{dc21} and V_{dc22} across C_{dc21} and C_{dc21} respectively to facilitate the bidirectional power flow.

When a DCMG is connected to an ac system, it is expected that the ac voltage will be high. The voltage can be brought to the level of DCMG by a transformer at the input of the IC. However, for medium voltage systems, only a VSC is sufficient. In this case the DAB transformer can provide the required isolation. In Fig. 6.2 (a), the IC holds the dc voltage (V_{dc1}). Therefore it cannot enable power flow control since it might adversely affect the power control in the DCMG. With the inclusion of the DAB, the voltage V_{dc1} is separated from V_{dc21} and V_{dc22}. Now V_{dc21} and V_{dc22} are controlled for power flow. Furthermore, the control of DAB is so robust that the power supply does not vary with the input voltage fluctuation.

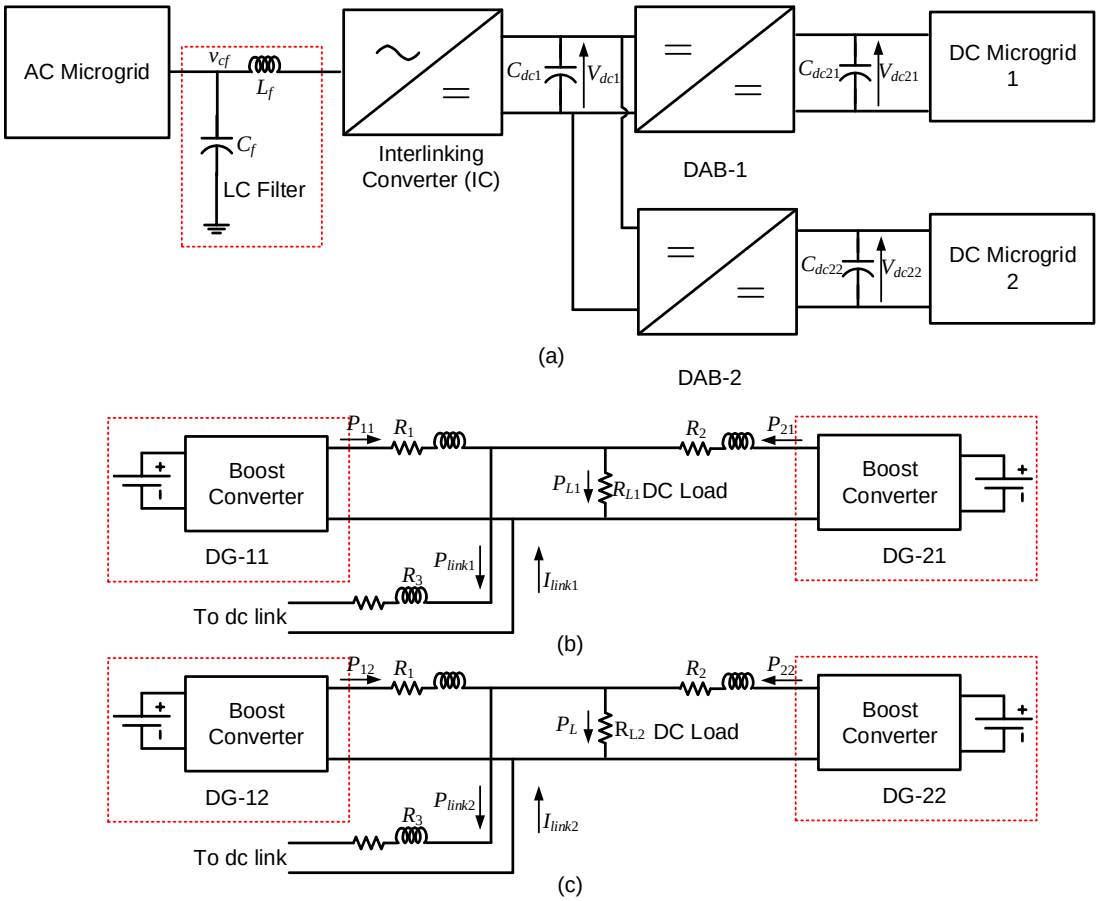

Fig. 6.1. (a) System structure of an AC/DC microgrid with multiple dc sub-grids, (b) DCMG-1 and (c) DCMG-2.

A simple DCMG structure is considered as shown in Fig. 6.2 (b) and (c). It contains two boost converters and a buck converter. The boost converters step up the voltage generated by the DGs to a dc distribution level. All these converters are controlled through their duty ratio to track the desired output voltage. The resistances R_1 and R_2 are the line resistances, while the inductors are damping inductors. The DAB

is connected to the dc distribution line through a resistor R_3. The power flow DAB-1 and DAB-2 are denoted by P_{link1} and P_{link2} with the positive direction indicated in the figure. The direction of power flow from DGs is also indicated in the figure.

An equivalent circuit diagram of the system of Fig. 6.1 is presented in Fig. 6.2. From the circuit analysis, it can be seen that V_1 and V_2 can vary depending on line resistances R_1 and R_2 and the current flowing in/out through the DABs I_1 and I_2. Overall, the IC holds V_{dc1} and the DABs are modulated with a robust control to facilitate desired amount of power flow at any direction.

In Fig. 6.2, for simplicity of analysis, it has been assumed that the DAB voltage transformation ration is 1:1. The input voltage of DAB-1 and DAB-2 is V_1 and V_2 respectively. Assuming the DABs to be lossless, the following equations can be written from Fig. 6.2

$$\begin{aligned} I_1V_1 &= I_{L1}V_{L1} \\ I_2V_2 &= I_{L2}V_{L2} \end{aligned} \tag{6.1}$$

Now I_1 and I_2 can be written to include V_{dc1} as

$$\begin{aligned} I_1 &= \frac{V_{dc1} - V_1}{R_1} \\ I_2 &= \frac{V_{dc1} - V_2}{R_2} \end{aligned} \tag{6.2}$$

Let us consider, V_{dc}= 550 V, R_1 and R_2 is equal to 0.1 and 0.2 respectively, and DAB-1 and DAB-2 have a load of 25 kW and 8 kW respectively. From (6.1) and (6.2) following equations are obtained.

$$\begin{aligned} I_1V_1 &= 25000 \\ I_1 &= \frac{550 - V_1}{0.1} \\ I_2V_2 &= 8000 \\ I_2 &= \frac{550 - V_2}{0.2} \end{aligned} \tag{6.3}$$

Solving (6.3) we get,

$$
\begin{aligned}
V_1 &= 545.41V \\
I_1 &= 45.83\,A \\
V_2 &= 547.08V \\
I_2 &= 14.62\,A
\end{aligned}
\tag{6.4}
$$

From this circuit analysis it can be seen that the current I_1 and I_2 are positive though the line resistances are not equal. I_{L1} is dependent on I_1 and I_{L2} is dependent on I_2. Since V_{L1} and V_{L2} is held constant by the DAB controller and V_{dc1} is also held constant by the IC, based on R_{L1} and R_{L2} the load current of the DAB will change. As a consequence, V_1 and V_2 will also change to facilitate the desired amount of power flow. As can be seen from (6.4) that there is a unique equilibrium point for the load considered. Since the DAB feedback controller regulates the power flow, there will not be any circulating current when this equilibrium point is reached. The case studies in this chapter validates this proposition.

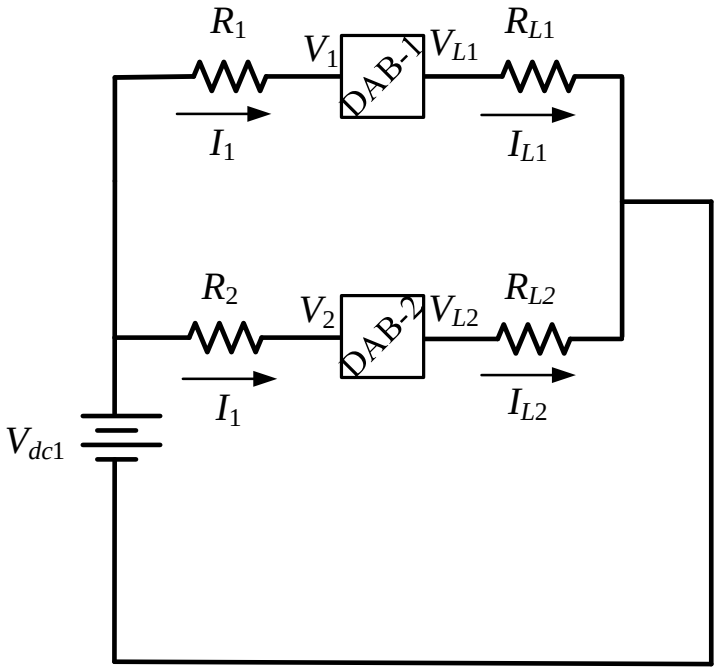

Fig. 6.2. Schematic diagram of the DAB connection to the dc capacitor.

6.2 SYSTEM PARAMETERS

The system parameters used in the study are listed in Table 6.1. It can be seen that DCMG-1 operates at a voltage level of 400 V and DCMG-2 operates at a voltage

level of 500 V. To design controllers for these DABs, the method outlined in Chapter 4, Subsection 4.3.2 has been used.

From Table 6.1, it can be seen that the DCMGs have power ratings of 300 kW and 500 kW. The DABs are designed for full rated power. Therefore the load resistance as per (4.29) for the two DABs are calculated as

$$\text{DCMG-1: } R_{L1} = \frac{V_{10}^2}{P_{10}} = \frac{400^2}{300 \times 10^3} = 0.53\,\Omega$$

$$\text{DCMG-1: } R_{L2} = \frac{V_{20}^2}{P_{20}} = \frac{500^2}{500 \times 10^3} = 0.5\,\Omega$$

In the proposed system architecture, the dual active bridge converters' duty is kept to a constant value at 0.5 and the phase is varied. The power transfer through DAB is dominated by its phase in between the triggering signal of the switch. For a given output voltage $\phi_{initial}$ is calculated. Since the power flow in a dual active bridge is controlled by varying the phase of the switching pulses, the duty ratio is translated in terms of phase. This is achieved by a simple calculation. For the controller duty to phase conversion calculation $\phi_{initial}$ is divided by 180. As the duty is 0.5, subsequently the output stays on for half the time of a switching cycle which means 180 degree so the angle is divided by 180. However, the steady state value, $\phi_{initial}$ for DAB-1 and DAB-2 are found 28.51 and 21.8531 respectively. Rest of the system is designed as described in the previous chapters. The system parameters are presented in table 6.1.

Table 6.1: System parameters

Quantities	**Values**
AC Side	
AC source voltage	11 kV (L-L)
System frequency	50 Hz
AC feeder impedance	Inductance: 38.6 mH and resistance: 1.21 Ω
Filter parameters	L_f = 33 mH, C_f = 50 μF
Interlinking Converter	

DC Capacitor (C_{dc1})	5000 μF
Voltage Magnitude (V_m)	9 kV (peak)
Carrier waveform	15 kHz
Sampling frequency	30 kHz
DC voltage reference (V_{dc}^*)	15 kV
PI controller	$K_{P\delta} = -0.1$, $K_{I\delta} = -0.5$
DAB 1 and 2	
Transformer	2.5 kV/2.5 kV
Inductance	L = 0.4 mH
Switching frequency	10 kHz
PI controller	K_{Pl} = 2, K_{Il} = 100
DC Capacitor (C_{dc2})	5000 μF
DCMG 1	
Voltage reference (V_{ref})	400 V
Maximum voltage drop (ΔV)	100 V
DG rating	DG-1: 200 kW, DG-2: 100 kW
Droop gains	n_1 = 0.5, n_2 = 1.0
Line resistances	R_1 = 0.01 Ω, R_2 = 0.06 Ω, R_3 = 0.001 Ω
DCMG 2	
Voltage reference (V_{ref})	500 V
Maximum voltage drop (ΔV)	100 V
DG rating	DG-1: 300 kW, DG-2: 200 kW
Droop gains	n_1 = 0.33, n_2 = 0.5
Line resistances	R_1 = 0.01 Ω, R_2 = 0.06 Ω, R_3 = 0.001 Ω

6.3 CASE STUDIES

Four case studies are presented in this chapter. In the case studies, power flowing from ACMG to the DCMGs is defined with a negative power reference. The cases can be outlined as follows:

Case A: ACMG supplies power to both the DCMGs.

Case B: Both DCMGs supply power to the ACMG.

Case C: One of the DCMGs receives power from the ACMG and the other DCMG.

Case D: One of the DCMGs supplies power to the ACMG and the other DCMG.

All the cases are started from cold, i.e., the initial transients are also shown.

6.4 CASE A: AC TO DC POWER SUPPLY

In this case the microgrids in the system are operated in islanded mode till 3.5 s. After 3.5 s, the power reference of the both the DABs – 100 kW (i.e., $P_{refdc1} = P_{refdc2} = -100$ kW) so that both the DCMGs receive power from the ACMG. The dc capacitor voltage of the IC is shown in Fig. 6.3 (a). From Fig. 6.3 (b), it can be seen that the ACMG power generation increased by 200 kW to supply power to the DCMGs. From Fig. 6.3 (c), the drop in the frequency to cater the extra power supply is visible. The local load of the ACMG is increased at 6 s. From Figs. 6.3 (b) and (c), it can be seen that that the generated power in the ACMG increases causing a further drop in the frequency.

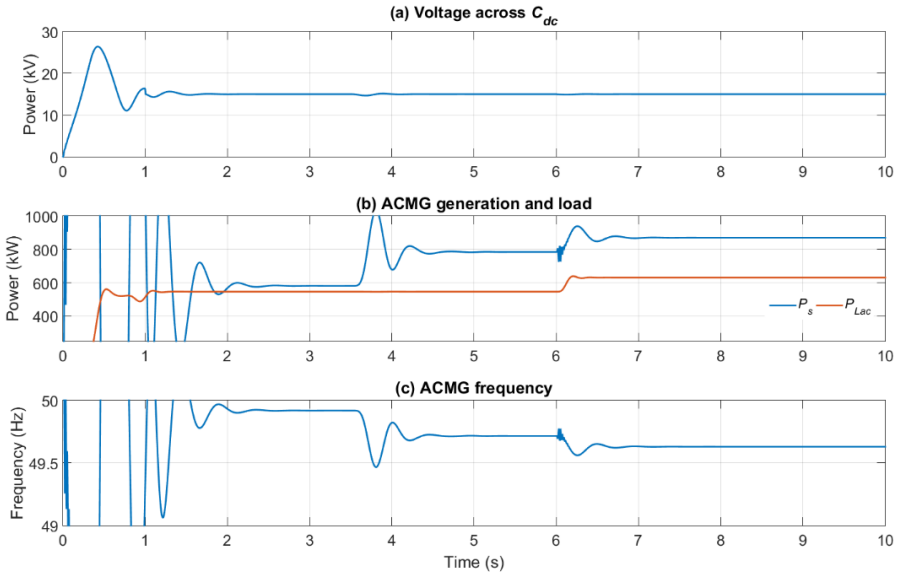

Fig. 6.3. (a) Voltage across dc capacitor, (b) ACMG generation and load and (c) ACMG frequency.

The results of this test for DCMG-1 are shown in Figs. 6.4 and 6.5. At 3.5 s when P_{refdc1} = – 100 kW is set, the output voltage of the DAB-1 V_{dc21} is changed to allow the power flow from the ACMG. V_{dc21} is the sub-grid voltage of DCMG-1. Since DCMG-1 will receive power, the reference voltage and output voltage has increased to reduce the DCMG-1 generation.

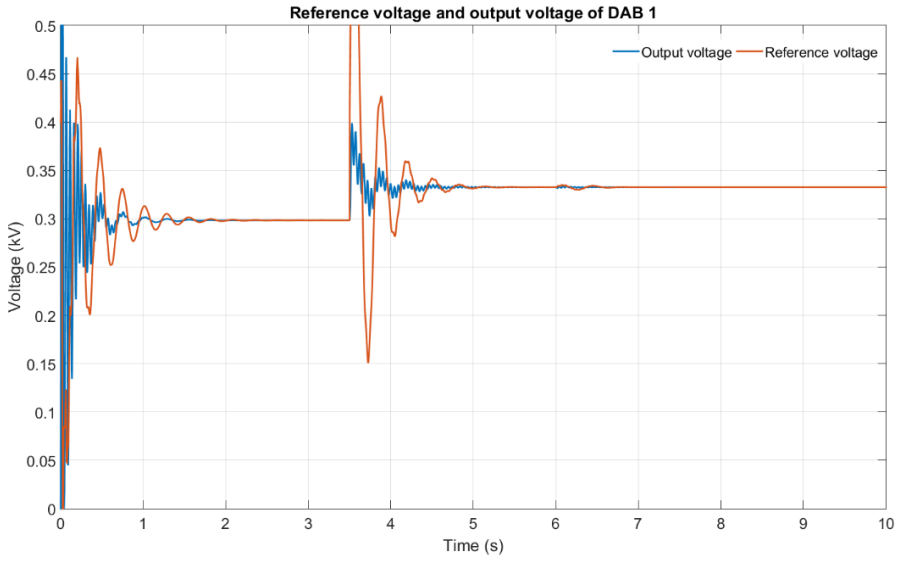

Fig. 6.4. Reference voltage and output voltage of DAB-1.

DCMG-1 voltages and powers are shown in Fig 6.5. From Fig. 6.5 (a) it can be seen that the voltage of the DG-1 and DG-2 has increased after 3.5 s according to the droop characteristics due to decreased generation. From Fig. 6.5 (b) it can be seen that the DCMG-1 has a load of 300 kW. According to the defined droop gains, DG-1 and DG-2 are sharing power in 2:1 ratio. After 3.5 s, when DCMG-1 starts to receive 100 kW power from ACMG, DG-1 and DG-2 power generation reduces to 133 kW and 67 kW respectively. The DCMG load however remains constant. Power through the DAB 1 is shown in Fig. 6.5 (c). It is to be noted that the increase in the ACMG local load at 6 s has no impact on the dc side.

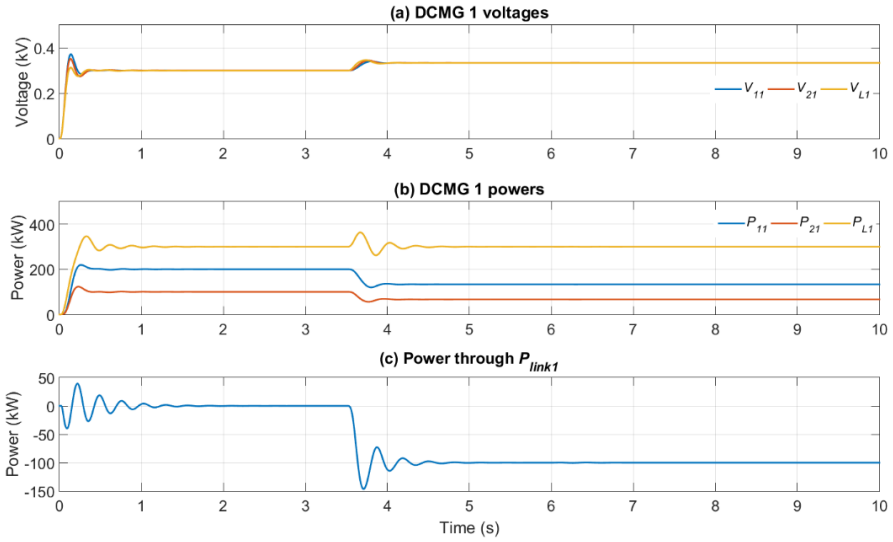

Fig. 6.5. (a) DCMG 1 voltages, (b) DCMG 1 powers and (c) power through P_{link1}.

The results of this test for DCMG-2 are shown in Figs. 6.6 and 6.7. It can be seen that all the quantities behave in the similar fashion as those of DCMG-1. It is to be noted that the power sharing between the two DGs of the DCMG is in the ratio 3:2 and this is maintained all throughout.

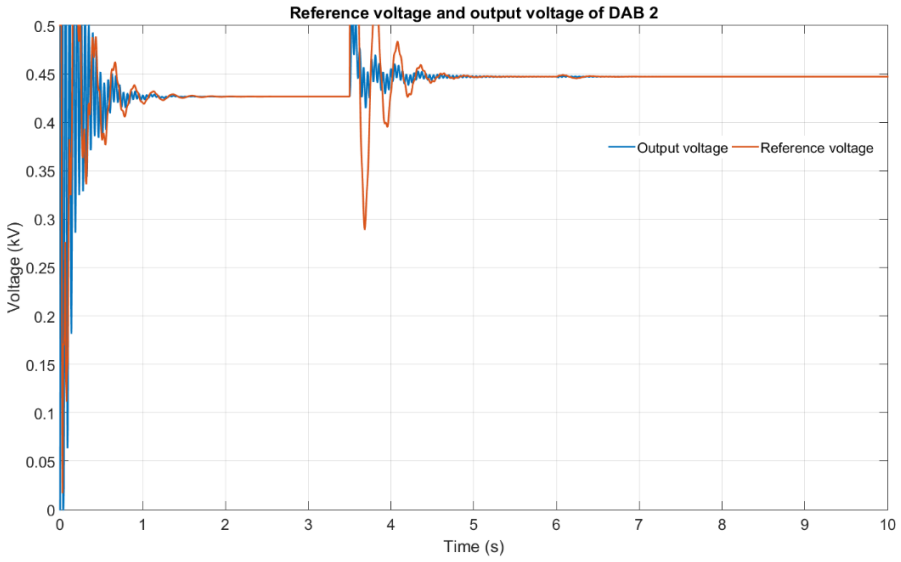

Fig. 6.6. Reference voltage and output voltage of DAB-2.

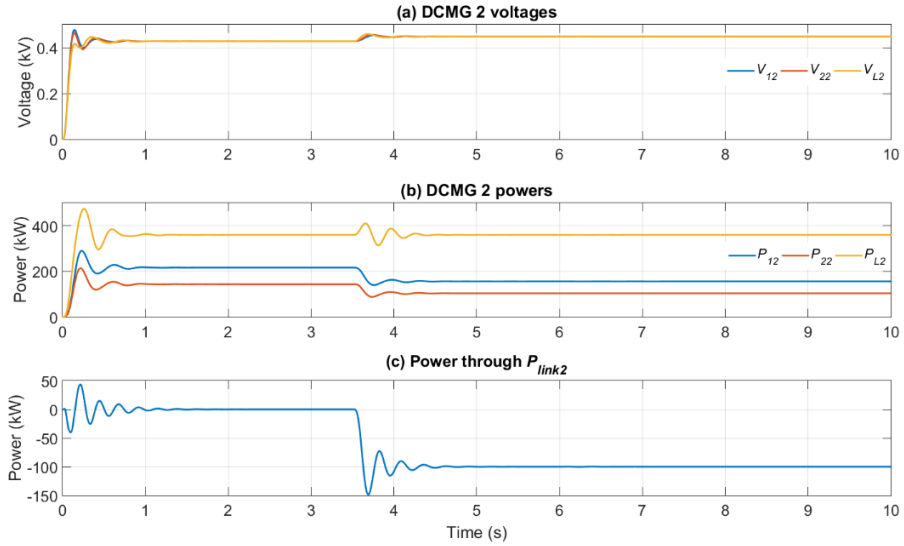

Fig. 6.7. (a) DCMG 2 voltages, (b) DCMG 2 powers and (c) power through P_{link2}.

6.5 CASE B: DC TO AC POWER SUPPLY

In this case the microgrids in the system are operated in islanded mode till 3.5 s. At this instant, the power reference of the two DABs set as P_{refdc1} = 50 kW and P_{refdc2} = 100 kW. The dc capacitor voltage of the IC is shown in Fig. 6.8 (a). From Fig. 6.8 (b), it can be seen that the ACMG power generation decreased by 150 kW. The ACMG frequency increases as the load supply reduces, as can be seen from Fig. 6.8 (c). At 6

s, the ACMG load increases, while it keeps on receiving 150 kW from the DCMGs. It can be seen that both load power and frequency behave as expected, i.e., load power increases and the frequency drops.

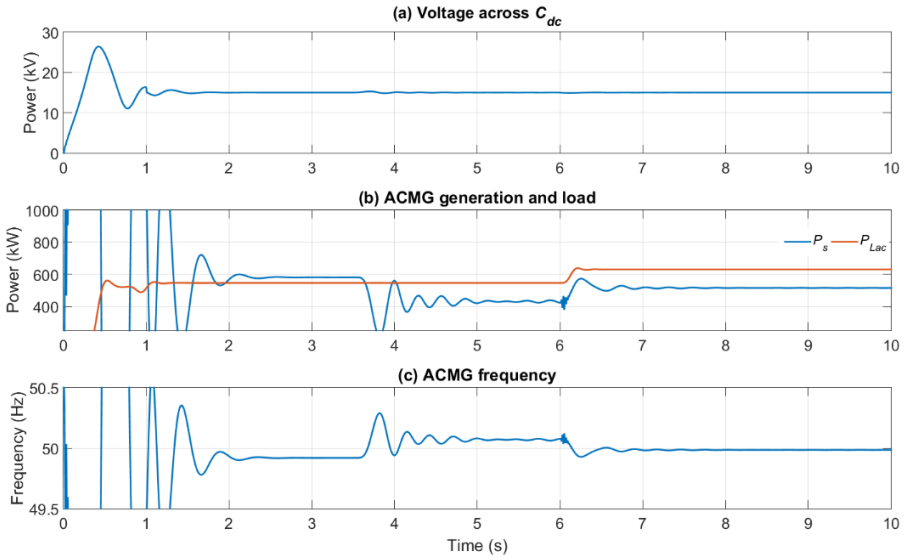

Fig. 6.8. (a) Voltage across dc capacitor, (b) ACMG generation and load and (c) ACMG frequency.

The behaviour of DGMG-1 is shown in Figs. 6.9 and 6.10. From Fig. 6.9, it can be seen that at 3.5 s, the output voltage of the DAB-1 V_{dc21} decreases to facilitate 50 kW power to be supply to the ACMG. DCMG-1 voltages and powers are shown in Fig 6.10. From Fig. 6.10 (a), it can be seen that the voltages of the DG-1 and DG-2 have decreased after 3.5 s according to the droop characteristics to supply 50 kW power towards the ACMG. From Fig. 6.10 (b), the power generation by the two DGs has increased at 3.5 s to supply the extra demand from the ACMG. The DCMG load however remains constant. The power sharing ratio between the DGs is maintained 2:1 all throughout. Fig. 6.10 (c) shows that 50 kW power flows through DAB after 3.5 s. The local load change in the ACMG has no impact on the operation of this DCMG.

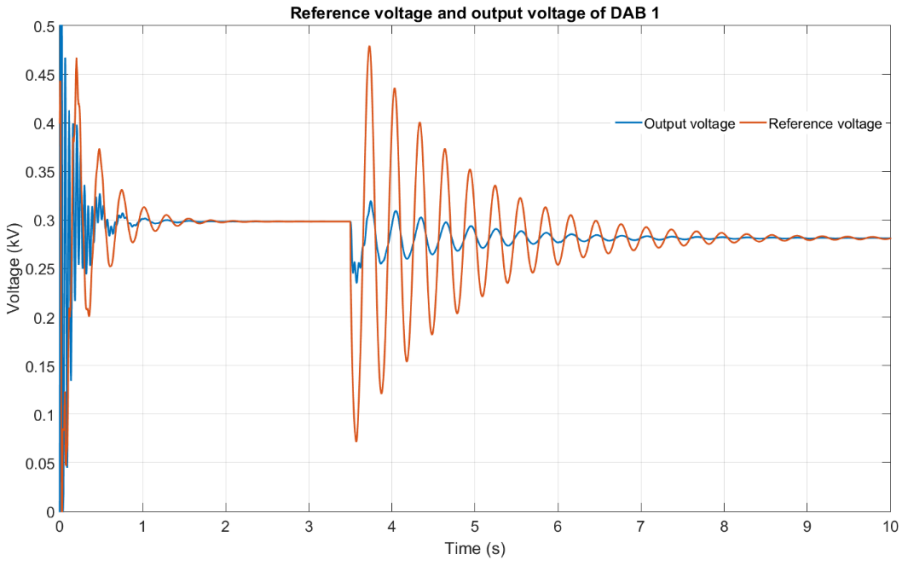

Fig. 6.9. Reference voltage and output voltage of DAB-1.

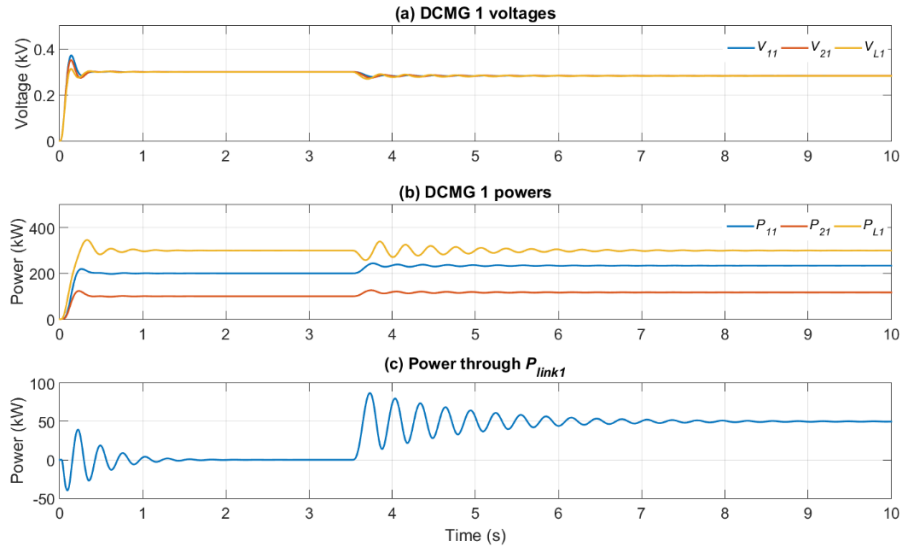

Fig. 6.10. (a) DCMG 1 voltages, (b) DCMG 1 powers and (c) power through P_{link1}.

The operation of DCMG-2 for this case is shown in Figs. 6.11 and 6.12. It can be seen that this behaves in the similar fashion as ACMG-1, albeit the power sharing ratio of 3:2.

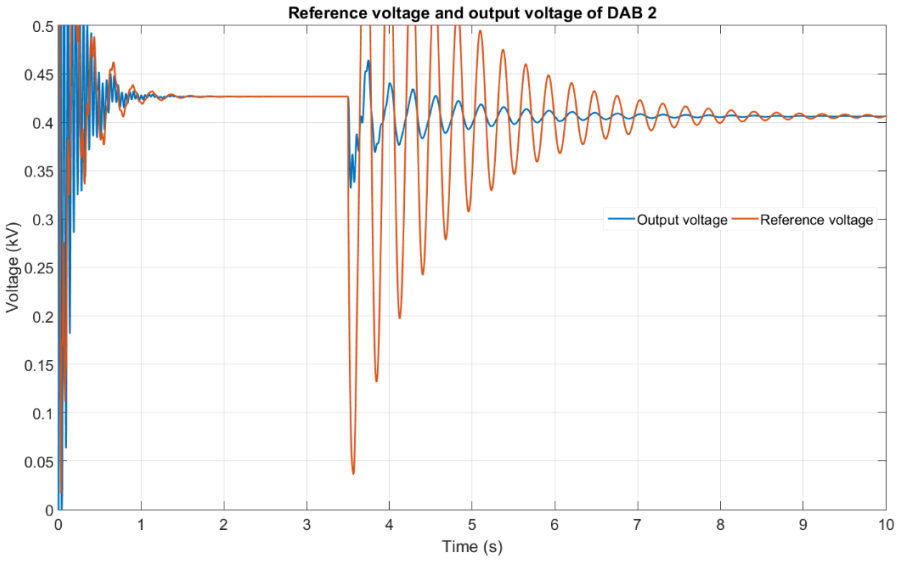

Fig. 6.11. Reference voltage and output voltage of DAB-1.

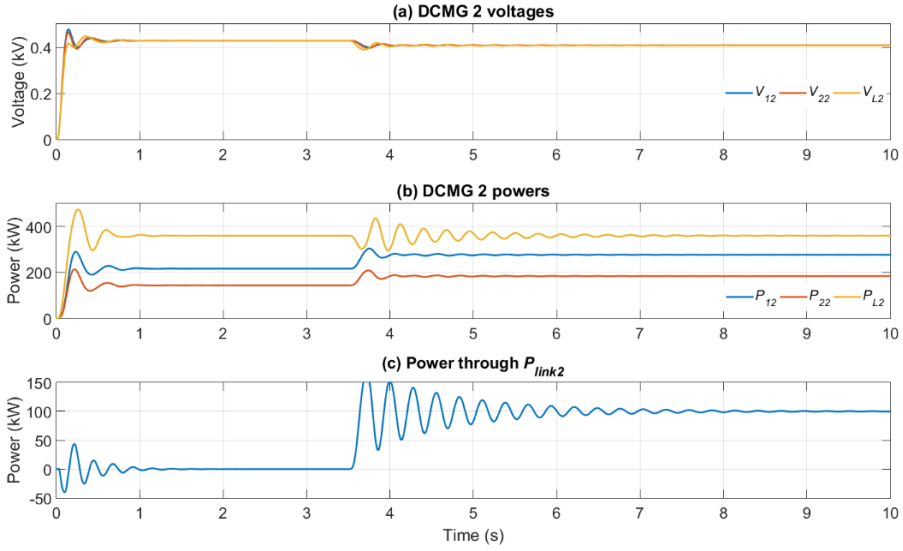

Fig. 6.12. (a) DCMG 2 voltages, (b) DCMG 2 powers and (c) power through P_{link2}.

6.6 Case C: Power Supply to a DCMG from the ACMG and the Other DCMG

In this case, it is considered that DCMG-2 requires 100 kW of power at 6 s, which will be shared equally by DCMG-1 and the ACMG. In Fig. 6.13 (a) the dc capacitor voltage of the IC is plotted. In Fig. 6.13 (b) ACMG generation and ACMG load are shown. At 3.5 s, when 50 kW power is required in DCMG-2, the ACMG

generates this 50 kW of excess power and, as a consequence, its frequency drops, as evident from Fig. 6.13 (c).

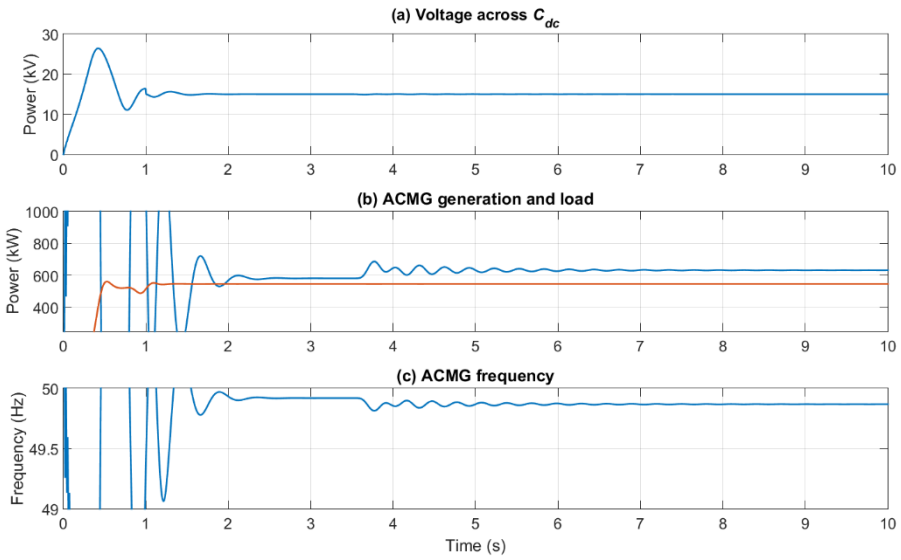

Fig. 6.13. (a) Voltage across dc capacitor, (b) ACMG generation and load and (c) ACMG frequency.

In Fig. 6.14 DAB-1 reference voltage and the output voltage are plotted. As this DAB starts to supply 50 kW extra power to DCMG-2, the output voltage reduces according to the feedback law of (4.27).

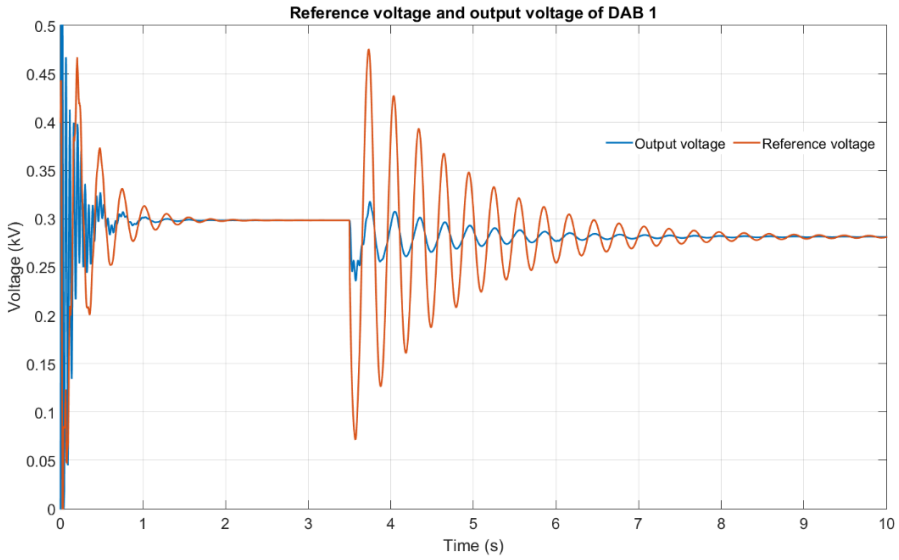

Fig. 6.14. Reference voltage and output voltage of DAB-1.

In Fig. 6.15 (a), DCMG 1 voltages are plotted. It can be observed that the voltages decrease after 3.5 s to supply extra 50 kW to DCMG-2. DCMG-1 powers are plotted in Fig. 6.15 (b). It can be seen that the local load remains unchanged at 300kW, however the generated power increases at 3.5 s. The power generation by the DGs settles to 233 kW and 118 kW according to the droop characteristics. From Fig. 6.15 (c) it can be observed that the power through the DAB-1 settles to 50 kW after 3.5 s.

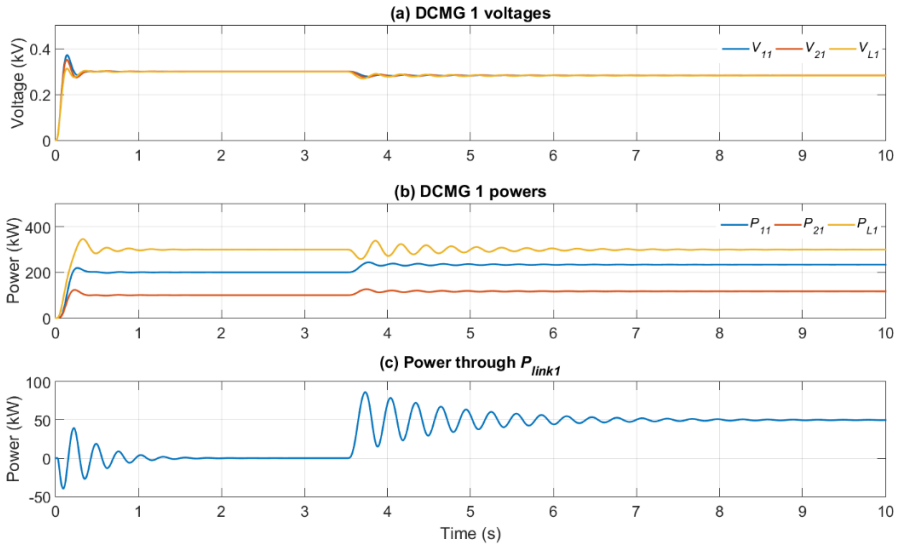

Fig. 6.15. (a) DCMG 1 voltages, (b) DCMG 1 powers and (c) power through P_{link1}.

The performance of DCMG-2 is shown in Figs. 6.16 and 6.17. In Fig. 6.15 DAB 2 reference voltage and the output voltage are plotted. Since this MG receives power from the two other MGs, its voltage reference increases (Fig. 6.16). Also the DGs voltages increase (Fig. 6.17 a), the generated powers drop (Fig. 6.17 b). Before 3.5 s, DG 1 and 2 supplies 220 kW and 144 kW respectively. After 3.5 s, DG 1 and DG 2 generation reduces to 156 kW and 105 kW respectively, maintaining 3:2 ratio. The negative power from of 100 kW through the DAB is shown in Fig. 6.17 (c).

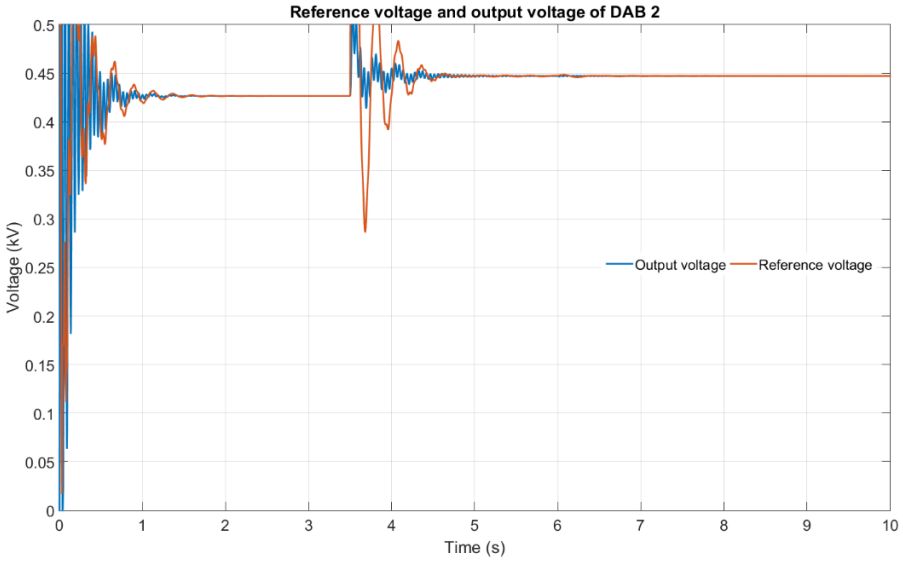

Fig. 6.16. Reference voltage and output voltage of DAB-2.

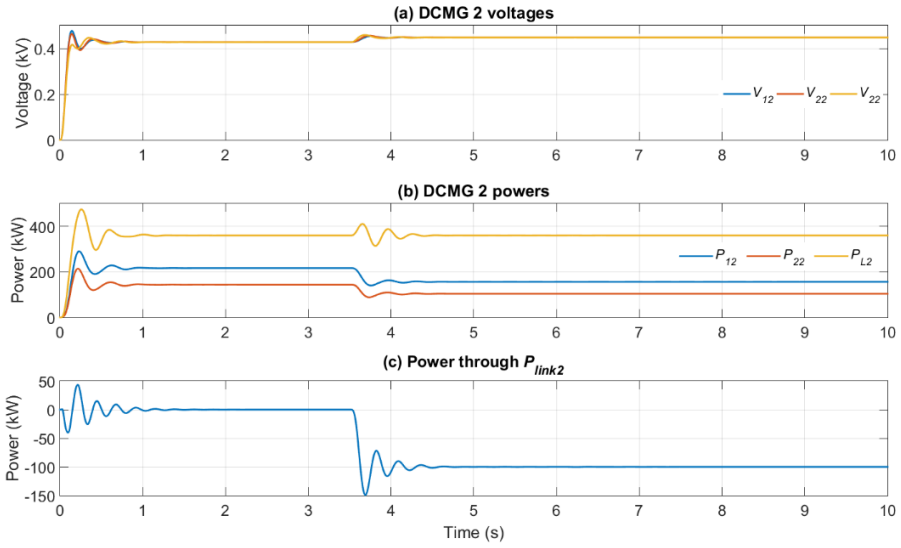

Fig. 6.17. (a) DCMG 2 voltages, (b) DCMG 2 powers and (c) power through P_{link2}.

6.7 Case D: Power Supply to a DCMG and ACMG from the Other DCMG

In this case study, DCMG-2 will supply 100 kW power to the DCMG-1 and ACMG, which will be shared equally amongst them. The local load of the ACMG is increased at 6 s. The dc capacitor voltage of the IC is plotted in Fig. 6.18 (a). It can be observed that the dc capacitor voltage stays stable and ripple free during any change in the system. Fig. 6.18 (b) shows the ACMG generation and load. It can be seen that, when the local load increases at 6 s, the ACMG generation is less than the load. This implies that the shortfall is covered by the power received by DCMG-2. The frequency behaves in the expected fashion as evident from Fig. 6.18 (c).

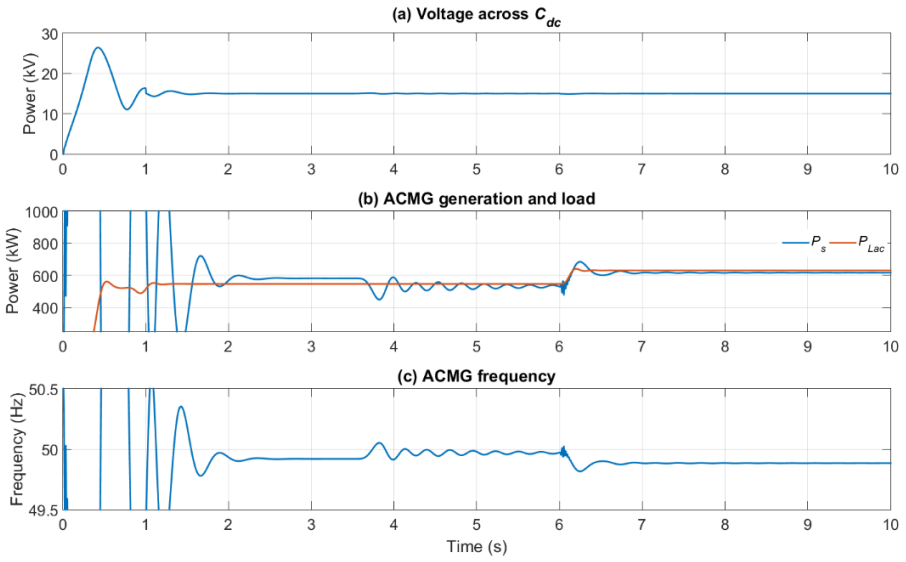

Fig. 6.18. (a) Voltage across dc capacitor, (b) ACMG generation and load and (c) ACMG frequency.

DCMG-1 quantities are plotted in Figs. 6.19 and 6.20. Since this MG receives power, its voltage reference increases (Fig. 6.19), the bus voltages increase (Fig. 6.20 a) and generated power decreases (Fig. 6.20 b). The link power is negative 50 kW as can be seen from Fig. 6.20 (c).

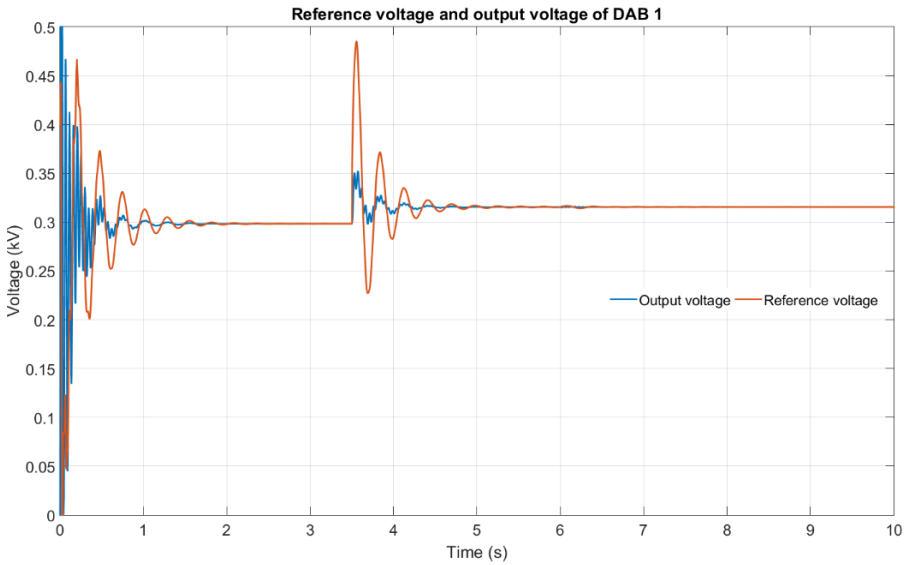

Fig. 6.19. Reference voltage and output voltage of DAB-1.

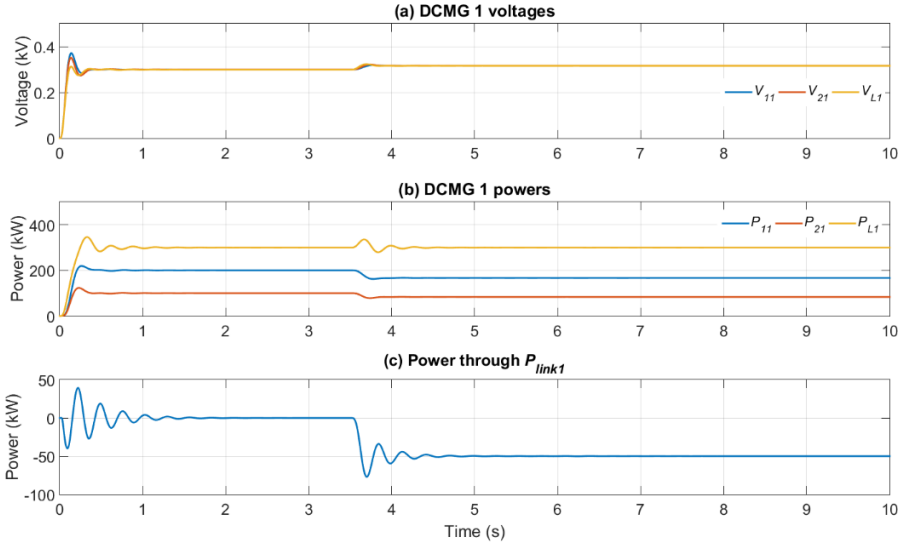

Fig. 6.20. (a) DCMG 1 voltages, (b) DCMG 1 powers and (c) power through P_{link1}.

DCMG-2 quantities are plotted in Figs. 6.21 and 6.22. Since this MG supplies power, its voltage reference decreases (Fig. 6.21), the bus voltages decrease (Fig. 6.22 a) and generated power increases (Fig. 6.22 b). The link power settles to 100 kW as can be seen from Fig. 6.22 (c).

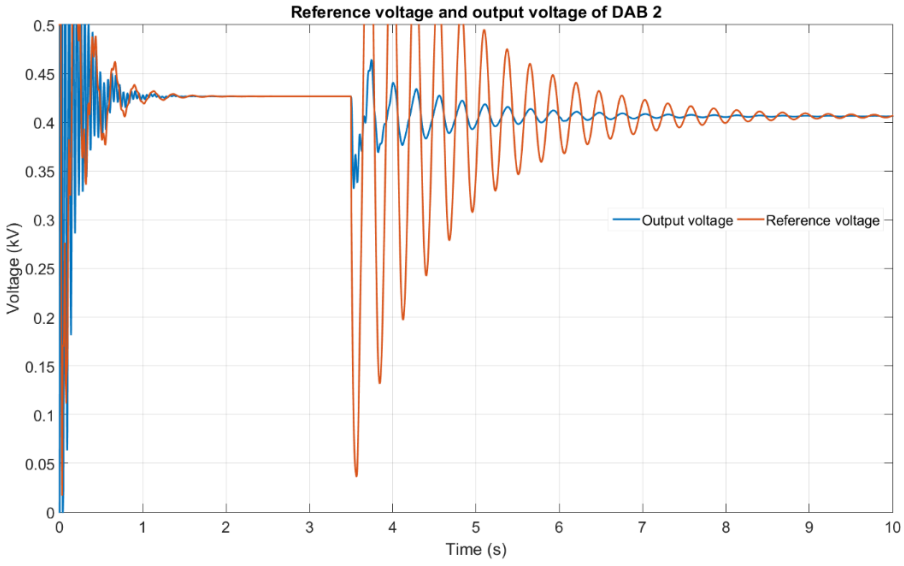

Fig. 6.21. Reference voltage and output voltage of DAB-2.

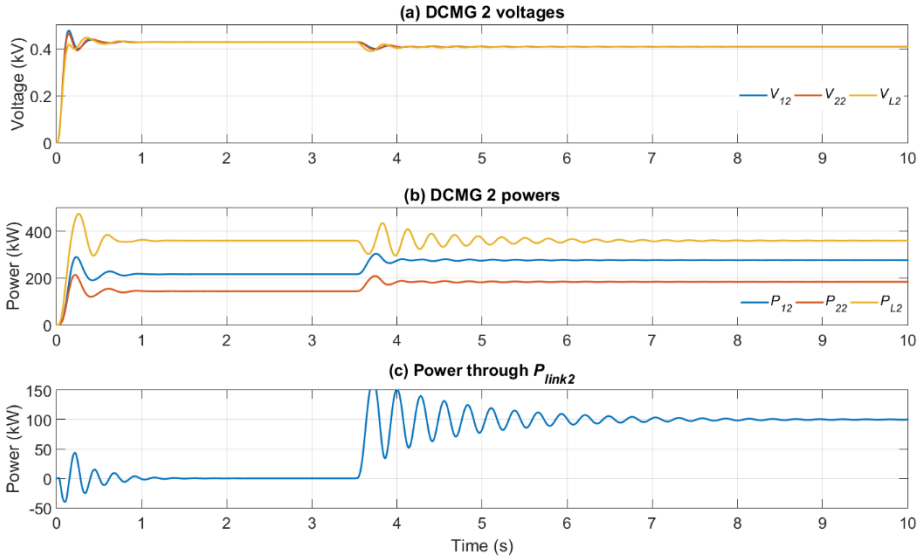

Fig. 6.22. (a) DCMG 2 voltages, (b) DCMG 2 powers and (c) power through P_{link2}.

The above four cases show that it is possible to facilitate controlled power flow from any of the microgrids to the others. In these examples, the power references are chosen arbitrarily to demonstrate the power flow capability. The main question however remains as how the references are chosen. To answer this question, three different methods are discussed, two of which are based on game theory. These are discussed in the next two sub-sections.

6.8. Power Transfer Reference Selection for Optimizing Cost

In this section, an analysis of power reference selection for the dual active bridge converters is proposed. It is assumed that the generation cost of the ACMG is the lowest. This analysis is also applicable for any ACMG connected DCMGs where the ACMG power generators are a mix of non-renewable sources (e.g., diesel generator, natural gas etc.) and renewable sources. It is also assumed that the per unit power generation cost of the DCMGs is larger than the per unit electricity generation cost of the ACMG. Usually, the generation cost for DCMG involves installation of power electronics equipment and dc switchgears. Thus their capital costs and discount rate will naturally be higher than the traditional sources. Moreover their replacement cost will also be higher. On the other hand, the capital cost of traditional generators is low, even though their running cost is higher due to the use of fossil fuel. Overall however, per unit cost of any ACMG will be less than that of a DCMG.

It is intended to minimize the power generation cost of the entire interconnected system. It is also designed to maximize the power generation from ACMG since it is cheaper. But when the ACMG will be overloaded, it will receive power from the DCMGs. This extra power will be supplied from the DCMG that has less electric power generation cost and also has less loads then its maximum capacity. In this analysis, 10% of the total generation capacity of any MG is kept as reserve to cater to any increase in its local load.

6.8.1. POWER TRANSFER REFERENCE SELECTION BY OPTIMIZATION METHOD

Let us define the per unit cost function of the three microgrids as follows

$$\begin{aligned} &\text{ACMG}: \quad C_{acpu} = x/kW \\ &\text{DCMG-1}: \quad C_{dc1pu} = 1.4x/kW \\ &\text{DCMG-2}: \quad C_{dc2pu} = 1.8x/kW \end{aligned}$$

where x is a unit of money. From the above equation, it can be seen that ACMG has the least per unit electric power generation cost and DCMG-2 is the most expensive one. A flowchart of the algorithm is presented in Fig. 6.23. ACMG, DCMG-1 and DCMG-2 are designed for 1 MW (P_{ac}), 500 kW (P_{dc1}) and 300 kW (P_{dc2}) generation capacity respectively. In the flow chart, P_{acL}, P_{dc1L} and P_{dc2L} represent the ACMG, the DCMG-1 and the DCMG-2 loads respectively. It has been assumed that DCMG-1 and DCMG-2 receive power of P_{dc1ref} and P_{dc2ref} from the other MGs. Surplus power generation capacity of ACMG is denoted as *Res.*

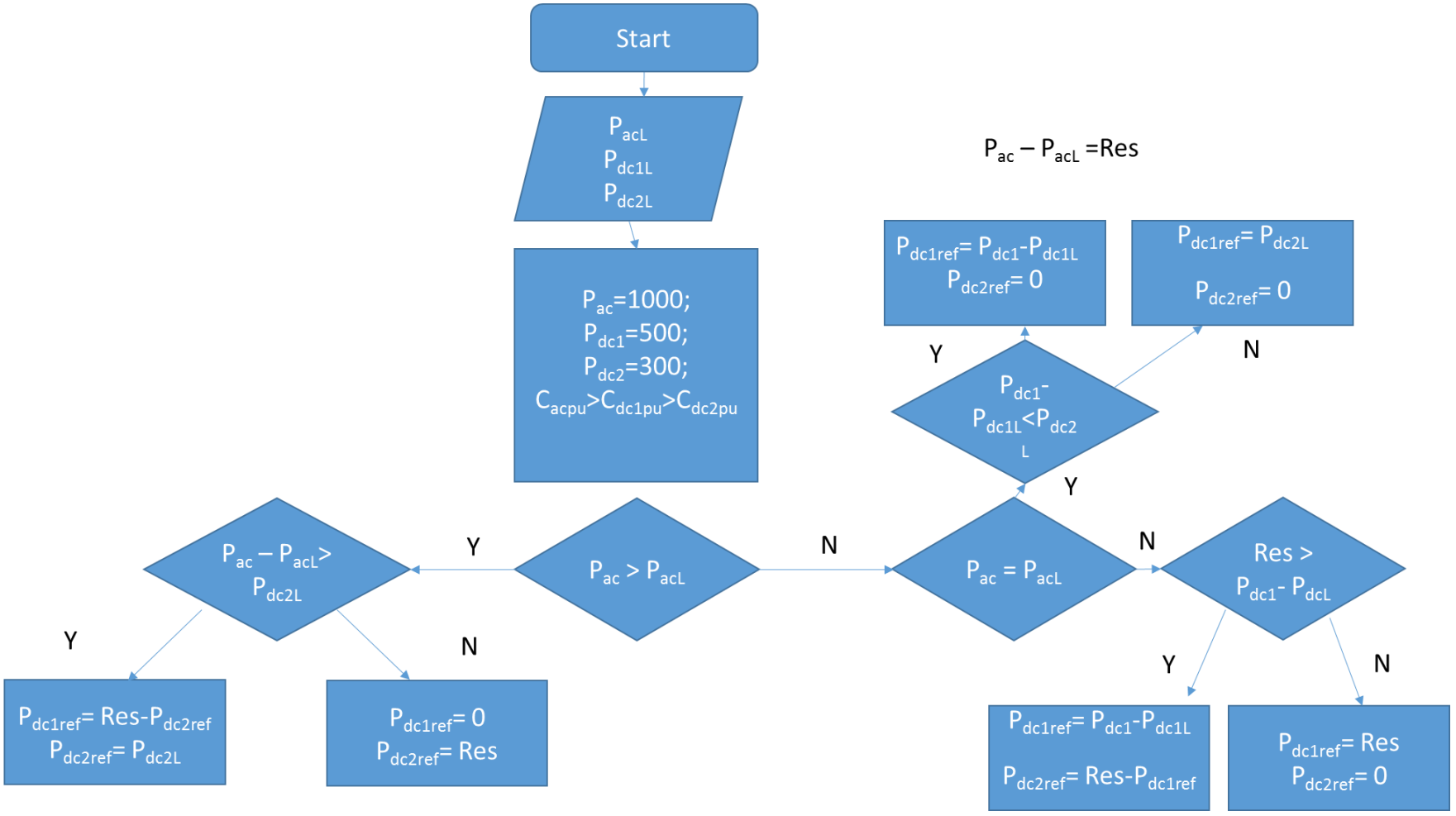

Fig. 6.23. Flowchart of the cost minimization algorithm.

The cost calculation can be summarized as follows for $Res \neq 0$:

$$C_{ac} = C_{acpu}\left(P_{acL} + P_{dc1ref} + P_{dc2ref}\right)$$
$$C_{dc1} = C_{dc1pu}\left(P_{dc1L} - P_{dc1ref}\right)$$
$$C_{dc2} = C_{dc2pu}\left(P_{dc2L} - P_{dc2ref}\right)$$
$$C_{total} = C_{ac} + C_{dc1} + C_{dc2}$$

And for $Res = 0$, DCMG-1 can supply power to DCMG-2 since its cost is lower. Therefore

$$C_{ac} = C_{acpu} \times P_{acL}$$
$$C_{dc1} = C_{dc1pu}\left(P_{dc1L} + P_{dc2ref}\right)$$
$$C_{dc2} = C_{dc2pu}\left(P_{dc2L} - P_{dc2ref}\right)$$
$$C_{total} = C_{ac} + C_{dc1} + C_{dc2}$$

Now let us consider the following cases:

A. Nominal operation

Power transfer can be initiated even during the nominal operation when the DGs in the microgrid are not overloaded. This case can be divided into two conditions: when the ACMG has sufficient surplus power to supply to an entire dc microgrid and ACMG has limited surplus power which can be supplied to the DCMG for overall cost minimization.

Table 6.2: ACMG, DCMG-1 and 2's loads, surplus power and P_{ref} for case-A (Example 1)

MG	Loads (kW)	Surplus (kW)	P_{ref} (kW)
ACMG	550	350	
DCMG-1	250	200	100
DCMG-2	250	20	250

First, let us assume ACMG, DCMG-1 and DCMG-2 has a load of 550 kW, 250 kW and 250 kW respectively (Table 6.2). Power received from the ACMG is denoted with positive value of P_{ref}. Considering 10% reserve, ACMG has a surplus of 350 kW. From the proposed algorithm it can be seen that it will be cost effective if the surplus power is first supplied (250 kW) to the

DCMG-2 since it is the most expensive one. The remaining power will be supplied to the DCMG-1 (100 kW). After implementing the proposed algorithm the total power generation cost is 1110*x*. Without this power sharing scheme the electric power generation cost for the same system would have been 1350*x*.

Table 6.3: ACMG, DCMG-1 and 2's loads, surplus power and P_{ref} for case-A (Example 2)

MG	Loads (kW)	Surplus (kW)	P_{ref} (kW)
ACMG	850	50	
DCMG-1	250	200	0
DCMG-2	250	20	50

Now, let us assume ACMG, DCMG-1 and DCMG-2 has a load of 850 kW, 250 kW and 250 kW respectively (Table 6.3). This time only 50 kW power will be supplied to the DCMG-2. After the power transfer the power generation cost will be 1610*x* which is still cheaper if no power transfer is initiated. If no power transfer is initiated then the cost will be 1650*x*.

B. Power shortfall in the ACMG

In this case, it is assumed that the ACMG is saturated. So no power can be supplied to the DCMGs from the ACMG. Since one of the DCMG has a lower electric power generation cost, power sharing in between the DCMGs can be initiated to minimize the power generation cost. This case can be segregated into three scenarios: (1) ACMG is saturated but DCMG-1 can cater some power to the DCMG-2, (2) ACMG is overloaded and the cheapest DCMG can supply surplus power and (3) ACMG is overloaded but the cheapest DCMG cannot supply the entire power shortfall. Power supplied to the ACMG or other DCMG is denoted with negative value of P_{ref}.

Table 6.4: ACMG, DCMG-1 and 2's loads, surplus power and P_{ref} for case-B (Example 1)

MG	Loads (kW)	Surplus (kW)	P_{ref} (kW)
ACMG	900	0	
DCMG-1	100	350	-250
DCMG-2	250	20	0

First, let us assume ACMG, DCMG-1 and DCMG-2 have loads of 900 kW, 100 kW and 250 kW respectively (Table 6.4, Example 1). In this case we can see that ACMG will not be able to supply any power to the DCMGs but the DCMG-1 can supply up to 350 kW power to the DCMG-2 to minimize the cost of electric power generation. For this case the cost of electric power generation for the entire system will be 1422*x*. Without initiating the power sharing the cost will be 1490*x*.

Table 6.5: ACMG, DCMG-1 and 2's loads, surplus power and P_{ref} for case-B (Example 2)

MG	Loads (kW)	Surplus (kW)	P_{ref} (kW)
ACMG	1050	0	
DCMG-1	100	350	– 150
DCMG-2	250	20	0

Now, let us assume ACMG, DCMG-1 and DCMG-2 have loads of 1050 kW, 100 kW and 250 kW respectively (Table 6.5, Example 2). In this case DCMG-1 will supply 150 kW to the ACMG. Power generation cost will be 1700*x*.

Table 6.6: ACMG, DCMG-1 and 2's loads, surplus power and P_{ref} for case-B (Example 3)

MG	Loads (kW)	Surplus (kW)	P_{ref} (kW)
ACMG	1100	0	
DCMG-1	280	170	– 170
DCMG-2	220	50	– 30

Finally, let us assume ACMG, DCMG-1 and DCMG-2 are loaded to 1100 kW, 280 kW and 220 kW respectively (Table 6.6, Example 3). In this situation DCMG-1 will supply 170 kW power and DCMG-2 will supply 30 kW to cater this power shortfall in ACMG. Using the proposed scheme the power generation cost is 1980*x*.

C. Power shortfall in the DCMG

Power shortfall in the DCMG is a simple case for the considered constrains. Since the power generation of the DCMGs are considered expensive so during a shortfall in either of the DCMG, first the ACMG will try to supply the deficiency. In case the ACMG cannot supply the entire power shortfall, the other DCMG will supply the remaining power shortfall.

6.9. POWER TRANSFER REFERENCE SELECTION BY GAME THEORY

As has been mentioned earlier, the power generation cost of ACMG has been justifiably assumed to be less than that of the DCMGs. Even the utility power cost is less as it uses the fossil fuel. Subsequently, when an ACMG or the utility have surplus power it can sell power to the DCMGs. DCMGs will be benefited as it will receive power in cheaper cost, which will allow to minimize cost at a certain time. This situation can be considered win-win situation for both ACMG and DCMGs as ACMG will be able to sell more power while the DCMGs will be able to buy some power from the ACMG to reduce their cost. A fair allocation of ACMG surplus power to the DCMGs can be computed based on "Shapely Value" [164] for cooperative game theory.

On the other hand, during daytime DCMGs, which may have considerable PV penetration, might have the capacity to generate maximum amount of power but might not have enough loads to cater. At this situation, DCMGs can sell some power and ACMG can back down its generation to minimize its cost. When there are multiple players in a market it introduces a competition. The power transfer from DCMGs to ACMG is solved using the two following methods of game theory:

1. For a monopoly situation "Price leadership" model is adopted and
2. For duopoly market situation "Stackleberg Duopoly" model is adopted.

6.9.1. USING SHAPELY VALUE

For this analysis, we can surmise that the DCMGs will supply power only when the ACMG is saturated; otherwise their power is too expensive. In this different approach of deciding a fair allocation in a cooperative game, we allocate an amount proportional to the benefit each coalition derives from having a specific player as a member [164]. An allocation $\boldsymbol{x} = (x_1, x_2, \ldots, x_n)$ is called the ***Shapely value*** if

$$x_i = \sum_{\{S \in \Pi^i\}} [v(s) - v(S - i)] \frac{(s_n - 1)!(n - s_n)!}{n!}, \quad i = 1, \cdots, n$$

where Π^i is the set of all coalitions $S \subset N$ containing i as a member, s_n is the number of members in S.

For example, Table 6.7 specifies the loads and surpluses of each MG. Let us define DCMG-1 by *A* and DCMG-2 by *B*.

Table 6.7:

MGs	Load (kW)	Surplus (kW)
ACMG	500	400
DCMG-1 (*A*)	250	NA
DCMG-2 (*B*)	200	NA

If the DCMGs were supplied power according to the ratings, then DCMG-1 would have received 250 kW, while DCMG-2 would have received 150 kW.

The characteristic functions of the cooperative games are defined as follows [164]

$$v(A) = 200,\ v(B) = 150,\ v(AB) = 400$$

The reason for this is that if the ACMG supplies the entire demand of DCMG-2, then DCMG-1 will have only 200 kW. Similarly, if the ACMG supplies the entire demand of DCMG-1, then DCMG-2 will have 150 kW. Also together they cannot have more than 400 kW power.

Then the Shapely value for *A* is

$$x_A = \left[v(A) - v(0)\right]\frac{(1-1)!(2-1)!}{2!} + \left[v(AB) - v(B)\right]\frac{(2-1)!(2-2)!}{2!}$$
$$= \frac{200}{2} + \frac{400-150}{2} = 225$$

The Shapely value for *B* is

$$x_B = \left[v(B) - v(0)\right]\frac{(1-1)!(2-1)!}{2!} + \left[v(AB) - v(A)\right]\frac{(2-1)!(2-2)!}{2!}$$
$$= \frac{150}{2} + \frac{400-200}{2} = 175$$

The cost for the three MGs will then be:

ACMG: Cost = 500*x* since it sells 400*x* power to the other MGs, while its consumption is 500*x*.

DCMG-1: Cost = (1.4×25 + 225)x = 260x since it only generates 25 kW and buys the rest from the ACMG.

DCMG-2: Cost = (1.8×25 + 175)x = 220x since it only generates 25 kW and buys the rest from the ACMG.

This might seem unfair but if ACMG and DCMG-2 join hands together to cheat DCMG-1, then the entire demand of 200 kW of DCMG-2 can be supplied by the ACMG. In that case, the cost of DCMG-2 will reduce to 200x. On the other hand, the cost of DCMG-1 will increase to 270x.

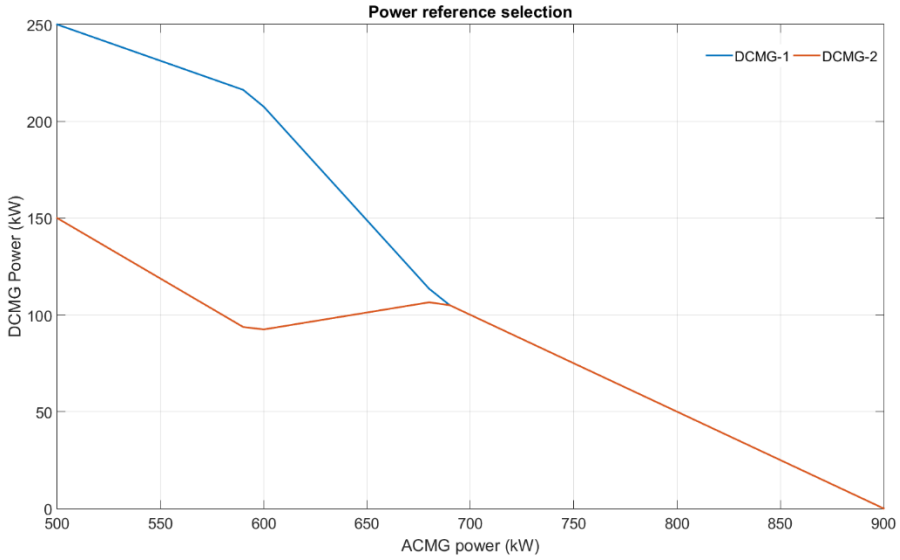

Fig. 6.24. Power reference selection using shapely values.

Now let us consider a case of a residential network. Usually in the residential area during the day time, the load demand is low and it keeps on increasing from the afternoon. Base load for the ACMG, DCMG-1 and DCMG-2 are considered 500 kW, 250 kW and 150 kW respectively. Considering this scenario, ACMG load is varied together with the DCMG-1 and DCMG-2 loads. As the loads are increased the power reference also changes. Surplus power of the ACMG decreases and the load demand increases at the same time. From Fig. 6.24, it can be seen that we can get the power reference at different load combination using shapely values. It can also be noted that the power demand reference becomes equal for both the DCMGs when the surplus becomes low. If the load profile of the ACMG is known, from the above analysis it can be identified how much power the ACMG will receive from the DCMGs.

With respect to Fig. 6.24, for the same amount of power, DCMG-2 is expensive as expected, as shown in Fig. 6.25. It can be also noticed that the price increase rate of DCMG-2 is steeper than of DCMG-1. From this cost analysis the operator can decide the quantity of power to be purchased from the DCMGs.

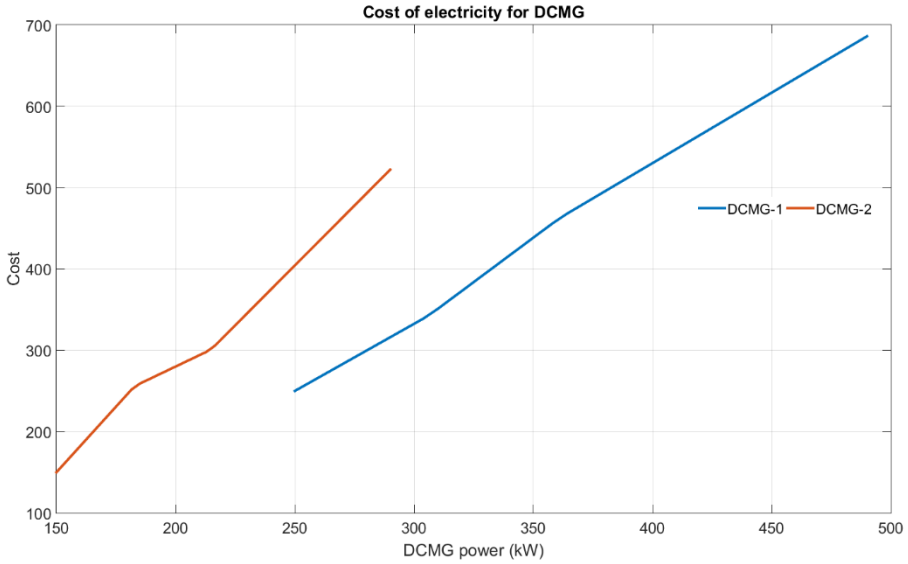

Fig. 6.25. Power generation cost for DCMGs.

6.9.2. DCMG TO ACMG POWER TRANSFER REFERENCE SELECTION AT DIFFERENT MARKET CONDITION

A. Monopoly Market Situation

For a situation where, DCMG-1 is of a larger capacity and DCMG-2 is a newly established microgrid. An analysis is presented using price leadership model [161, 162] in this section to optimize the power generation and supply to the ACMG at a competitive price. In this study, DCMG-1 has a marginal cost advantage over DCMG-2. If DCMG-2 decides to start introducing lower prices, DCMG-1 will emerge as the winner of an eventual war price. This would occur because of the marginal cost advantage. Under this market conditions, it is assumed that DCMG-1 as the market leader and DCMG-2 as the market follower. Let us consider a demand function to define how much power to be supplied to the ACMG as following

$$p^d = 100 - 2\left(Q_T\right) \tag{6.5}$$

Where p^d and Q_T represent the demand function and the total quantity of power to be delivered to the ACMG.

$$Q_T = q_1 + q_2$$

where q_1 and q_2 respectively are the power supplied by DCMG-1 and DCMG-2 respectively.

Now let us consider the inverse supply of DCMG-1 and 2 are defined by MC_1 and p_2^s respectively and we assume the following relation to iterate it as a function of their power to be supplied:

$$MC_1 = q_1$$

$$p_2^s = 3q_2$$

Rearranging (6.5) as the function of p, we get the following

$$D\left(p\right) = Q_T = 50 - \frac{1}{2}p$$

$$S_2(p) = q_2 = \frac{1}{3}p$$

Since, DCMG-2 is a newly established microgrid, DCMG-2 is new entrant in the market. Demand function of a new entrant in a market is termed as the residual demand function, *R(p)* can be expressed as following [165]:

$$\begin{aligned} R(p) &= D(p) - S_2(p) \\ &= \left(50 - \frac{1}{2}p\right) - \frac{1}{3}p \\ &= 50 - 0.833p \\ p^r &= 60 - 1.2q \end{aligned}$$

For this case study, DCMG-1 will set the price and will act as a monopolist facing the residual demand. Assuming DCMG-1 marginal revenue as MR^r we get

$$MR^r = 60 - 2.4q \qquad (6.6)$$

The condition of market leader's (DCMG-1) profit maximisation is when marginal revenue will be equal to marginal cost. It can be expressed as follows

$$MR_r = MC_1$$

From (6.6) we get the following

$$60 - 2.4q_1^* = q_1^*$$

$$q_1^* = \frac{60}{3.4} = 17.65$$

Now, the market leader will define the price at which it will it will export power to the customer (ACMG).

$$p_1^{r*} = 60 - 1.2(17.65) = 38.82 \text{ cents/kW}$$

Similarly, q_2 can also be calculated.

$$p = 38.82 : D(p) = 50 - \frac{1}{2} \times 38.82 = 30.59 \text{ kW}$$

$$q_2^* = 30.59 - 17.65 = 12.94 \text{ kW}$$

Normalizing the quantities for same demand function but for an increased proportional demand we get:

$$q_1 = \frac{17.65}{30.59} \times Q_T = 0.577 Q_T$$

$$q_2 = \frac{12.94}{30.59} \times Q_T = 0.423 Q_T$$

Now, let us consider that ACMG decides to import 200 kW electric power from the DCMGs. DCMG-1 will supply 200×0.577=115.4 kW and DCMG-2 will supply 84.6 kW power at 30.59 cents/kW rate given that they have surplus amount of that power to be delivered. From the above analysis it can be summarized that at a monopoly market condition, the market leader will set the price of power to be exported. Then based on the inverse supply equation it can be calculated how much power each dc microgrid will supply to the ACMG.

B. Duopoly Market Situation

Now let us consider a duopoly situation for the microgrid. DCMG 1 is generating power using solar panel and DCMG-2 is another recently established solar power based dc microgrid. Stackelberg's model is adopted to analyse this situation. According to the Stackleberg model, DCMG-1 will first set how much power it will supply to the ACMG. Later DCMG-2 will decide how much power it will supply to the ACMG. We also assume that DCMG-1 "knows" how DCMG-2 is going to react to its decisions (if DCMG-1 does not know all the information it will adjust production by trial and error until it sees its profits being maximised). DCMG-2 will make an economic profit and influence the price, however neither DCMG-1 nor DCMG-2 will not have total control over the price. We shall be using the same market inverse demand function as the previous study.

- DCMG-1 total cost function: $C_1 = q_1$

- DCMG-1 total cost function: $C_2 = 3q_2$

Let us first obtain DCMG-2's reaction function

$$\begin{aligned} Max_{q2}\pi_2 &= pq_2 - C_2(q_2) \\ &= \left[100 - 2(q_1 + q_2)\right]q_2 - 3q_2 \\ &= 100q_2 - 2q_1q_2 - 2q_2^2 - 3q_2 \\ &= 97q_2 - 2q_1q_2 - 2q_2^2 \end{aligned}$$

From the first-order condition we get the following:

$$\pi_2^{/} = 97 - 2q_1 - 4q_2 = 0$$

Since DCMG-2 is the market follower, a "reaction function" can be derived as follows which is by definition dependent on the action of other players (DCMG-1) [165, 166]

$$q_2 = \frac{97}{4} - 0.5q_1 \qquad (6.7)$$

Now let us maximize DCMG-1's profit subject to DCMG-2's reaction function

$$\begin{aligned} Max_{q1}\pi_1 &= pq_1 - C_1(q_1) \\ &= \left[100 - 2(q_1 + q_2)\right]q_1 - q_1 \\ &= 100q_1 - 2q_1q_2 - 2q_1^2 - q_1 \\ &= 99q_1 - 2q_1q_2 - 2q_1^2 \end{aligned}$$

Using (6.7) we get

$$\begin{aligned} Max_{q1}\pi_1 &= 99q_1 - 2q_1\left(\frac{97}{4} - 0.5q_1\right) - 2q_1^2 \\ &= 99q_1 - 2q_1^2 + q_1^2 - \frac{194}{4}q_1 \\ &= 50.5q_1 - q_1^2 \end{aligned}$$

From the first-order condition we get the following:

$$\pi_1^{/} = -2q_1 + 50.5 = 0$$

Finally we get the quantity, q_1

$$q_1 = \frac{50.5}{2} = 25.25$$

q_2 can be calculated using (6.7) as

$$\begin{aligned} q_2 &= \frac{97}{4} - 0.5 * 25.25 \\ &= 24.25 - 12.625 \\ &= 11.625 \end{aligned}$$

Normalizing the quantities for same demand function but for an increased proportional demand we get:

$$q_1^* = \frac{25.25}{25.25 + 11.625} Q = 0.6847Q$$

$$q_2^* = \frac{11.625}{25.25 + 11.625} Q = 0.3153Q$$

From (6.5) we get the price at which the DCMGs will export power to the ACMG

$$\begin{aligned} p &= 100 - 2 \times (25.25 + 11.625) \\ &= 26.25 \,\text{cents/kW} \end{aligned}$$

Now, let us consider that ACMG decides to import 200 kW electric power from the DCMGs. DCMG-1 will supply 200×0.6847=136.94 kW and DCMG-2 will supply 63.06 kW power at 26.25 cents/kW rate given that they have surplus amount of that power to be delivered. From the above analysis it can be summarized that at a duopoly market condition, the market leader will set the price of power to be exported. Then based on the inverse supply equation it can be calculated how much power each dc microgrid will supply to the ACMG.

6.9. CONCLUSIONS

From the analysis presented in this chapter, it can be concluded that accurate power sharing can be achieved by connecting multiple DABs on the dc side of the interlinking converter. The advantage of using DAB to connect the DCMG to the ac grid is that it reduces the possibility of generating circulating current and also does not require passive filters on the dc side of the interlinking converter. Multiple approaches for power reference selection at different market condition are also discussed in this chapter. Perfect market condition and also monopoly and duopoly market condition are considered to analyse the amount of power to be delivered in between the microgrids. More complicated market situation can be solved with bargaining solutions which has not been attempted in this thesis.

CHAPTER 7

POWER HARDWARE IN THE LOOP (PHIL) SIMULATION OF AN INTERCONNECTED AC AND DC MICROGRID

The power hardware-in-the-loop (PHIL) concept is used in this chapter to test the coupling of an ac microgrid (ACMG) and a dc microgrid (DCMG). The PHIL method experimentally verify control algorithms. These experiments verify the control algorithms and the operations of integrated ac-dc microgrids proposed in the thesis. In this, the ACMG side with an interlinking voltage source converter is simulated (virtual circuit) and is interfaced with the hardware of the DCMG through a suitable converter, termed as the power flow converter (PFC). The PFC supplies the desired amount of power from the ACMG to the DCMG, while the interlinking converter (IC) holds the DC bus voltage, as has been discussed in Chapter 4. The dc converters are operated under voltage droop sharing and the virtual ac microgrid (ACMG) is operated using frequency droop control. The operation of the interconnected system is also validated through simulation studies with PSCAD/EMTDC for the same hardware setup and the simulation results are compared with the PHIL results. It has been shown that they match closely.

7.1. PHIL CONCEPT

In PHIL simulation, a large network is usually partitioned into two parts: virtual side and hardware under test (HuT). Part of the power network simulated in a real-time simulator is defined as virtual side and the remaining part of the network is setup with a physical circuit referred as HuT [168].This concept of the PHIL simulation is illustrated in Fig. 7.1, where Fig. 7.1 (a) represents the current control and Fig. 7.1 (b) represents the voltage control. In these figures, v_1, Z_1 represent the Thevenin equivalent of the virtual side network. The HuT may have separated generator with some feeders and local loads. Thus represented with Thevenin equivalent v_2, Z_2.

In Fig. 7.1 (a), the current i_1 originated from the virtual side controls the current source of the HuT. Voltage at the point of common coupling (PCC) controls the virtual side voltage v_f[168]. v_p is passed through a low pass filter (LPF) so that high frequency components originated from dynamic simulation can be suppressed. A resistance R_3 is connected in parallel to the current source

to avoid current mismatch. For voltage control of Fig. 7.1 (b), current in HuT, i_2 is passed through a LPF to control the current source in the virtual side and v_p is used as a reference to control the voltage $v_p^{/}$.

For stable and accurate PHIL simulation proper selection of converter bandwidth and time delay and elimination of sensor noises are required [125, 133, 169, 170]. Dargahi et al [124] presented a discrete time analysis as a PHIL simulation is operated in discrete time. The study shows that the condition $\beta(Z_{eq}/Z_1) < 0$ has to be fulfilled for a stable operation where,

$$\beta = 1 - e^{-\alpha \Delta T}, \quad Z_{eq} = \frac{R_3 Z_2}{R_3 + Z_2} \tag{7.1}$$

where α is the cut-off frequency of the low-pass filter $T_{LPF} = \alpha/(s + \alpha)$. The closed-loop block diagram is shown in Fig.7.2 where T_{DAC}, T_{ADC} and T_{PFC} respectively are the transfer functions of DAC, ADC and PFC (Power flow controller).

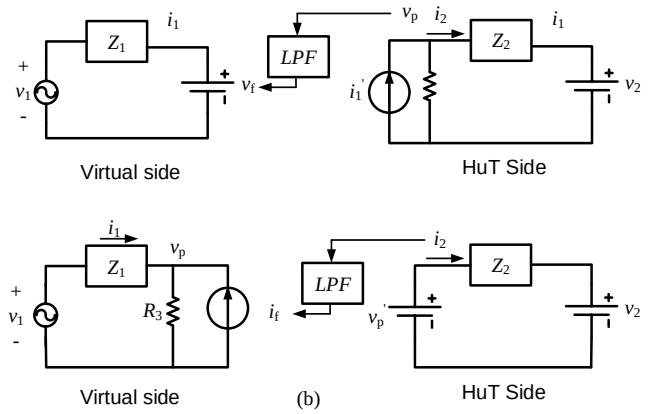

Fig. 7.1: Conceptual PHIL simulation diagram; (a) current control (b) voltage control.

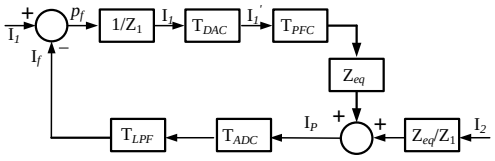

Fig. 7.2: Block diagram of the system under voltage control.

7.2. SYSTEM STRUCTURE

The system structure considered in this study is shown in Fig. 7.3, where the network tearing line is also indicated. The DCMG is consider as the HuT and the rest is considered as the virtual circuit. In this study, a voltage controlled voltage source represents the virtual side that drives the HuT. A current controlled current source represents the HuT and drives the virtual side. Thus it can be said that voltage control mode is used.

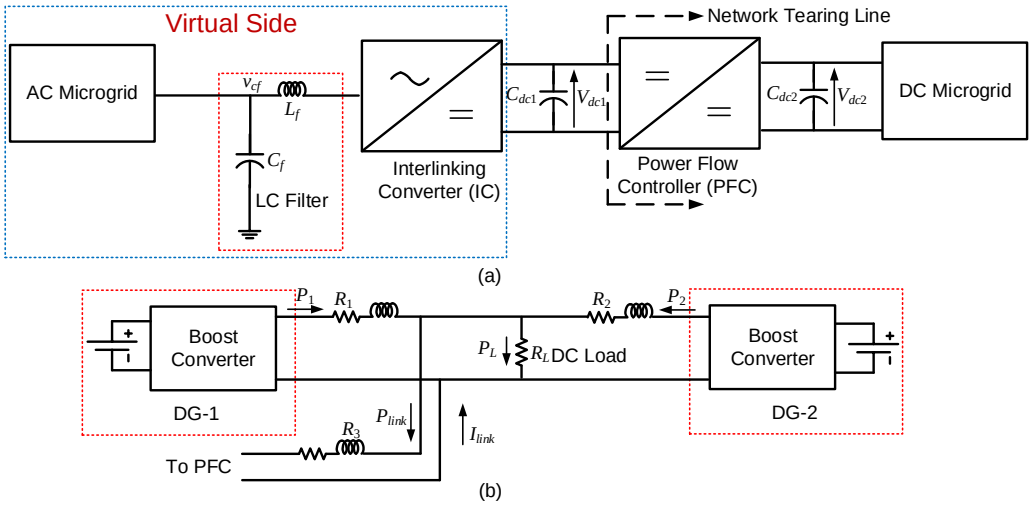

Fig. 7.3. (a) The overall system structure and (b) the structure of the dc microgrid.

The DCMG is connected to the ACMG through an IC and a dc-dc power flow controller (PFC). On the AC side of the IC, an LC filter (L_f and C_f) is used to bypass high frequency switching harmonics. A voltage source converter (VSC) is used as IC to hold the dc capacitor voltage V_{dc1} across C_{dc1} to a constant value. During PHIL simulation, the DCMG is represented with a controlled current source in the virtual side.

In the HuT, a buck converter is used as PFC. Given that V_{dc1} is constant, the PFC modulates the voltage V_{dc2} across C_{dc2} to facilitate power flow to the DCMG from the ACMG in a controlled manner. Since the power flow in this case is unidirectional, the PFC is connected to a DC power supply.

The DCMG structure, shown in Fig. 7.3 (b), contains two boost converters and a load. A buck converter is used as PFC to supply desired amount of power to the load. This converter holds the dc bus voltage and also to step down the voltage to the dc bus level. The boost converters are

used to step up the voltage to the dc bus level. All these dc converters are designed and tuned in such a way that it can hold its output voltage even during any fluctuations in the input side of these converters. The line resistances are represented by R_1 and R_2, while the inductors acts as damping inductors. The PFC is connected to the dc bus through a resistor R_3 and the power flow from the ac ACMG is considered as P_{link}. The power flow through boost converter 1 and 2 respectively are P_1 and P_2.

7.3. TEST RESULTS

In this section, test results of three case studies are presented. At first the hardware results of islanded mode of DCMG operation is presented. Followed by this, PHIL simulation of constant power supply to the DCMG and 'islanded mode' to 'constant power supply to the DCMG' mode switching is presented. Simulation results are also presented in this section to compare the test results. DS1104 (DSPACE) is used as real time simulator and PSCAD is used to run the simulation studies. A photograph of the test setup is shown in Fig. 7.4. The system parameters used in this study are listed in Table 7.1.

In order to operate the hardware setup under safety operating limit, the converter voltage and current is scaled down to a factor of 100. The power rating subsequently is scaled down by 10000.

Table 7.1: System Parameters

Quantities		Parameters
AC side	Operating frequency Voltage L-L RMS	50Hz 11kV
IC	Transformer DC capacitor Filter capacitor Switching frequency Reference DC voltage	11/1.72kV 5000 μF 50μF 15kHz 2.5kV
PFC	Input voltage Inductor Capacitor	60V 8.2mH 1100μF
Boost converters	Input voltage Inductor Capacitor	15V 8.2mH 1100μF
Line resistance	R_1 R_2	1.2 Ω 1.4 Ω

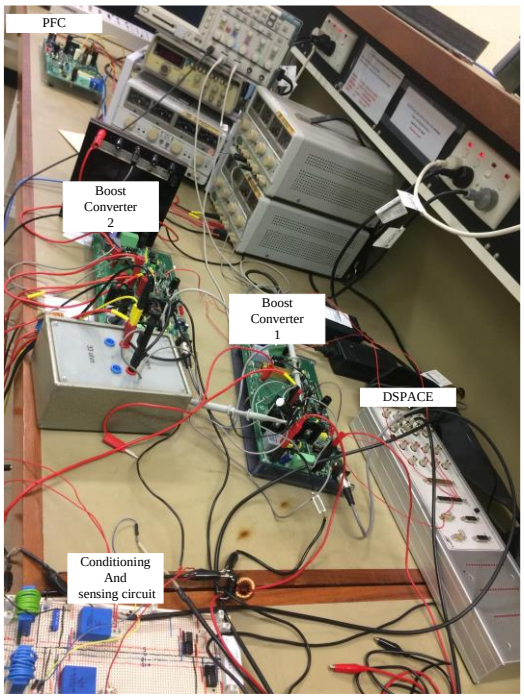

Fig. 7.4 Photograph of the hardware setup

7.3.1. ISLANDED MODE OF OPERATION

For the islanded mode of DCMG study, a simple DCMG with two boost converter and a load is considered (Fig. 7.3-b). Power sharing is governed by the selected droop gains of the individual converters. At first the droop gains are selected in such a way that they share power in 2:1 ratio. Subsequently, for 15 W load the power supplied by DG_1 and DG_2 is: P_1 is equal to 10 W and P_2 is equal to 5W respectively. In Figs. 7.5 and 7.6, a comparison between the simulation results and the hardware result is presented. Measured power and voltage of both the converters are plotted respectively. No major discrepancy is observed in between the simulation result and the hardware results.

The same system was tested for equal power sharing. Subsequently, for 15 load the power, the power supplied by both DG_1 and DG_2 is equal 7.5 W. In Figs. 7.7 and 7.8, a comparison between the simulated result and the hardware result is presented. No major discrepancy is observed in between the simulation result and the hardware results.

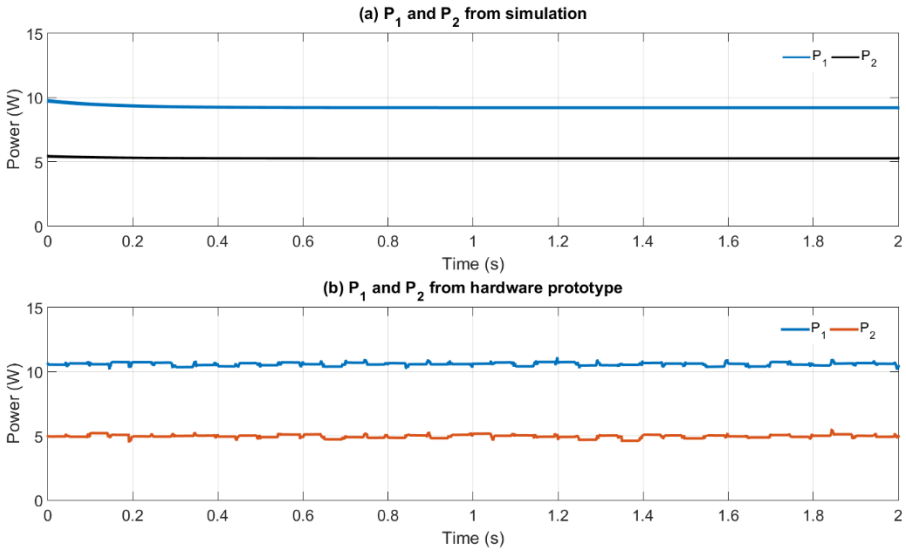

Fig. 7.5 Power sharing in islanded mode of operation.

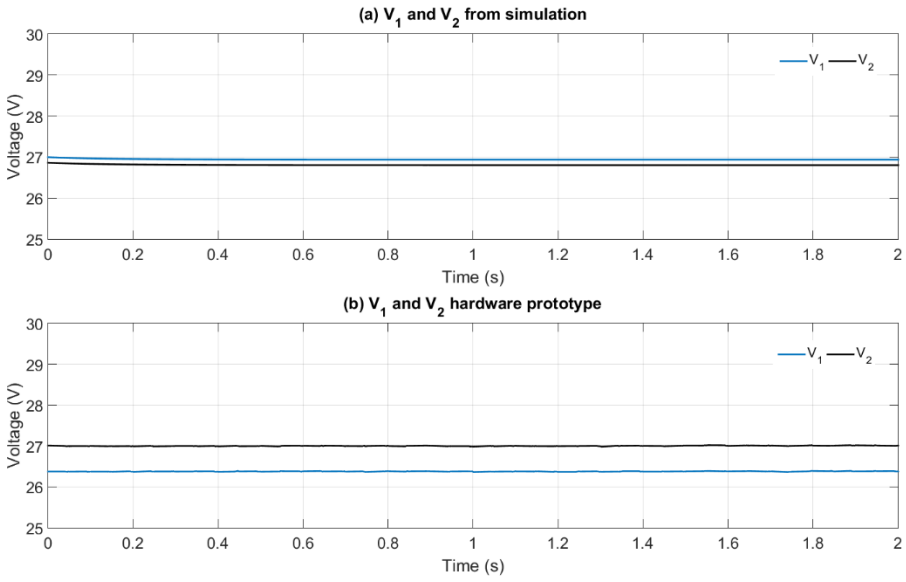

Fig. 7.6. Voltages in islanded mode of operation.

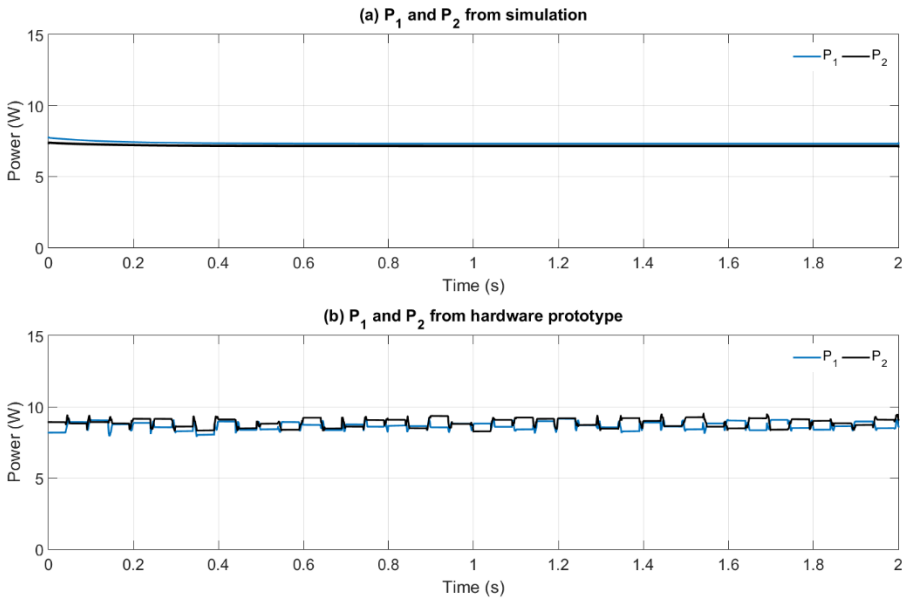

Fig. 7.7. Power sharing in islanded mode of operation when same droop gain selected for both DGs

7.3.2. CONSTANT POWER SUPPLY TO THE DCMG

PHIL simulation results of the case of constant power supply to the DCMG is presented in this section. At first the PFC is set to facilitate 15 W power to the DCMG. This case is studied to demonstrate a constant amount of power supply from the ACMG to the DCMG.

In Figs. 7.9 and 7.10, the power supplied to the DCMG is plotted, the former from the PHIL simulation and the latter from PSCAD simulation. PFC in the HuT is set such that it supplies 15 W power to the DCMG. In the virtual side it is found to be around 150 kW because of the scaling factor of 10×10^3. It can be seen that the PHIL simulation results match with PSCAD simulation results.

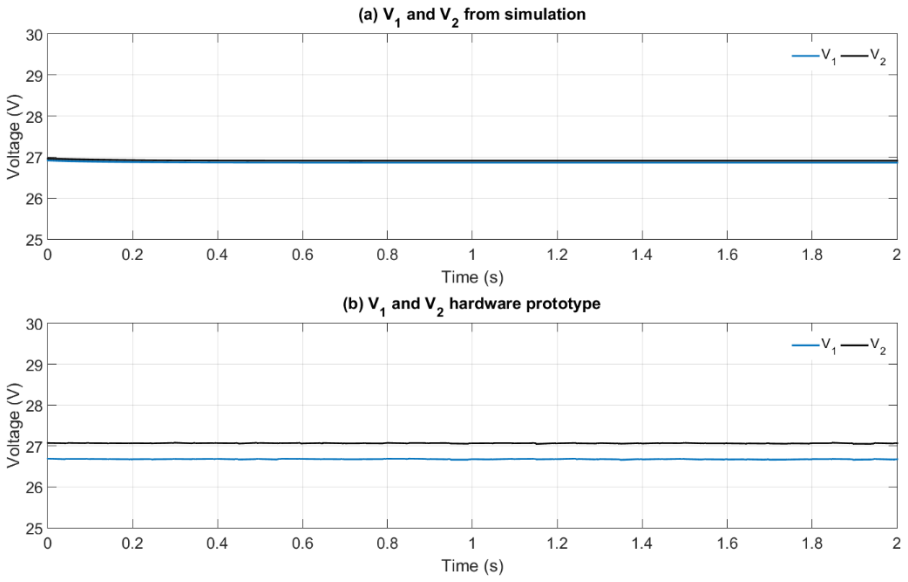

Fig. 7.8: Voltages during islanded mode of operation when same droop gain selected for both DGs.

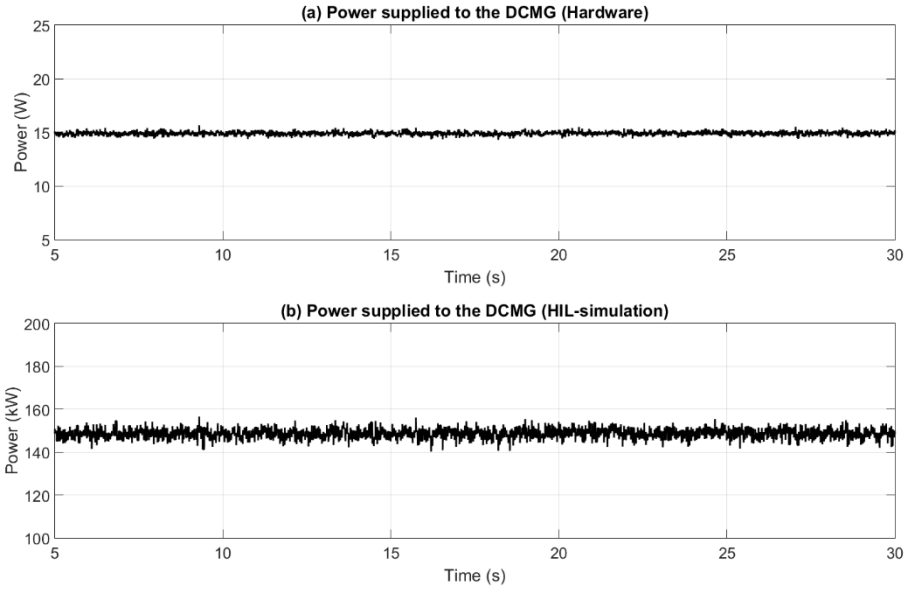

Fig.7.9: Hardware and PHIL results of Constant power supply to the DCMG when P_{ref}=15 W.

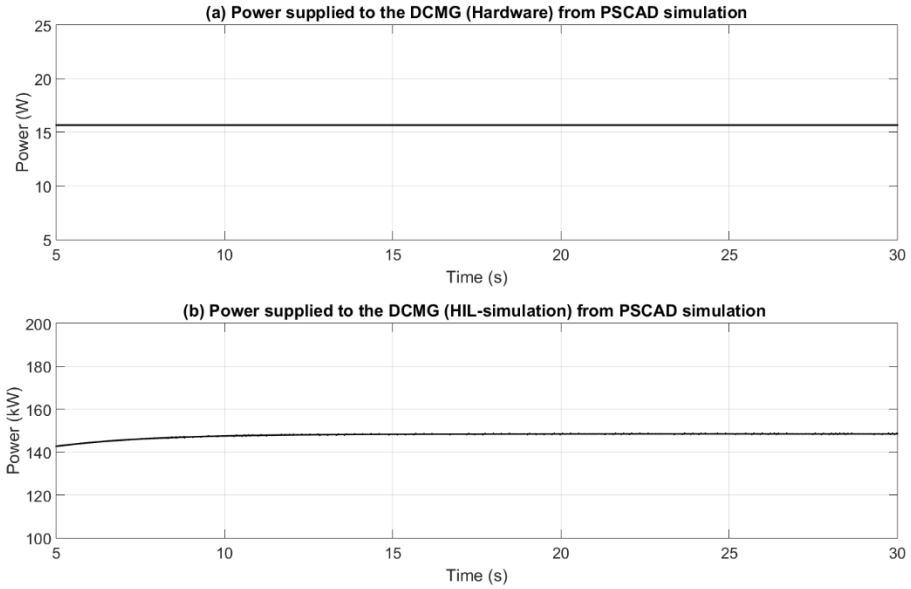

Fig.7.10: Simulation results of the hardware setup for Constant power supply to the DCMG when P_{ref}=15 W.

The results shown in Figs. 7.11 and 7.12 are for the case when P_{ref} is changed to 10 W. From Fig. 7.13 it can be observed that the input current, I_i to the PFC is the same current scaled up and passing through current controlled current source of the virtual side. Output current of the PFC, I_{link} is also shown in Fig. 7.13 (a). PSCAD simulation result is presented in Fig. 7.14 and it can be seen that the tests show similar results.

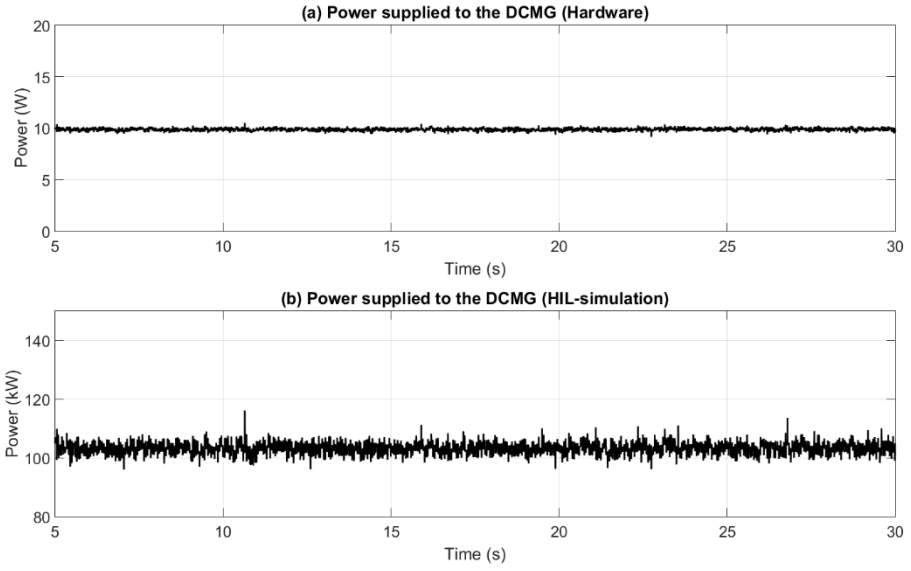

Fig.7.11: Hardware and PHIL results of Constant power supply to the DCMG when P_{ref}=10 W

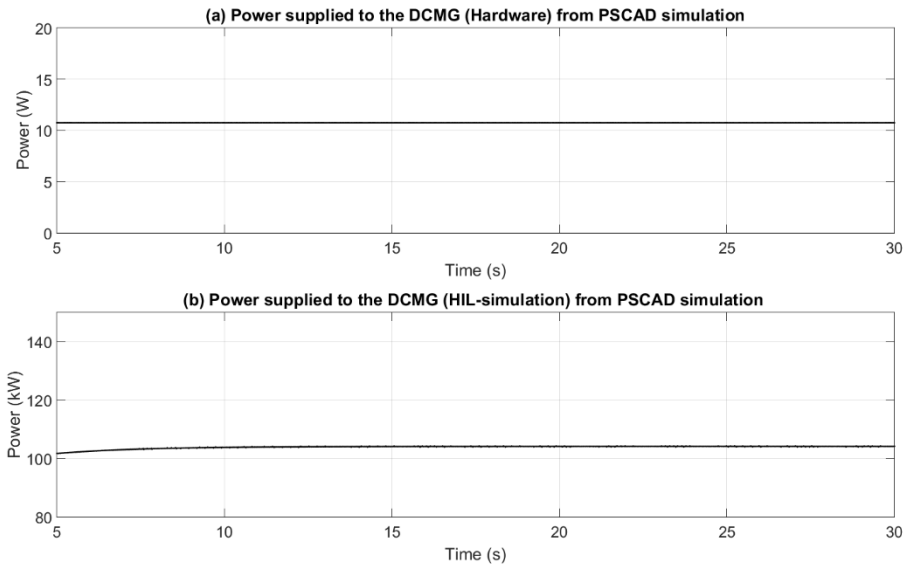

Fig.7.12: Simulation results of the hardware setup for Constant power supply to the DCMG when P_{ref}=10 W

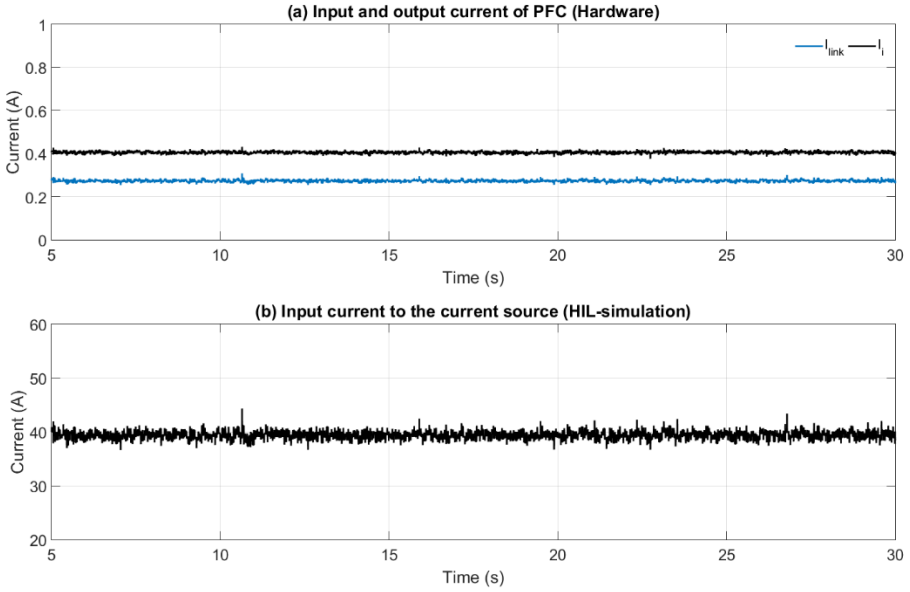

Fig. 7.13: Current measurements of PHIL

7.3.3. DCMG FROM ISLANDED MODE TO ACMG CONNECTED MODE

In this example, the DCMG is switched to ACMG connected mode from the islanded mode. Subsequently a fixed amount of power is supplied to the DCMG. In this case, DCMGs are sharing 35 W load in the islanded mode. At the beginning, the DGs in the DCMG supply the load demand.

In the connected mode, the PFC is set up to facilitate 10 W power transfer from the ACMG to the DCMG. From Fig. 7.15, it can be seen that, in order to accommodate the power coming from the ACMG, P_1 and P_2 decrease. Voltage (V_1 and V_2) and current (I_1 and I_2) magnitudes also change. The output voltage, current and power of PFC are shown in Fig. 7.16. From Fig. 7.17 it can be seen that the frequency of the ACMG decreases according to droop characteristics. The ACMG has a load of 600 kW and it increased to 700 kW to supply extra 100 kW to the DCMG. It is to be noted that a scale factor of 10000 is considered in between HIL simulation and hardware circuit.

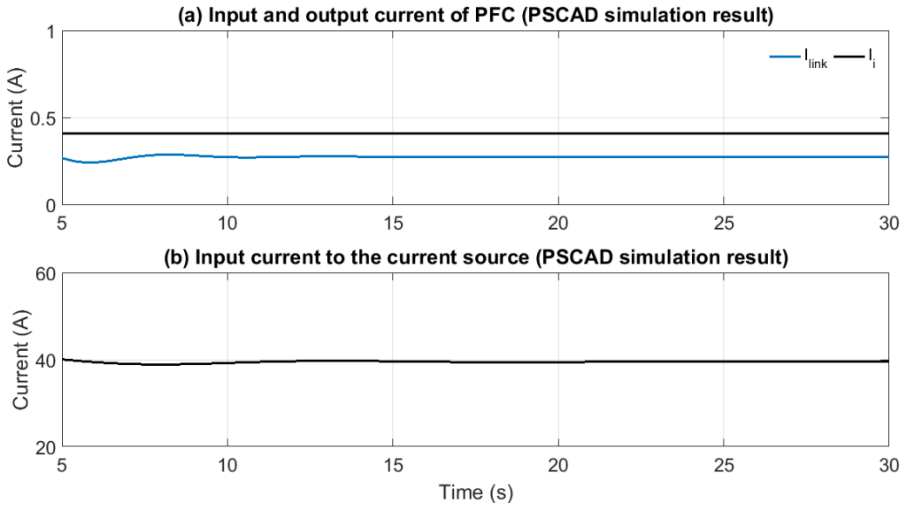

Fig.7.14 PSCAD simulation results of the current of the PHIL test

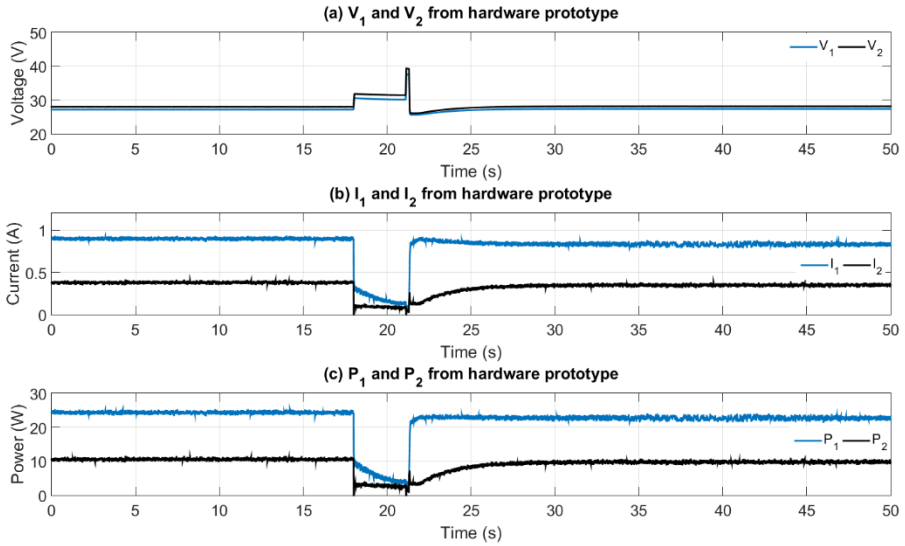

Fig. 7.15: DCMG quantities during mode transfer.

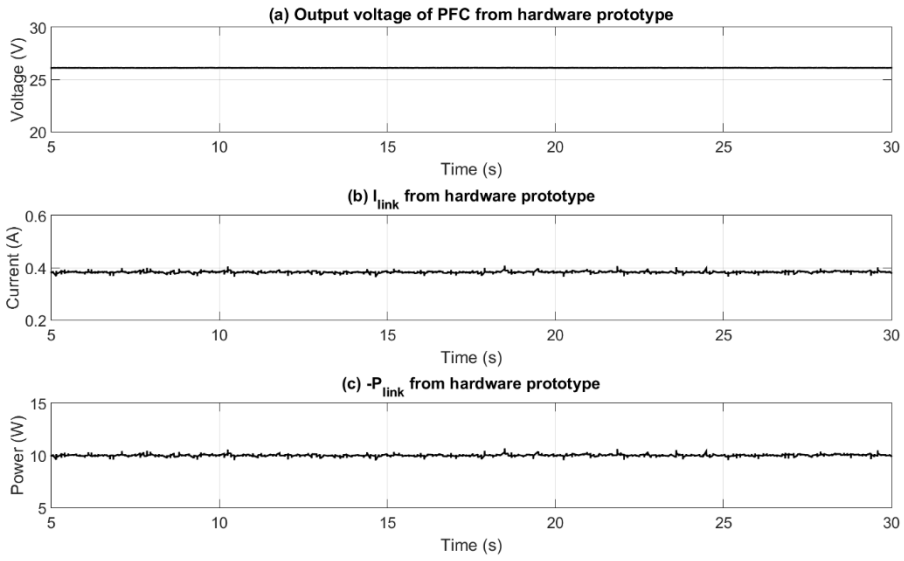

Fig. 7.16: PFC measurements during mode transfer

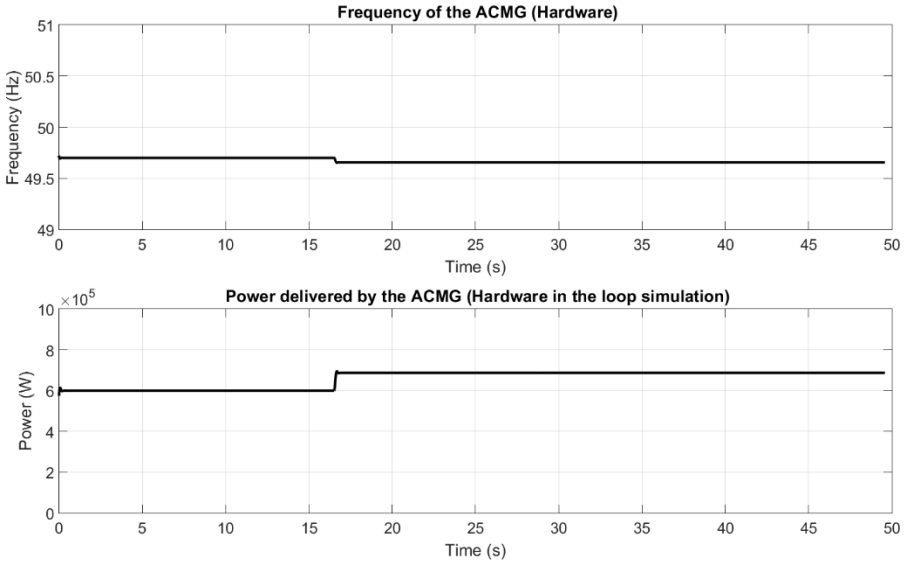

Fig. 7.17: frequency and load change during PHIL test

7.4. CONCLUSION

In this chapter, the power hardware-in-the-loop (PHIL) concept is used to test a coupled AC-DC microgrid. A power flow controller is used to facilitate a controlled power flow to the dc

loads from the ACMG. The controller draws a predefined amount of power from the ACMG and this concept is analyzed with PHIL tests. The PFC is operated in voltage control mode to support the load in DCMG. Simulation studies of the PHIL test is also presented in this chapter to support the test results.

CHAPTER 8

CONCLUSIONS

In this chapter, general conclusions of the thesis and scopes of future work are presented.

8.1 GENERAL CONCLUSIONS

1. A dc grid consists of dc-dc converters and therefore their modelling and control are of paramount importance. For the control design, two different linearization procedures are presented. One of these methods use the state transition equation to derive a discrete-time model of the converter behaviour, while the other method uses the celebrated state space averaging. Both these methods are used for deriving state feedback with integral control for regulating the output voltage. Additionally, a proportional-plus-integral (PI) is controller is also used and a method for stable gain selection has been presented. It has been shown that the state feedback controllers are more robust than the PI controller. The PI controller lacks in tracking accuracy, error minimization and mostly sensitive to any input transients. However, the PI controller is easier to implement than other two controllers in a hardware set up.

2. A linearized state space model of an autonomous DCMG, which contains two boost converters, is developed. Both V-P and V-I droop equations are considered separately. Eigenvalue analyses are conducted around a nominal operating point of the DCMG using continuous-time state space averaged state feedback controller for the boost converters. From the eigenvalue analysis, it has been observed that the power sharing is affected by the droop coefficients, and it is not sensitive with the variation of the load. However, using the droop gain selection process outlined in Chapter 3, the system is never unstable. This implies that the state feedback controller design is very robust if the droop gains are selected based on a voltage drop criterion. Finally, with the proposed control method, it is shown that proper load sharing is possible while keeping the voltage drop of this system in the defined droop range.

3. Power sharing in the ac microgrid is governed by the frequency droop equation, while the power sharing in the dc microgrid is designed with the voltage droop equation. This results in a mismatch of droop coefficient if it is intended to supply power from one side to another in an

interconnected ac-dc microgrid. Subsequently, the power flow between an ac microgrid and a dc microgrid through the interlinking converter cannot be defined through a common droop equation. Furthermore, it is also not practical to make all the DGs in the interconnected ac/dc microgrid to share power according to their ratings since ac generators are more robust and can provide substantially more power. Also, diesel generators have a minimum power rating and therefore can keep supplying to the dc loads when the ac loads are less. In light of this, three power flow controllers (PFCs) are proposed to enable a smooth power flow in an interconnected ac/dc microgrid. All three PFCs are proven to allow power flow in a controlled manner. Through the control method, the dc microgrid side voltage of the PFC is modulated, while its output voltage is held constant by the IC.

4. A linearized model for the DAB has been developed. A small signal model of the DAB has been derived based on state transition equation, where the continuity of the state variables during the switching operation has been retained. The phase shift between two H-brides of DAB is considered as the control, and this is modulated around its steady state value to facilitate power flow. For the proposed linearized model of DAB, the steady state value is obtained for any particular value of output power. A DLQR with integral controller has been designed and, as the results show, this controller is fairly robust. The veracity of the scheme is verified through extensive simulation studies.

5. Power sharing between utility and DCMGs, and between ACMG and DCMGs are interconnected through IC and PFC. It is shown that an interconnected microgrid system can be designed without defining droop coefficient of the IC. It is further shown that the power shortfall of a microgrid system can be identified by local measurements such as frequency for ac microgrid and voltage for dc microgrid. Consequently, power sharing between microgrids can be initiated after sensing power shortfall such that only the required amount of power can also be supplied to cover the shortfall.

6. For an ac/dc interconnected system, the feedback controller of the DAB regulates the power flow, ensuring no circulating current flows in the system.

7. For power reference selection in an interconnected ac/dc system, different market conditions are considered in this thesis. A fair allocation of surplus power supply between microgrids is achieved using Shapely value. Three market conditions, namely monopoly, duopoly and perfect, has been studied. Power sharing at these three market conditions is considered to

analyse the amount of power to be delivered in between the microgrids. From the study it is found that at duopoly market condition (most competitive) the price gets comparatively lower.

8. Finally, in this thesis, the power hardware-in-the-loop (PHIL) concept is used to test a coupled AC-DC microgrid. A power flow controller is used to facilitate a controlled power flow to the dc loads from the ACMG.

8.2 RECOMMENDATIONS FOR FUTURE WORKS

Few recommendations for future work are discussed below

1. In this thesis, stability analysis of a dc microgrid is performed with only two DGs and a load. In a future, stability studies can be performed with multiple DGs and loads, where the loads are also connected through dc-dc converters.

2. A dynamic model of the power transfer reference can be developed and tested. In the dynamic model different constrains can be considered.

3. Hardware test of the discrete time controller and the continuous time controller can be implemented for the dc converters. Upon successful implementation, a PHIL system using these converters can be developed and tested.

4. Since power sharing between interconnected microgrids depends on the cost of generation, it is evident that proper consideration must be given to cost minimization. Also, in case where multiple microgrids are connected together, market studies need to be performed based on the formation of coalition and through bargaining process (such as Nash Bargaining). Therefore, game theoretic models for power exchange need to be developed.

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Appendices

9.1. BUCK-BOOST DC-DC CONVERTER MODEL DERIVATION

The schematic diagram of a dc-dc buck-boost converter is shown in Fig. 9.1 (a). It contains a switch *S* that is periodically switched on and off in duty ratio control, a diode, which allows the current to flow in only one direction, and three passive elements. The converter is said to be in continuous conduction mode (CCM) if the inductor current does not need to be blocked by the diode; otherwise it is said to be in discontinuous conduction mode (DCM). We shall only use CCM for analysis.

As mentioned above, the switch *S* is switched on and off periodically as shown in Fig. 9.1 (b). If the switching frequency is *f*, then the time period between two successive switching is $T = 1/f$. From Fig. 9.1 (b), we can write the following equations

$$\begin{aligned} t_2 - t_0 &= T \\ t_1 - t_0 &= DT \\ t_2 - t_1 &= (1-D)T \end{aligned} \tag{9.1}$$

where D, $0 \le D \le 1$, is called the duty ratio.

The equivalent circuit when the switch is closed is shown in Fig. 9.1 (c) and when the switch is open is shown in Fig. 9.1 (d). Let us the state vector as $x = [V_0 \;\; i_L]^T$. Then the state space equation when the switch is closed is

$$\dot{x} = A_1 x + B_1 V_{dc} \tag{9.2}$$

and when the switch is open is

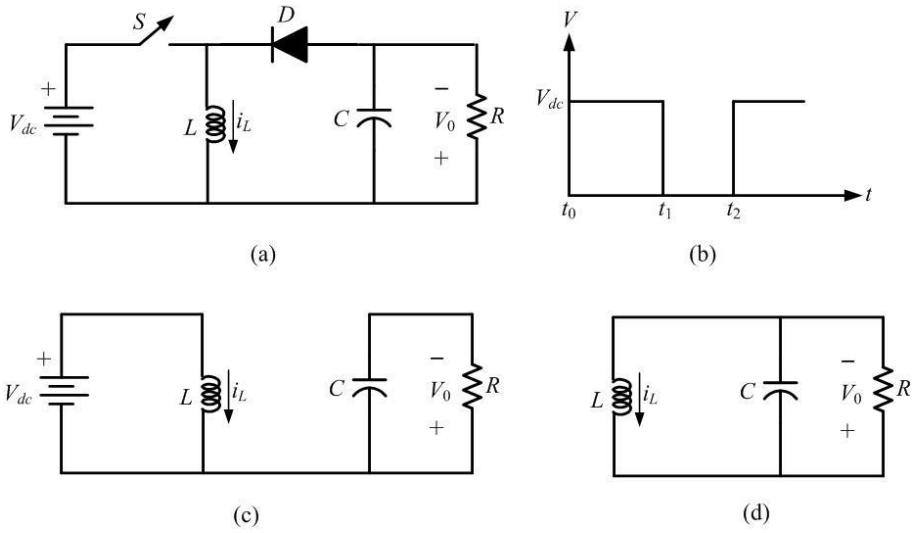

Fig. 9.1. (a) Schematic diagram of a buck-boost converter; (b) its switching sequence; equivalent circuit when the switch (c) is closed and (d) is open.

$$\dot{x} = A_2 x \tag{9.3}$$

where

$$A_1 = \begin{bmatrix} -1/RC & 0 \\ 0 & 0 \end{bmatrix}, A_2 = \begin{bmatrix} -1/RC & 1/C \\ -1/L & 0 \end{bmatrix}, B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix}$$

The output equation for both these cases is

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} x = Cx \qquad (9.4)$$

Since V_{dc} is constant, the solution of the state equation (9.2) is given by

$$x(t_1) = e^{A_1(t_1-t_0)}x(t_0) + \left\{\int_{t_0}^{t_1} e^{A_1(t_1-\tau)}d\tau\right\}B_1V_{dc} \tag{9.5}$$

Similarly, the solution of (9.3) is

$$x(t_2) = e^{A_2(t_2-t_1)}x(t_1) \tag{9.6}$$

Substituting (9.5) in (9.6), we get

$$x(t_2) = e^{A_2(t_2-t_1)}e^{A_1(t_1-t_0)}x(t_0) + e^{A_2(t_2-t_1)}\left\{\int_{t_0}^{t_1} e^{A_1(t_1-\tau)}d\tau\right\}B_1V_{dc} \tag{9.7}$$

Unfortunately the matrix A_1 is singular and is therefore non-invertible. However since this is essentially a diagonal matrix with one of the diagonal elements being zero, we get

$$\begin{aligned}\int_{t_0}^{t_1} e^{A_1(t_1-\tau)}d\tau &= \int_{t_0}^{t_1}\begin{bmatrix} e^{-(t_1-\tau)/RC} & 0 \\ 0 & e^0 \end{bmatrix}d\tau = \begin{bmatrix} -RCe^{-(t_1-\tau)/RC} & 0 \\ 0 & \tau \end{bmatrix}\Bigg|_{t_0}^{t_1} \\ &= \begin{bmatrix} -RC\left\{1-e^{-(t_1-t_0)/RC}\right\} & 0 \\ 0 & t_1-t_0 \end{bmatrix}\end{aligned} \tag{9.8}$$

Using the definition of the duty ratio given in (9.2), (9.7) and (9.8) can be combined as

$$x(t_2) = e^{(1-D)TA_2}e^{DTA_1}x(t_0) + e^{(1-D)TA_2}\begin{bmatrix} -RC\left\{1-e^{-DT/RC}\right\} & 0 \\ 0 & DT \end{bmatrix}B_1V_{dc} \tag{9.9}$$

Linearized Model

In this section, we shall derive a linearized model that relates two successive swathing instants, i.e., t_0 and t_2. For linearization, we define the following state and input variables

$$x = x_0 + \Delta x, \quad D = D_o + \Delta D \tag{9.10}$$

where the subscript 0 denotes the steady state values around which the linearization takes place and Δ denotes its perturbation. In the steady state, the values of the state variables remain the same at the end of each switching cycle, i.e., $x(t_2) = x(t_0)$. We can obtain the steady state description from the solution of the state equation (9.9) as

$$x_0 = \left[I - e^{(1-D_0)TA_2} e^{A_1 D_0 T}\right]^{-1} e^{(1-D_0)TA_2} \begin{bmatrix} -RC\left\{1 - e^{-D_0 T/RC}\right\} & 0 \\ 0 & D_0 T \end{bmatrix} B_1 V_{dc} \tag{9.11}$$

9.2. PSCAD MODEL OF CHAPTER 3

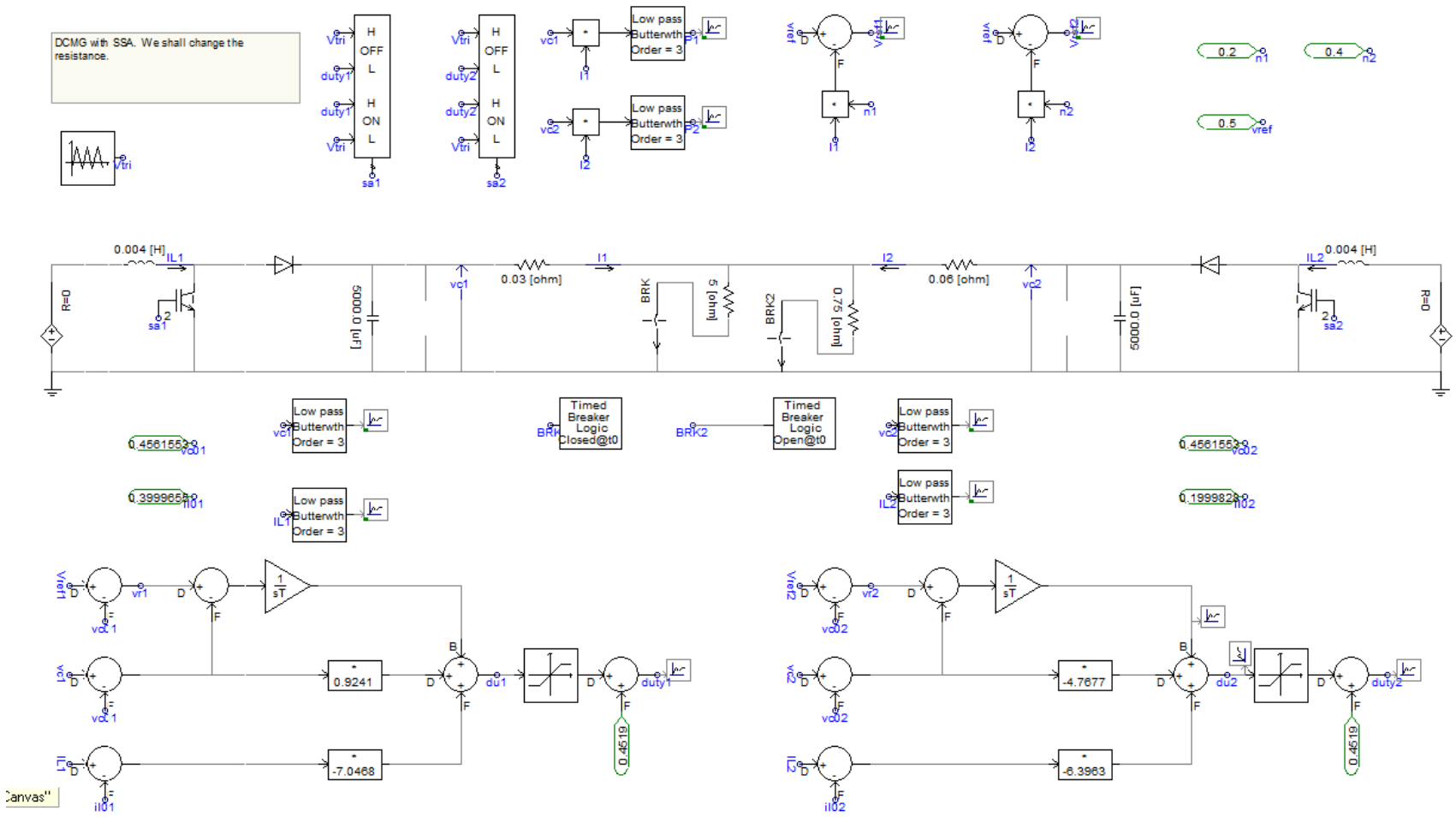

Fig 9.2. PSCAD model of the DCMG discussed in Chapter-3

9.3. PSCAD MODEL OF CHAPTER 4 AND 5

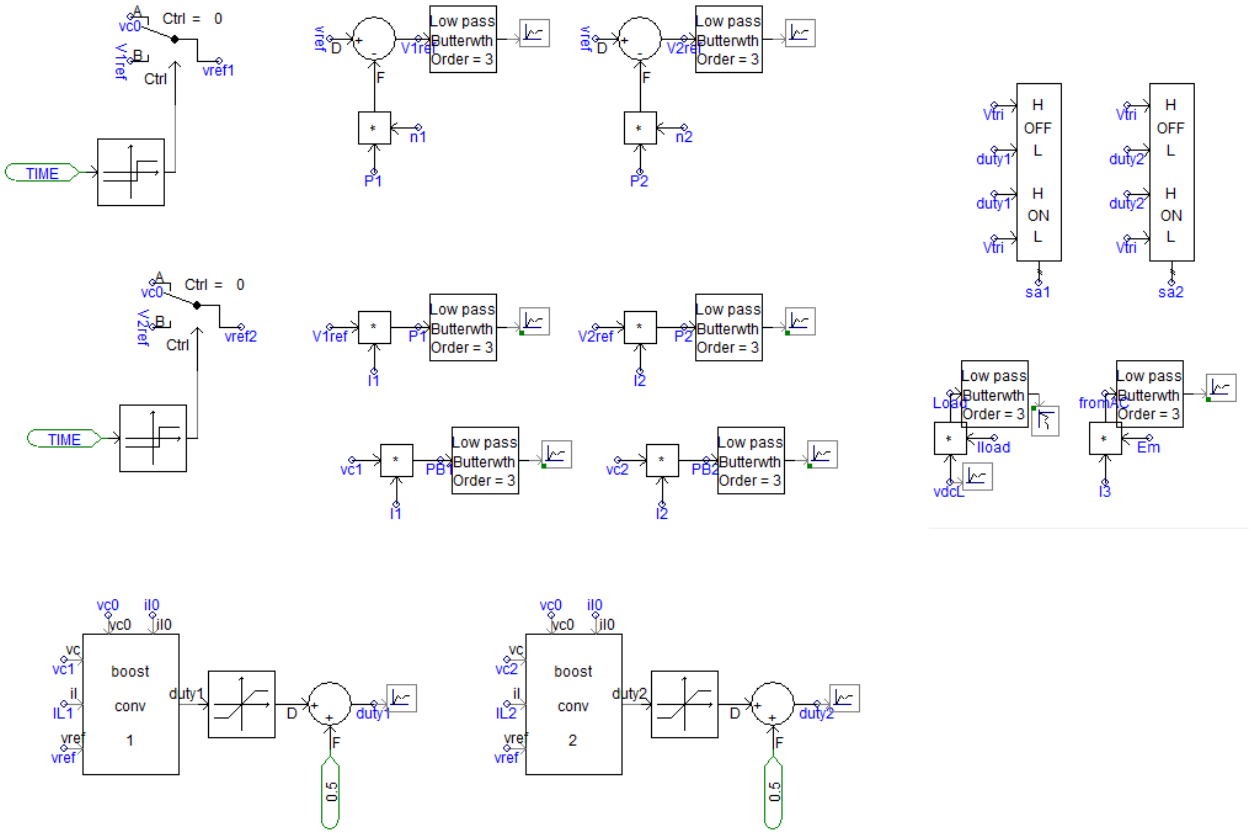

Fig 9.3. DCMG controllers of the PSCAD model of the utility connected DCMG with PFC

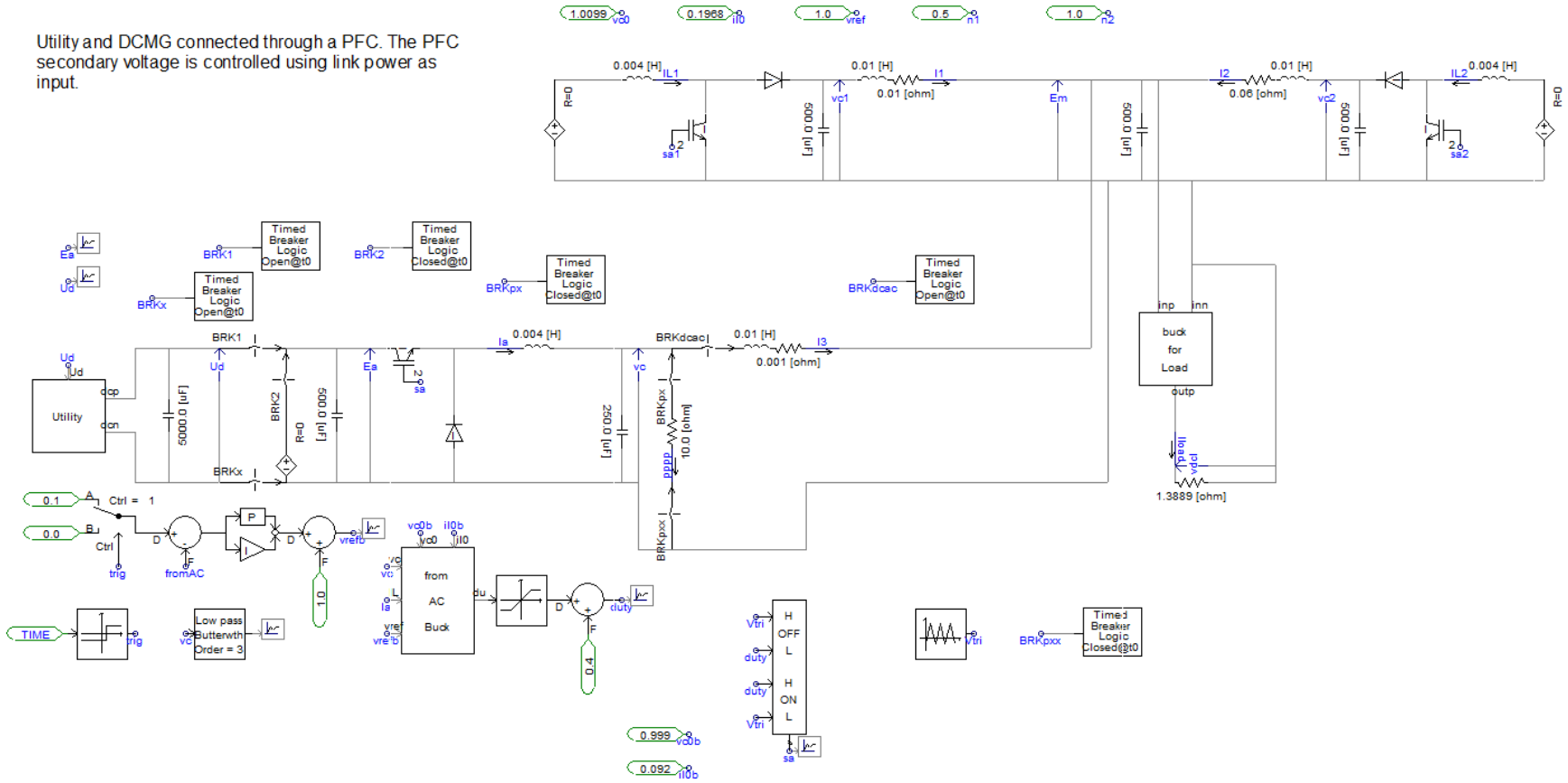

Fig 9.4. PSCAD model of the utility connected DCMG with PFC

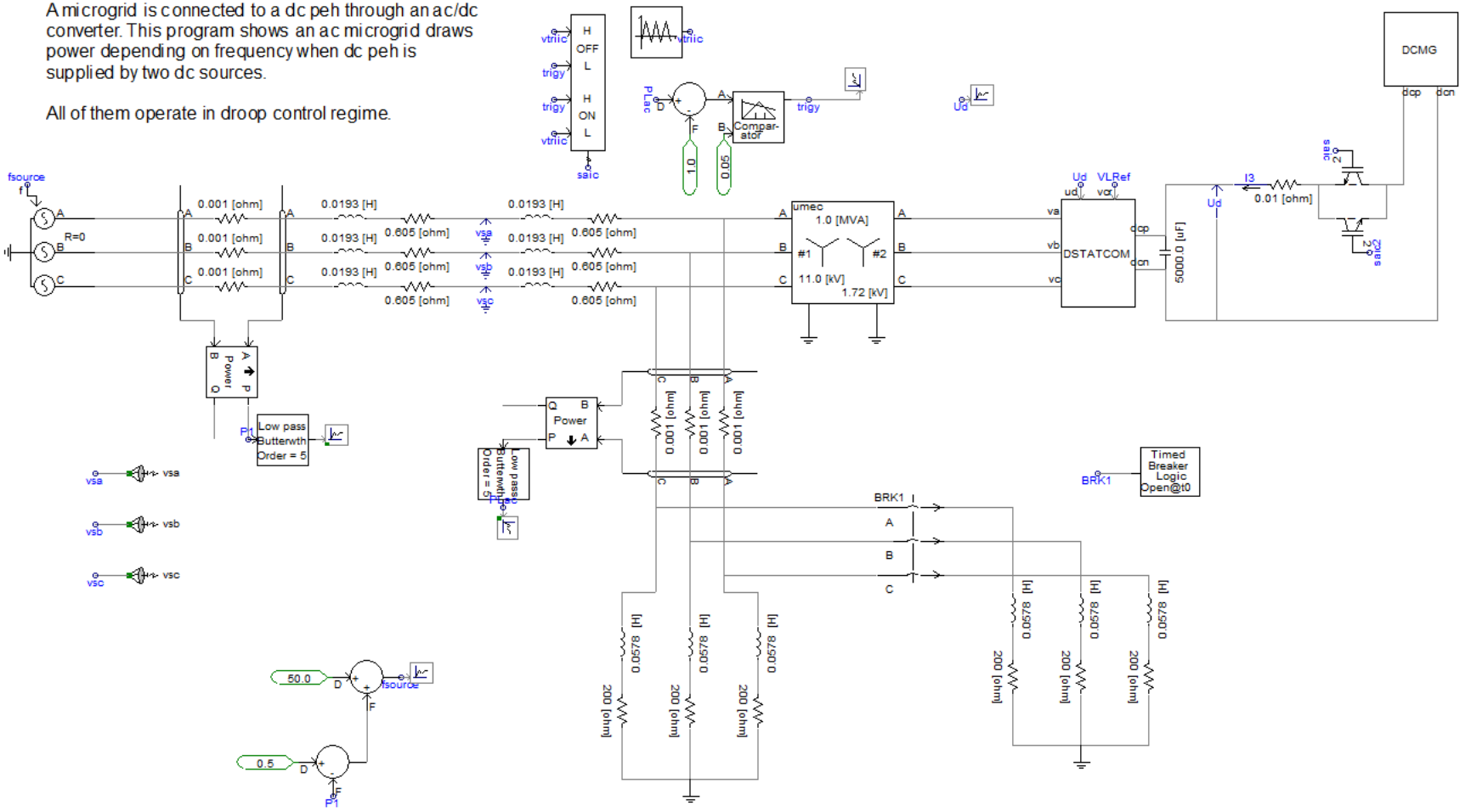

Fig 9.5. PSCAD model of the utility connected DCMG with bidirectional switch

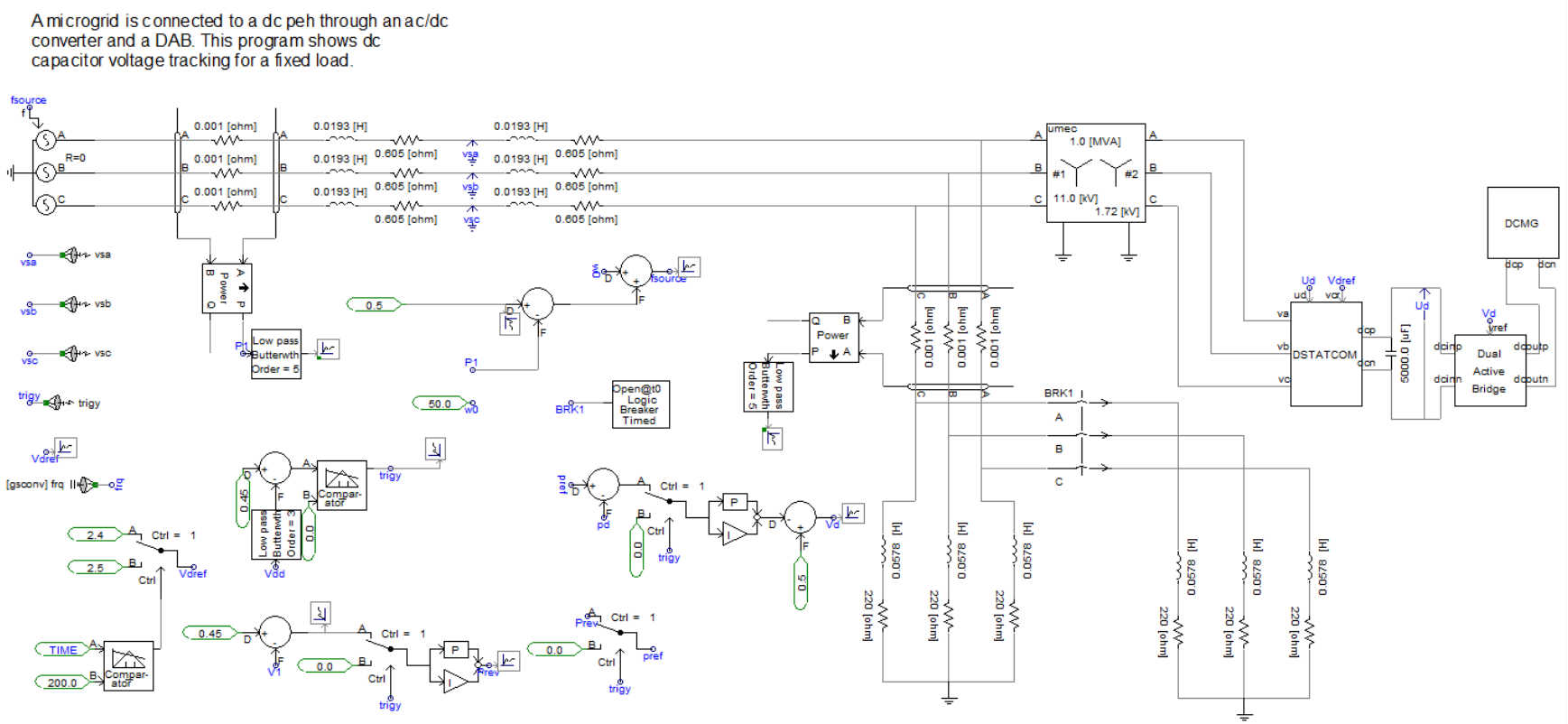

Fig 9.6. PSCAD model of the utility connected DCMG with DAB

9.4. PSCAD MODEL OF CHAPTER 6

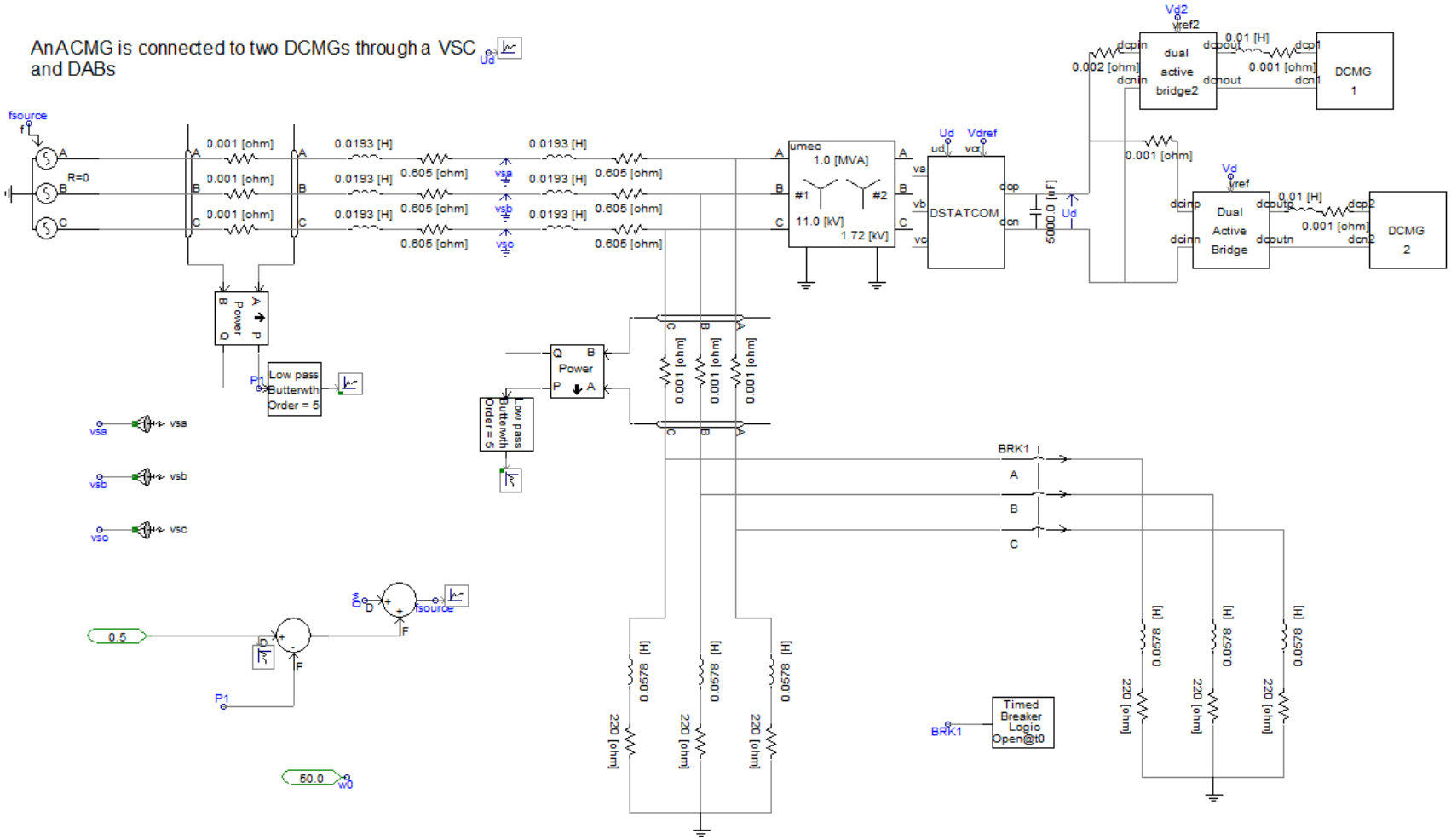

Fig 9.7. Power Sharing in a AC/DC Microgrid with Multiple DC Sub-grids

9.5. MATLAB/SIMULINK MODEL OF CHAPTER 7

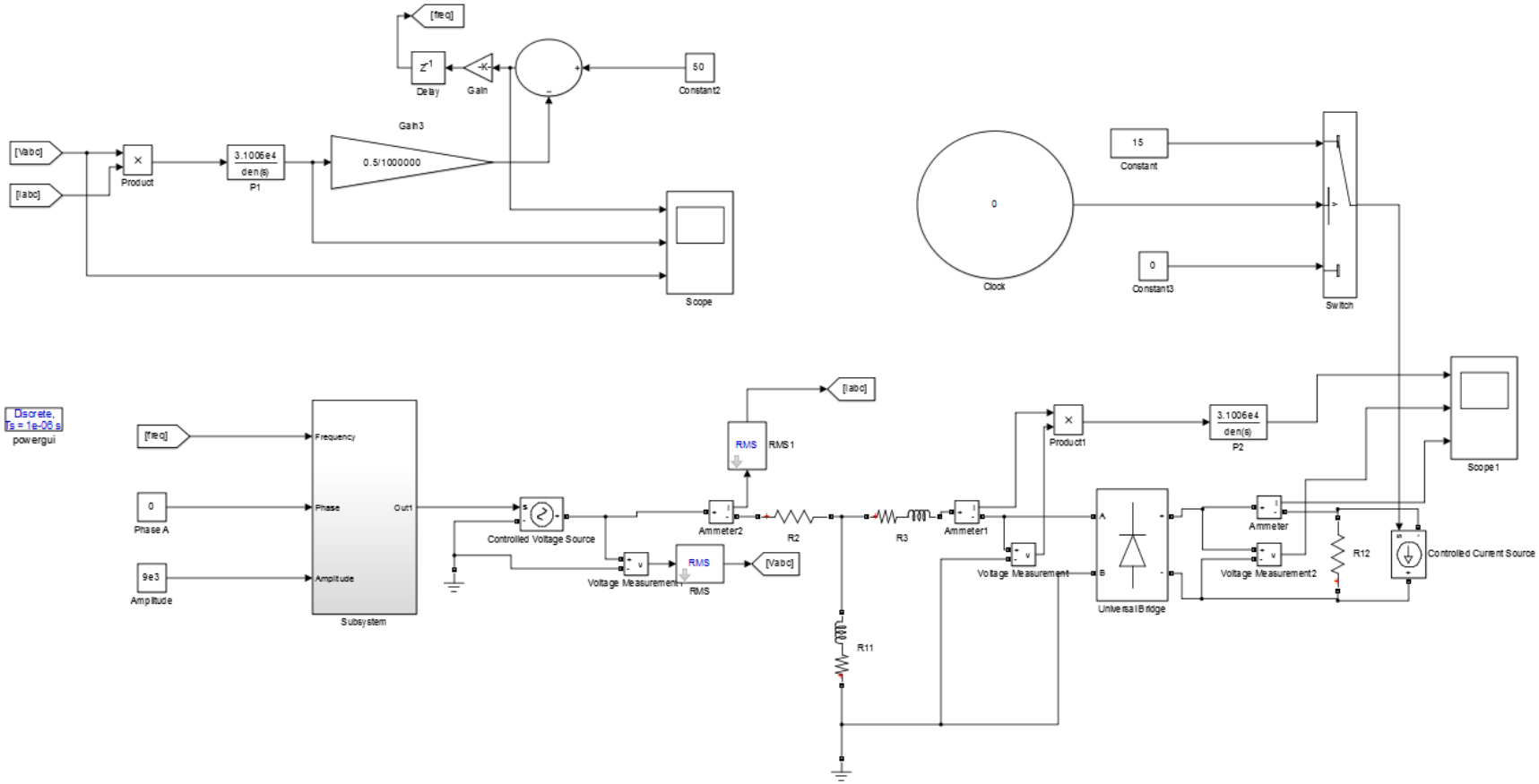

Fig 9.8. MATLAB/Simulink model of the PHIL test

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1. Research

Project Title:	Operation and Control of DC Microgrid		
Project identifier (if applicable)			
Principal Investigator	Amit Jyoti Datta		
Other named investigator/s[#]	Prof. Arindam Ghosh	**Role**	Principal supervisor
Other researcher/s[#]	Dr. Sumedha Rajakaruna	**Role**	Co-supervisor

[#] Insert additional rows if required

2. Publications/Outputs – the intended outputs from the above research are identified below

Pub[#]	Description (e.g. method paper)	Publication Type (Conference, journal article etc)
1	Bidirectional Power Sharing in an AC/DC system with a Dual Active Bridge Converter	IET Generation, Transmission & Distribution
2	Power sharing in a hybrid microgrid with bidirectional switch	Power & Energy Society General Meeting, 2017 IEEE, pp. 1-5. IEEE, 2017
3	Power sharing and management in a utility connected DC microgrid.	Australasian Universities Power Engineering Conference (AUPEC), 2017, pp. 1-6. IEEE, 2017

[#] Insert additional rows if required

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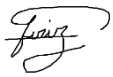
Prof. Firuz Zare School of ITEE, University of Queensland, St Lucia, Brisbane, Qld, Australia		04/03/2019

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