Department of Electrical and Computer Engineering

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Vector Control of Multilevel Cascaded H-Bridge Inverter Based Static Synchronous Compensator with Simultaneous Functionalities

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Declaration

To the best of my knowledge and belief this thesis contains no material previously published by any other person except where due acknowledgment has been made.

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university.

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Abstract

In recent years, the STATic Synchronous COMpensator (STATCOM) has gained popularity among many utilities for solving power quality problems in distribution substations. The performance of power factor correction and harmonic mitigation exceeds that of the other popular controller, the shunt-connected Flexible Alternative Current Transmission System (FACTS). There are many types of topologies of STATCOM found in the literature, of which the Multilevel Cascaded H-bridge Inverter (MCHI) is the most adaptable and energy efficient power inverter topology. The main goal of this thesis is to define a control scheme and its transfer function in order to achieve low-switching frequency and high-bandwidth power control of MCHI. The controller of STATCOM system is to provide vector control with simultaneous functionalities; namely, (i) reactive power or Voltage-Ampere Reactive (VAR) compensation and (ii) active harmonic filtration at the Point of Common Coupling (PCC) under balanced loading conditions. To accomplish this, mathematical equations for a STATCOM system is derived in dq-coordinates based on Park's transformation. Then, the designed equations are used to calculate appropriate values of the controller's gain parameters for realizing the cascade Pulse Width Modulation (PWM) STATCOM with various voltage and current ratings. After that, a new control scheme is developed for the proposed STATCOM system to attain the above-mentioned simultaneous functionalities. Lastly, the performance of the proposed control scheme is verified through simulation and numerical analysis using MATLAB-Simulink. The recorded improved power factor is up to 0.97 and an average 5.5 % Total Harmonic Distortion (THD) filtration with the total average of 31.87 % compensation percentage.

Keywords: Control schemes, Multilevel Cascaded H-bridge Inverter (MCHI), STATic Synchronous COMpensator (STATCOM), Flexible Alternative Current Transmission System (FACTS)

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Nomenclature

AC	Alternative Current
APOD-PWM	Alternate Phase Opposition Disposition-Pulse Width Modulation
BESS	Battery Energy Storage System
CB-PWM	Carrier Based-Pulse Width Modulation
CSI	Current Sources Inverter
DC	Direct Current
DSP	Digital Signal Processor
EPLL	Extended Phase Locked Loop
FACTS	Flexible Alternative Current Transmission System
FC-TCR	Fixed Capacitor-Thyristor Controlled Reactor
FPGA	Field Programmable Model Gate Array
IGBT	Insulated-Gate Bipolar Transistor
IPD-PWM	In-Phase Disposition-Pulse Width Modulation
LS-PWM	Level Shifted-Pulse Width Modulation
MCCI	Multilevel Capacitor-Clamped Inverter
MCHI	Multilevel Cascaded H-Bridge Inverter
MDCI	Multilevel Diode-Clamped Inverter
MPC	Model Predictive Control
NPC	Neutral-Point Clamped
PCC	Point of Common Coupling
PF	Power Factor

PI	Proportional Integral
PLC	Programmable Logic Controller
POD-PWM	Phase Opposition Disposition-Pulse Width Modulation
PSO	Particle Swarm Optimization
PS-PWM	Phase Shifted-Pulse Width Modulation
SDBC	Single-Delta Bridge Cells
SHE-PWM	Selective Harmonic Elimination Pulse Width Modulation
SRF	Synchronous Reference Frame
STATCOM	STATic Synchronous COMpensator
SVC	Static VAR Compensator
SVM	Space Vector Modulation
TCR	Thyristor Controlled Reactor
THD	Total Harmonic Distortion
TSC	Thyristor Switched Capacitor
TSC-TSR	Thyristor Switched Capacitor-Thyristor Controlled Reactor
TSR	Thyristor Switched Reactor
VAR	Voltage-Ampere Reactive
VSI	Voltage Source Inverter

List of Contents

List of Figures

List of Tables

Chapter 1

Introduction

The ever-increasing power quality issues arising from the growing complexity of loads, such as motor speed drive systems, Programmable Logic Controllers (PLC), rectifiers, electronic ballasts, computers etc., have caused great adverse effects in the power industry. These include low-Power Factor (PF), high Total Harmonic Distortion (THD), excessive reactive power consumption, and phase unbalance imposition onto the distribution system [1]. Nevertheless, with proper power flow controls such as providing reactive power compensation, these problems can be mitigated. Conventional reactive power or Voltage-Ampere Reactive (VAR) compensation methods, such as Static VAR Compensators (SVC), prove to have many drawbacks in terms of its power rating, response, accuracy, and cost. The discovery of inverter-based Flexible Alternative Current (AC) Transmission System (FACTS), specifically the Multilevel Cascaded H-Bridge Inverter (MCHI) based, grid-tied, STATic Synchronous COMpensator (STATCOM), offers substantial advantages over its conventional counterparts and has resulted in massive research in the last two decades.

1.1 FACTS and Shunt-connected Controllers

FACTS technology was first presented by Gyugyi in the late 1980s [2] and later by Hingoroni in 1991 [3, 4] with the aim of enhancing the value of electrical power based on the gate turn-on property of thyristor devices. Both FACTS and conventional power system controllers such as tap-changing and phase-shifting transformers have the same functionality: acting as devices for solving power quality issues. But FACTS are preferable in power transmission systems as FACTS deliver faster response rates, higher reliability, better adaptability and more timely effectiveness compare to conventional controllers [5]. According to IEEE, the word “FACTS” covers a full range of power electronic controllers as quoted below [6]:

"*A power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability*."

FACTS controller can be categorized as follows [5, 7] and is further illustrated in Figure 1.1:

a) Shunt controllers are where current, $i_{c,}$ is injected into the power system at the Point of Common Coupling (PCC) either by variable shunt impedance connected to the line voltage or by power electronics based variable source, or both. In other words, it compensates the reactive power by injecting or absorbing the current to or from the system.
b) Series controllers are where voltage, $V_{c,}$ is injected in series with the line either by variable series impedance multiplied with the current flow through it or by power electronics based variable source. In other words, it provides reactive power if the voltage obtained is in phase quadrature, or else, it deals with active power.
c) Combined series-series controllers are where the independent series VAR compensation takes place in each line and the real power is transferred among the lines through the Direct Current (DC)-power link.
d) Combined series-shunt controllers are where both current, $i_{c,}$ and voltage, $V_{c,}$ is injected into the power system at PCC. This allows interchange of real current between the controllers through a DC-power link. In other words, it is a combination of series and shunt controllers in order to obtain the characteristics of both controllers.

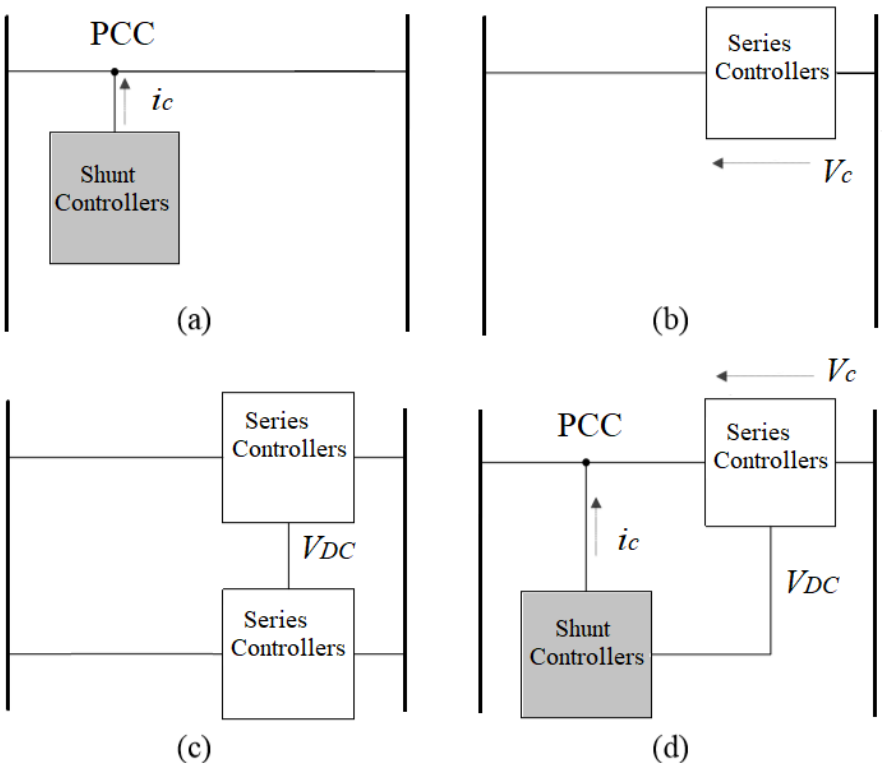

Figure 1.1 Types of FACTS controller: (a) Shunt controllers, (b) Series controllers, (c) Combined series-series controllers, and (d) Combined series-shunt controllers

Shunt controllers are the most optimum option in terms of cost for VAR compensation and harmonic filtration [8]. It has been widely known for improving the transient stability of the power system and damping the power oscillations at the PCC by injecting a combination of active and reactive currents [7].

For these reasons, the following subsections present the functions of the Shunt-connected FACTS controllers.

1.1.1 First Generation of Shunt-connected FACTS Controllers

Supplying the required reactive current into the power system via reactive impedance which consists of capacitor and inductor banks that are controlled by thyristor switches are the main function of the first generation, shunt-connected, FACTS controllers [9]. These controllers

are designed in such a way that only variable reactive current is supplied or consumed when the condition of injected reactive current is always in phase quadrature to grid voltage. When an under-load situation occurs, the shunt-connected inductors are ready to operate as an overvoltage reducer, whereas during an over-load situation, shunt-connected capacitors are responsible to maintain the rated voltage in the grid [10].

Different designs of the first generation of shunt-connected FACTS are addressed and illustrated in the Figure 1.2 below [7]:

(a) Thyristor Controlled Reactor (TCR) and Thyristor Switched Reactor (TSR) with both having the effective reactance of a fixed inductor. The difference is that the effective reactance of TCR is continuously changing, with respect to partial conduction of the bidirectional thyristor valve with the control over firing delay angle, and the effective reactance for TSR is varied in steps by full- or zero-conduction operation of the bidirectional thyristor valve.

(b) Thyristor Switched Capacitor (TSC) is having a fixed capacitor, where the effective reactance is varied in steps by fully closing or opening the bidirectional thyristor valve.

(c) Fixed Capacitor-Thyristor Controlled Reactor (FC-TCR) produces the required VAR output by having the generation of constant capacitive VAR be countered by the variable VAR absorption of the TCR.

(d) Thyristor Switched Capacitor-Thyristor Controlled Reactor (TSC-TSR) and SVC are both a combination of 2 or 3 types of the TSC, TSR, and TCR controllers where it enables the adjustment of output in order to exchange between capacitive or inductive currents of the power system which is mainly to have control over the grid voltage.

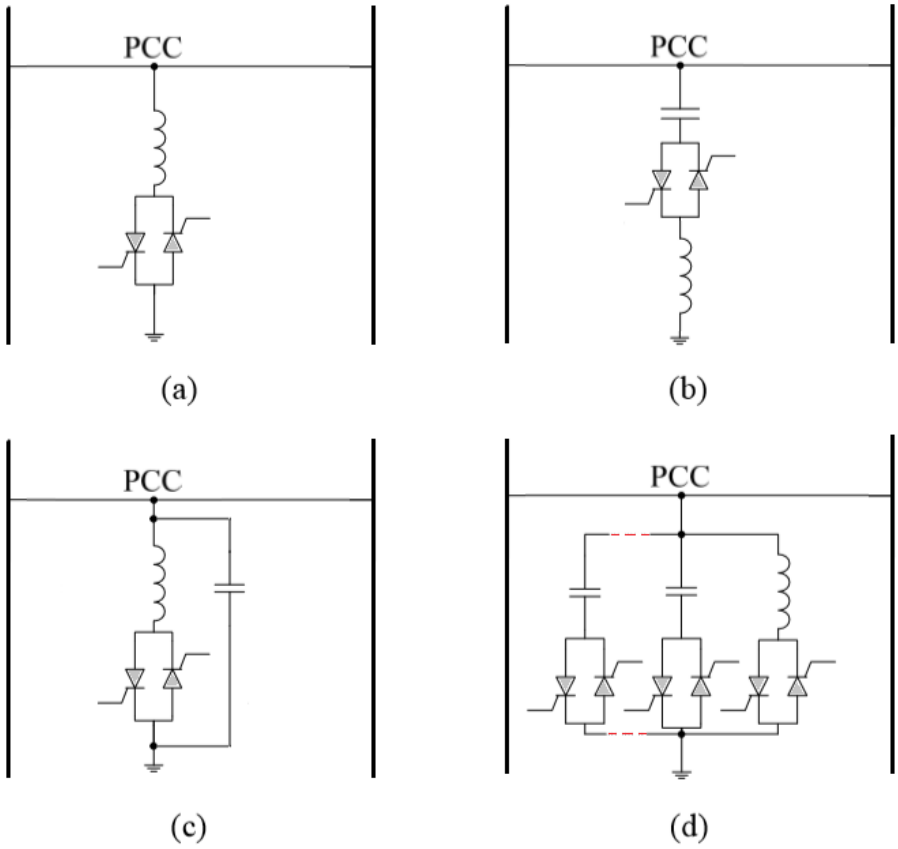

Figure 1.2 Illustration of different shunt-connected controllers: (a) TCR or TSR, (b) TSC, (c) FC-TCR, and (d) TSC-TCR or SVC

With the limitation of the slow response of switching capacitors, the SVC is unable to trace the highly dynamic reactive current reference. SVC can only achieve its optimum performance when the rate of change is hundreds of fundamental cycles or a slow rate of change [7]. Functions and advantages of static inverters-based shunt-connected FACTS controllers are presented in the next subsection.

1.1.2 Second Generation of Shunt-connected FACTS Controllers

With the rising of high-power static inverters in power system applications especially power line transmission, the second generation of shunt-connected FACTS controllers which control the current of the power system by providing common compensation characteristics has become more popular. Comparing to the SVC in the first generation of

shunt-connected FACTS controllers, Voltage Source Inverter (VSI) based STATCOM is better version of SVC which consists of a Pulse Width Modulation (PWM) switching inverter with a capacitor connected at the DC-link as shown in Figure 1.3, in terms of having a lower rating of capacitors and invertors as well as diodes and switches [7]. The required reactive current flowing to the power system through the coupling inductor or transformer is the reference current for STATCOM to rapidly adjust its AC output voltage.

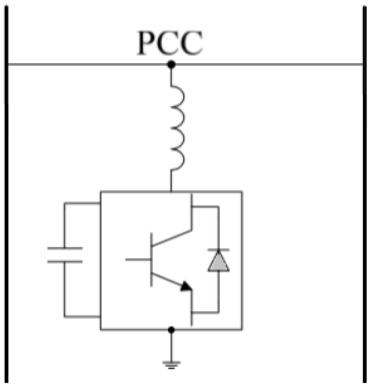

Figure 1.3 Single-line diagram of VSI based STATCOM

Summary of advantages of STATCOM compared to SVC under same comparison circumstances are presented as below [11-14]:

a) High stability of STATCOM operation throughout its full output current range from maximum capacitive to maximum inductive including during the event of low voltage in the AC system. In another words, STATCOM continue to absorb the required real current from the AC systems in order to supply its operating losses even if the voltage of the AC system is as low as 0.2 p.u. [7].
b) STATCOM provide better active compensation by exchanging real power to increase the efficiency of the power system and reduce the chances of having power outages. This is due to its fast response rate and high consistency in regulating the transient margin.

c) With proper thermal rating design, which reduces the passive element, STATCOM promises shorter overload time in the power system as well as more cost-effectiveness when compared to SVC.

Working principle of shunt connected STATCOM are documented in the next subsection.

1.2 Working Principle of STATCOM

STATCOM system consists of three main key components as follows and as illustrated in Figure 1.4:

a) Self-commutated VSI that consists of power semiconductors and Battery Energy Storage System (BESS) which is controlled to absorb and distribute power from or into the AC system.
b) Coupling inductor, Z_f, which interfaces the STATCOM with the power system as well as reduces the harmonic currents.
c) Control system which performs feed-forward or feedback control per measured variables as well as produces PWM-modulation switching signals to drive the power inverter.

The STATCOM is shunted to the power system by passing through Z_f, which is provided by the leakage inductance of each phase of the coupling transformer at the PCC [7].

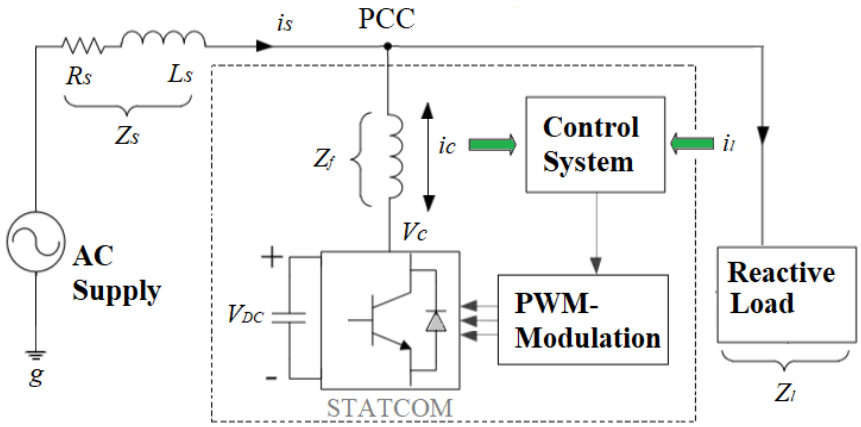

Figure 1.4 Single-line block diagram of a basic STATCOM system

According to Kumar [15], the required inductance of the Z_f is affected by THD of the STATCOM output current, i_c, with respect to the operating range of the inverter. Besides that, reviews regarding the relationship of switching frequency and amplitude modulation ratio on iron loss for coupling transformers were presented by Liu et al [16] and Boglietti et al [17]. Both studies show that the effect of switching frequency on iron loss was insignificant or negligible, while on the other hand, modulation ratio was highly responsible for the iron loss. Iron loss reduces as the amplitude of the harmonic components decreases which is directly caused by a relative increase in amplitude modulation ratio.

The main part of the STATCOM would be VSI where it starts off with a two-level inverter, which is also known as a six-pulse inverter that engages turn-off capability semiconductor devices in three-phase systems. Later with the introduction of multilevel inverters, multiple six-pulse inverters were cascaded through different configurations of transformer connections to reduce harmonic currents and increase the output power of the STATCOM system [18-21]. Those large-size and inefficient transformers are not economical and contribute up to 70 % of the total system losses [22], which is caused by the magnetizing characteristic of the transformer and surge overvoltage due to saturation of the transformers in transient states [23].

As the technology of power semiconductors continues to grow, multilevel VSI topologies has become more reliable compared to the conventional VSI in terms of their applications in FACTS technology. MCHI with separated DC capacitors has been nominated to be the most feasible topology amongst many other novel multilevel inverter topologies in terms of catering to different applications and requirements of STATCOM systems.

The review of problem statements when it comes to introducing MCHI based STATCOM during the early stage are presented in the next section.

1.3 Problem Statements

There is a huge drawback in the form of poor transient performance when choosing a Proportional Integral (PI) controller for the control system. This drawback is also known as high steady-state error with respect to its dynamic response and integral function. In other words, zero steady-state error can be achieved by having high integral gain at the cost of poor dynamic response and vice versa. But this issue can be mitigated to achieve high bandwidth and good harmonic performance by just stacking more H-bridge inverters to form a higher level of multilevel inverter [24]. In order to acquire good dynamic response as well as low steady-state error in STATCOM system, both low integral gain and low switching frequency can be employed through MCHI. On top of that, other issues such as bulky, heavy and expensive line frequency transformers can be avoided with the integration of MCHI based STATCOM into the power system [25, 26].

Much research and many studies over different control schemes for MCHI based STATCOM have been carried out in the past three decades. All studies focused on the dynamic responses and transient responses in STATCOM system to compensate VAR [23-34]. Among all the control schemes, PI-controllers have been nominated by the majority of researchers as the easiest way to do control in the feedback loops. However, some research work has also shown that the PI-controllers are unable to precisely track down the command values [27] because of parameter variations and operating points [28], which leads to poor transient response [29] and causes STATCOM system to be unstable [30]. Furthermore, another issue that occurs when solving poor transient response in PI-controllers was high switching frequency such as 5 kHz [26], 10 kHz [27], and 12 kHz [31]. Besides that, the integral gain parameters are case dependent and not specifically defined [32-33]. As the levels of multilevel inverters increase, the complexity of STATCOM formulation in control systems increase as well, which prompts more problems related to unbalanced voltage [24, 34]. Thus, the computational burden of the Digital Signal Processor (DSP) greatly increases and this causes the overall STATCOM performance, in terms of its stability and reliability, to decrease.

1.4 Objectives

The main aim of this research work is to provide power compensations and harmonic filtration at the PCC using the MCHI based grid-tie STATCOM system. All the proposed control schemes have been implemented and integrated together via derivation of mathematical models to achieve the above-mentioned features. The objectives of the research are as follows:

a) Develop a control strategy based decoupling feed-forward current vector controller to enhance transient performance of STATCOM by providing reactive current compensation and active harmonic filtration, taking into consideration the response time and the compensation accuracy.

b) Implement digital control algorithms that allow MCHI to operate in different manners without changing the MCHI's physical structure.

c) Validate the proposed control strategy using MATLAB-Simulink to resemble the real STATCOM system.

1.5 Thesis Contributions and Significance

The key contribution of this research work is summarized as follows:

a) This dissertation proposed an innovative, simple, intuitive and practical control strategy based on the decoupling feed-forward current vector controller for reactive as well as active harmonic filtration with improved response time and higher compensation accuracy.
b) This dissertation successfully implemented the designed digital control algorithm to allow MCHI to operate in different manners without the need of changing its physical structure.
c) This dissertation presented the detailed modelling of the STATCOM with its associated proposed control scheme and validated it using MATLAB-Simulink to resemble the real STATCOM system.

Research significance is listed as follows:

This research work focused on reactive current compensation and active harmonic filtering using a MCHI-based, grid-tied, STATCOM system. A designed control strategy based on the instantaneous current control method incorporating CB-PWM and PI-controller had been developed using MATLAB-Simulink. The developed control scheme was able to achieve fast dynamic response, good transient and steady-state responses, and produce high quality output voltage waveforms with an acceptable switching frequency value.

1.6 Thesis Outline

The dissertation is organized as follows:

Chapter 1 presented the problem statements and the objectives of the research with some introduction of FACTS and Shunt-connected Controllers as well as the working principle of STATCOM.

Chapter 2 presented the fundamental concepts associated with the VSI based STATCOM including an overview of various configurations of multilevel VSIs. Since the fundamental focus of this dissertation is on MCHI based STATCOM, therefore the common multilevel PWM techniques and control schemes for reactive current compensation as well as active harmonic filtration have been documented in this chapter.

Chapter 3 presented the mathematical modeling derivation of the designed control scheme framework.

Chapter 4 presented the selected simulation results which shows the implementation and validation of the designed controller.

Chapter 5 gave the conclusion and recommendation for future works followed by several appendices containing information on the derivation of controller and associated analysis.

Chapter 2

Literature Review

In this chapter, literature on self-commuted inverters structural of STATCOM system including different multilevel inverter topologies were reviewed in Section 2.1 followed by the detailed review of the working principles of the MCHI based STATCOM in Section 2.2. Section 2.3 consisted of literature reviews on power quality solution patents in recent years. Later, an overview literature on STATCOM modulation techniques was reviewed in Section 2.4. Numerous literature on STATCOM control schemes and studies covering the most recently developed and published methods were reviewed in Section 2.5 as it was the main component of this dissertation. Finally, the chapter was summarized in Section 2.6.

2.1 Self-commuted Inverters Structural of STATCOM System

2.1.1 Conventional Inverters

Single-phase inverters such as H-bridge and three-phase inverters are normally referred to as two- and three-level inverters. AC waveform generated by these inverters with a DC source supplied by renewable energy sources, energy storage in batteries and distributed power generation devices such as photovoltaic power systems are delivered into the power system. Current Sources Inverter (CSI) which uses inductive energy storage as a DC current source and VSI which uses capacitive energy storage as a DC voltage source are the basic two conventional inverters [7]. Both CSI and VSI for conventional three-phase six-pulse has only one polarity and the power reversal that takes place through reversal of DC voltage polarity for CSI and DC current polarity for VSI are shown in Figure 2.1.

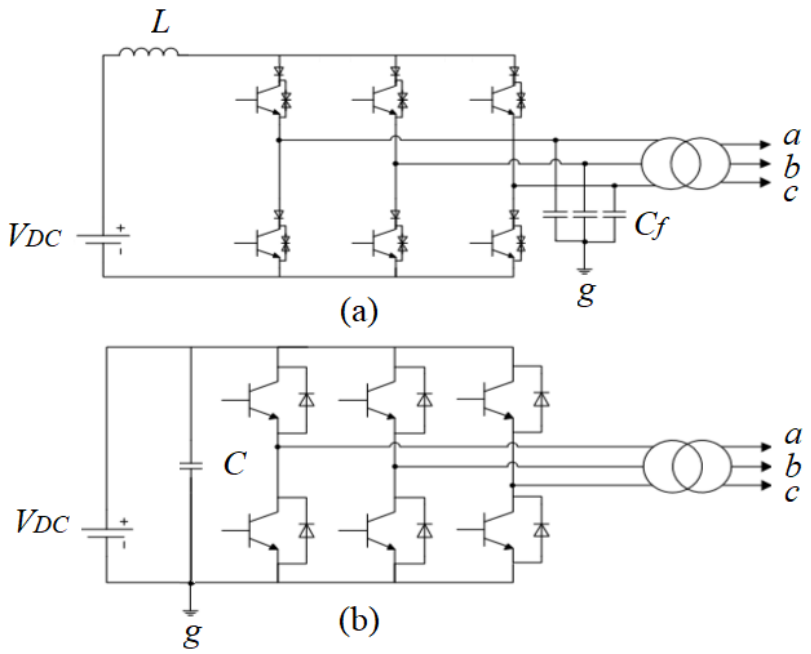

Figure 2.1 Conventional three-phase six-pulse (a) CSI and (b) VSI

However, current source termination in CSI by a current charged inductor produces more loss when compared to voltage source termination in VSI by a voltage charged capacitor. CSI requires an additional capacitive filter for voltage source termination and an additional overvoltage protection device such as a bi-directional diode for clamping the commutation voltage transients. Based on this drawback of CSI, VSI is the better choice in terms of overall system construction cost, dynamic performance and control strategy. However, there are some limitations associated with these configurations in high power applications such as power line transmission due to the constraint of the number of series-connected power semiconductors [7].

Conventional inverters require high PWM switching frequency in order to achieve optimal harmonic performance, but it also causes higher switching losses, stress and unwanted heat stress on the semiconductors [35]. These led to the development of multilevel inverters as a power inverter option for high power applications, where higher voltages can

be produced, and harmonic reduction achieved by its own circuit topology [36-39].

The next subsection reviews multilevel inverter circuits with their different topologies.

2.1.2 Multilevel Inverters

For various utilizations, DC power supplied by renewable energy sources, energy storages, and distributed power generation devices such as photovoltaic power systems, batteries and fuel-cells needs to be in the AC framework. Due to its considerable benefits in endless applications over the past three decades, interest in multilevel inverters has become important in the field of power electronics.

Multilevel Inverter is a semiconductor switch-based circuit that is designed to process the power by alternating its level (*n*) and frequency based on the load requirements. Multilevel inverters consist of an array of power semiconductors, capacitors and voltage sources in order to generate an output voltage as a stepped waveform. The commutation of the switches allows the addition of the capacitor voltages to reach a higher voltage at the output as the semiconductors withstand only the reduced voltages.

The realization of multilevel inverters requires the implementation of multiport switch functions using semiconductor power devices. This can only be done by a complicated network of switches compared to the conventional inverter. Therefore, multilevel inverters apply more devices, are more expensive to implement and are more prone to malfunction [40]. The capacitive voltage divider at the DC side of the inverter implies the need for some means to divide the total DC input voltage. This increases the DC-supply cost and complexity. If this voltage division is done using capacitors, it is required to maintain the capacitors' voltage balance [41]. The high number of switch combinations leads to complexity in the control compared to basic inverters [42].

Baker and Bannister [43] introduced and patented the concept of multilevel VSI in 1975. With the increasing number of levels in the inverter, the output voltages had more steps creating a staircase waveform to reduce harmonic distortion at the cost of increased control complexity and more unbalanced voltages occurring in the power system.

Multilevel inverters are receiving a lot of attention by researchers and studies have been carried out aiming to produce a staircase waveform which is as good as an ideal sinusoidal waveform with an improved harmonic spectrum. The three main, and most popular, multilevel inverter topologies over the past three decades are namely: Multilevel Diode-Clamped Inverter (MDCI), Multilevel Capacitor-Clamped Inverter (MCCI), and MCHI. Parallel to this trend, modulation techniques and control schemes have also been developed and implemented for multilevel inverters to cater for different performance requirements.

The following subsections described the above-mentioned multilevel inverter topologies.

2.1.2.1 Multilevel Diode-Clamped Inverter

A series of capacitor banks connecting the phases in diode-clamped configuration could allow numerous voltage levels in a multilevel inverter and produce a sinusoidal voltage waveform. Initially, MDCI was limited to a three-level inverter that includes two capacitors placed in series and connected across the DC-link which was unveiled by Nabae in 1981 [44]. Figure 2.2 shows a single-phase five-level diode-clamped inverter with four in-series capacitors connected across the DC-link. By formula, an *n*-level diode-clamped inverter requires $2(n-1)$ switching devices, $(n-1)(n-2)$ clamping diodes, and $(n-1)$ DC-link capacitors.

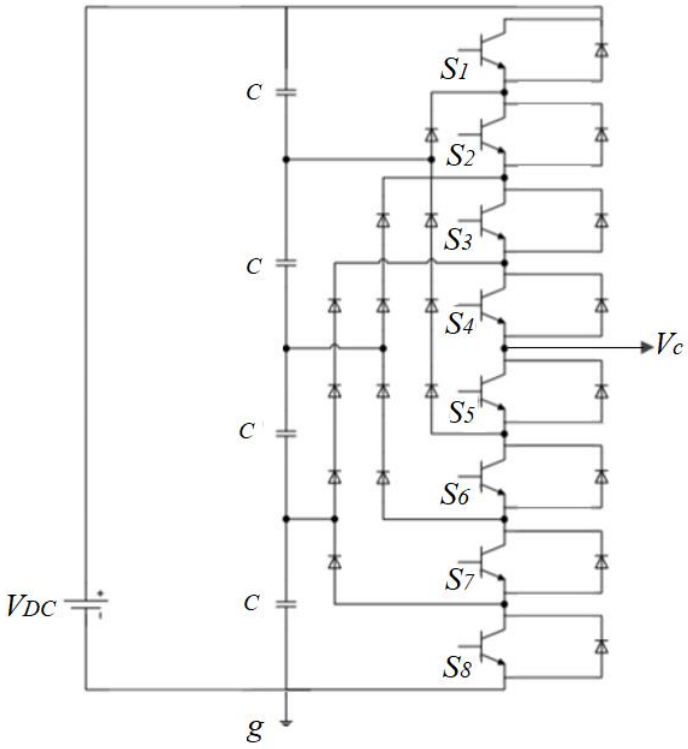

Figure 2.2 Phase leg of five-level MDCI [45]

In order to achieve a multi-step output voltage waveform, these diodes play an importance role to clamp the voltages across each DC capacitor at $\frac{V_{DC}}{n-1}$. The minimum number of power electronic components for other levels of MDCI is given in the Table 2.1.

Table 2.1 The required power electronics components for different voltage steps in MDCI

Number of Voltage steps	Number of DC-link Capacitors	Number of the Switching devices	Number of clamping diodes
3	2	4	2
4	3	6	6
5	4	8	12
.	.	.	.
.	.	.	.
n	$(n-1)$	$2(n-1)$	$(n-1)(n-2)$

2.1.2.1.1 Advantages of Multilevel Diode-Clamped Inverter

a) The change between adjacent states is done by changing only the state of the two switching devices.

b) The number of capacitors is low compared with other topologies. And this topology does not require any transformer, and there is only one DC-link bus.

c) Voltage drop across the switches is half the DC-bus voltage, effectively doubling the power rating of three-level VSIs for a given power semiconductor device [38].

2.1.2.1.2 Disadvantages of Multilevel Diode-Clamped Inverter

a) Due to DC capacitor voltage balancing issues which caused a high number of diodes to be required, the implementation of MDCI has been mostly limited to the three-level [46].

b) Every level of the inverter requires different current ratings of power semiconductors due to the non-similarity of the operation duty cycle.

c) Unoptimized physical power layout due to stray inductance of the interconnection between power components [32].

2.1.2.1.3 Applications of Multilevel Diode-Clamped Inverter

The MDCI is widely used in more conventional high-power AC motor drive applications such as conveyors, pumps, fans, and mills, which offer power solutions for industries including oil and gas, metals, mining, marine, and chemical [47].

2.1.2.2 Multilevel Capacitor-Clamped Inverter

MCCI or flying-capacitor multilevel inverter is a relatively new topology that was introduced by Meynard and Foch in 1992 [48]. Comparing with the MDCI, the configuration utilizes capacitors as clamping devices instead of diodes. Since then, MCCI has been applied intensively in a plethora of high-power applications. A typical five-level MCCI is depicted in Figure 2.3 [49-51].

Table 2.2 Switching states and the corresponding output voltage for five-level MCCI

Switching states								Output voltage
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{cg}
On	Off	Off	Off	On	On	On	Off	$\frac{V_{DC}}{4}$
Off	Off	Off	On	Off	On	On	On	
Off	Off	On	Off	On	Off	On	On	
On	On	Off	Off	On	On	Off	Off	$\frac{V_{DC}}{2}$
Off	Off	On	On	Off	Off	On	On	
On	Off	On	Off	On	Off	On	Off	
On	Off	Off	On	Off	On	On	Off	
Off	On	Off	On	Off	On	Off	On	
Off	On	On	Off	On	Off	Off	On	
On	On	On	Off	On	Off	Off	Off	$\frac{3V_{DC}}{4}$
Off	On	On	On	Off	Off	Off	On	
On	Off	On	On	Off	Off	On	Off	
On	On	On	On	Off	Off	Off	Off	V_{DC}

The voltage across each of the ten capacitors need to be maintained at $\frac{V_{DC}}{4}$. Since it offers more redundancy, The MCCI is more flexible compared to the MDCI. Hence, using said redundancies, the imbalance in the capacitor voltages can be significantly reduced

[52]. To extend the topology to a higher number of voltage levels, it is worth mentioning that *n*-level MCCI necessitates $2(n-1)$ switching devices, $\frac{(n-1)(n-2)}{2}$ clamping capacitors, and $(n-1)$ DC-link capacitors.

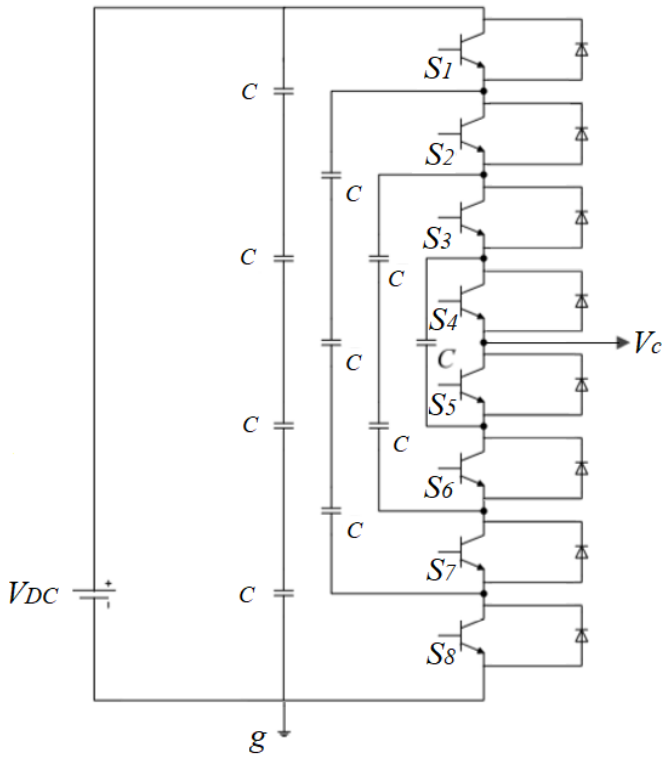

Figure 2.3 Phase-leg of the five-level capacitor-clamped inverter [38]

2.1.2.2.1 Advantages of Multilevel Capacitor-Clamped Inverter

a) Phase redundancies are available for balancing the voltage levels of the capacitors.
b) Real and reactive power flow can be controlled.
c) A large number of the utilized capacitors enables the inverter to ride through short-duration outages and deep voltage sags.

2.1.2.2.2 Disadvantages of Multilevel Capacitor-Clamped Inverter

a) Improving the inverter output profile increases the number of capacitors. Consequently, the balancing of voltage levels for all the capacitors is complicated. Complex control with high-switching frequency is needed to stabilize the voltages across each capacitor [37].
b) Switching utilization and efficiency are poor for real power transmission.
c) The large number of capacitors are more expensive and are bulkier than the clamping diodes in MDCI.

2.1.2.2.3 Applications of Multilevel Capacitor-Clamped Inverter

Because it needs a single power supply, inverters based on the flying capacitor are quite attractive for industrial adjustable-speed drive applications [38].

2.1.2.3 Multilevel Cascaded H-bridge Inverter

Although MCHI was first discovered in 1975, it was never a recognized multilevel inverter topology during the time [43]. It only started to become popular over the past 40 years. Multiple research studies have been carried out to prove its strength in producing an output voltage waveform as high as twenty-one level [28, 53] and even twenty-five level [54].

The schematic of a single-phase H-bridge inverter is shown in Figure 2.4. It consists of two inverter legs. Each leg contains two switching devices. Table 2.3 provides the possible switching combinations with the corresponding output voltages for the single-phase H-bridge inverter.

Table 2.3 Switching combination with the corresponding output voltages for the single-phase H-bridge inverter

State	Switches states				V_{ab}
	S_1	S_2	S_3	S_4	
1	ON	ON	OFF	OFF	V_{DC}
2	ON	OFF	ON	OFF	0
3	OFF	ON	OFF	ON	0
4	OFF	OFF	ON	ON	$-V_{DC}$

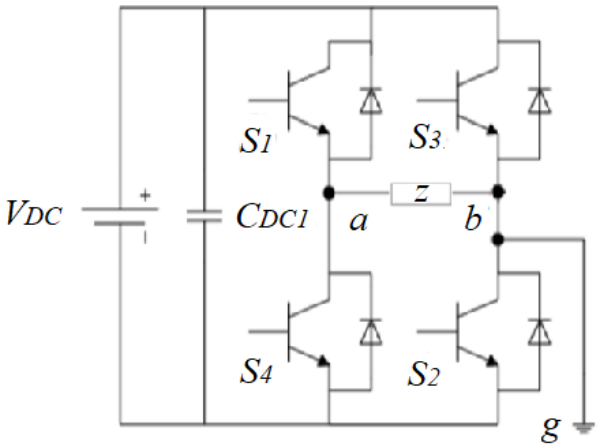

Figure 2.4 Single-phase H-bridge inverter

The three-level converter in Figure 2.4 is the basic unit used to construct a MCHI. Multiple units of single-phase H-bridge inverter cells are connected in a series chain in order to generate high AC voltages with a large number of levels. Which means, MCHI requires $(n-1)/2$ number of H-bridge inverters and $(n-1)/2$ number of DC sources for each phase-leg to produce n-level of output voltage. The voltage waveform is synthesized based on summing up the inverter outputs.

The symmetric structure of MCHI makes use of equal DC voltage sources and for H-bridge cells per phase, there are $(2n+1)$ levels

produced in the output of phase voltage. Each cell of the H-bridges needs a separate DC-source which is usually obtained by an arrangement of three-phase or single-phase diode-based rectifiers [55]. Multiple transformers are used to provide the electrical isolation. Recently, high frequency transformer-based modules are utilized in building cascaded multilevel inverters [56] without isolated DC-links and diode-based rectifiers. Such modules utilize an active front-end rectifier which is more suitable for regenerative operation [57, 58]. In some applications, these DC voltages can be acquired directly by isolating DC-sources like photovoltaic panels [59] or DC/DC isolated converters [60].

A typical single-phase configuration of a five-level MCHI is shown in Figure 2.5. To reach such a level count, two single-phase H-bridge inverter cells are cascaded. Table 2.3 gives the switching states with the corresponding voltage levels for the single-phase five-level MCHI.

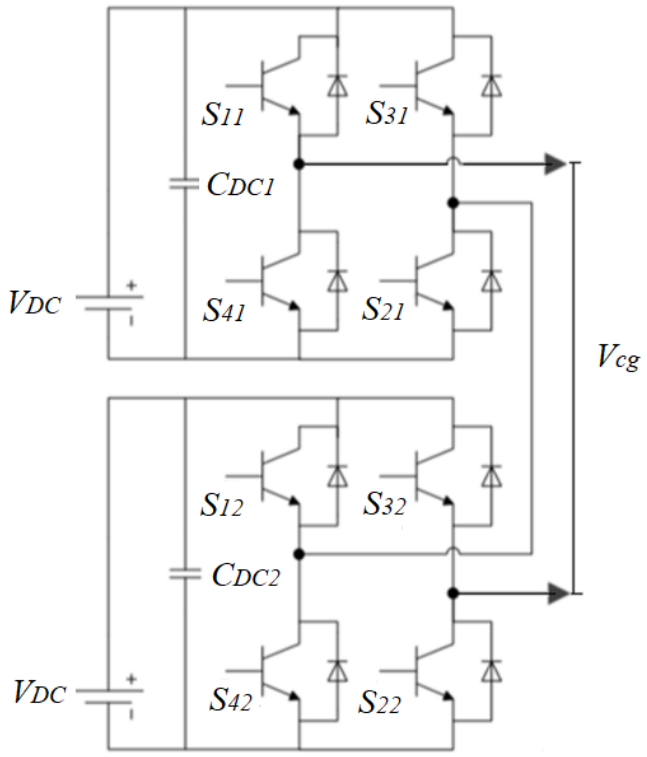

Figure 2.5 Single-phase five-level MCHI

Based on Table 2.3 and Table 2.4 it is observed that more than one switching state may lead to a similar voltage level. For instance, four dissimilar sets of switching states redundantly produce the voltage level V_{DC}. The switching state redundancies offer more flexibility in the design and control of MCHI.

Table 2.4 The switching states with the corresponding voltage levels for the single-phase five-level MCHI

State	Switching states								V_{cg}
	S_{11}	S_{21}	S_{31}	S_{41}	S_{12}	S_{22}	S_{32}	S_{42}	
1	ON	ON	OFF	OFF	ON	ON	OFF	OFF	$2V_{DC}$
2	ON	ON	OFF	OFF	ON	OFF	ON	OFF	V_{DC}
3	ON	ON	OFF	OFF	OFF	ON	OFF	ON	
4	ON	OFF	ON	OFF	ON	ON	OFF	OFF	
5	OFF	ON	OFF	ON	ON	ON	OFF	OFF	
6	ON	OFF	ON	OFF	ON	OFF	ON	OFF	0
7	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	
8	OFF	ON	OFF	ON	ON	OFF	ON	OFF	
9	OFF	ON	OFF	ON	OFF	ON	OFF	ON	
10	ON	ON	OFF	OFF	OFF	OFF	ON	ON	
11	OFF	OFF	ON	ON	ON	ON	OFF	OFF	
12	OFF	OFF	ON	ON	ON	OFF	ON	OFF	$-V_{DC}$
13	OFF	OFF	ON	ON	OFF	ON	OFF	ON	
14	ON	OFF	ON	OFF	OFF	OFF	ON	ON	
15	OFF	ON	OFF	ON	OFF	OFF	ON	ON	
16	OFF	OFF	ON	ON	OFF	OFF	ON	ON	$-2V_{DC}$

2.1.2.3.1 Advantages of Multilevel Cascaded H-bridge Inverter

a) The DC-link unbalancing problem is avoided because of the utilized isolated DC-links.

b) The switching state redundancy phenomenon in MCHI provides immense flexibility for switching pattern design.

c) MCHI has a high degree of modularity since each inverter can be treated as a module with similar circuit topology, control structure, and modulation [61]. Therefore, any faulty module in the inverter can be quickly and easily replaced. Moreover, with the appropriate control technique, there is a probability to bypass the faulty module without stopping the load, bringing an almost continuous overall availability [62].

d) This structure needs only standard low-voltage, mature, technology components to output medium voltage levels.

e) Three-phase, *n*-level MCHI employs $6(n-1)$ switching devices with built-in freewheeling diodes. Hence, no extra diodes or capacitor banks are needed.

2.1.2.3.2 Disadvantages of Multilevel Cascaded H-bridge Inverter

Comparing with the other topologies, the number of DC-sources is higher and *n*-level inverter requires number of $V_{DC} = \frac{n-1}{2}$ voltage sources [7].

2.1.2.3.3 Application of Multilevel Cascaded H-bridge Inverter

a) This topology is an attractive candidate for harvesting energy from renewable energy sources such as solar panels and fuel cells.

b) MCHI has also been used as the main traction drive in electric vehicles, where several batteries or ultra-capacitors

are positioned as separated DC-sources. Moreover, these topologies may serve as rectifiers in order to charge the batteries of an electric vehicle [10].

2.1.3 Comparison among Multilevel Inverters

The higher the number of levels for a multilevel inverter, the higher the performance of the multilevel inverter. As the number of levels rises, low harmonic sinusoidal voltage waveform can be acquired through a low-switching frequency PWM technique. But, the number of voltage levels and system consistency is restricted by the control complexity, impediments of the system structure, and cost-budgeting. According to Akagi et al. [24] and Jimichi et al [25], the weight of a three-phase frequency transformer rated at 6.6 kV and 1 MVA ranges from 3 to 4 tons, while the weight of a three-phase MCHI with the same voltage and current ratings could ranges from 1 to 2 tons. On top of that, approximately 70 % total power losses of the MVA rating for the STATCOM system result from these transformers [23]. Table 2.5 shows the total number of components needed for MDCI, MCCI, and MCHI to achieve the same number of voltage levels, n.

Table 2.5 Comparison of required components per phase-leg among MDCI, MCCI and MCHI

Multilevel inverter Topologies	MDCI	MCCI	MCHI
Power switching devices with anti-parallel diode	$2(n-1)$	$2(n-1)$	$2(n-1)$
Clamping-diode	$(n-1)(n-2)$	0	0
Clamping-capacitor	0	$\frac{(n-1)(n-2)}{2}$	0
DC-link capacitor	$n-1$	$n-1$	$\frac{n-1}{2}$

2.2 Working Principle of MCHI Based STATCOM

MCHI Based STATCOM topology aims to reduce the overall system energy losses by topping up the level of H-bridge inverters and lessening the requirement of coupling transformers including reducing the number of large size higher-order output filters [38]. This idea was first suggested in 1997 by Rodriguez at al [23], which later led to more research and development on this topology. The application of MCHI based STATCOM could range from low-power applications, such as green energy electric vehicles, to very high-power application, such as FACTS controllers and variable speed drive control applications. Generally, MCHI synchronizes its phase voltage by adding and subtracting the voltage levels supplied by each H-bridge inverter [37]. Comparing to other topologies in recent FACTS technology, a three-phase MCHI which contains three identical phase-legs of series-connected H-bridge inverters can produce dissimilar output voltage waveforms to compensate and alleviate the reactive currents in a three-phase systems [39, 63, 64].

A complete STATCOM controller contains external, internal, and gate control. An excessive number of gate-controlled semiconductor switches comprises an MCHI which is similar to other inverter topologies. The gating commands of switches are produced by the internal controller in response to the real and/or VAR reference signals from the external controller. Therefore, to achieve a constant and well-organized operation of STATCOM, a suitable mathematical model is required to outline and improve their parameters for these controllers. According to the grid codes, 200 ms is the response time required by STATCOM to reach steady-state [35]. This is also why the idea of MCHI based STATCOM still remains a fascinating topic among power electronic researchers to improve its dynamic and transient performances by introducing diversified control schemes [32-62].

Having a suitable modulation technique is very crucial for MCHI topology to accomplish the production of quality waveforms under minimum filtering and a low-switching frequency. It is because the switching losses of the power semiconductor devices directly impact power losses in the inverter that causes the overall performance to drop [65]. An interesting comparison between the

switching frequencies which ranges from 1 kHz to 12 kHz with the IGBT inverter was shown by Malfait et al. [66], with the conclusion that the minimum losses of an inverter occurred at the frequency of 3 kHz.

2.3 Power Quality Solutions

In recent years, machine and drive components in industrial applications have become more technically advanced which came together with an increased voltage sag susceptibility due to unmanaged power flow. A resistive load connected and disconnected occasionally represents a large load change in the PCC causing bus voltage magnitude deviations as well as phase jumps which lead to a weak power system. This means, more interruptions in the production phase in terms of more power quality related costs caused by poor PF, excessive reactive power consumption, and phase voltage unbalance. Thus, it is crucial to improve the voltage stability of the power utility distribution systems under various operating conditions especially systems with a large share of constant power loads [67-69].

A common solution in recent days for substantial voltage-magnitude fluctuations is to install SVCs or STATCOM [59]. Power quality issues such as voltage sags, power interruptions and voltage flicker can be improved through introducing active and reactive power compensation, which includes active harmonic filtration under unbalanced voltage conditions, into the power utility systems.

2.3.1 Reactive Power Compensation

Research in active power and reactive power filters for current quality compensation is getting more and popular in both industrial and utility applications right after the concept of an active AC power filter was first introduced in 1976 by Gyugyi [70]. The author proposed a unique scheme namely the “power doubling scheme”, which showed that all solid-state realization of static reactive power sources or passive

storage elements were not required in a practical reality. Later in 1992, the author [71] proposed a new design control concept of shunt compensation to provide power factor correction for reducing or cancelling the reactive power demand from large and fluctuating industrial loads. Figure 2.6 illustrates a simplified single-phase equivalent circuit of STATCOM, where V_{pcc} is the grid voltage, i_c is the STATCOM current and V_c is the STATCOM voltage.

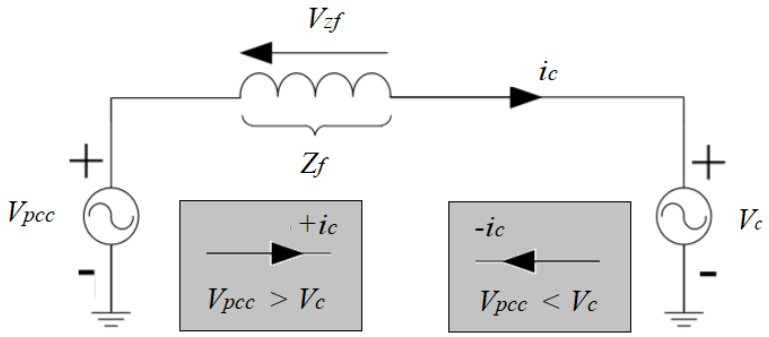

Figure 2.6 Simplified single-phase equivalent circuit of STATCOM

In the exchange of active current and reactive current between the power system and STATCOM through the coupling inductor Z_f, the amplitude of V_c and phase angle δ with respect to V_{pcc} can be controlled according to the required specific conditions. In the first condition, when V_{pcc} is higher than V_c, the STATCOM operates in inductive mode and draws reactive current from the PCC. On the other hand, the second condition of whenever V_c is higher than V_{pcc}, the STATCOM operates in capacitive mode and supplies reactive current back to the PCC. This relationship is also shown in the phasor diagram of Figure 2.7, where V_{pcc} and V_c are controlled to be in-phase for pure reactive current exchanges.

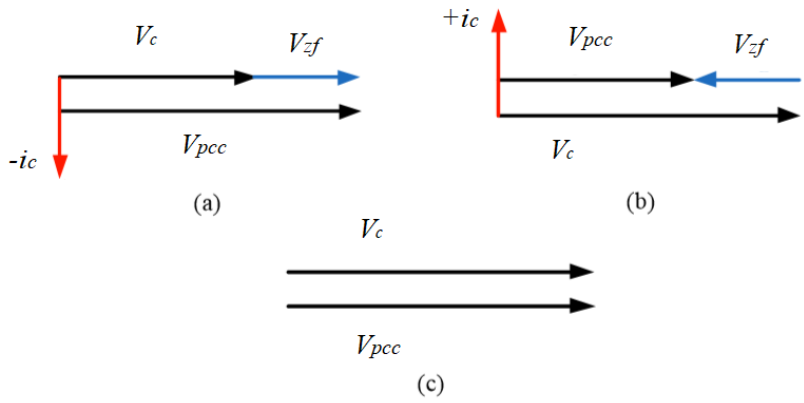

Figure 2.7 Phasor diagram of STATCOM operating in (a) inductive mode, (b) capacitive mode, and (c) floating mode

Lastly the third condition is when both V_{pcc} and V_c are equal and are in-phase, the STATCOM operates in floating mode and no active current or reactive current exchanges between V_{pcc} and V_c occurs. But if both V_{pcc} and V_c are equal but not in-phase, which under the scenario where V_c lags V_{pcc} with phase difference by an angle of δ, STATCOM then absorbs the active current from the PCC. When in the alternate scenario where V_c leads V_{pcc}, active current is delivered to the PCC from the STATCOM.

STATCOM active power and reactive power compensation working principle can be seen from the Equation (2.1):

$$S_{pcc} = P_{pcc} + Q_{pcc} = \left(\frac{V_{pcc}V_c}{z_f}\right)\sin\theta + \left(\left(\frac{V_{pcc}}{z_f}\right)(V_{pcc} - V_c)\right)\cos\theta \tag{2.1}$$

where S_{pcc} is the apparent power of the power system, P_{pcc} is the active power of power system and Q_{pcc} is the reactive power of the power system.

2.3.2 Active Harmonic Filtration

Harmonics is another factor that contributes to poor power quality. A harmonic is defined as the voltage or current with frequencies where the integer is a multiple of the fundamental frequency [71]. This can be expressed as Equation (2.2):

$$f_H = f_{fund} H \tag{2.2}$$

where f_H is frequency of a harmonic, f_{fund} is fundamental frequency and H is harmonic order.

If in the case of $f_{fund} = 50$ Hz, the 2nd harmonic is 100 Hz and 5th harmonic is 250 Hz, etc. These harmonics, specifically the negative sequence components cause unnecessary overheating, low efficiency of equipment [72] and shortens the lifespan of the equipment. In addition, the harmonics also result in telephone interference which causes metering and instrumentation difficulties including damaging the capacitors [73].

In order to overcome the harmonic problem in the system, a harmonic filter including a passive filter and an active filter needs to be installed. Passive filter, which provides a minimum impedance path for tuning the harmonic frequency is simple and less expensive. However, it does have some drawbacks. For instance, it can only produce regular compensation, is unable to compensate an unbalanced load, has resonance issues with the inductive-capacitive filter, and is large [74].

Due to these drawbacks, the active harmonic filter s developed to tackle the harmonic issue in the system. There are two different types of active harmonic filtration which are the series and shunt active harmonic filter. The series active harmonic filter is typically used to minimize the voltage harmonic while the shunt active harmonic filter is normally used for compensating the current harmonic for non-linear loads [75]. The shunt active harmonic filter injects the harmonic current at the

point of PCC to compensate the non-linear load current and to produce a sinusoidal current source curve.

2.4 STATCOM Modulation Techniques

There is a huge amount of literature on PWM techniques for different applications especially in industrial devices and power transmission [76-80]. Three widely used techniques for high power applications are namely:

a) Carrier Based-Pulse Width Modulation (CB-PWM)
b) Space Vector Modulation (SVM)
c) Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM)

PWM techniques can be categorized as open loop, also known as feedforward, and closed loop schemes. CB-PWM operating with high-switching frequency performs many commutations of the power semiconductors in one cycle to generate a fundamental output voltage. SVM and SHE-PWM, on the other hand, operate with low-switching which performs one or two commutations of the power semiconductors to generate one cycle of staircase voltage waveform. The characteristic of each technique is further reported in the following subsections.

2.4.1 Carrier Based-Pulse Width Modulation

CB-PWM illustrates the intersection of a modulating signal with a triangle waveform where the a-phase duty cycle is compared with triangle waveforms. CB-PWM is also known as the easiest technique of describing voltage source modulation among the aforementioned modulation techniques. CB-PWM can be categorized into two different approaches, namely Phase Shifted-Pulse Width Modulation (PS-PWM) and Level Shifted-Pulse Width Modulation (LS-PWM).

2.4.1.1 Phase Shifted-Pulse Width Modulation

PS-PWM is a conventional form of scalar PWM techniques. It employs phase shifted carriers to distribute the switching angles among sub-waveforms and reduce the frequency of each component. Therefore, it fits well with cascaded multilevel inverters [81]. Overall, PS-PWM techniques require several $(n-1)$ triangular carriers to modulate a multilevel inverter of *n*, voltage levels. In PS-PWM carriers of similar frequency and amplitude are used [82]. The phase shift between any two adjacent carrier signals is equal to $\frac{360^\circ}{n-1}$.

Such optimal phase shifting amongst the carriers significantly reduces the THD. This modulation technique offers better flexibility since the modulating signal is maintained with adjustable amplitude and frequency. For a five-level CHBI in Figure 2.8, two bridges are used and four carriers need to be compared with a single reference signal. Hence any two adjacent carries are $\frac{360^\circ}{90} = 40^\circ$ electrical degree shifted.

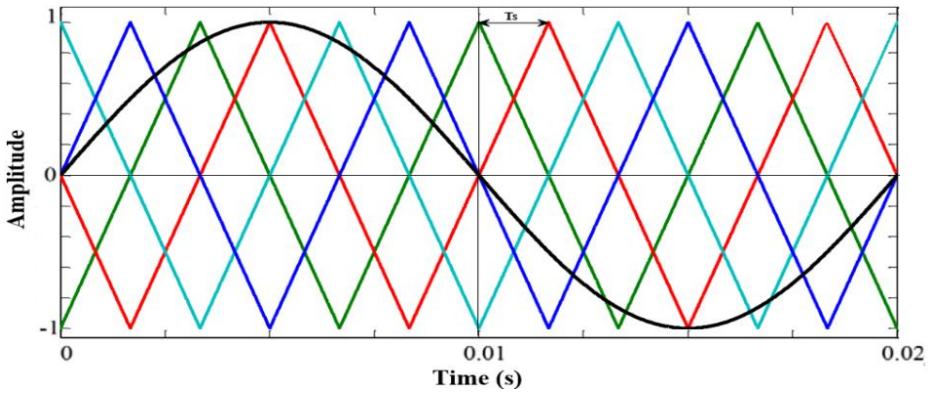

Figure 2.8 Illustration of PS-PWM for five-level MCHI

Unfortunately, in three-phase application PS-PWM does not equalize the switching frequency of cascaded inverter's legs. In [83] a technique was proposed in order to equalize the switching frequency of cascaded inverter's legs. However, the distribution of switching angles is not uniform in this technique. Authors in [84] used a state machine decoder

to uniformly distribute the switching angles between the legs but it was a bit complicated to implement [85].

2.4.1.2 Level Shifted-Pulse Width Modulation

LS-PWM is widely used for the modulation of MCHI, where each cell is modulated independently using a sinusoidal unipolar PWM and bipolar PWM respectively. The modulation technique provides an even power distribution among the cascaded cells. Like PS-PWM [81], the use of level-shifted multicarrier modulator for MCHI requires $(n-1)$ triangular carriers. As shown in Figure 2.9 to Figure 2.11 all carriers have the same frequency and amplitude.

The $(n-1)$ triangular carriers are vertically disposed such that the bands they occupy are contiguous where the carriers shifted by a DC-offset level equivalent to the peak-to-peak amplitude of the carrier signals. Such arrangement generates a stepped multilevel output waveform with lower distortion. The triangular waves are compared to one sinusoidal signal. Hence there is flexibility to work under different modulation indices and different switching frequencies. The frequency modulation index (M_f) is equal to Equation (2.3):

$$M_f = \frac{f_{cr}}{f} \tag{2.3}$$

where f_{cr} is the frequency of the carrier and f represents the modulating signals. Both f_{cr} and f remain the same respectively for the phase-shifted modulation scheme. Within the linearity range, the LS-PWM modulation index (M_i) is equal to Equation (2.4):

$$M_i = \frac{V_{peak}}{V_{pa(n-1)}} \tag{2.4}$$

where V_{peak} is the peak voltage and V_{pa} is the peak amplitude for each carrier wave. Period of the carrier signal, T_s is equal to $\frac{1}{f_{cr}}$.

Three popular disposition technique of LS-PWM, namely:

i) In-Phase Disposition-Pulse Width Modulation (IPD-PWM)
ii) Phase Opposition Disposition-Pulse Width Modulation (POD-PWM)
iii) Alternate Phase Opposition Disposition-Pulse Width Modulation (APOD-PWM)

2.4.1.2.1 In-Phase Disposition-Pulse Width Modulation

When carriers of similar phase shift are utilized and vertically shifted as depicted in Figure 2.9, the arrangement is called IPD-PWM.

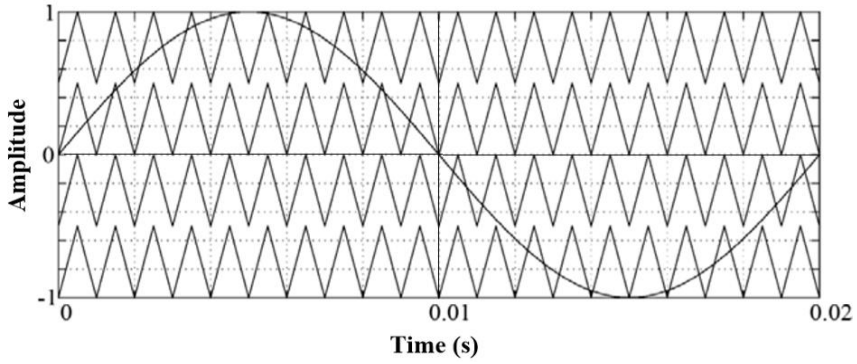

Figure 2.9 Illustration of IPD-PWM method for single-phase five-level inverter

2.4.1.2.2 Phase Opposition Disposition-Pulse Width Modulation

In this scheme, the carriers above the zero-reference point are out of phase with those below zero reference point by 180°. The amplitude and frequency of carrier signals are maintained the

same, but they differ in DC-offset. For a five-level MCHI the modulating signal is used with four carrier signals as shown in Figure 2.10.

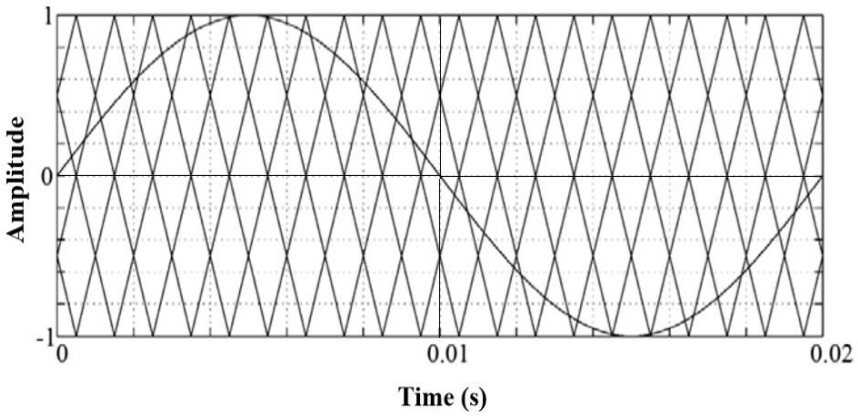

Figure 2.10 Illustration of POD-PWM method for single-phase five-level inverter

2.4.1.2.3 Alternate Phase Opposition Disposition-Pulse Width Modulation

In APOD-PWM method depicted in Figure 2.11, all the carriers have the same amplitude, frequency and different DC-offset. Each carrier is phase shifted by 180∘ from the adjacent carrier.

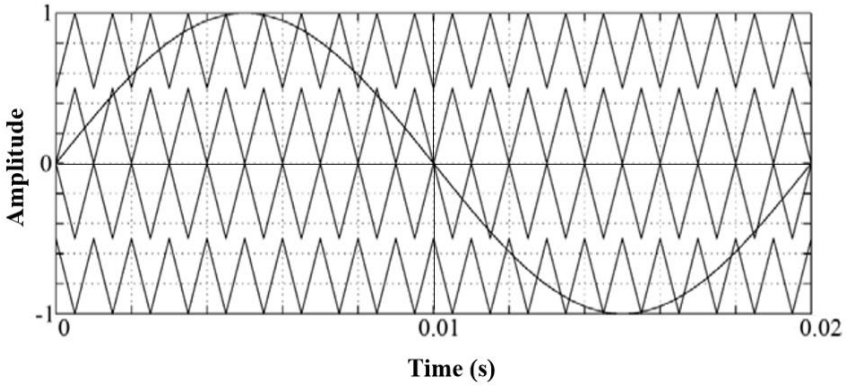

Figure 2.11 Illustration of APOD-PWM method for single-phase five-level inverter

2.4.1.3 Summary for Carrier Based-Pulse Width Modulation

A study made by Agelidis and Calais [86] in 1998, compared IPD-PWM, POD-PWM, APOD-PWM and PS-PWM in terms of THD on the output voltage (THD_V) and the output current (THD_i) at different modulation indexes and frequency indexes. The analysis revealed that IPD-PWM technique is more convenient in terms of THD of output voltage and current signals and in terms of the quality of power factor in AC multilevel inverters. Later in 2007 [87], the effects of different M_f and M_i values on the waveform profile of an AC multilevel inverter was investigated by Baier et al and the results tabulated in Table 2.6.

Table 2.6 THD variation of THD_V and THD_i for different M_f and M_i

f_{cr} (Hz)	M_i	IPD-PWM		POD-PWM		APOD-PWM		PS-PWM	
		THD_V	THD_i	THD_V	THD_i	THD_V	THD_i	THD_V	THD_i
950	0.8	23.95	4.09	23.83	3.99	23.86	3.94	56.20	6.46
	1	16.77	3.32	17.66	3.78	17.67	3.31	33.55	7.52
	1.2	15.62	5.98	15.93	6.46	15.88	6.53	26.20	4.14
2000	0.8	22.90	2.27	21.50	2.29	22.72	2.15	44.84	4.09
	1	17.02	1.69	17.52	1.68	17.04	1.67	24.08	7.27
	1.2	15.23	5.99	14.64	5.77	15.15	5.75	20.48	5.69
3000	0.8	21.20	1.87	21.16	1.75	21.63	1.85	51.78	9.94
	1	16.49	1.59	16.77	1.74	16.54	1.50	30.49	7.14
	1.2	14.64	5.90	14.67	6.21	14.60	5.94	23.08	5.59
4000	0.8	21.02	2.94	20.62	3.36	20.39	2.65	48.53	6.48
	1	15.70	1.54	14.83	1.12	15.20	1.05	25.83	6.77
	1.2	14.62	5.85	14.23	5.93	14.37	5.94	21.78	6.22
5000	0.8	22.21	2.30	23.04	2.32	21.21	2.39	32.37	4.72
	1	17.81	2.68	17.73	2.83	17.26	3.15	29.27	6.21
	1.2	15.07	6.00	14.53	5.98	14.89	5.92	19.79	5.83

In 2014, a comparison was done between IPD-PWM and PS-PWM by Darus et al [88] and the results shown that the IPD-PWM had lower THD_V output compared to PS-PWM. When using the sorting algorithm, both IPD-PWM and PS-PWM presented good results in terms of voltage balancing. But when it came to minimalizing harmonic distortion, IPD-PWM was shown to be the better option.

Dheeraj et al [89] in 2014 also stated that IPD-PWM performed better in the THD_i output compared with POD-PWM and APOD-PWM under different M_i. When M_i increased, THD_i decreased as reflected in Table 2.6.

Even though CB-PWM has less THD and is easy to implement, it cannot directly manipulates the harmonic contents which causes high-switching losses. The switching losses increase as the switching frequency goes higher in order to reduce the THD values [90, 91]. Plus, under this switching scheme the maximum M_i can only go up to round number one.

2.4.2 Space Vector Modulation

In 1991, Choi et al [92] was the first author to extend the two-level SVM pulse width modulation technique to more than three-level for the Neutral-Point Clamped (NPC) multilevel inverter. SVM is based on vector selection in the dq-stationary reference frame. The SVM diagram of any three-phase *n*-level inverter consists of six sectors. Each sector consists of a total number of $(n-1)^2$ triangles. The tip of the reference vector can be located within any triangle. Every vertex of the triangle represents a switching vector. A switching vector represents one or more switching states depending on its location. There is n^3 switching states in the space vector diagram for an *n*-level inverter. The SVM is performed by properly selecting and executing the switching states of the triangle for the respective on-times. It is also known as the

nearest three vector approach. The performance of the inverter significantly depends on the selection of these switching states. Figure 2.12 shows the space vector diagram of a five-level NPC. There are six sectors (Sector1-Sector6), four triangles in a sector, and a total of 27 switching states in this space vector diagram.

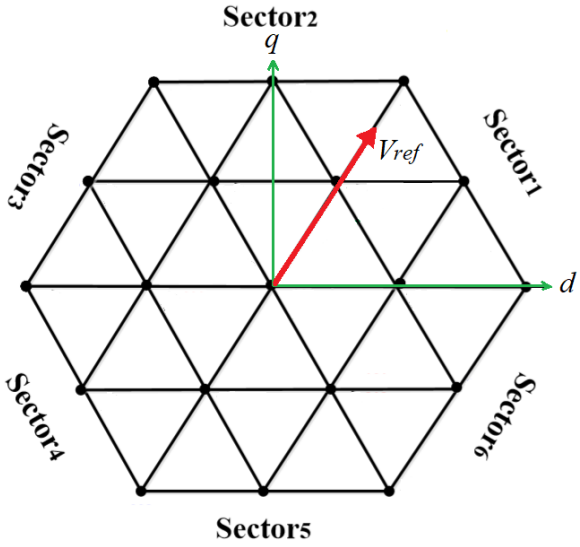

Figure 2.12 Illustration of SVM diagram for single-phase five-level inverter

SVM has several advantages like having decent utilization of DC-link voltage, low-current ripple, adapting with high power application and user-friendly hardware employment through DSP boards, when compared to CB-PWM [38]. Due to the increasing levels of modern multilevel inverters, the switching states also increase which causes trouble in computing the duty cycles, sector selection where the voltage reference (V_{ref}) falls onto and getting the desired switching states. Li et al [93] have attempted to mitigate the above-mentioned issues by simplifying the computation and control scheme. Yet, this method could not be applied when the number of levels was decreased. Error, in terms of generated vectors with respect to the reference, was going to be large which later introduced ripple currents and affected the capacitor lifetime [54].

2.4.3 Selective Harmonic Elimination Pulse Width Modulation

CB-PWM and SVM normally come with extra losses because of the high switching frequencies. For this reason, low-switching frequency control methods, such as SHE-PWM, has been in-depth reviewed and nominated as a competitive solution for multilevel inverter control by Dahidah [94]. This technique calculates a series of switching angles to combine separate elements into a single unit of a desired sinusoidal voltage waveform [95].

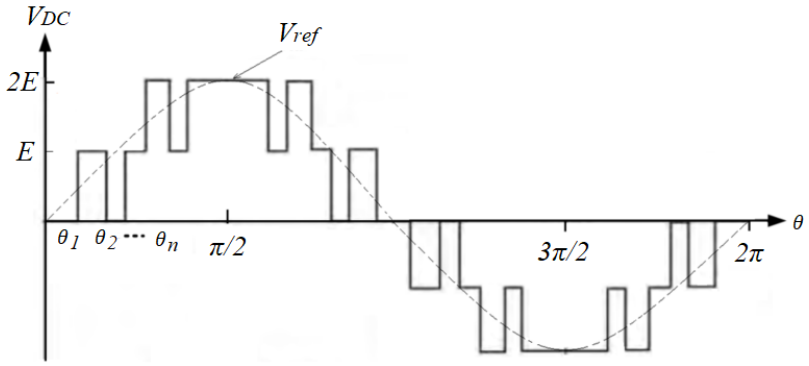

Figure 2.13 Illustration of SHE-PWM output voltage waveform for single-phase five-level inverter

By referring to Figure 2.13, the mathematical equation of Fourier series representation of the output voltage waveform using fundamental frequency modulator is expressed as Equation (2.5) [96]:

$$V_{DC}(\omega t) = \sum_{k=1,3,5,..}^{\infty} \frac{4E}{k\pi}(\cos(k\theta_1) + \cos(k\theta_2) + \cdots + \cos(k\theta_n))\sin(\omega t) \quad (2.5)$$

where E is V_{DC} and $\theta_1, \theta_2, \theta_3, \dots, \theta_n$ are the independent switching angles defined by solving the following Equation (2.6):

$$\begin{cases} \cos\theta_1 + \cos\theta_2 + \cdots + \cos\theta_n = \frac{\pi V_{ref}}{4E} \\ \cos(3\theta_1) + \cos(3\theta_2) + \cdots + \cos(3\theta_n) = 0 \\ \vdots \\ \cos(k\theta_1) + \cos(k\theta_2) + \cdots + \cos(k\theta_n) = 0 \end{cases} \tag{2.6}$$

The SHE-PWM modulation index M_i is given by Equation (2.7):

$$M_i = \frac{\frac{\pi V_{ref}}{nE}}{n} \tag{2.7}$$

where V_{ref} is the magnitude of the fundamental harmonic and n represents the level of inverter.

Different algorithms such as iterative method and artificial neural networks are used to solve the set of non-linear equations. [97] introduced a simple method to calculate the switching angles (θ_n) based on the following Equation (2.8):

$$\theta_n = \sin^{-1}\frac{nE}{V_{peak}} \tag{2.8}$$

where V_{peak} is the peak value of V_{ref}.

The frequency of the output voltage is the same as the frequency of the sine reference wave. The basic concept of the conduction angle determination is also shown in Figure 2.13.

MCHI with separated DC capacitors is certainly the most versatile power inverter topology for STATCOM applications. However, due to the ill-defined transfer functions, complex control schemes and formulations have emerged to achieve a tolerable low-switching frequency, high-bandwidth power control. These complex algorithms also increase the computational burden on digital processors. Thus, adequate controller parameters were generally obtained by using the trial and error method, which is practically ineffective and time-consuming. In addition, excluding the BESS from STATCOM has limited its capability to perform four-quadrant operating mode, especially when dealing with three-phase unbalanced loading conditions.

According to Kazmierkowski et al. [98] in 1998, various techniques with different concepts can be categorized into two main groups: linear and non-linear. The linear controllers include PI (i.e. Stationary PI-Controller and Synchronous Vector PI-Controller), State Feedback Controllers, and predictive techniques with constant switching frequency (Predictive and Deadbeat Controller). The non-linear comprise of Bang-Bang Controllers (Hysteresis Current Controller) and Predictive Controllers with on-line optimization. Nevertheless, new research trends in the current control method such as Neural Networks Controllers and Fuzzy-Logic based Controllers favor fully digital control even with some sacrifice in accuracy and dynamic performance.

In 2009, Liu et al. [99] proposed a dead-band controller via a small-signal model for balancing individual DC capacitor voltages in three-phase cascade multilevel inverter based STATCOM. An improved feed-back loop control (a.k.a Dead-Band controller) based on a small-signal control system balancing individual DC capacitor voltages for three-phase cascaded multilevel inverter based STATCOM was demonstrated. The proposed controller could eliminate the variable part of the gain to control the DC capacitor voltage. With the control of the DC capacitor voltage, the phase shift of H-bridge voltages and the unnecessary switching of power switches were stabilized and reduced respectively. Moreover, the controller allowed the H-bridges to run with

different switching patterns and have parameter variations. However, there is no detailed explanation of harmonic filtering.

In 2009, Luo et al. [100] reported that traditional PI-controller with constant parameters was not robust enough due to the variations of the system parameters. Therefore, a fuzzy-PI-based direct output voltage control scheme was introduced to regulate the voltages at the PCC and the DC-link voltage simultaneously. The proposed scheme was not affected by the uncertainties in the STATCOM system. However, the design process of fuzzy control involves defining complex rules and factors which relate the input variables with the output model properties. Moreover, this method provides only a moderate improvement of compensation performance over the conventional PI-controllers.

In 2009, an active power compensation scheme based high pass filter time constant calculation which mostly depended on the frequency of the load variation by providing a certain range of reactive power support was proposed by Xie et al [101]. Together with an energy storage capacitor bank connected on the DC side of the STATCOM, the converter can compensate active power to reduce the phase jump and the bus voltage magnitude deviation. This means the total apparent power rating of STATCOM is almost uniform at all times since the active and reactive powers are in orthogonal.

In 2010, a sliding mode controlled five-level MCHI was proposed by Gupta et al. [102] based on generalized multiband hysteresis modulation and switching characterization. This is a frequency-domain technique which is used to find the net hysteresis bandwidth based on a given desired maximum switching frequency of the inverter. The switching transition concept of Tsypkin's method [103] and the function of the non-linear relay were used to derive the results. To provide a self-balancing capability for a capacitor supported DC-link, the hierarchy of each cell was sequentially swapped, and the switching components were most likely to be at higher frequency levels for reducing ripple content in the output-controlled voltage. However, there are going to be more losses in switching due to higher frequency characteristics in multiband hysteresis modulation.

In 2010, a self-tuning PI-controller using Particle Swarm Optimization (PSO) algorithm was extended by Liu and Hsu [104] to the STATCOM system aiming to achieve satisfactory dynamic response under balanced load. The PSO method did not require inference rules to get the gain of the controller when compared with normal fuzzy control. It required an evaluation function attained by Runge-Kutta's numerical method [105] to speed up the gain adaption procedure in real-time applications. However, these two fuzzy and PSO algorithms involve complex formulations which increase the computational burden to the digital signal processor.

In 2011, an active power compensator based single-phase back to back converter was proposed by Shu et al. [106] to improve the power quality of electric railway power supply systems. Where a co-phase active power compensator based on Field Programmable Model Gate Array (FPGA) connected the transformer between the load and the supply. The author claimed that the proposed multifunctional control algorithm could achieve active power balancing, reactive power compensation and even harmonics filtering. However, the proposed control algorithm is very complex and may not be applicable when a STATCOM system is used instead.

In 2011, Wang et al. [107] proposed a direct output voltage control scheme for STATCOM system using PI-controller based on multiple control models. Each control model, which consisted of two PI-controllers, could be attained from the voltage drop of the PCC after connecting it with an impact load. Between the two PI-controllers, one was chosen at a time to realize control based on the switching index. The instantaneous dq-converter method, which converted the three-phase voltage instantaneous value to a dq-axis component, was used to obtain the maximum value and the rms-value of the voltage. While maintaining the simple structure and short calculation time of PI-controllers, it also applied the control effect by using different PI-controllers under different reactive load conditions.

In 2011, a novel vector control algorithm was proposed by Mekhilef et al. [108] to avoid the undesirable high switching frequency for high and medium voltage stages. The control scheme was not affected by the fact that the inverter's DC

sources were chosen to maximize the inverter levels by cancelling redundant voltage stages. From the proposed algorithm, the authors discovered that the switching frequency at high-voltage stage was equal to the output fundamental frequency and the switching frequency was not more than five times for the medium-voltage stage. However, the proposed control is not suitable for CB-PWM technique as it subjects the high-voltage stage to high switching frequency.

In 2012, Liu et al. [109] presented a novel DC capacitor voltage control method for STATCOM system and a general analytical method. In the digest, comparisons between three types of balance control scheme, namely, the active voltage vector superposition, M_i regulation, and phase shift angle regulation were also made for delta-connected twelve-level CHI topology controlled by CB-PWM technique. In summary, the active voltage vector superstition method offers good control performance with strong regulation capability followed by the phase shift angle regulation method and M_i regulation method.

In 2012, a Model Predictive Control (MPC) scheme was demonstrated by Townsend et al. [110] for a nineteen-level CHI based STATCOM to simultaneously balance the H-bridge capacitor voltages, provide good current reference tracking, and minimize the converter switching losses. The scheme adopting the dead-beat current controller which had been integrated with heuristic models of the voltage balancing and the switching loss characteristics. This scheme was further improved by Townsend et al. [111] in 2013 by incorporating the SVM technique to further reduce the switching losses and DC capacitor voltage ripple.

In 2012, Hagiwara et al. [31] presented a control method that creates a feedback loop of the circulating current in Single Delta Bridge Cells (SDBC) based STATCOM. The method allowed voltage of the DC capacitors to be controlled by not only limited to positive sequence reactive power but negative sequence reactive power as well and low frequency active power simultaneously. The experiment results based on the downscaled model of 100 V and 5 kVA have been documented and verified. Thus, the author has suggested that the SDBCs is applicable to a STATCOM for flicker compensation of arc furnaces.

In 2013, a voltage regulation converter scheme was presented by Cunha et al. [112] to regulate the voltage at the PCC feeding or draining a sinusoidal current with 90 degrees' displacement in relation to PCC voltages. An additional high frequency pole PI-controller was implemented in the PCC voltage loop control. The total and the differential of the voltage in the DC bus was closely regulated even under maximum reactive power mode. This was to maintain the voltage level at an adequate level despite different load steps to achieve a good dynamic response time.

In 2014, a capacitor voltage filtering control scheme for MCHI based STATOM was proposed by Farivar et al. [113]. The scheme cancelled the low frequency ripple of the capacitor's voltages which presented when smaller film capacitors were used. Cancellation of low frequency ripple was a very effective method to deal with high magnitude voltage ripple. The simulation results shown in the paper were based on three different cases which were: a sudden change in the reactive power reference, step change in the capacitor voltage reference, and grid voltage variation. Although the authors claimed that the proposed filtering scheme is not computationally demanding and only imposes negligible delay, the supporting results provided is not enough especially for the voltage variation in a grid-tied system.

In 2014, decoupling current vector controllers-based Synchronous Reference Frame (SRF) were proposed by Law and Dahidah [114] for a three-phase MCHI based STATCOM system to tackle the unbalanced grid-tie loading conditions. From this work, a new version of multilevel SHE-PWM technique was also employed to regulate both the positive and negative sequence variables. This ensured good power factor correction and balanced source current were attained at PCC. The authors [115] also proposed another new reactive current reference algorithm for MCHI based STATCOM with separated DC capacitors driven by CB-PWM technique in 2015. The rotated switching swapping scheme was used to regulate the voltage across each DC-link capacitor. The proposed algorithm was proven to improve the transient performance of the closed-loop with only P-controller and reduce the STATCOM current ripples.

In 2015, Geyer et al. [116] presented a MPC scheme for STATCOM system. The author [117] adopted and improved the load current prediction by an Extended Phase Locked Loop (EPLL) of the MPC scheme introduced in 2014 and successfully implemented with SDBC modular multilevel converter based STATCOM. This control scheme operated by manipulating the set-points of the subsequent PWM, where the STATCOM currents were regulated to achieve reactive power compensation, load balancing and current harmonic filtering at the PCC.

In 2015, Chunyan and Zhao [118] presented an individual phase instantaneous current control method to solve the problem of active power balance for the chained STATCOM under unbalanced voltage. The proposed method also avoided the complex decomposition of positive, negative and zero phases. Two extra compensation strategies (Reactive control mode & Voltage control mode) were used in the control scheme to solve the voltage imbalance problem. Both compensation modes have been verified under small unbalanced factor and changed unbalanced factor. However, the authors only verified the reactive control mode due to the limited experimental condition.

In 2016, Kumar et al [119] proposed a different control scheme of sliding mode controller approach comparing with Gupta et al [102], which was designed for cascaded two-level inverter-based grid-connected photovoltaic system. The controller maintains the maximum power delivered by the photovoltaic into the STATCOM system with the capability of supplying active and reactive power under different solar irradiance. Due to frequency variation in multiband hysteresis modulation causing higher switching loss, the author chose to use simple PWM modulation technique over space vector PWM technique. However, the proposed control schemes can only work under fixed switching frequency for all operating condition.

In 2017, Lu et al [120] established a linear relationship in negative sequence between both clustered active power and the modulation reference voltages in a dq-frame for star-connected cascaded H-bridge eleven-level STATCOM. This linear relationship allows active power in all three phases of the power system to be balanced with only a single clustered voltage balancing control.

The proposed voltage balancing control with P-controller has been tested under both symmetric and asymmetric grids. However, the presented experiment results still showed static errors even after the proposed voltage balancing control was activated.

In 2018, a flexible third harmonic control strategy was proposed by Ge and Gao [121] for compensating reactive power in low-capacitance cascaded H-bridge STATCOM. In order to prevent the DC capacitor of STATCOM to operate in overvoltage condition and suffer from low frequency oscillation due to the second harmonic component of DC voltage, the third harmonic voltage injection method was used to minimize the voltage stress and the switching losses on the semiconductors. In other words, the proposed control strategy reduced the instantaneous power of the DC capacitor by increasing the proportional gain in P-controller.

In 2018, Hou et al. [122] presented a general decentralized control scheme for cascaded H-bridge STATCOM, where the H-bridge modules were controlled independently by each local controller with no central controller in the whole STATCOM system. The local controller consisted of proposed reactive power control mode and active power control mode, which aimed to achieve voltage balancing in the DC-link as well as frequency synchronization. The author claims the computational burden has been lowered compare to the centralized control schemes as the burden was distributed to different local processors. However, it may not always be the case as the redundancy increases for some of the repetitive computational processes that occur independently across all the local processors.

In 2019, Nasiri et al. [123] demonstrated a new control set MPC in 15-level cascaded H-bridge STATCOM with energy storage capability for a short-term active power supply and reactive power compensation for wind farm applications. The different between [110], [116] and [117] was the author using Diophantine equations in domain of integers to optimize the dynamic performance, despite the input being searched over a large data set of switching combinations. The Diophantine solution reduced the switching combination

finding time and allowed all its redundancies to be generated in each sample time range by changing an integer variable.

In 2019, Gui et al [124] proposed a control strategy for exponentially stable tracking controller of STATCOM through port-controlled Hamiltonian system form. The proposed control strategy used dynamic extension algorithm based on input-output linearization framework with a bounded solution to the driven zero dynamics equation to regularize the performance of STATCOM. From results shown by the author, the proposed control strategy improved the transient performance especially in the inductive operating mode. However, it requires additional designed feedback damping in order to deal with the parameter uncertainty of STATCOM.

2.6 Chapter Summary

Detailed literature reviews on MCHI based STATCOM as well as various modulation techniques have been reported in order to strengthen the background of this research work. All the above-mentioned control schemes can be categorized into two main groups, linear and nonlinear. Linear controllers include conventional PI-controller (i.e. Stationary PI-controller and Synchronous Vector PI-controller), state feedback controller, and predictive techniques with constant switching frequency (i.e. Predictive and Deadbeat controller). On the other hand, nonlinear controllers comprise of Bang-Bang controllers (Hysteresis Current controller) and predictive controllers with on-line optimization which lead to new research trends such as Neural Networks controllers and Fuzzy-Logic based controllers that favors fully digital control. The main reason Current Vector PI-controller was chosen is due to its modular structure and simplicity in control even with higher number of levels which can improve the transient performance of the closed-loop simple structure and short calculation time. Drawbacks in nonlinear and fully digital controllers consist of complex computational algorithms and yet only provides moderate improvement which is caused by more losses in switching due to higher characteristics in multiband hysteresis modulation.

Chapter 3

Methodology

After having understood the characteristics of multi-level inverter based STATCOM, what follows is the designing of a MCHI's control scheme with IPD CB-PWM modulation technique, as well as the construction of a software MCHI prototype model based STATCOM. As the main purpose of this research work is to improve STATCOM's transient performance, a decoupling feed-forward current vector controller integrating reactive current reference i_{cq}" algorithm for PI-controller was designed based on the MCHI with separated DC capacitors which was first proposed by Law et al [115]. The switching pattern swapping scheme at every two fundamental frequency cycles is used to regulate the voltage across each DC-link capacitor of the STATCOM system.

In this work, the STATCOM is controlled to provide both reactive current compensation and active harmonic filtering for STATCOM either in single-phase or three-phase systems at the PCC with a dynamic varying reactive load system. The reason behind having multiple data collection of both single-phase and three-phase STATCOM system was to have better comparison and implementation of the designed controller to improve the transient performance of the desired STATCOM power system. The designed i_{cq}" algorithm enhances the transient performance of the closed loop system with PI-controller. STATCOM based on a five-level MCHI is presented in this work and the performance of the designed controller is studied through various simulation experiments using MATLAB-Simulink software for both steady-state and transient conditions.

3.1 The Derivation of Mathematical Model

The necessary parameters for developing the mathematical model for STATCOM system (e.g., grid voltage V_{pcc}, STATCOM voltage V_c, STATCOM output current i_c, and load current i_l) were extracted from the power grid and converted to dq-vector components via abc-to-dq transformation [125]. Mathematical derivation of closed-loop control for STATCOM system has been developed to

attain the total gain, K_{total}, of the preferable PI-controller based on the selection of operating switching frequency and passive components used in the proposed STATCOM model. Figure 3.1 below demonstrates the overall proposed STATCOM modeling work with block diagrams.

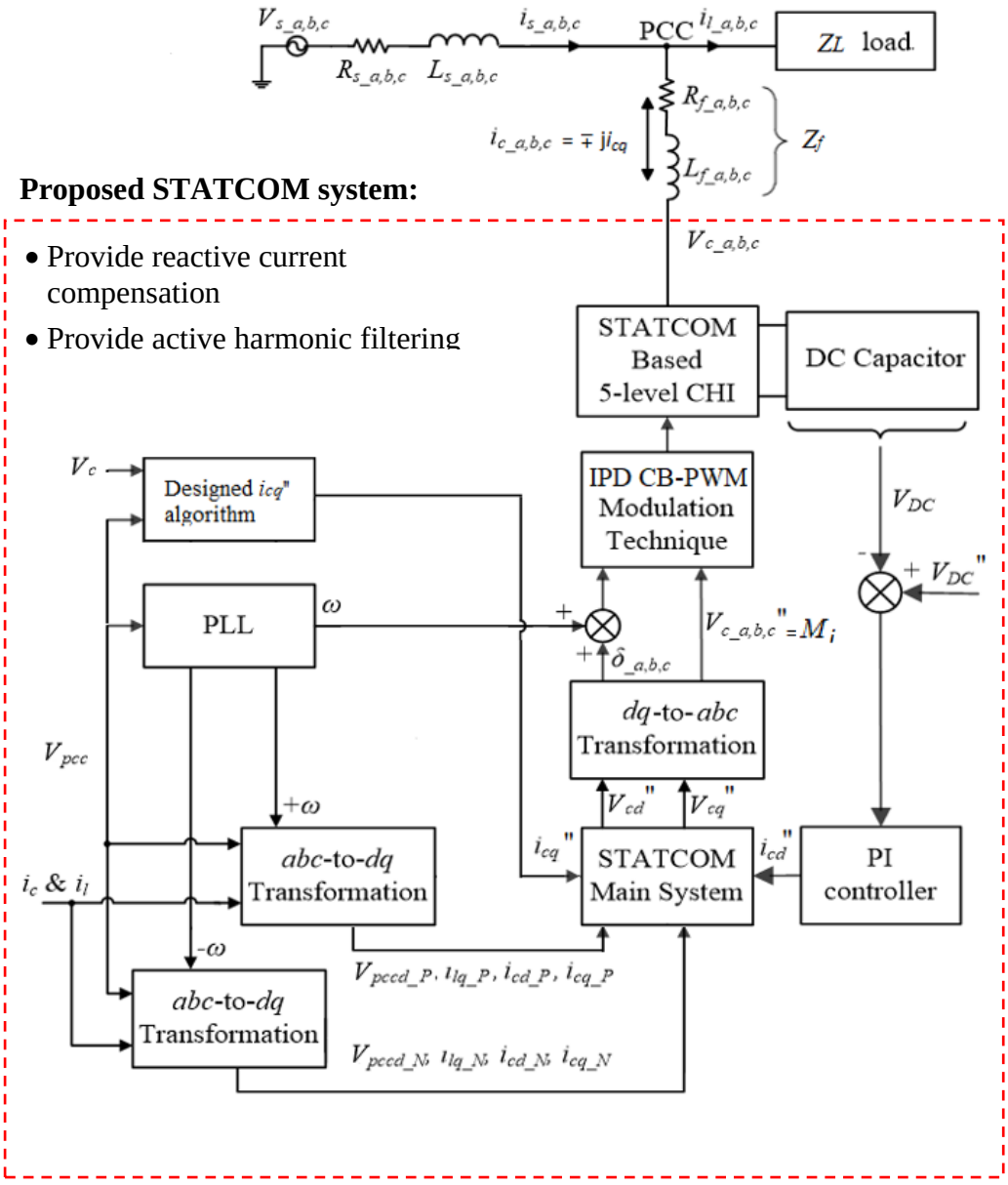

Figure 3.1 Block diagram of the proposed grid-tie STATCOM system

The amount of d-active and q-reactive current exchange through the coupling inductor Z_f is as in Equation (3.1):

$$i_c = \frac{V_{pcc} - V_c \angle \delta}{Z_f} = \; i_c \angle \varphi = \pm i_c \cos(\theta) \pm j i_c \sin(\theta) = \; \pm i_{cd} \; \pm j i_{cq} \tag{3.1}$$

where δ is the phase angle between the grid voltage V_{pcc} and STATCOM output voltage V_c, Z_f is the coupling impedance, φ is PF angle between i_c and V_{pcc}, i_{cd} is the active or real current used to charge and discharge the DC capacitor , and i_{cq} is the reactive current flowing through Z_f.

The desired STATCOM output voltages magnitude $V_c^{"}$ and its phase angle δ with respect to V_{pcc} is given as Equation (3.2) and (3.3):

$$V_{c\_abc}^{"} = \sqrt{\left(V_{cd\_P}^{"} - \; V_{cd\_P}^{"}\right)^2 + (V_{cq\_N}^{"} - \; V_{cq\_N}^{"})^2} \tag{3.2}$$

$$\delta_{\_abc} = tan^{-1}\left(\frac{V_{cq}^{"}}{V_{cd}^{"}}\right) \tag{3.3}$$

From equation (3.3), M_i is modulation index, $V_{cd/q\_P/N}$ values for both the positive and negative sequence of controllers from the PLL.

3.2 Designed Mode Selector Framework

The current references mode selector has been designed to assign an operational mode for MCHI to perform the selected mode function. Each operational mode has its own current reference and Figure 3.2 below illustrated the mode selector flowchart used to select the mode operation.

- Mode 1: Reactive Current Compensation
- Mode 2: Active Harmonic Filtering

Figure 3.1 shows the block diagram of the proposed grid-tie STATCOM system together with the designed control scheme. The STATCOM is

implemented in five-level inverter, where the phase voltages V_c are the total up of output voltage from positive V_{DC}, 0 and negative V_{DC} of each individual H-bridge inverter. The ability to switch ON/OFF corresponding occurs at the leg of the H-bridge inverter, which has two series-connected switching devices that prevents it from short circuiting at the DC-link by ensuring one of the leg is completely off before switching-on the another leg.

In order to derive equation (3.1), it is required to transform the load current i_{lq}, the STATCOM output voltage V_c, STATCOM output current i_c into *dq* constant vectors using 'Park Transformation' (see Appendix A) reference phase angle δ of V_{pcc} is dependent on the PLL. The feedback control of decoupling feed-forward current vector controller produces a set of switching signals by going through designed modulation technique to drive the power semiconductor switches of MCHI.

The STATCOM link inductor's transfer function can be defined in dq-coordinates as:

$$\begin{bmatrix} V_{cd} \\ V_{cq} \end{bmatrix} = \begin{bmatrix} V_{pccd} \\ V_{pccq} \end{bmatrix} - R_f \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} - L_f \frac{d}{dt} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \omega L_f \begin{bmatrix} i_{cq} \\ -i_{cd} \end{bmatrix} \tag{3.4}$$

Integrating equation (3.4) between sample current of (x) and $(x + 1)$ with respect to T_{id} and T_{iq} for *dq*-axes current vector controller, the average voltage of the *dq*-vectors can then be derived as follows:

$$\begin{aligned} V_{cd}(x, x+1) = {} & V_{pccd}(x, x+1) + \omega L_f i_{cq}(x, x+1) \\ & - R_f i_{cd}(x, x+1) - \frac{L_f}{T_{id}} [i_{cd}(x+1) - i_{cd}(x) \end{aligned} \tag{3.5}$$

$$V_{cq}(x, x+1) = -\omega L_f i_{cd}(x, x+1) = R_f i_{cq}(x, x+1) - \frac{L_f}{T_{eq}}[i_{cq}(x+1) - i_{cq}(x)] \quad (3.6)$$

Next, the STATCOM output currents at the following $i_{cd}(x+1)$ and $i_{cq}(x+1)$ are established to find the current references at the current $i_{cd}"(x)$ and $i_{lq}(x)$ as follows:

$$i_{cd}(x+1) = i_{cd}"(x) \quad (3.7)$$

$$i_{cq}(x+1) = i_{cq}(x) \quad (3.8)$$

Finding the linearity of equation (3.8) and (3.9) between sample current (x) and $(x+1)$ under the same sampling period,

$$i_{cd}(x, x+1) = \frac{1}{2} i_{cd}(x) + \frac{1}{2} i_{cd}"(x) \quad (3.9)$$

$$i_{cq}(x, x+1) = \frac{1}{2} i_{cq}(x) + \frac{1}{2} i_{lq}(x) \quad (3.10)$$

Let V_{pcc} be constant and equal to the voltage reference within the same sampling period:

$$V_{pccd}(x, x+1) = V_{pccd}(x) \quad (3.11)$$

$$V_{pccq}(x, x+1) = V_{pccq}(x) \quad (3.12)$$

From the relationship of equation (3.11) and (3.12), V_c of both dq-frame are equal to:

$$V_{cd}(x, x+1) = V_{cd}"(x) \tag{3.13}$$

$$V_{cq}(x, x+1) = V_{cq}"(x) \tag{3.14}$$

It is worth noting that $V_{pccq}(x)$ is equal to 0 due to no reactive and by substituting (3.7)–(3.14) into (3.5) and (3.6), the resultant dq-voltage reference values are obtained as follows:

$$V_{cd}"(x) = V_{pccd}(x) - R_f i_{cd}(x) + \omega L_f \left[\frac{1}{2} i_{cq}(x) + \frac{1}{2} i_{lq}(x)\right] - K_{p\_id}[i_{cd}"(x) - i_{cd}(x)] \tag{3.15}$$

$$V_{cq}"(x) = -R_f i_{cq}(x) - \omega L_f \left[\frac{1}{2} i_{cd}(x) + \frac{1}{2} i_{cd}"(x)\right] - K_{p_{iq}}[i_{lq}(x) - i_{cq}(x)] \tag{3.16}$$

The proportional gain $K_{p\_i(d,q)}$ of the PI-controller is given by

$$K_{p\_i(d,q)} = \frac{L_f}{T_{i(d,q)}} + \frac{R_f}{2} \tag{3.17}$$

Let the total gain of the PI-controller K_{total} with respect to controller-poles (s) be equal to:

$$K_{total}(s) = \frac{K_p(s) + K_i}{S} = K_p + \frac{K_i}{S} \quad (3.18)$$

Although the actual STATCOM control system having non-linear elements such as saturation effects and is a discrete time or sampled data system, the model developed according to the designed algorithm is useful for determining reasonable values of K_p and K_i for a given STATCOM application.

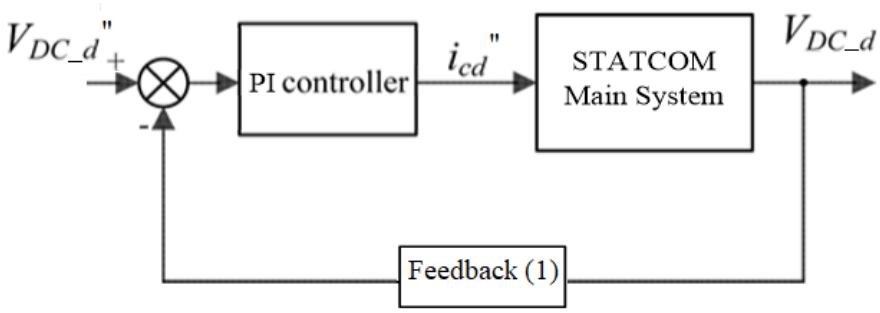

Figure 3.2 Flowchart of the feedback loop

From the figure 3.2, the feedback loop gain K_{loop} has been designed and derived as:

$$K_{loop}(s) = \left(\frac{K_p}{L_f(S)}\right) * \left(\frac{S + \frac{K_i}{K_p}}{S + \frac{R_f}{L_f}}\right) \quad (3.19)$$

It is noted that the controller-pole (s) is very near to the origin where:

$$s = -\left(\frac{R_f}{L_f}\right) \quad (3.20)$$

The magnitude and the phase of the loop gain initiate to decrease from relatively low frequency. Thus, the controller-pole (s) is first canceled by the

compensator zero where $(s) = \frac{(-K_i)}{K_p}$, and the loop gain of the ideal case study to be set in the form as:

$$K_{loop}(s) = \left(\frac{K_p}{L_f(S)}\right) \tag{3.21}$$

Then the feedback loop transfer function G_{loop} is written as:

$$\left(\frac{K_{loop}(s)}{1+ K_{loop}(s)}\right) = G_{loop} = \frac{1}{T_{i(d,q)}\,(s) + 1} \tag{3.22}$$

Thus, the relationship of integral gain $K_{i\_i(d,q)}$ of the designed PI-controller with respect to the $K_{p\_i(d,q)}$, which is shown in equation (3.17) can be derived as:

$$K_{i\_i(d,q)} = \frac{L_f}{(2T_{i(d,q)})^2} \tag{3.23}$$

And by substituting both $K_{p\_i(d,q)}$ and $K_{i\_i(d,q)}$ into equation (3.18), the total gain of the PI-controller K_{total} with respect to controller-poles (s) can be found:

$$K_{total}(s) = \left(\frac{L_f}{T_{i(d,q)}} + \frac{R_f}{2}\right) + \frac{\frac{L_f}{(2T_{i(d,q)})^2}}{(S)}$$

$$= \left(\frac{2L_fT_{i(d,q)}+L_f(S)}{(2T_{i(d,q)})^2}\right) + \frac{R_f}{2} \tag{3.24}$$

Hence, the desired STATCOM output voltage magnitude $V_c^{"}$ and its phase angle δ with respect to V_{pcc} are given as follows:

$$V_{c\_a,b,c}{}^{"} = \sqrt{(V_{cd}{}^{"})^2 + (V_{cq}{}^{"})^2} = M_i \tag{3.25}$$

$$\delta_{a,b,c} = \tan^{-1}\left(\frac{V_{cq}^{"}}{V_{cd}^{"}}\right) \quad (3.26)$$

3.2.1 Mode 1: Reactive Current Compensation

Figure 3.3 shows the implementation of the resulted STATCOM dq-voltage reference values given by equation (3.25) and (3.26).

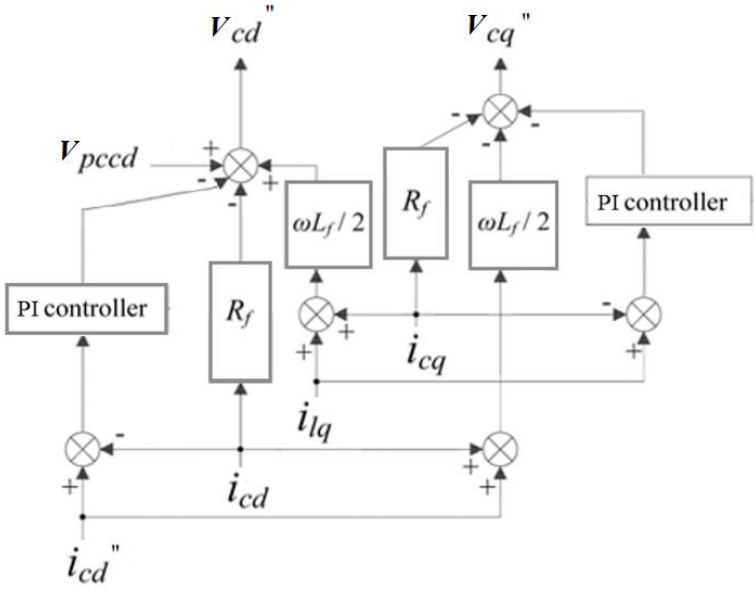

Figure 3.3 Block diagram of current decoupling control with PI-controller

Referring to Figure 3.1, the amount of the DC-voltage levels V_{DC_dq} is controlled by following the current reference i_{cd}" in the voltage control feedback loop and the current i_{cd} of the MCHI as well as the total DC-capacitance C of the H-bridges (2 units) via a PI-controller based on total gain as shown in equation (3.24) and can be calculated as such:

$$i_{DC\_dq} = C_{DC}\frac{dV_{DC\_dq}}{dt} \quad (3.27)$$

DC-link capacitors require only the d-axis current component to operate and all the q-axis components can be ignored. The average magnitude of active current vector within the sample periods x to $(x + 1)$ can be calculated by integrating equation (3.27) given as:

$$i_{DC\_d}(x, x+1) = \frac{C_{DC}}{T_{vd}} V_{DC\_d}(x, x+1) \tag{3.28}$$

The total amount of the V_{DC_d} across the DC-link capacitors with the constant current I_{DC_d} is shown as:

$$V_{DC\_d}(x+1) = V_{DC\_d}"(x) \tag{3.29}$$

$$i_{DC\_d}(x, x+1) = i_{cd}"(x) \tag{3.30}$$

Applying equation (3.29) and (3.30) into (3.28) to calculate the resultant current reference value:

$$i_{cd}"(x) = \frac{C_{DC}}{T_{vd}} \left[V_{DC\_d}"(x) - V_{DC\_d}(x) \right] \tag{3.31}$$

Referring to the block diagram in Figure 3.2, set the 1 per unit of DC-voltage reference $V_{DC\_d}"$ to find the total gain K_{total_vd} for the PI-controller as per the equation shown below:

$$K_{total\_vd} = \frac{C_{DC}}{T_{vd}} \tag{3.32}$$

The designed i_{cq}" algorithm is derived from learning the difference between the controlled voltage V_{cc}", voltage drop V_{Lf} across the coupling inductor L_f and grid voltage V_{pcc}.

$$V_{cc}" = \sqrt{\left(v_{pccd} + \omega L_f i_{lq}\right)^2 + \left(\omega L_f i_{cd}"\right)^2} \tag{3.33}$$

$$V_{Lf} = \sqrt{\left(\omega L_f i_{cd}"\right)^2 + \left(\omega L_f i_{lq}\right)^2} \tag{3.34}$$

Calculating the i_{cq}" by setting the V_{cc}" to 1p.u as an ideal STATCOM voltage V_c in steady-state operating point:

$$i_{cq}" = \frac{1-\left(\omega L_f i_{cd}"\right)^2-\left(\omega L_f i_{lq}\right)^2-V_{pccd}^2}{(2)\left(V_{pccd}\right)(\omega L_f)}$$

$$= \frac{1-V_L^2-V_{pccd}^2}{(2)\left(V_{pccd}\right)(\omega L_f)} \tag{3.35}$$

The designed i_{cq}" algorithm is used to find the voltage difference and use a feed-forward decoupling control scheme to provide a suitable counter reaction to reduce the reactive current ripples of STATCOM as shown in the block diagram in Figure 3.5 below.

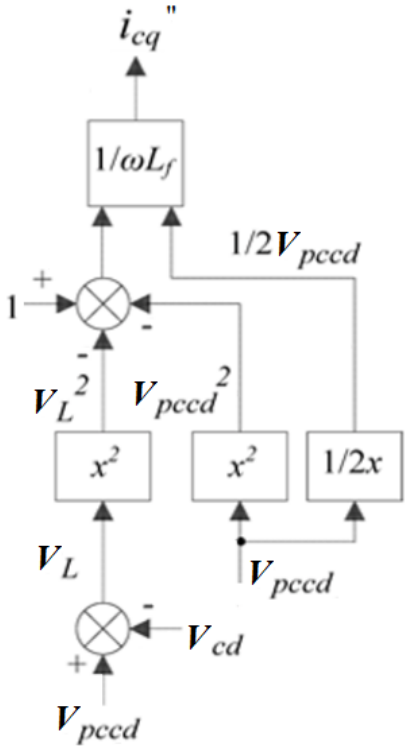

Figure 3.4 Block diagram of designed reactive current reference i_{cq}"

Lastly, the i_{cq}" is applied to the load reactive current i_{lq} in equation (3.8) to calculate the final dq-voltage reference as:

$$V_{cd}"(x) = V_{pccd}(x) - R_f i_{cd} + \frac{\omega L_f}{2}\left[i_{cq}(x) + \left(i_{lq}(x) + i_{cq}"\right)\right] - K_{total\_id}[i_{cd}"(x) - i_{cd}(x)] \quad (3.36)$$

$$V_{cq}"(x) = -R_f i_{cq}(x) - \frac{\omega L_f}{2}[i_{cd}(x) + i_{cd}"(x)] - K_{total\_iq}\left[\left(i_{lq}(x) + i_{cq}"\right) - i_{cq}(x)\right] \quad (3.37)$$

3.2.2 Mode 2: Active Harmonic Filtering

After the STATCOM main system performs the reactive current compensation with equation (3.36) and (3.37), the controller acts as a checker for the availability of harmonic in the system. Once the harmonic been detected, the current controller then tunes the STATCOM current reference i_c" based on:

$$i_{c\_a,b,c}" = i_{l\_a,b,c} - i_{cd}" - i_{cq}" \tag{3.38}$$

The current ripple caused by the inverter switches can be minimized by implementing the coupling inductor. By assuming the active harmonic filter voltage V_{ahf} is double of the PCC voltage V_{pcc}, the coupling inductor L_f can be calculated by using equation (3.39)

$$L_f = \frac{2V_{ahf} - V_{pcc}}{2\pi f_{cut} \times i_{c\_a,b,c}"} \tag{3.39}$$

where f_{cut} represents the cut off frequency when it reaches double the fundamental frequency and $i_{c\_a,b,c}$" is the maximum rms of STATCOM current.

The capacitor C_{DC} at H-bridge inverter acts as an energy storage element and it can be calculated by using a similar method as L_f which is expressed as:

$$C_{DC} = \frac{\frac{i_{c\_a,b,c}"}{2V_{ahf} - V_{pcc}}}{2\pi f_{cutoff}} \tag{3.40}$$

3.3 Summary for the Designed Mode Selector Framework

The designed reactive current reference i_{cq}" algorithm and total gain K_{total} for PI-controller have been utilized as well as mathematically proven to be able to improve transient performance through decoupling feed-forward current vector for five-level MCHI based STATCOM with separated DC capacitors, which can be applied in both single and three-phase system. Both reactive current compensation and active harmonic filtering control mode formulation have been presented. On top of that, the designed mode control system is able to reduce the effect of inherent PLL delay to prevent STATCOM from showing huge current fluctuations.

Chapter 4

Implementation and Validation

In this chapter, the proposed simultaneous functionalities compensator has been tested and integrated with the ability to perform two main operational modes (i.e. Mode 1 and Mode 2). Each mode has a specific current reference i_{mod}^{*} that obtained through instantaneous current control method. After the mode is selected, the measured MCHI output current was subtracted from the load current reference i_l and sent the result of true signal to STATCOM main system as compensator current reference i_{cpr}^{*}. Then, PLL was assigned to synchronize the MCHI output current with the voltage V_{pcc} which to be used in the MCHI.

4.1 Implementation of the Designed Mode Selector

Intensive simulation studies have been carried out using MATLAB-Simulink based on the fundamental mathematical derivation of STATCOM controller's parameters as well as the steady-state and small-signal equivalent circuits of the proposed MCHI based STATCOM system. The simulation model for both single-phase and three-phase have been tested in order to study of the performance of the proposed mode selector controller such as:

- Mode 1: Reactive Current Compensation
- Mode 2: Active Harmonic Filtering

From the block diagram shown in Figure 4.1, a mode selector block was introduced alongside with the PI-controller to determine the operating mode of the MCHI based STATCOM system.

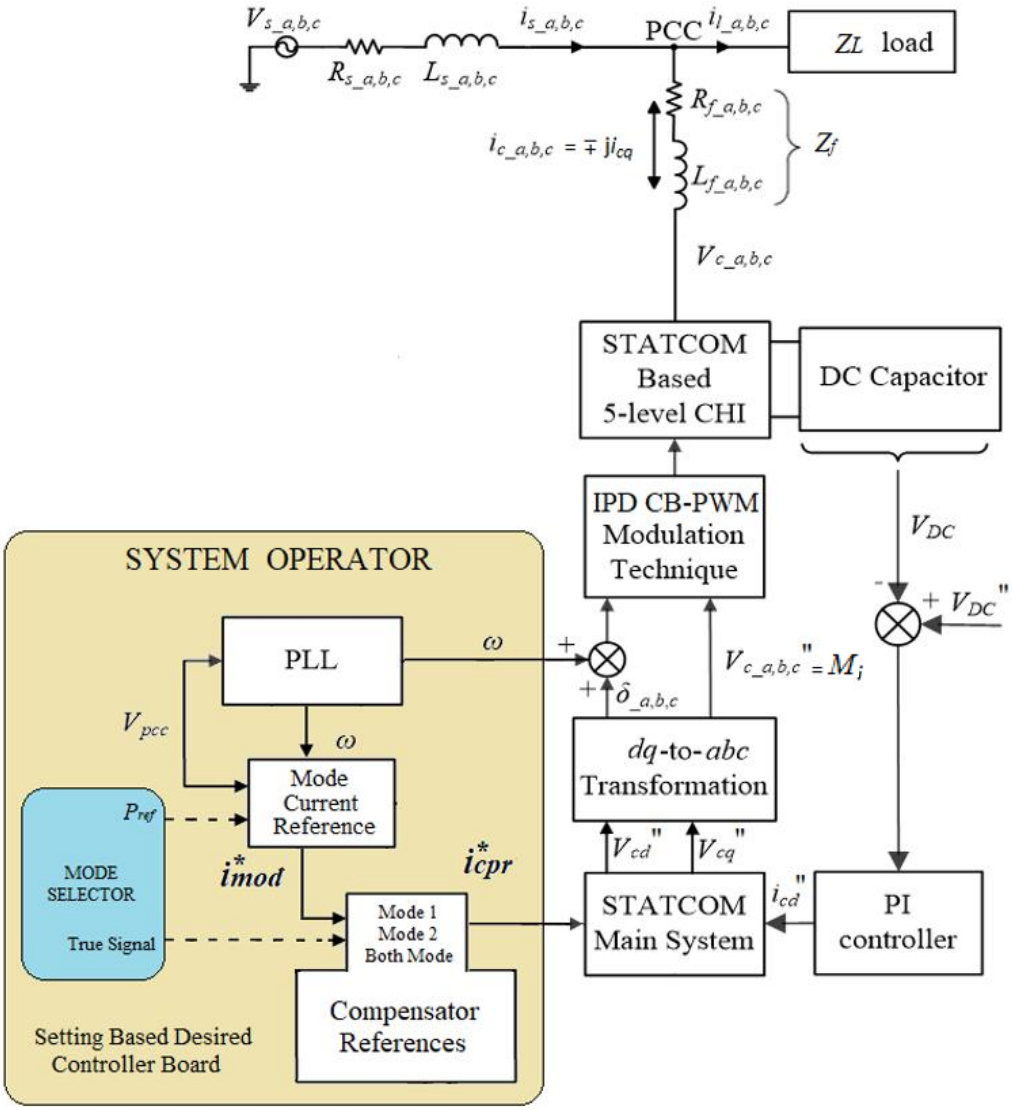

Figure 4.1 Block diagram of the designed mode selector

The designed mode selector is responsible for choosing the operation mode with the assumption that there is an external agent or intelligent control board which also known as system operator. The system operator has been established for continuous checking on the STATCOM system and sending the required information back to the mode selector. Other assumptions which also needs to be considered such as phases of STATCOM system is in balanced condition and the grid does not required active power injection from STATCOM as well as having enough grid power supply when the load demand is high while designing the mode selector. This is because the decision of the mode selector is based on the analysis

of the power quality consists of knowing the THD and the voltage magnitude at the PCC.

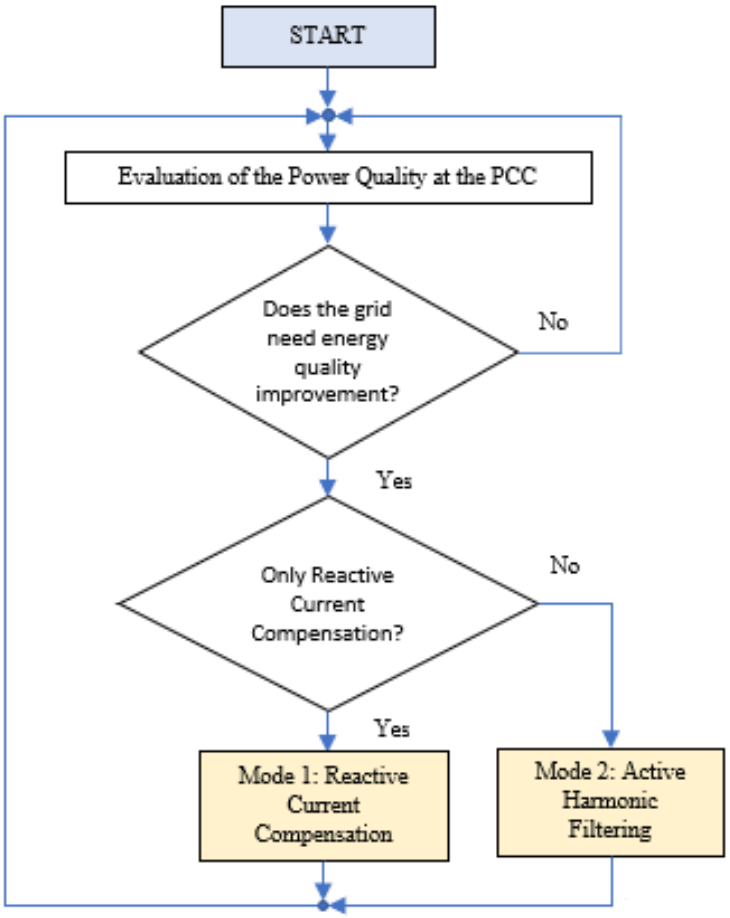

Figure 4.2 Flowchart of the mode selector

The flowchart of the mode selector shown in Figure 4.2 was drawn based on the required grid power quality, where the PCC current is set with respect to its fundamental value and the voltage range from 0.95 to 1.05 p.u. As soon as the mode current reference has received the information signal P_{ref} from the system operator in the mode selector, the next action is to evaluate the power quality at the PCC with respect to PLL. If the percentage of difference for PCC current is 5 % off compare to its fundamental or the voltage is out of the setting range, then STATCOM system will operate to improve the power quality of the grid.

After that STATCOM system will decide if the compensation to be both mode 1 and 2 or single mode compensator. Both mode 1 and 2 means STATCOM system supplying all the reactive energy and filtering the harmonic currents from the non-linear load. This is when both the percentage of difference for PCC current is off compare to its fundamental and the voltage is out of the setting range. On the other hand, single mode compensator means either reactive energy or harmonic currents compensation to be take place in the STATCOM system. Reactive current compensation happens when the percentage of difference for PCC current is 5 % lower than its fundamental and the voltage is within or lower than the setting range. Harmonic currents compensation happens when the percentage of difference for PCC current is 5 % higher than its fundamental and the voltage is higher than the setting range.

From the way how the mode selector works, communication between the STATCOM system and the system operator is essential. In the system operator, the mode current reference i^*_{mod}, where $i^*_{mod\_1}$ for mode 1 and $i^*_{mod\_2}$ for mode 2 plays an important role in getting the essential compensator current reference i^*_{cpr} to be send to STATCOM main system for selecting the right compensation mode to be carry out.

The formulation to calculate i^*_{mod} for both mode 1 and 2 have been derived as below with $i^*_{mod} = i_{l\_a,\,b,\,c}$:

Mode 1: Reactive Current Compensation

$$i^*_{mod\_1} = i_{load} - i_{real} - i_{residual} = i_{reactive} \tag{4.1}$$

Mode 2: Active Harmonic Filtering

$$i^*_{mod\_2} = i_{load} - i_{real} - i_{reactive} \tag{4.2}$$

In time domain (t) for given voltage $V_c(t)$ and current $i_c(t)$, the real current i_{real} responsible for the grid real power, reactive current $i_{reactive}$ and residual current $i_{residual}$ of the STATCOM as:

$$i_{s\_real}(t) = \frac{V_c(t) \times i_c(t)}{||V_c||^2} V_c(t) \quad (4.3)$$

$$i_{s\_reactive}(t) = \frac{V_c"(t) \times i_c(t)}{||V_c||^2} V_c"(t) \quad (4.4)$$

$$i_{s\_residual}(t) = i_c(t) - i_{s\_real}(t) - i_{s\_reactive}(t) \quad (4.5)$$

As the current controller is based PI-control with feedforward compensation, this is enough to make the current follow the reference disregard the operation mode. Referring to Figure 4.1, the MCHI terminal voltage V_c can be written as:

$$V_c(t) = V_{DC}(t) \quad (4.6)$$

$$V_{DC}(t) = L_f \frac{di^*_{cpr}(t)}{dt} + R_f i^*_{cpr}(t) + V_{PCC}(t) \quad (4.7)$$

When MCHI transfer function in (s) pole domain, the resistance losses can be ignored and treating the PCC voltage as disturbance:

$$i_{cpr}(s) = \frac{V_{DC}(s)}{L_f(s)} \quad (4.8)$$

Thus, the close-loop feedback transfer function of the PI-controller can be written as:

$$\frac{i_{cpr}(s)}{i^*_{cpr}(s)} = \frac{V_{DC}(s) K_{total}(T+1)}{(s)^2 T L_f + (s) T K_{total} V_{DC} + K_{total} V_{DC}} \quad (4.9)$$

where K_{total} and T are the total PI-controller gain and fundamental switching time constant which has been scaled at 20ms, respectively. The PI-parameters can be tuned for any desired requirements.

Referring to equation (3.35) in Chapter 3, relationship of i^*_{cpr} and $i_{cq}"$ for reactive current compensation can be derived as:

$$i_{cpr}^{*} = i_{lq} + i_{cq}" \tag{4.10}$$

The damping ratio is derived as:

$$\zeta = \frac{1}{2}\sqrt{\frac{TK_{total}V_{DC}}{L_f}} = 1 \tag{4.11}$$

4.2 Validation of the Designed Mode Selector

The single-phase STATCOM simulation model based five-level MCHI has been developed and numerous simulations have been conducted to validate the designed mode selector with IPD CB-PWM technique as the modulation technique. The MATLAB-Simulink simulation was done based on the automatic code generation according to the chosen controller board dSPACE-DS1104 target as a reference for the simulation validation purposes. The mode selector is not limited to any specific controller board. Table 4.1 presents the setup parameters.

Table 4.1 Parameters of STATCOM system used in MATLAB-Simulink simulation

Parameter	Symbol	Value
Load apparent power	S_l	1.44 kVA
Grid voltage	V_{pcc}	240 V_{rms} = 1 p.u
Grid current	i_s	6 A_{rms}
Grid resistor	R_s	0.4 mΩ
Grid inductor	L_s	12.7 mH
Grid impedance	Z_s	4 Ω
Coupling resistor	R_f	4 Ω

Coupling inductor	L_f	127 mH
Coupling impedance	Z_f	40 Ω
Load current	i_l	4 Arms
Fundamental frequency	f	50 Hz
Switching frequency	f_{sw}	1.6 kHz
Sampling frequency	f_{sam}	9.6 kHz
DC Capacitance of the H-bridges	C_{DC}	5000 µF
Proportional current gain for PI-controller	K_{p_i}	0.21
Integral current gain for PI-controller	K_{i_i}	3.97
Total current gain for PI-controller with the $(s) = i_s$	K_{total}	0.87
Total voltage gain for PI-controller	K_{total_vd}	0.25
Time constant/ Fundamental switching time	T	20 ms

The inductive load $R_L L_L$ and capacitive load $R_L C_L$ can be calculated with the given power factor 0.67 lagging and leading respectively by dividing load current i_l with grid current i_s which also can be written as:

$$PF = \frac{P_L}{Z_L} = 0.67 \tag{4.12}$$

$$P_L = PF \times S_L = 0.67 \times 1440 = 960 \text{ W} \tag{4.13}$$

$$R_L = \frac{V_s^2}{P_L} = \frac{240^2}{960} = 60 \ \Omega \tag{4.14}$$

$$L_L = \frac{X_L}{2\pi f} = \frac{60}{2\pi \times 50} = 190 \text{ mH} \tag{4.15}$$

$$C_L = \frac{1}{X_c \times 2\pi f} = \frac{1}{60 \times 2\pi \times 50} = 53 \ \mu\text{H} \tag{4.16}$$

Where P_L represent the power of the inductive load in watt, R_L is the resistive of the load, L_L is the inductive of the load and C_L is the capacitive of the load.

4.2.1 Simulation Results of Mode 1

The simulation result for the designed MATLAB-Simulink model for Mode 1 (see Appendix B) was shown in this section. The simulation studied the characteristic of a linear single-phase reactive load which changes from $R_L L_L$ to $R_L C_L$ as the PF changes from lagging to leading at the time of 1s. The assumption made was the system in balanced condition as well as the load. Thus, the result for single-phase can be uses to represent as a three-phase system. Figure 4.3 and 4.4 present the performance of STATCOM in response to a step change in load.

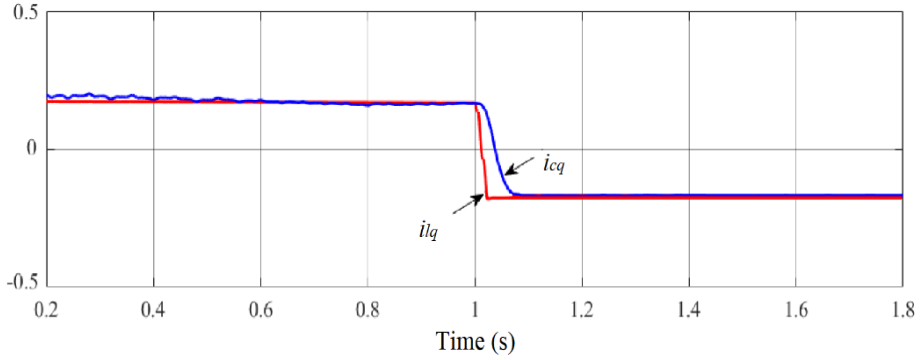

Figure 4.3 Mode 1 simulation result of step change in the load current i_{lq} without the designed i_{cq}" algorithm

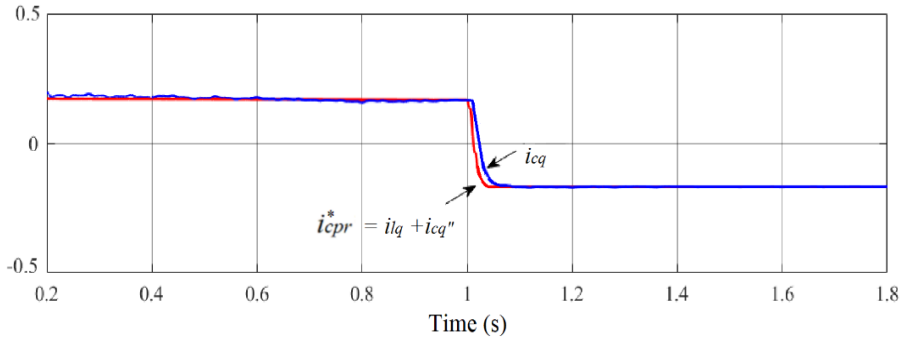

Figure 4.4 Mode 1 simulation result of step change in the load current i_{lq} with the designed i_{cq}" algorithm as current compensator i^*_{cpr}

By comparing Figure 4.3 and 4.4, it can be seen that the STATCOM steady-state error and the transient response have been significantly improved after the designed i_{cq}" algorithm been applied in the system operator which produce i^*_{cpr} as the current compensator reference for the STATCOM main system. A zoomed view of Figure 4.4 is also presented in Figure 4.5 where it is evidently shown that the STATCOM transient response during the step change of load has been recorded as 0.05s or 50ms, which it is a short period of time. This hugely improved the transient response time compare to similar individual phase instantaneous current control method used by Chunyan and Zhao [118]. It is worth mentioning that the oscillation of the measured STATCOM reactive current i_{cq} has been mitigated without applying any additional filtering circuit.

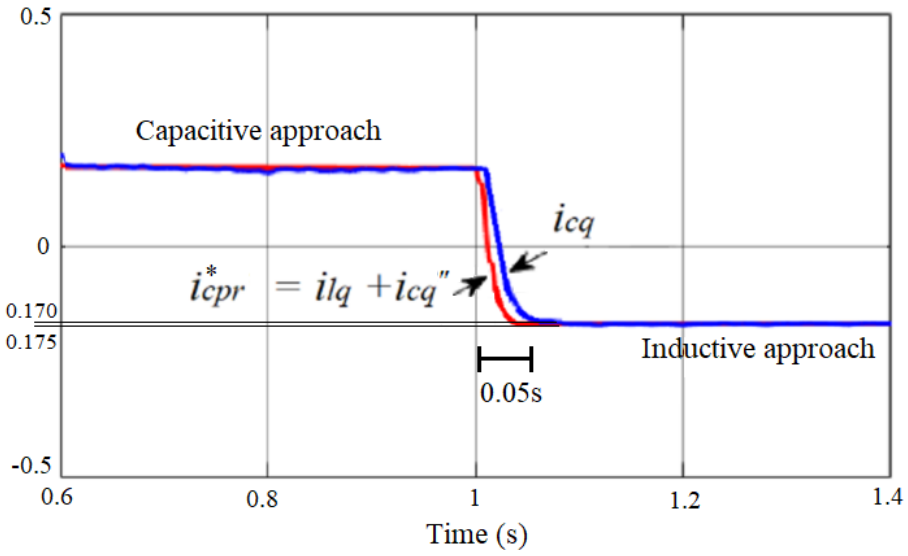

Figure 4.5 Zoomed view of Figure 4.4 with the designed i_{cq}" algorithm as current compensator i^*_{cpr}

The compensation accuracy *CA* in percentage of i_{cq} with respect to i^*_{cpr} in p.u can be calculated by the formula as:

$$CA = \left|\frac{i_{cq}}{i^*_{cpr}}\right| \times 100\ \% = \frac{0.170}{0.175} \times 100\ \% = 97\ \% \qquad (4.17)$$

From Figure 4.1, the DC voltage level across each DC-link capacitor is maintained constant using the switching pattern swapping scheme to maintain the low switching losses and stable power handling between the H-bridges. This is to achieve shorter transient response time during the load changing from $R_L L_L$ to $R_L C_L$. When the DC peak voltage V_{DC} is more than grid peak voltage V_{pcc}, the STATCOM is operating in capacitive approach to inject reactive current into the power system. On the other hand, when the STATCOM operates in an inductive approach means the V_{DC} is lesser than V_{pcc} for absorbing reactive current from the power system. This relationship has been explained in Table 4.2 below.

Table 4.2 Relationship of STATCOM operating approaches and loads

STATCOM operating approach	Indication with V_{DC} and V_{pcc}	Characteristic of the load	Reactive current in the power system
Capacitive approach	$V_{DC} > V_{pcc}$	Inductive load, $R_L L_L$	Injecting reactive current
Inductive approach	$V_{DC} < V_{pcc}$	Capacitive load, $R_L C_L$	Absorbing reactive current

The effect caused by the processing delay at half of the fundamental cycle which required by PLL to synchronize the phase angle δ with the STATCOM output voltage V_c on the grid current i_s during the load variation phases have been illustrated in Figure 4.6 below. Because of this effect, more oscillations exhibited in the grid real and reactive current as VAR exchange occurs between STATCOM and the transmission lines during the load changes moment as shown in Figure

4.6(a). When the designed i_{cq}" algorithm been applied to the decoupling feed-forward current vector controller, the oscillations in the grid reactive current $i_{s\_reactive}$ is substantially reduced by half as shown in Figure 4.6(b).

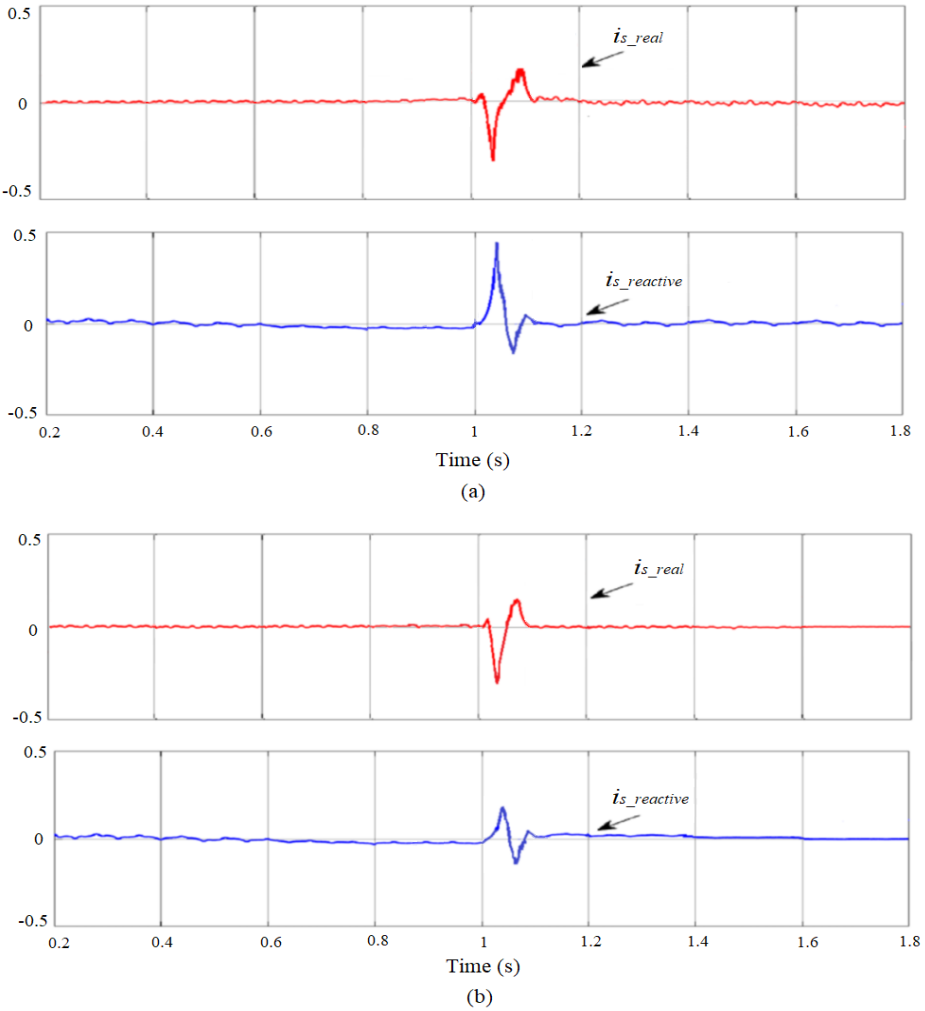

Figure 4.6 Mode 1 simulation result of grid real current i_{s_real} and reactive current $i_{s\_reactive}$ (a) without and (b) with the designed i_{cq}" algorithm

Figure 4.7 has presented the simulation where the load changing at time 1s for both load voltage V_l and load current i_l with the designed i_{cq}" algorithm. It is also worth to note that the current is in phase with the voltage. As reactive load changes from $R_L L_L$ to $R_L C_L$, simulation result for both STATCOM operating approaches which consists of capacitive and

inductive have been presented in Figure 4.8 with time frame of 0.8-0.9s and 4.9 with the time frame of 1.4-1.5s.

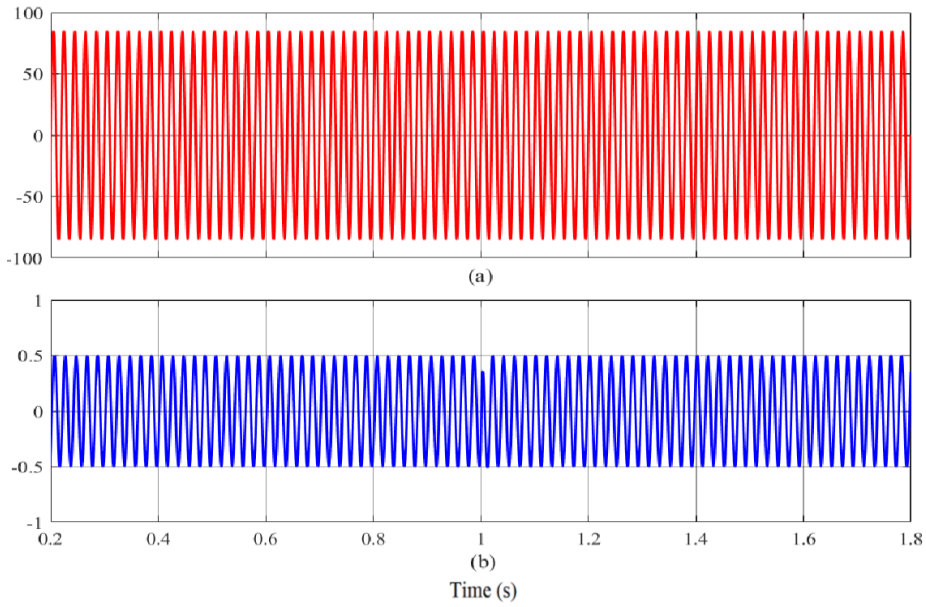

Figure 4.7 Overall Mode 1 simulation result for (a) load voltage V_l and (b) load current i_l

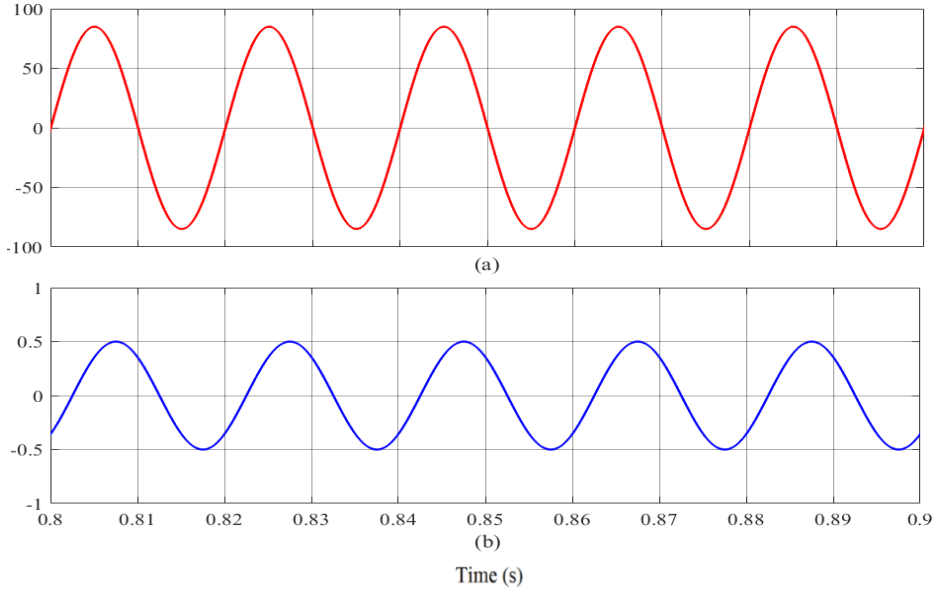

Figure 4.8 Zoomed view of Figure 4.7 when the STATCOM is operating in capacitive approach

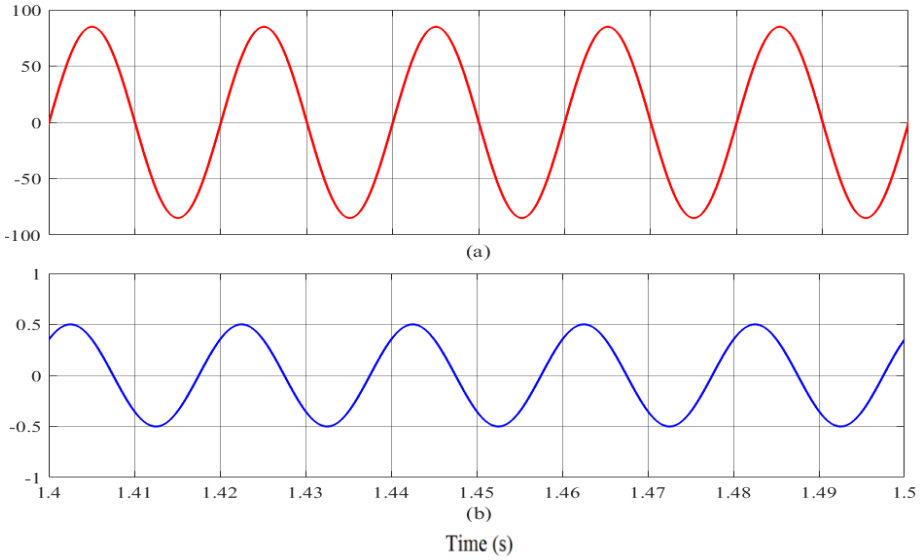

Figure 4.9 Zoomed view of Figure 4.7 when the STATCOM is operating in inductive approach

Figure 4.10 has presented the simulation where the load changing at time 1s for both grid voltage V_s and grid current i_s with the designed i_{cq}" algorithm. As reactive load changes from $R_L L_L$ to $R_L C_L$, simulation result for both STATCOM operating approaches which consists of capacitive and inductive have been presented in Figure 4.11 and 4.12.

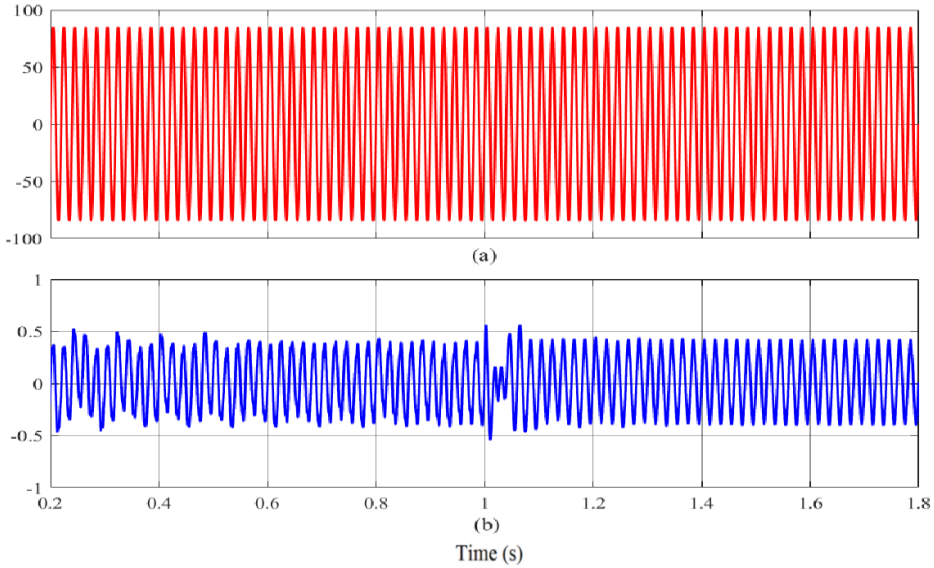

Figure 4.10 Overall Mode 1 simulation result for (a) grid voltage V_s and (b) grid current i_s

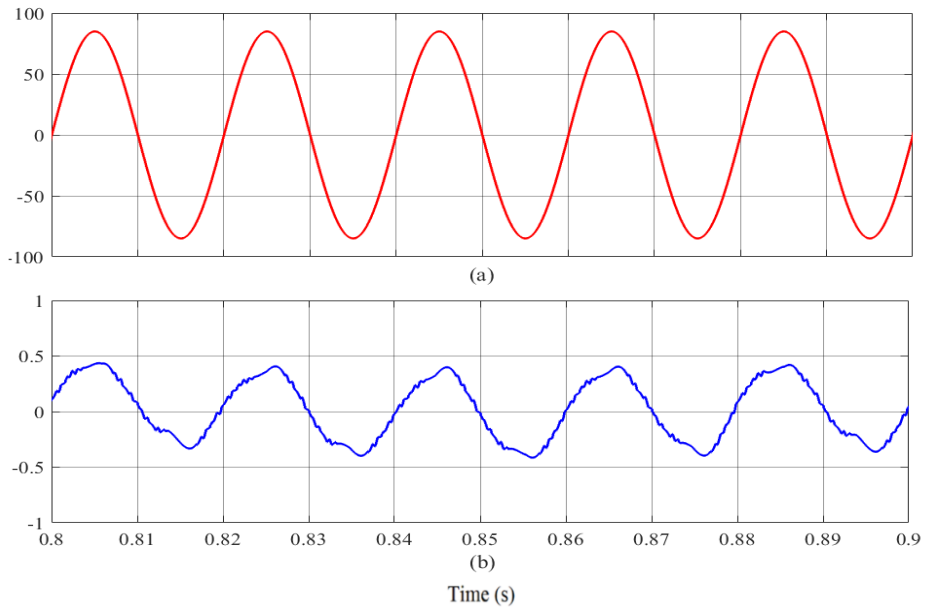

Figure 4.11 Zoomed view of Figure 4.10 when the STATCOM is operating in capacitive approach

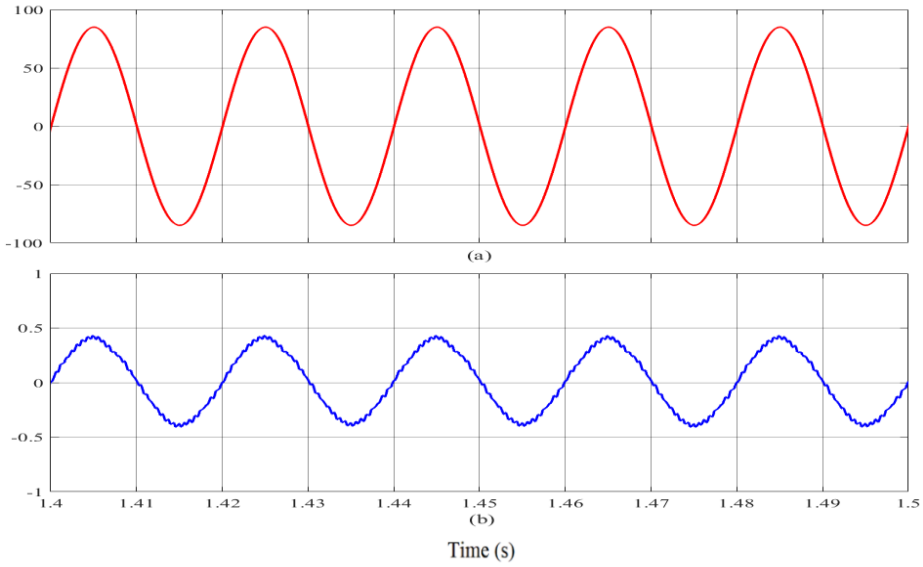

Figure 4.12 Zoomed view of Figure 4.10 when the STATCOM is operating in inductive approach

Figure 4.13 has presented the simulation where the load changing at time 1s for both STATCOM voltage V_c and STATCOM current i_c with the designed i_{cq}" algorithm. As reactive load changes from $R_L L_L$ to $R_L C_L$,

simulation result for both STATCOM operating approaches which consists of capacitive and inductive have been presented in Figure 4.14 and 4.15.

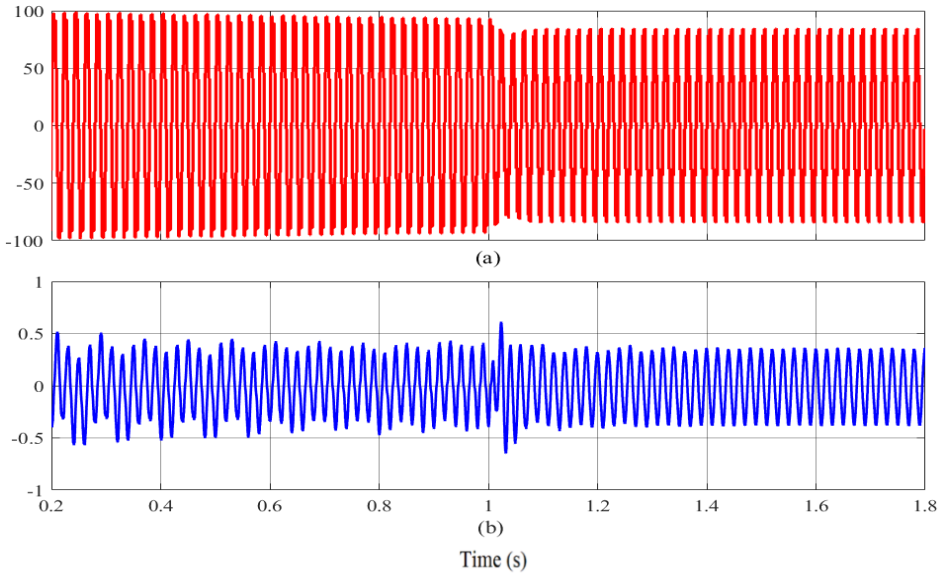

Figure 4.13 Overall Mode 1 simulation result for (a) STATCOM voltage V_c and (b) STATCOM current i_c

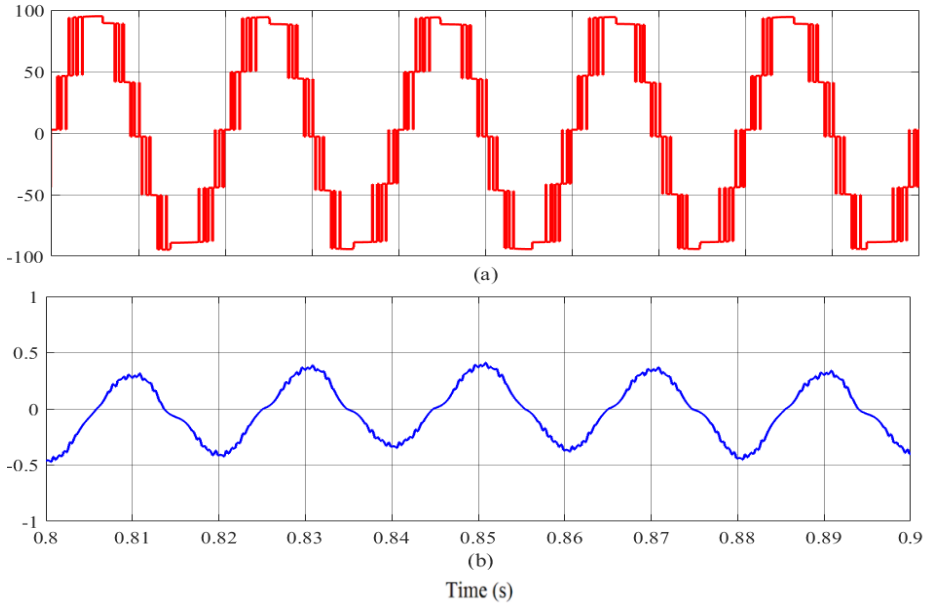

Figure 4.14 Zoomed view of Figure 4.13 when the STATCOM is operating in capacitive approach

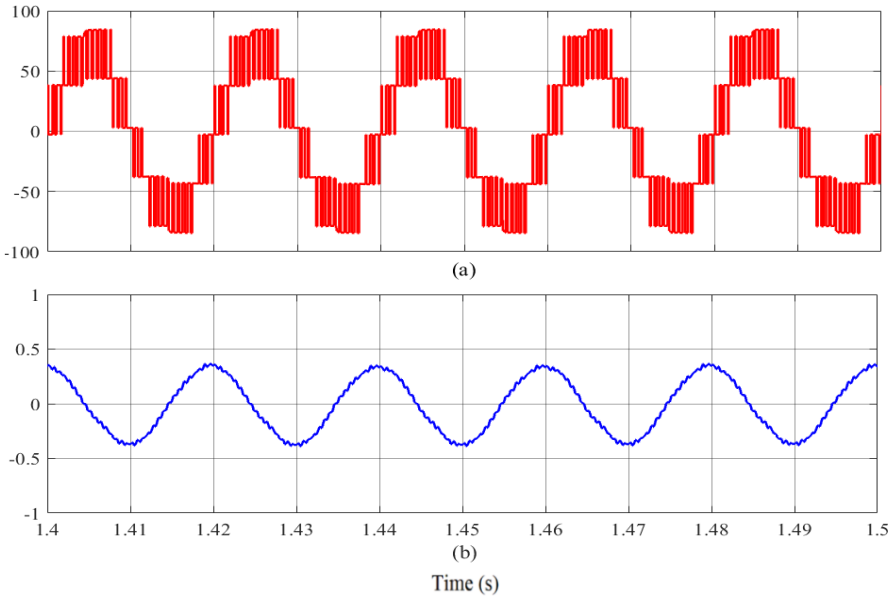

Figure 4.15 Zoomed view of Figure 4.13 when the STATCOM is operating in inductive approach

In Figure 4.16 and 4.17, the Fast Fourier Transform (FFT) analysis has been used to find the THD for both STATCOM operating approaches with respect to STATCOM voltage V_c. The result has shown that, the Mode 1 can accurately performs reactive current compensator in the proposed simultaneous functionalities compensator based designed i_{cq}" algorithm. The total harmonic distortion for the system with respect with V_c, when the STATCOM operating in capacitive approach is 23.10 % and 35.57 % when the STATCOM operating in inductive approach.

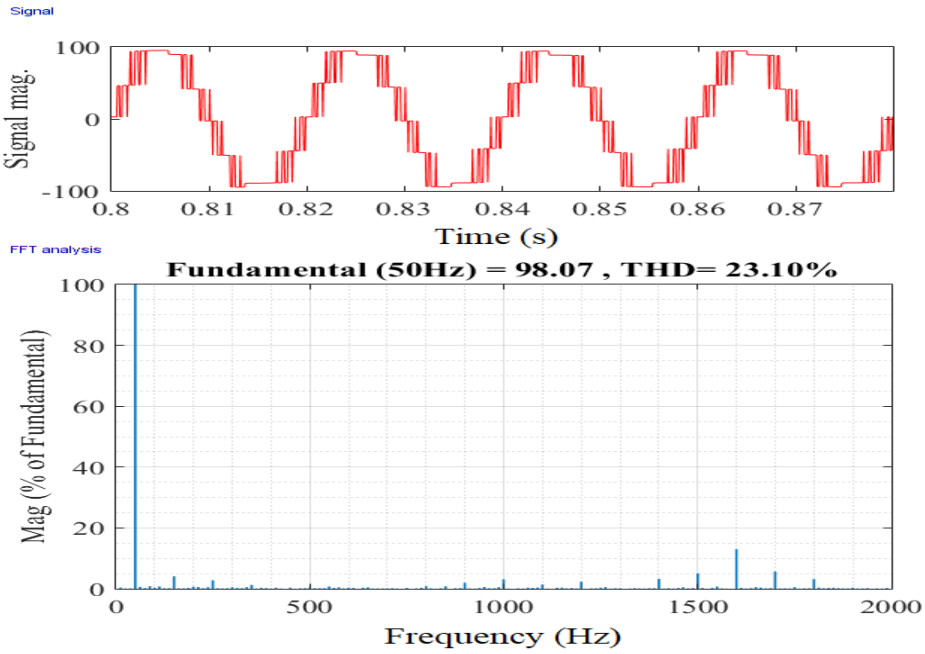

Figure 4.16 Mode 1 FFT analysis for the STATCOM voltage V_c , when the STATCOM is operating in capacitive approach

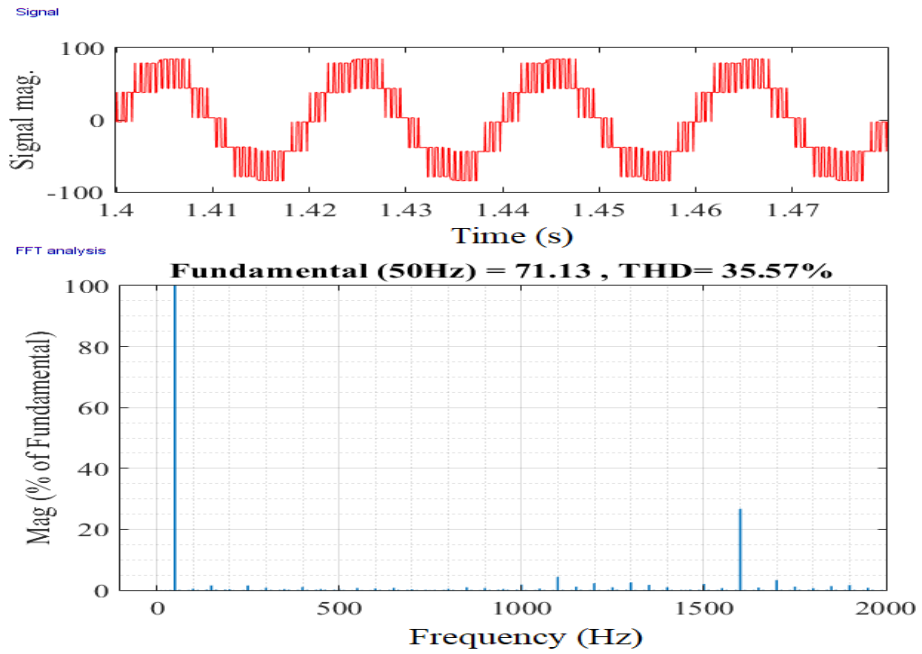

Figure 4.17 Mode 1 FFT analysis result for the STATCOM voltage V_c when the STATCOM is operating in inductive approach

4.2.2 Simulation Results of Mode 2

The simulation result for the designed MATLAB-Simulink model for Mode 2 (see Appendix C) has been shown in this section. The simulation was to study the characteristic and the effect of active harmonic filtering on a non-linear three-phase STATCOM system where the load changing from $R_L L_L$ to $R_L C_L$ at time of 2s. The system waveform only reaches steady-state at the time of 1s during STATCOM operating in capacitive approach and at the time of 3s during the STATCOM operating in inductive approach. Thus, the time frame uses for result taking was 1.5-1.6s for capacitive approach and 3.5-3.6s for inductive approach. The simulation model is similar to the model which was used for Mode 1 and with the assumption where the system is in balanced condition as well as the load. Therefore, both results for Mode 1 and Mode 2 can be used to study and investigate the effectiveness of the proposed simultaneous functionalities compensator based on the designed i_{cq}" algorithm. Figure 4.18 presents the overall performance of the three-phase STATCOM system in response to active harmonic filtering. Simulation result for the same three-phase systems with the designed i_{cq}" algorithm is illustrated in Figure 4.19 and 4.20. It can be seen that the harmonics in the waveform has been filtered out for both capacitive and inductive STATCOM operating approaches.

The mode 2 simulation results have been presented in two different STATCOM operating approaches. Referring to Table 4.2, when the DC peak voltage V_{DC} is more than grid peak voltage V_{pcc}, the STATCOM is operating in capacitive approach to inject reactive current into the power system. On the other hand, when the STATCOM operates in an inductive approach means the V_{DC} is lesser than V_{pcc} for absorbing reactive current from the power system.

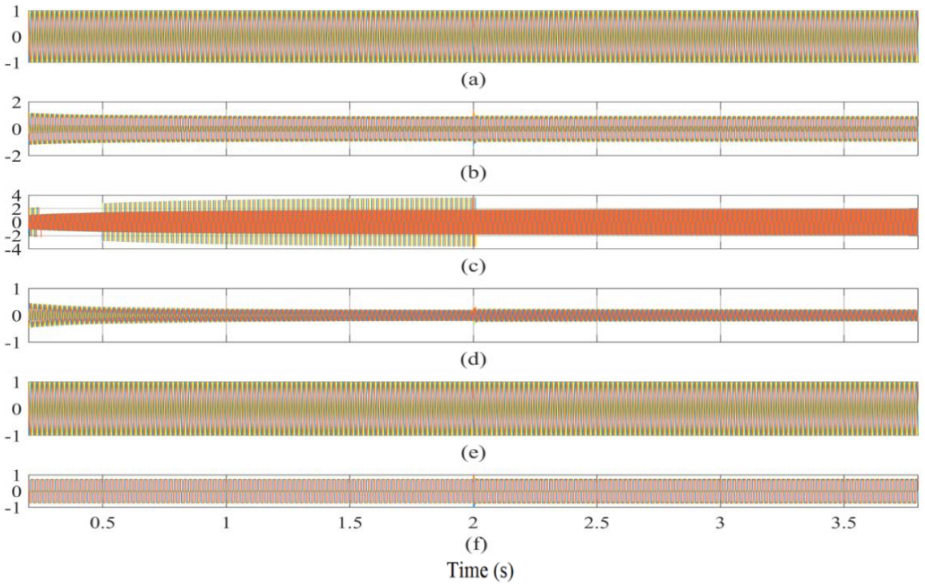

Figure 4.18 Overall Mode 2 simulation result for (a) grid voltage V_s, (b) grid current i_s, (c) STATCOM voltage V_c, (d) STATCOM current i_c, (e) load voltage V_l, and (f) load current i_l

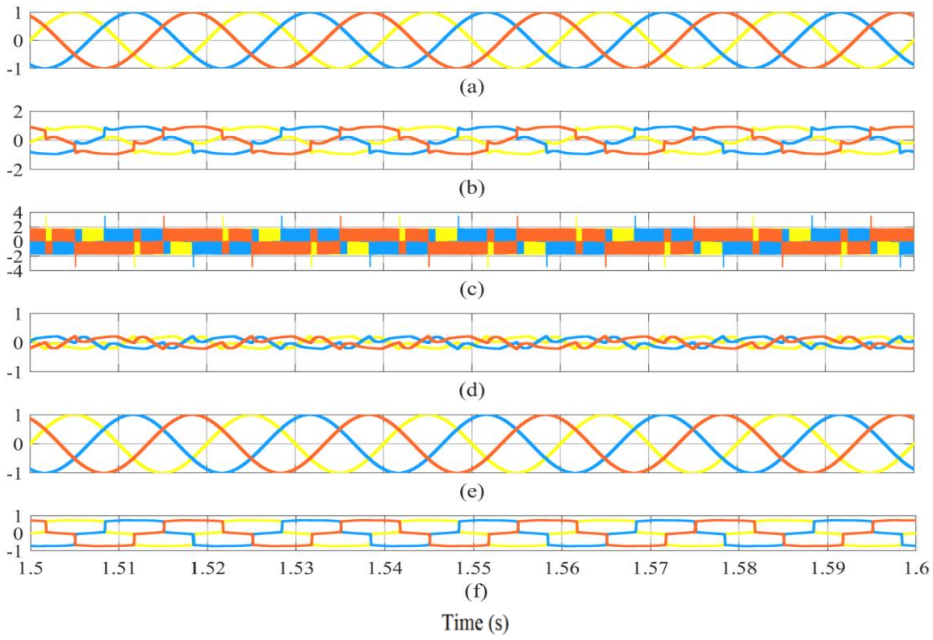

Figure 4.19 Zoomed view of Figure 4.18 when the STATCOM is operating in capacitive approach

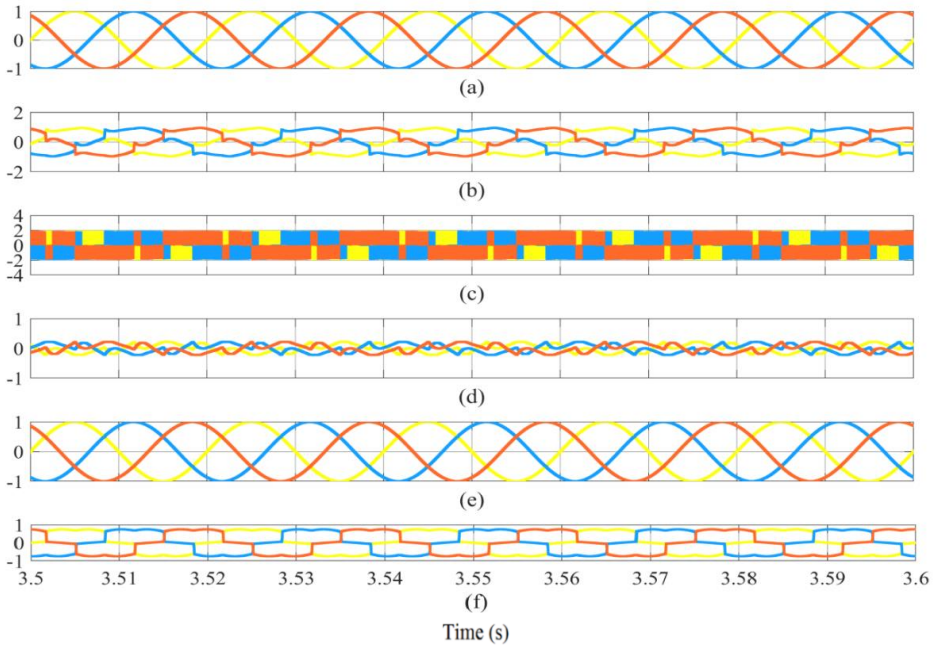

Figure 4.20 Zoomed view of Figure 4.18 when the STATCOM is operating in inductive approach

Continue to study Mode 2, an overall result comparison between phase current and line current for both load and grid have been shown in Figure 4.21. The zoomed version of result for a clearer view of the same three-phase systems with the designed i_{cq}" algorithm is illustrated in Figure 4.22 and 4.23.

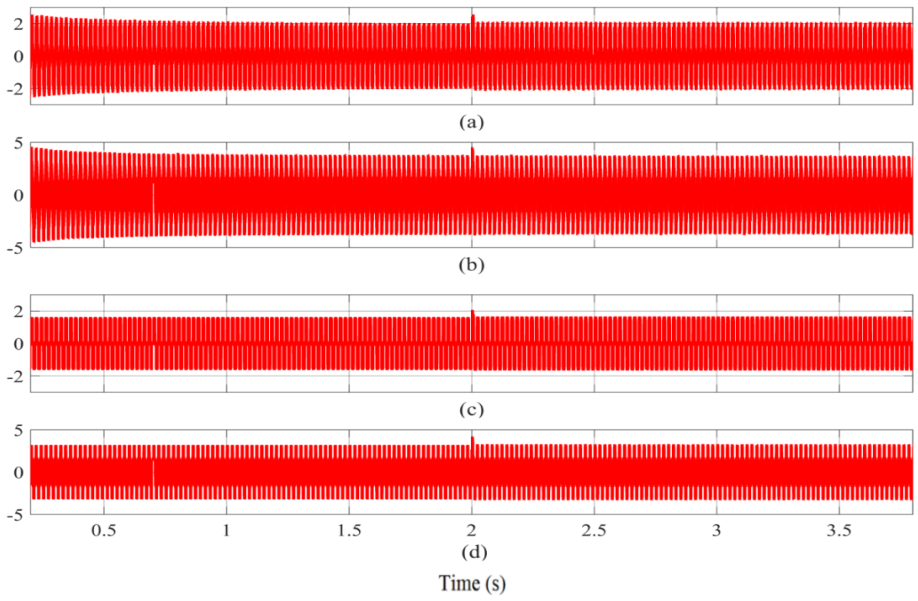

Figure 4.21 Overall Mode 2 simulation comparison result for (a) phase grid current i_s, (b) line grid current i_s, (c) phase load current i_l, and (d) line load current i_l

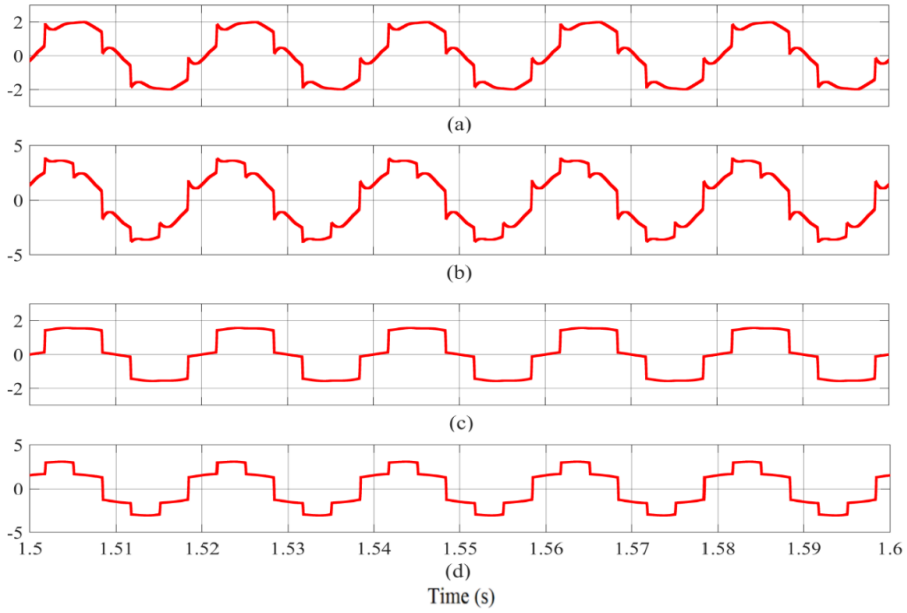

Figure 4.22 Zoomed view of Figure 4.21 when the STATCOM is operating in capacitive approach

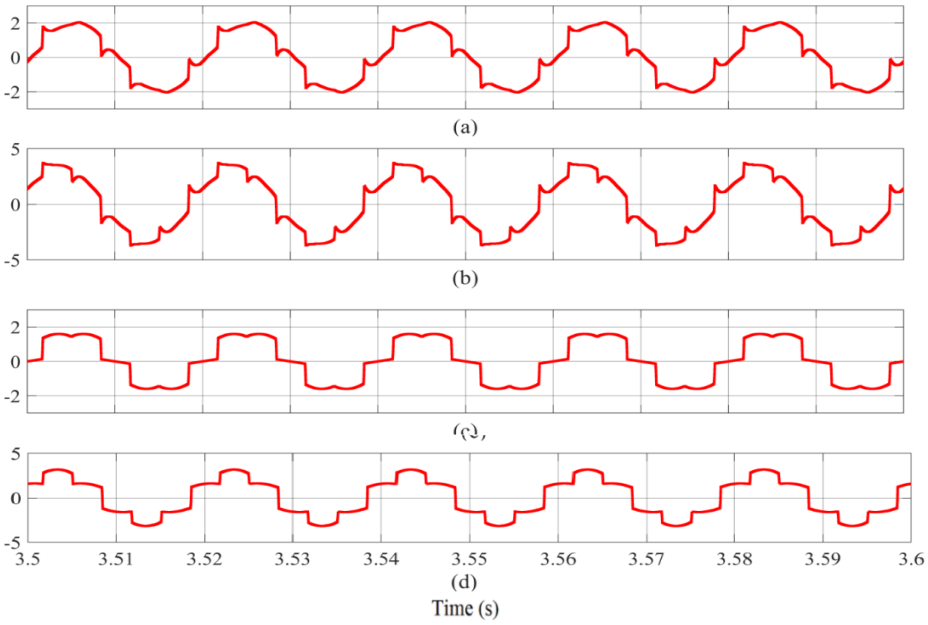

Figure 4.23 Zoomed view of Figure 4.21 when the STATCOM is operating in inductive approach

Figure 4.24 has presented the simulation where the load changing at time 2s for both phase load voltage V_l and phase load current i_l with the designed i_{cq}" algorithm. It is also worth to note that the current is in phase with the voltage. As reactive load changes from $R_L L_L$ to $R_L C_L$, simulation result for both STATCOM operating approaches which consists of capacitive and inductive have been presented in Figure 4.25 and 4.26.

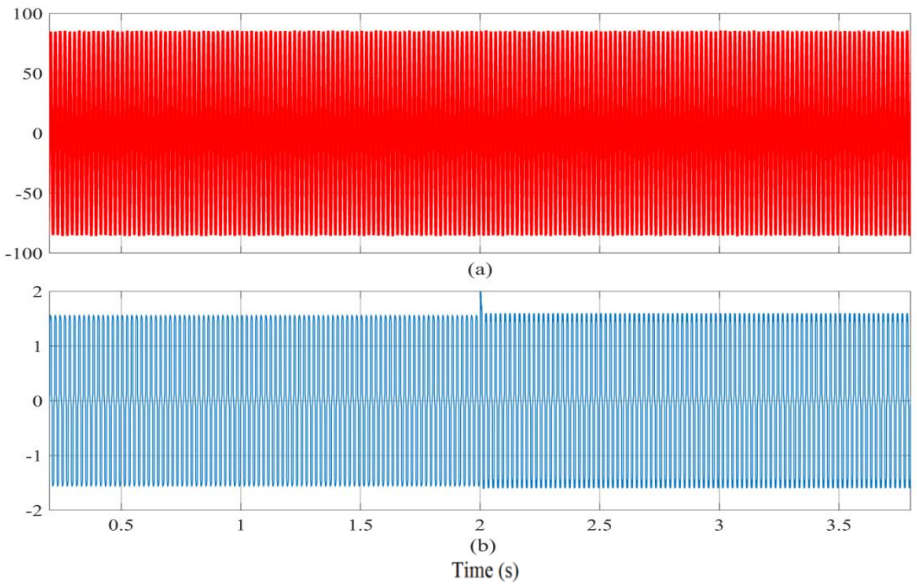

Figure 4.24 Overall Mode 2 simulation result for (a) phase load voltage V_l and (b) phase load current i_l

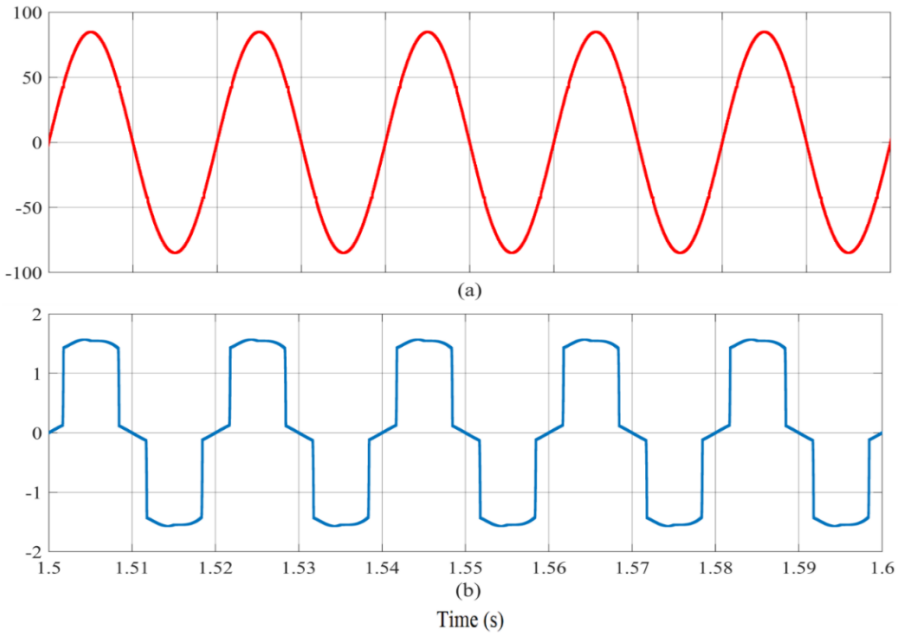

Figure 4.25 Zoomed view of Figure 4.24 when the STATCOM is operating in capacitive approach

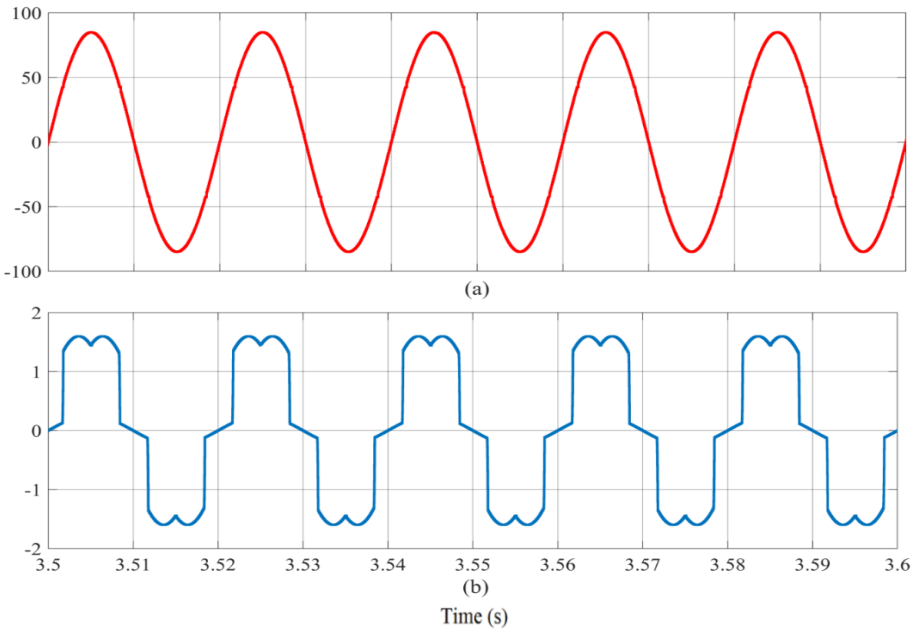

Figure 4.26 Zoomed view of Figure 4.24 when the STATCOM is operating in inductive approach

Figure 4.27 has presented the simulation where the load changing at time 2s for both phase grid voltage V_s and phase grid current i_s with the designed i_{cq}" algorithm. It is also worth to note that the current is in phase with the voltage. As reactive load changes from $R_L L_L$ to $R_L C_L$, simulation result for both STATCOM operating approaches which consists of capacitive and inductive have been presented in Figure 4.28 and 4.29.

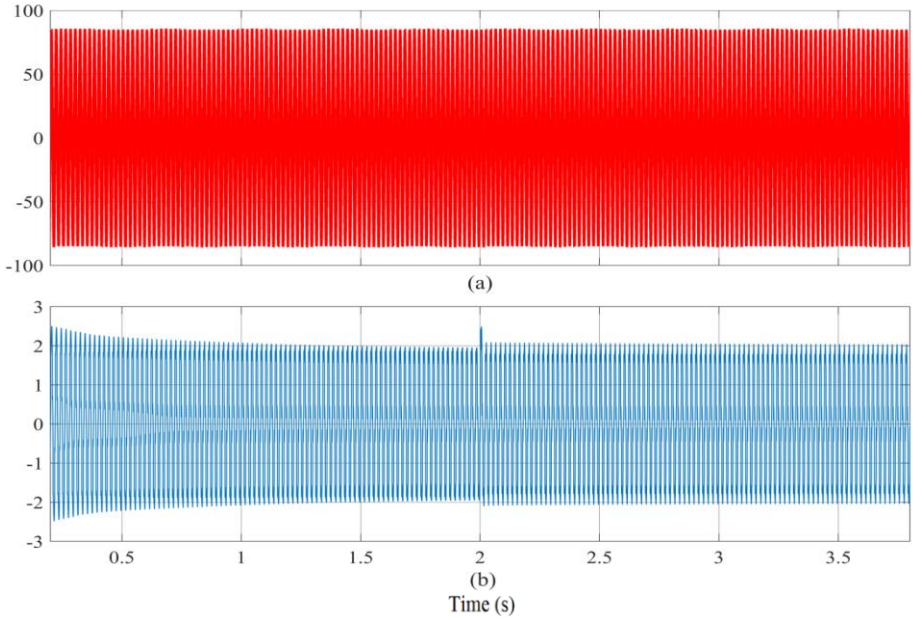

Figure 4.27 Overall Mode 2 simulation result for (a) phase grid voltage V_s and (b) phase grid current i_s

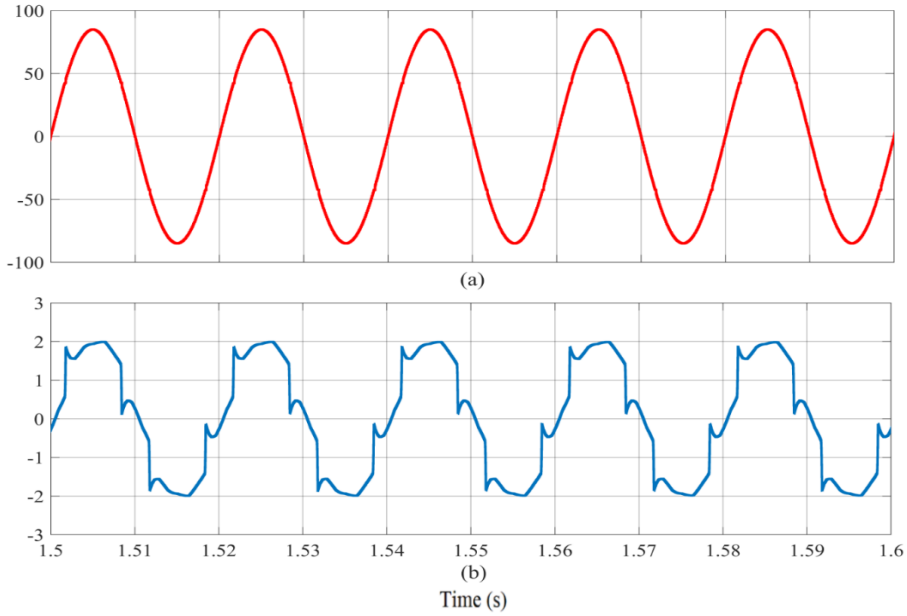

Figure 4.28 Zoomed view of Figure 4.27 when the STATCOM is operating in capacitive approach

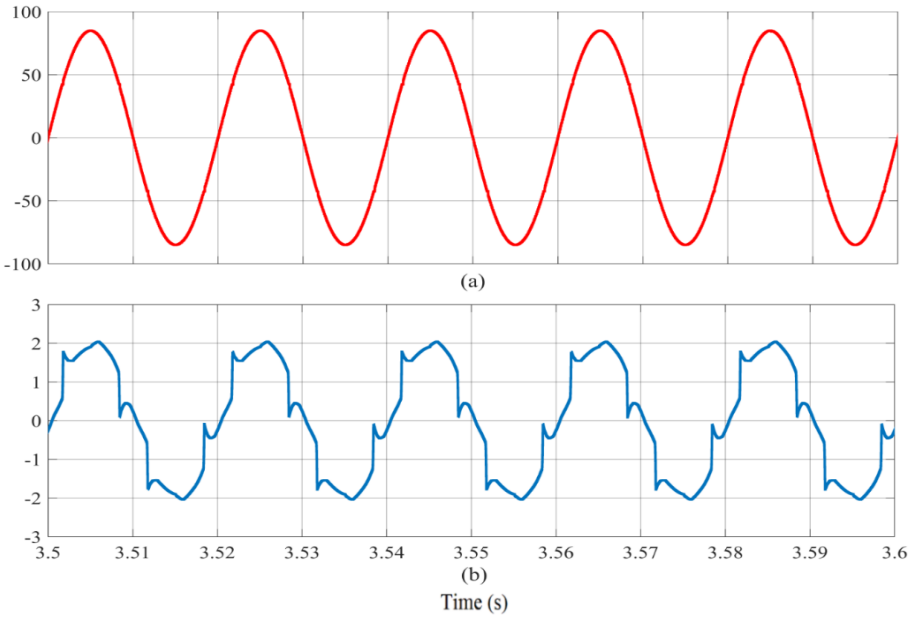

Figure 4.29 Zoomed view of Figure 4.27 when the STATCOM is operating in inductive approach

Figure 4.30 has presented the simulation where the load changing at time 2s for both phase STATCOM voltage V_c and phase STATCOM current i_c with the designed i_{cq}" algorithm. As reactive load changes from $R_L L_L$ to $R_L C_L$, simulation result for both STATCOM operating approaches which consists of capacitive and inductive have been presented in Figure 4.31 and 4.32. The harmonic filtering can be clearly seen in Figure 4.32 as the STATCOM operating in inductive approach after the load changes to $R_L C_L$. The transient response time can also be seen in Figure 4.30 and recorded as 50ms or 0.05s with respect with the i_c waveform.

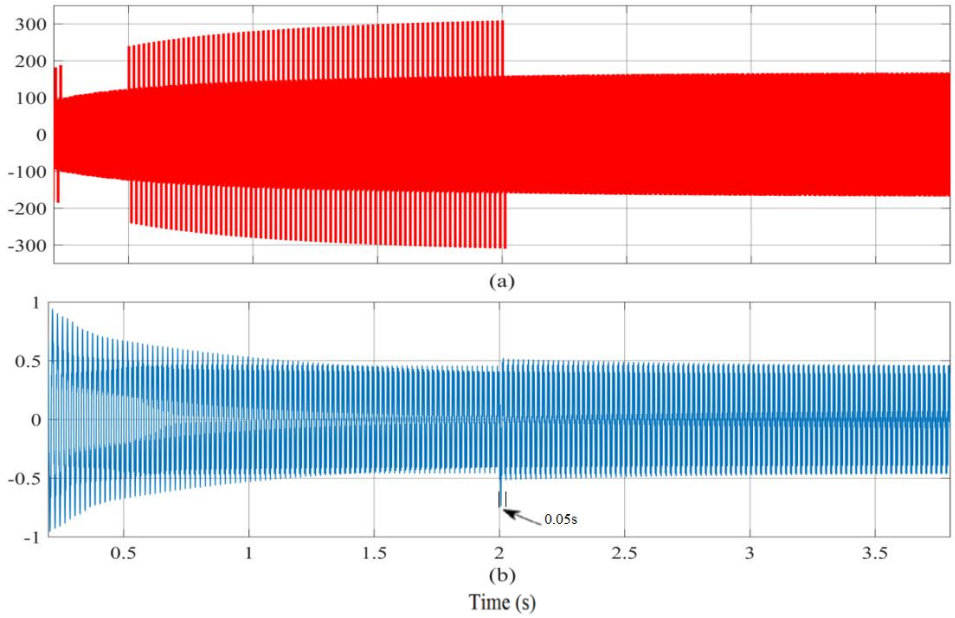

Figure 4.30 Overall Mode 2 simulation result for (a) phase STATCOM voltage V_c and (b) phase STATCOM current i_c

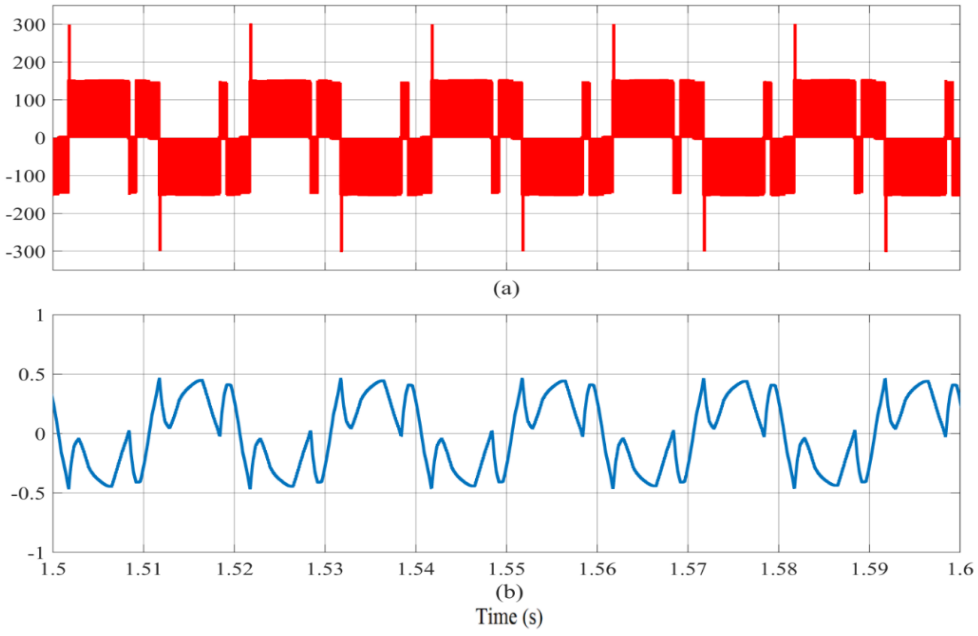

Figure 4.31 Zoomed view of Figure 4.30 when the STATCOM is operating in capacitive approach

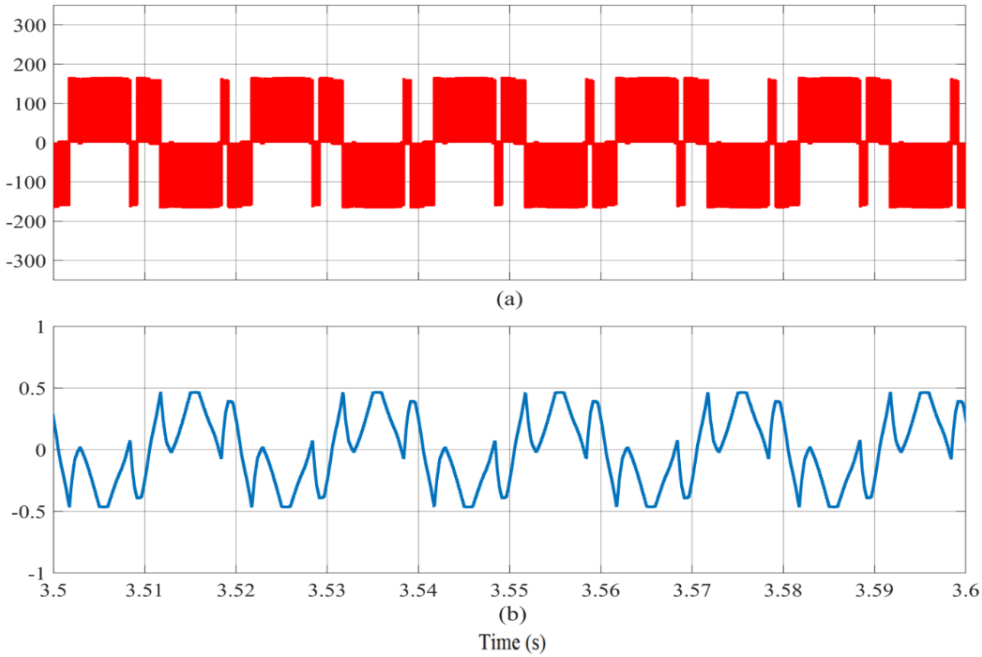

Figure 4.32 Zoomed view of Figure 4.30 when the STATCOM is operating in inductive approach

Figure 4.33 presented an overall Mode 2 simulation result in modulation waveform for load, grid and STATCOM. The improvement in modulation index for the STATCOM system has been shown and results in Figure 4.34 and 4.35 was studied. It was still a success although the improvement is not very huge.

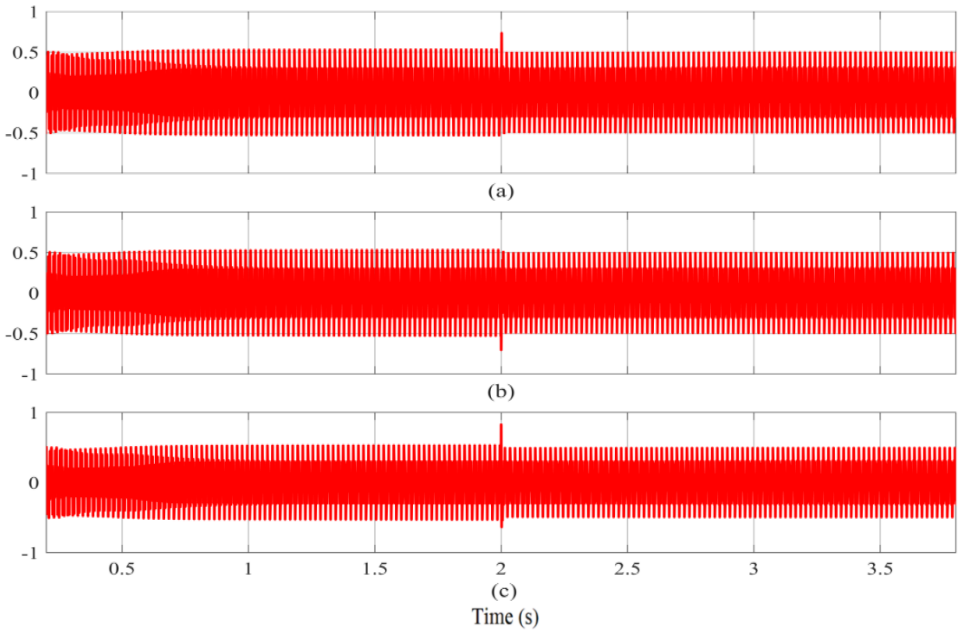

Figure 4.33 Overall Mode 2 simulation result in modulation waveform for (a) load, (b) grid and (c) STATCOM

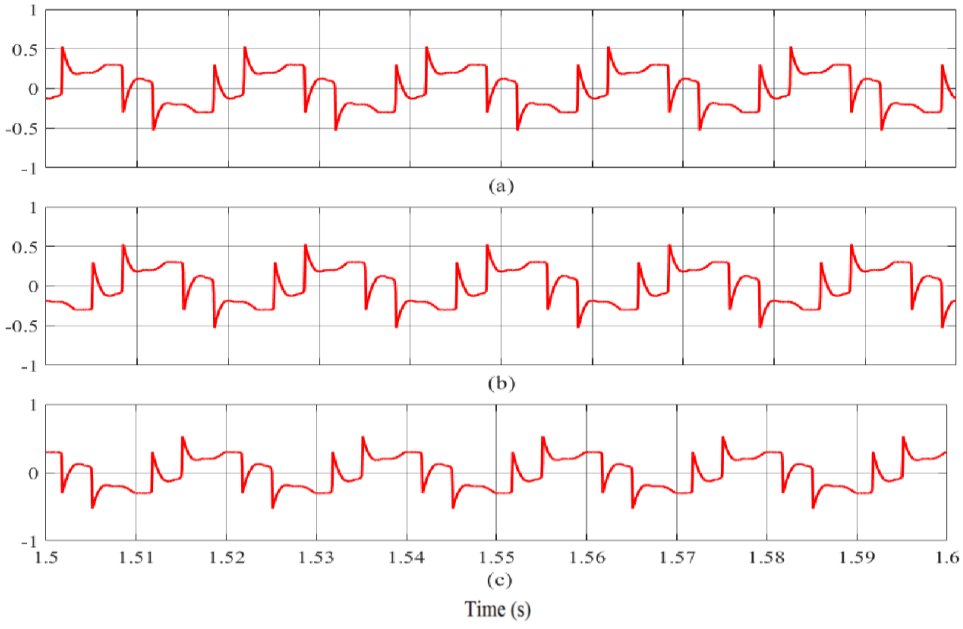

Figure 4.34 Zoomed view of Figure 4.33 when the STATCOM is operating in capacitive approach

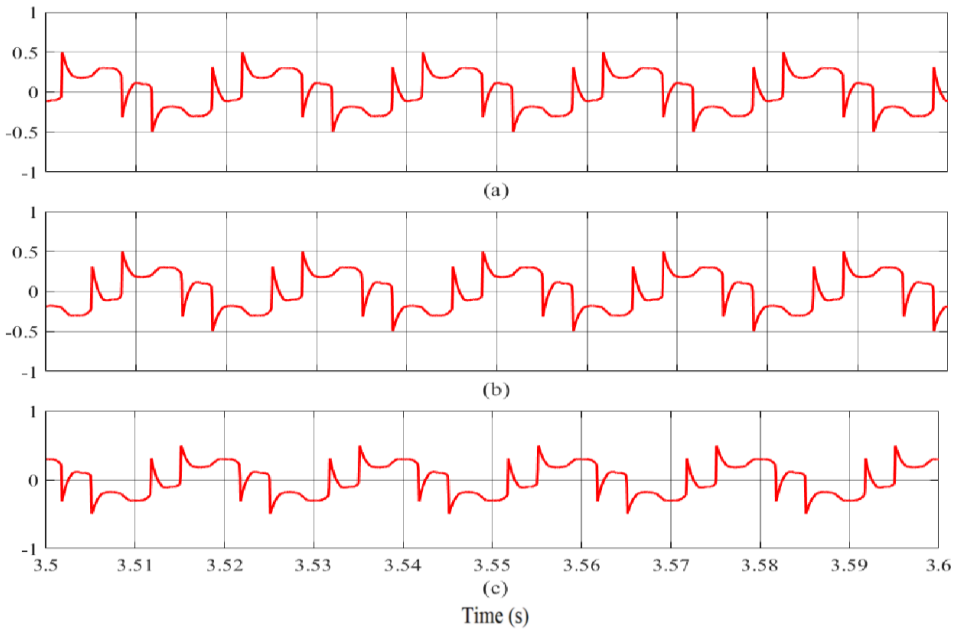

Figure 4.35 Zoomed view of Figure 4.33 when the STATCOM is operating in inductive approach

To further study the active harmonic filtering in Mode 2, FFT analysis result has been generated to find the THD for both phase and line operating approaches with respect to current for load i_l and grid i_s, which have been illustrated in Figure 4.36 and 4.37 for phase load voltage i_l, Figure 4.38 and 4.39 for line load voltage i_l, Figure 4.40 and 4.41 for phase grid voltage i_s as well as Figure 4.42 and 4.43 for line grid voltage i_s. The studied of the result has shown that, Mode 2 can accurately perform harmonic current compensator in the proposed simultaneous functionalities compensator based designed i_{cq}" algorithm. The compensation percentage has been calculated and listed in the Table 4.3 with formula as:

$$\text{Compensation percentage} = \left|\frac{THD\_is - THD\_il}{THD\_il}\right| \times 100\ \% \qquad (4.17)$$

Table 4.3 Comparison between load current $THD_{\_il}$ and grid current $THD_{\_is}$

STATCOM Operating Approaches	Load Current THD (%), $THD_{\_il}$	Grid Current THD (%), $THD_{\_is}$	Compensation percentage (%)
Phase; capacitive approach	25.7	17.63	31.40
Line; capacitive approach	25.7	17.60	31.51
Phase; inductive approach	25.64	17.38	32.22
Line; inductive approach	25.64	17.35	32.33

From Table 4.3, the compensation percentage has been calculated using formula (4.17) and the result are recorded as 31.40 % for phase and 31.51 % for line during the STATCOM operating in capacitive approach. For STATCOM operating in inductive approach, the compensation percentage has been recorded as 32.22 % for phase and 32.33 % for line. THD for grid current for both phase and line during the STATCOM operating in capacitive approach are calculated as 17.63 % and 17.60 %, respectively. On the other hand, THD of 17.38 % and 17.35 % for grid current has been recorded for both phase and line during the STATCOM operating in inductive approach. According to IEC61000-3-12 standard documentation for low voltage equipment which has been discussed in [126, 127], the limitation of the THD for the proposed grid system has to comply with the harmonic current emission limits corresponding to a short circuit ratio of 33, which is at 23 %. This indicate that an average of 5.5 % THD has been successfully reduced. From the result observation, the THD for line grid current then to be 0.03 % lesser then the phase grid current. This is because the harmonic which generated by the non-linear loads such as rectifiers under well balanced three-phase, the vector sum of the 50 Hz current in neutral conductor is equal to zero. Thus, harmonics in the three-phase systems which containing positive, zero and negative sequence components to be taken into consideration when trying to filter any

specified harmonic on the power system since the potential effects of series and parallel resonances required each component to be treated differently.

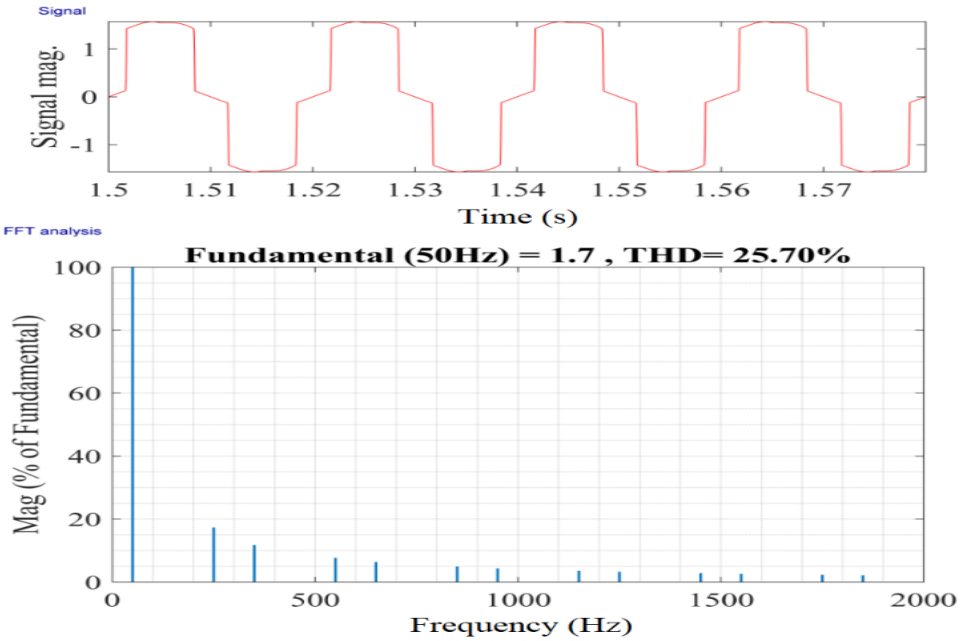

Figure 4.36 Mode 2 FFT analysis result for phase load current i_l, when the STATCOM is operating in capacitive approach

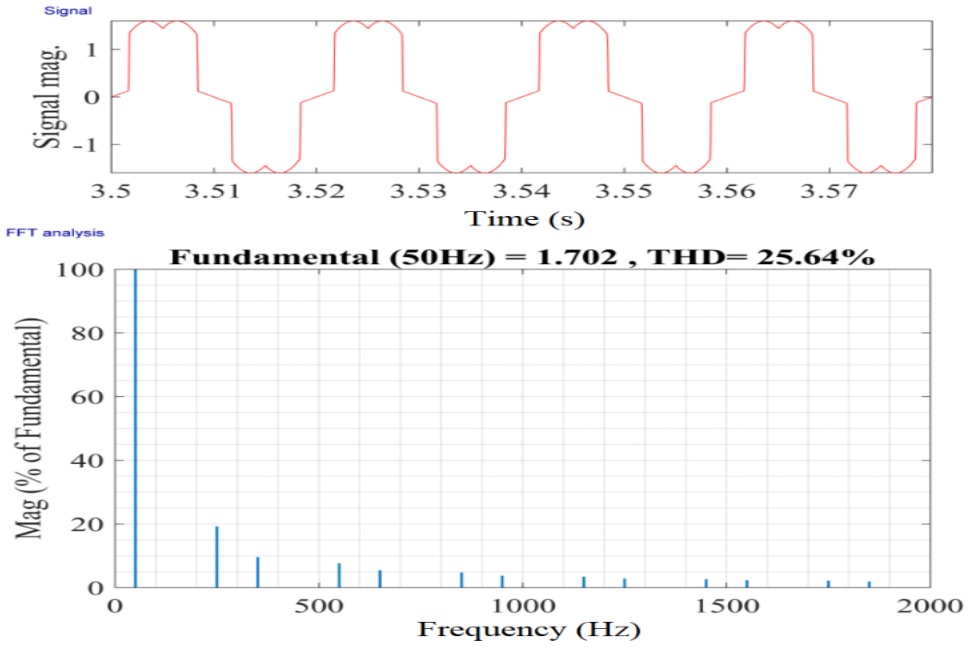

Figure 4.37 Mode 2 FFT analysis result for phase load current i_l, when the STATCOM is operating in inductive approach

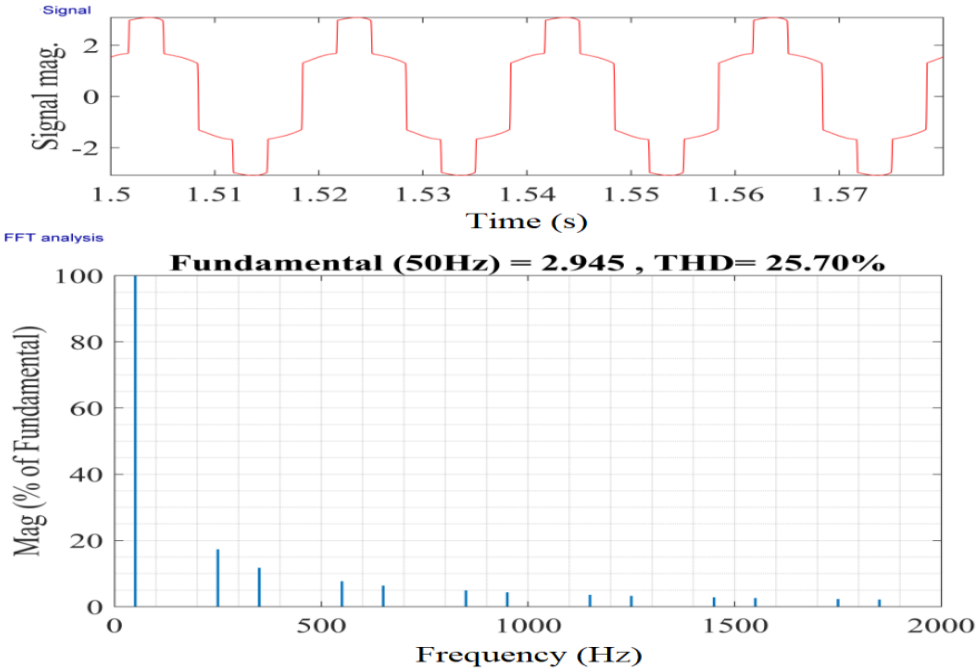

Figure 4.38 Mode 2 FFT analysis result for line load current i_l, when the STATCOM is operating in capacitive approach

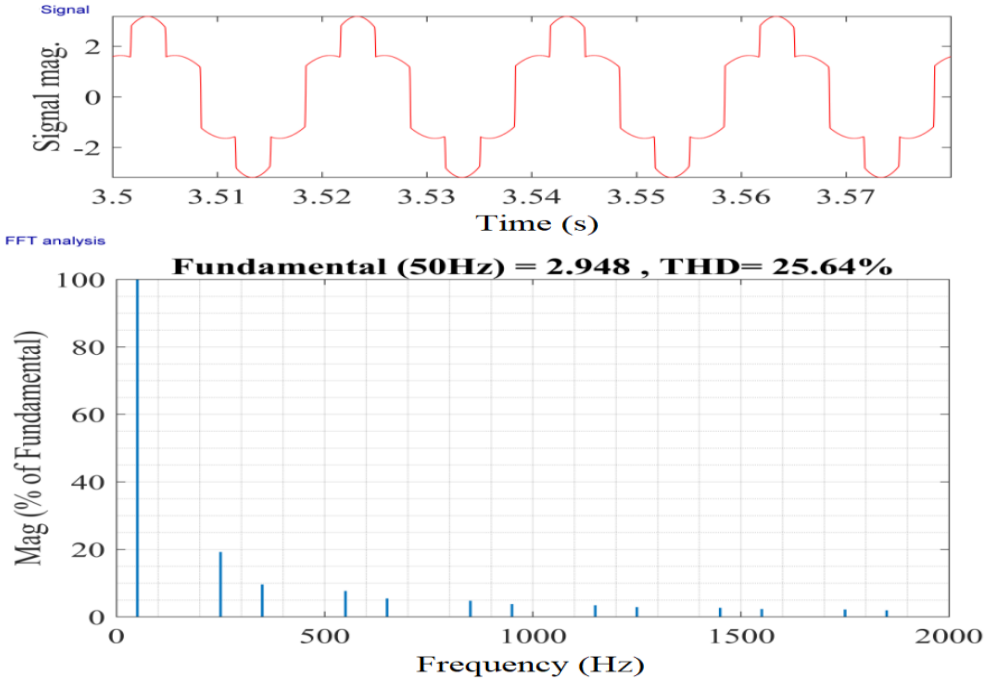

Figure 4.39 Mode 2 FFT analysis result for line load current i_l, when the STATCOM is operating in inductive approach

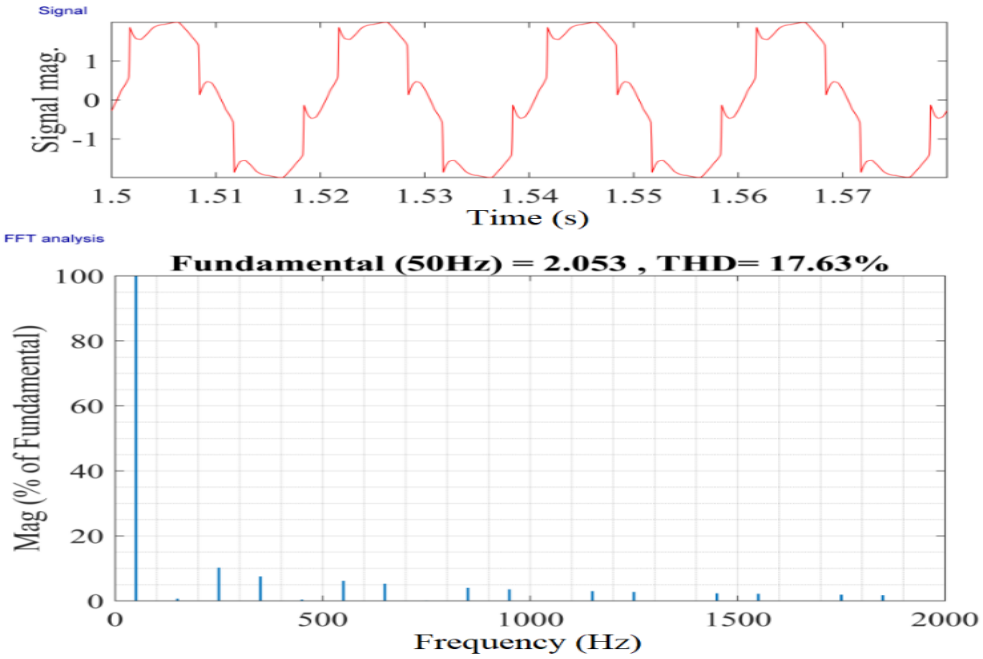

Figure 4.40 Mode 2 FFT analysis result for phase grid current i_s, when the STATCOM is operating in capacitive approach

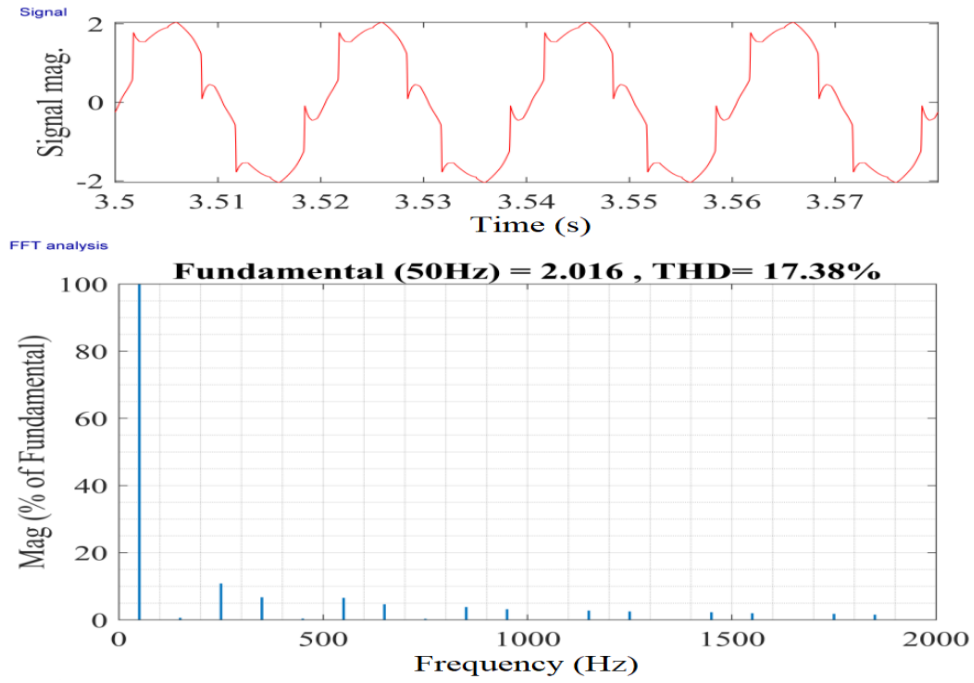

Figure 4.41 Mode 2 FFT analysis result for phase grid current i_s, when the STATCOM is operating in inductive approach

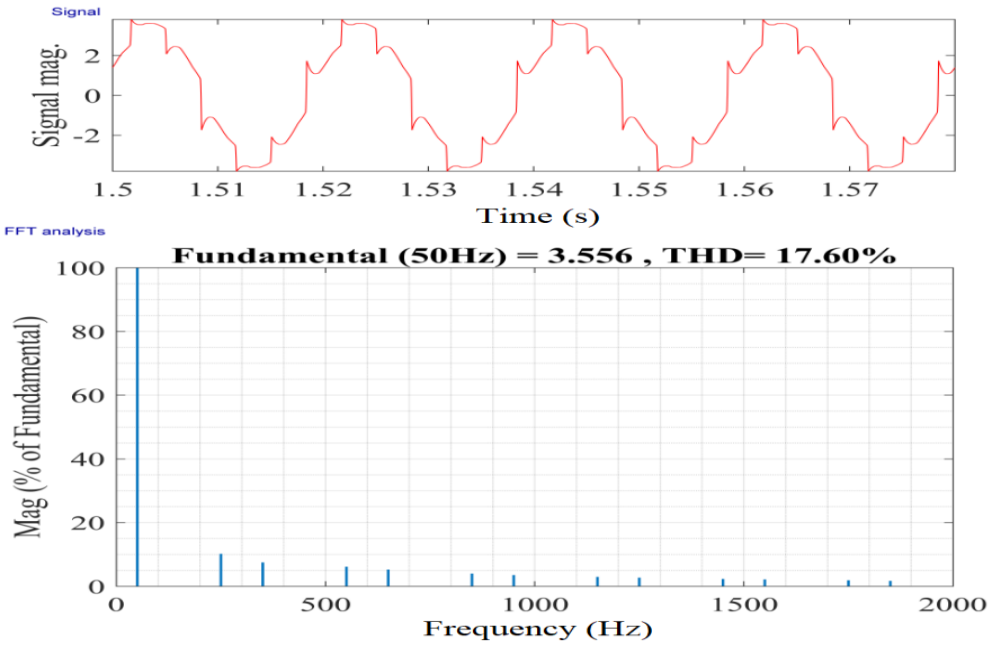

Figure 4.42 Mode 2 FFT analysis result for line grid current $i_{s,}$ when the STATCOM is operating in capacitive approach

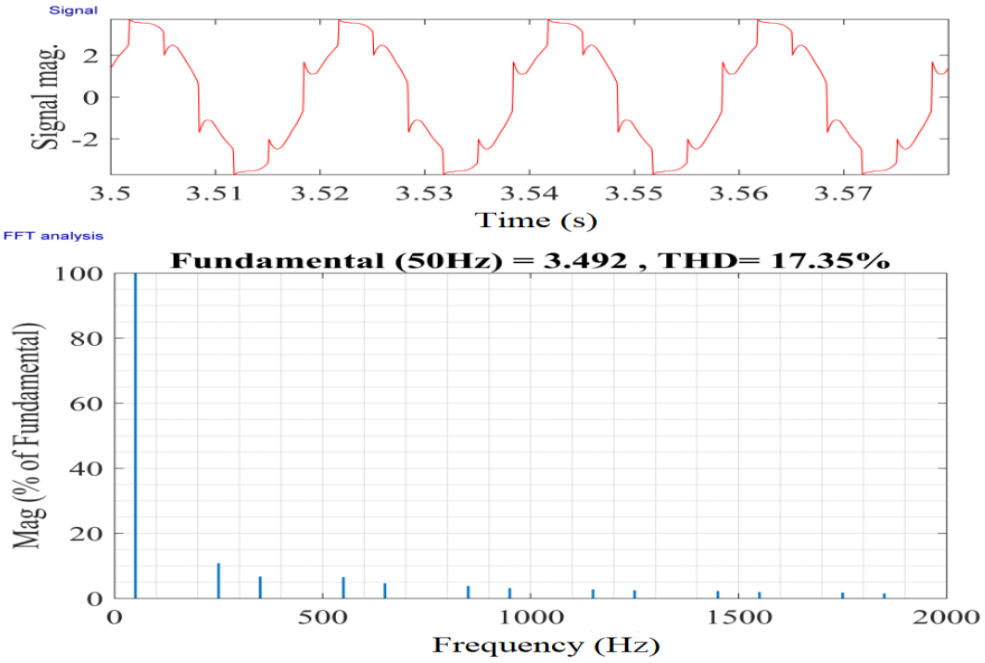

Figure 4.43 Mode 2 FFT analysis result for line grid current $i_{s,}$ when the STATCOM is operating in inductive approach

4.3 Summary for the Simulation Results

The designed current reference i_{cq}" algorithm for MCHI based STATCOM system has been implemented in the proposed simultaneous functionalities compensator using MATLAB-Simulink. The ability to perform two main operational modes (i.e. Mode 1-Reactive Current Compensation and Mode 2-Active Harmonic Filtering) in the proposed compensator has been validated through the simulation result which has been presented in this chapter. The specific current reference i^*_{mod} can be obtained through instantaneous current control method from each mode. Once decided the suitable mode, compensator current reference i^*_{cpr} was sent as a true signal to STATCOM main system from any desired controller board in order to allow the compensation to take place. In another words, compensator current reference i^*_{cpr} was the output from the measured MCHI output current minuses by the load current reference i_l. PLL then synchronized the MCHI output current with the voltage V_{pcc} in the MCHI. The STATCOM steady-state error and the transient response have been significantly improved after the designed i_{cq}" algorithm been applied in the system. The STATCOM transient response time during the step change of load for both Mode 1 and 2 have been recorded as 0.05 s or 50 ms, which it is only 2.5 times of the fundamental switching time (i.e. 20 ms) as shown in Figure 4.5 and 4.30. The compensation accuracy of i_{cq} with respect to i^*_{cpr} in p.u with the designed i_{cq}" algorithm has been calculated as 97 % or $\pm$3 %. In another words, the power factor has been improved from 0.67 to 0.97. The THD for line grid current usually lower than the phase grid because the vector sum of the 50 Hz current in neutral conductor is equal to zero for harmonic generated by the non-linear loads under well balanced three-phase. In order to further reduces the THD for the proposed system, the switching frequency must tune higher or increases the level of MCHI based STATCOM system.

Chapter 5

Conclusion and Recommendations for Future Works

5.1 Conclusions

With the growing popularity of high-power static inverters in power system applications especially power line transmission, the second generation of shunt-connected FACTS controllers which control the current of the power system by providing common compensation characteristics have become the top choice. Comparing to the SVC in the first generation of shunt-connected FACTS controllers, Voltage Source Inverters (VSIs) based STATCOM is a better version of SVC which consists of a PWM switching inverter with capacitor connected at the DC-link, in terms of having lower rating of capacitors and inverters as well as diodes and switches [7].

This research work studied and investigated the diversity of the available multilevel topologies. Since the fundamental focus of this dissertation is on MCHI based STATCOM, therefore the common multilevel PWM techniques and control schemes for reactive current compensation as well as active harmonic filtration have been fully documented in Chapter 2. All literature reviews have been documented in Chapter 2, which consists of the characteristic as well as both advantages and disadvantages of the MCHI based STATCOM. In summary, the required reactive current flowing to the power system through coupling inductor or transformer is the reference current for STATCOM to rapidly adjust its AC output voltage.

This research work proposed a decoupling feed-forward current vector controller based on the dq-method to provide VAR compensation and PF correction under balanced loading conditions for both single-phase and three-phase STATCOM system. To exhibit a rapid correction response, PI-controllers were employed to achieve both fast and robust control of the reactive current compensation as well as active harmonic filtration. The mathematical derivation of the designed reactive reference current i_{cq}" algorithm framework has been presented in Chapter 3. Both proportional K_p and integral K_i gain of the PI-controller have been calculated based on the designed reactive reference current i_{cq}" algorithm as total gain, K_{total}.

The proposed simultaneous functionality compensator with the ability to perform two main operational modes (i.e. Mode 1-Reactive Current Compensation and Mode 2-Active Harmonic Filtering) have been validated through simulation work. The simulation results presented in Chapter 4 have clearly shown that the proposed operational modes have successfully reduced the unwanted reactive by improving the power factor to 0.97 from 0.67 and excessive harmonics at the grid with average 5.5 % THD that has been filtered for both single-phase and three-phase STATCOM system with the total average of 31.87 % compensation percentage. The model achieved good transient response time at 50 ms, which is only 2.5 times of the 20 ms fundamental switching time during the step change of load for both Mode 1 and 2. These STATCOM simulation model based five-level MCHI with IPD CB-PWM technique as the modulation technique studies were carried out using MATLAB-Simulink software package. The simulation parameter was based on the automatic code generation according to the chosen controller board dSPACE-DS1104 target as a reference for validation purposes. The mode selector is not limited to any specific controller board.

5.2 Future Works

With the promising simulation result from Mode 1-Reactive Current Compensation and Mode 2-Active Harmonic Filtering in the proposed simultaneous functionality compensator, more modes can be added as add-ons such as injecting active power from STATCOM into the grid and to rectify unbalanced loading conditions. The proposed simultaneous functionalities compensator also can be tested with higher switching frequency in order to reduce the THD of the STATCOM system. Hardware implementation can be performed in the future to further verify the robustness of the derived mathematical equations.

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Appendix A Park's Transformation

Park's transform is a space vector transformation of time-domain signals (i.e., from a stationary *abc*-coordinate system to a rotating *dq*- coordinate system) which has been employed to simplify the analysis of three-phase system. First, the derivation begins by representing the target AC quantities (i.e., grid voltage V_{pcc}) in *abc*-coordinates with a voltage vector V_{pcc} that rotates around the stationary $\alpha\beta$-frame with the angular velocity of ω (i.e., $2\pi f$ at the grid frequency):

$$v_{pcc}\angle\theta^{\circ} = v_{pcc\_a}e^{j0} + v_{pcc\_b}e^{j2\pi/3} + v_{pcc\_c}e^{j4\pi/3} = v_{pcc\_\alpha} + jv_{pcc\_\beta} \tag{A1}$$

where *Vpcc_a*, *Vpcc_b*, and *Vpcc_c* defines the phase vectors for each phase, *Vpcc_α* and *Vpcc_β* defines the projection value of the *Vpcc* onto the stationary $\alpha\beta$ reference frame, and θ is the phase angle of *Vpcc*.

Since $e^{j\sigma} = \cos(\sigma) + j\sin(\sigma)$, (A1) is represented as follows:

$$\begin{aligned} v_{pcc\_\alpha} &= v_{pcc\_a}\cos(0^{\circ}) + v_{pcc\_b}\cos(120^{\circ}) + v_{pcc\_c}\cos(240^{\circ}) \\ &= v_{pcc\_a} - 0.5v_{pcc\_b} - 0.5v_{pcc\_c} \end{aligned} \tag{A2}$$

$$\begin{aligned} v_{pcc\_\beta} &= v_{pcc\_a}\sin(0^{\circ}) + v_{pcc\_b}\sin(120^{\circ}) + v_{pcc\_c}\sin(240^{\circ}) \\ &= +j0.866v_{pcc\_b} - j0.866v_{pcc\_c} \end{aligned} \tag{A3}$$

And can be represented in matrix format as given by:

$$\begin{bmatrix} v_{pcc\_\alpha} \\ v_{pcc\_\beta} \end{bmatrix} = \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & 0.866 & -0.866 \end{bmatrix} \begin{bmatrix} v_{pcc\_a} \\ v_{pcc\_b} \\ v_{pcc\_c} \end{bmatrix} = v_{pcc} \begin{bmatrix} \cos(\theta^{\circ}) \\ \sin(\theta^{\circ}) \end{bmatrix} \tag{A4}$$

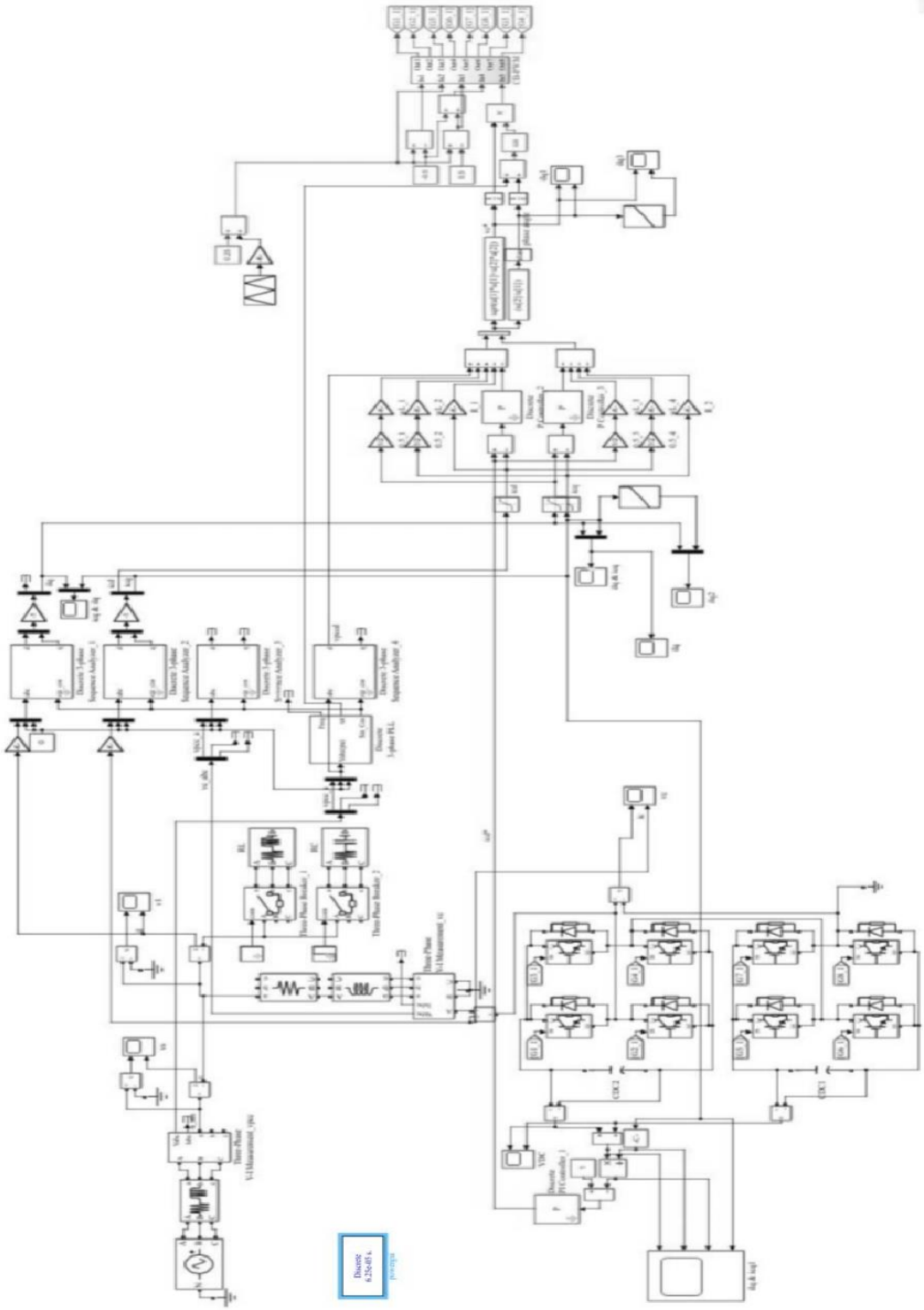
The next- and final-step of Park's transformation is to rotate the stationary *αβ*-coordinates in synchronous with the voltage vector *vpcc*.

Thus, making the *vpcc_α* and *vpcc_β* to become constant. This transformation matrix is given as follows:

$$\begin{aligned} \begin{bmatrix} v_{pcc\_d} \\ v_{pcc\_q} \end{bmatrix} &= \begin{bmatrix} v_{pcc\_\alpha} \\ v_{pcc\_\beta} \end{bmatrix} \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \\ &= v_{pcc} \begin{bmatrix} \cos(\theta) \\ \sin(\theta) \end{bmatrix} \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \\ &= v_{pcc} \begin{bmatrix} \cos^2(\theta) + \sin^2(\theta) \\ -\sin(\theta)\cos(\theta) + \sin(\theta)\cos(\theta) \end{bmatrix} \\ &= v_{pcc} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \end{aligned} \tag{A5}$$

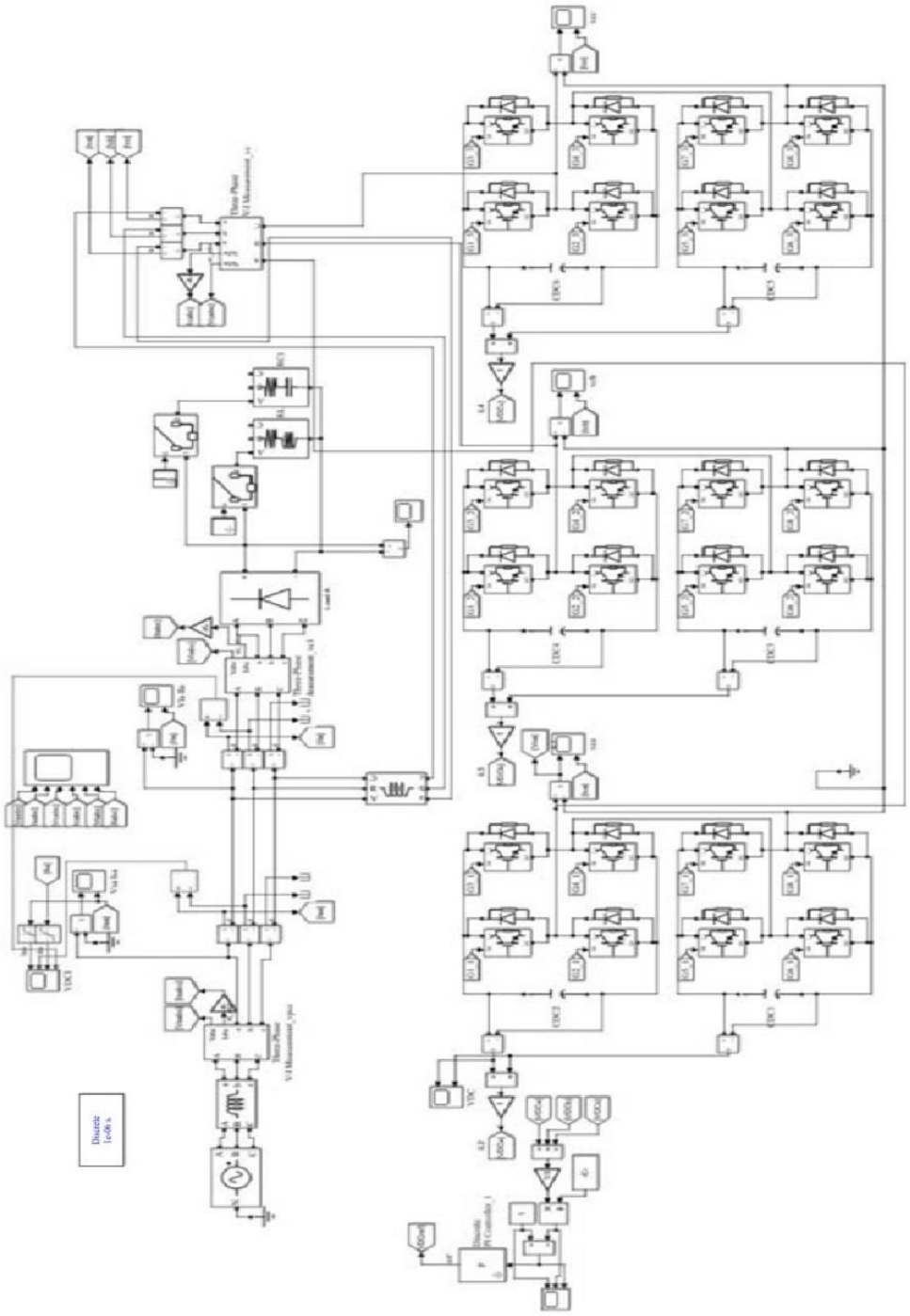
Vpcc_d and *Vpcc_q* defines the projection of the *Vpcc* onto the rotating *dq* reference frame.

Appendix B MATLAB-Simulink model for Mode 1



Appendix C MATLAB-Simulink model for Mode 2

Part (a)



Part (b)