

Research on a Composite Voltage and Current Measurement Device for HVDC Networks

Abstract—With the global trend to develop digital substation automation systems, measurement devices are required to be reliable, of small size and light weight and of acceptable accuracy in a wide frequency band. This paper presents a combined high voltage direct current (HVDC) measurement method which comprises the above-mentioned features that makes it suitable for smart grids protection and control applications. The proposed measurement method utilizes Hall sensor array for DC current measurement. DC voltage is measured using a voltage divider circuit while the harmonic currents are measured using a square Rogowski coil made of four straight bars along with a high precision digital integration algorithm. A four-spectral line interpolation fast Fourier transform algorithm based on trapezoidal convolution window is proposed to improve the extraction accuracy of the DC and harmonic components from the measured signal. Experimental results show that the error variation of the proposed method is less than 0.098% for voltage measurement while it is less than 0.104% for current measurement. The harmonic measurement ratio error is less than 0.2% and the angle error is less than 8'.

Index Terms— DC measurement, hall sensor array, Rogowski coil, digital integration.

I. INTRODUCTION

High voltage direct current (HVDC) transmission systems have been given much attention in the last few years. This calls for the essential development of new HVDC measurement devices of specific features [1]-[5]. As such, traditional methods based on electromagnetics and diverters to measure the DC current and voltage signals are gradually replaced by new sensing technologies that feature small volume, light weight, high accuracy and large dynamic range [6]-[9].

For DC current measurement, current transformer based on diverter principle and zero flux DC current transformer are widely used [10]-[12]. Although these transformers feature high measurement accuracy, its large volume and heavy weight restrict their practical field applications on site.

For DC voltage measurement, optical-based method using Pockels effect has been used due to its good insulation performance [13]-[16]. However, optical crystals used in this method are susceptible to temperature, vibration and other factors, which affect the stability and accuracy of this measurement method. A voltage transformer based on photoelectric field integration method is proposed in [17], [18]. However, the presented method is mainly focusing on the simulation of electric field integration and interference factors, without practical validation. Furthermore, the stability and reliability of this technique over a long-term operation still need to be tested.

In order to monitor, protect and control the HVDC networks precisely, it is necessary to accurately measure the harmonic currents and voltages. Rogowski coil is usually used to measure the harmonic currents. However, the commonly used Rogowski coil based on printed circuit board (PCB) technology is difficult

to design with enough turns because of the limited space and technical constraints. This results in a small output signal that is vulnerable to noise interference [19]-[21]. The traditional fast Fourier transform (FFT) algorithm is used to analyze the voltage and current signals with harmonic components in most existing measurement methods [22], [23]. However, the FFT algorithm may decrease the accuracy of signal analysis when the signal exhibits external interference noise. This also calls for a high precision and robust algorithm that can function properly in the expected strong electromagnetic environment of electrical substations.

In summary, existing methods to measure the DC voltage and current exhibit some shortcomings and most of these methods are usually of a single measurement function. The difficulty of multitask measurement devices lies in the design of a suitable sensing method of stable operation, simple structure and the use of various integrated sensors of different reliabilities. Developing a high precision signal processing algorithm, especially for harmonic measurement is another challenge. The main contribution of this paper is:

- the presentation of a new cost-effective combined HVDC digital measurement technique.
- the development of a detailed prototype device of the proposed combined sensing method that can simultaneously measure the DC voltage, DC and harmonic currents with higher accuracy than existing conventional measurement methods.
- for DC current measurement, a ring magnetic field sensor array is utilized to effectively reduce the influence of the external electromagnetic field and improve the measuring accuracy.
- for DC voltage measurement, a method based on resistance and capacitance divider is adopted.
- for harmonic current measurement, a square Rogowski coil that can be equipped with more coil turns in a small space to accurately measure weak harmonic signals is designed and a precise digital integration algorithm is proposed.

II. PROPOSED STRUCTURE OF THE COMBINED MEASUREMENT DEVICE

The structure of the proposed multitask measurement device is shown in Fig.1. The DC current measurement unit, harmonic measurement unit, and the acquisition and transmission unit are located in the high voltage shell. The DC voltage measurement unit is located in the insulating bushing. The signals of the measurement units are transmitted to the acquisition and transmission unit through a shielded cable. Analog to digital conversion takes place in the acquisition and transmission unit which transmits the digital signals to the merging unit through optical fiber (inside the bushing and base) and cable (outside the base). The merging unit also supplies laser energy to the acquisition and transmission unit and it analyzes, processes and displays the measured data, and transmits them to other intelligent devices or computers. Various units in the proposed structure are briefly explained below.

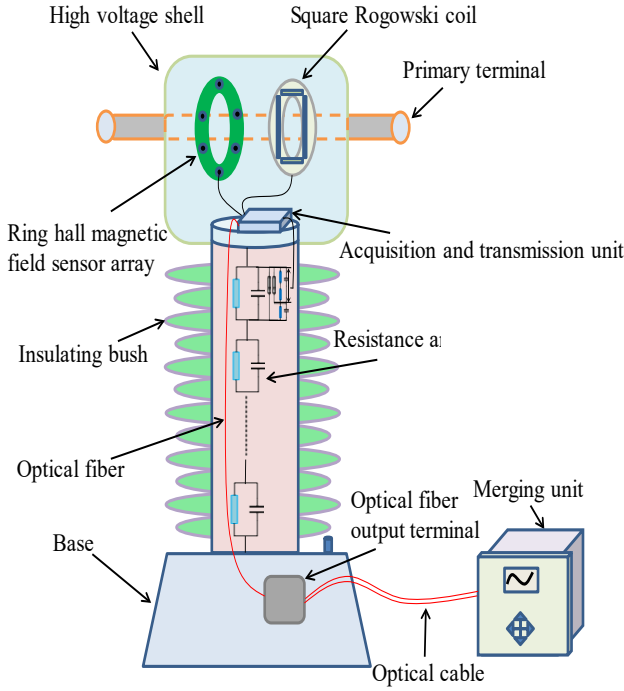


Fig. 1. Schematic diagram of the proposed multitask device.

III. MEASUREMENT UNITS

This includes DC current, voltage and harmonic measurement units. The DC voltage measurement unit is of resistive and capacitive components distributed within the insulating bushing. The DC current and harmonic measurement units are located in the high voltage shell, as shown in Fig.1.

A. DC Current Measurement Unit

1) Basic Principle:

A measuring method for DC current based on a ring Hall magnetic field sensor array is proposed. In this technique, several Hall sensors are evenly distributed on a circular ring and the average measuring value of all Hall sensors is considered as the output value. In this way, the influence of the external magnetic field on the measured current can be minimized and the measurement accuracy can be improved.

The ring Hall magnetic field sensor array has a circular structure of a center coinciding with the axis of the primary conductor. As there is no iron core, no magnetic saturation issue is arising when measuring large DC current. All Hall sensors are evenly distributed on the vertices of the inner regular polygon of the ring forming the sensor array. Fig.2 shows a ring Hall sensor array consisting of eight Hall sensors. The center of the sensor array O coincides with the axis of the primary conductor. Assuming the ring sensor array comprises n Hall sensors, the magnetic induction strength of the j th Hall magnetic field sensor is B_j , which is correlated to the output voltage e_j by the Hall coefficient K , then:

$$e_j = KB_j \quad (1)$$

The sum of the Hall output voltages of all sensors e_{HS} is:

$$e_{HS} = \sum_{i=1}^n e_j = K \sum_{i=1}^n B_j = \frac{\mu_0 n K I}{2\pi r} = K^* I \quad (2)$$

where μ_0 is the permeability of free space and r is the distance between the Hall sensor and the conductor.

Then, the primary current I can be calculated as follows.

$$I = \frac{e_{HS}}{K^*} \quad (3)$$

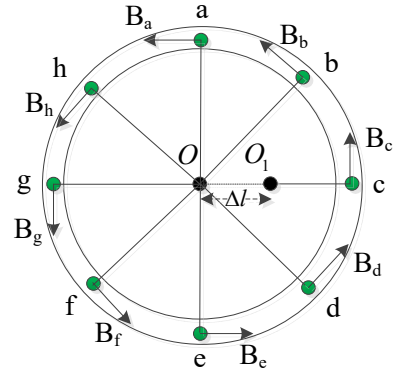


Fig. 2. Hall magnetic field sensor array.

2) Analysis of Interference Factors:

The influence of the number of Hall sensors, off-center position of the primary conductor and the uneven current distribution on the measurement accuracy is analyzed in this section.

In order to analyze the influence of the number of Hall sensors on the measurement accuracy, measurement error when employing various number of Hall sensors in the array is calculated as given in the Appendix. As shown in Table I, for small number of sensors, the measurement error is substantial e.g. it is 9.23% when only one sensor is employed. As the number of sensors increases, the measurement error decreases, but the cost also increases. The error is 6×10^{-7} when the number of sensors is 8. This negligible error meets the accuracy requirement of 0.2 level. Thus, considering the required measurement accuracy and implementation cost, 8 sensors are used to build the array in the developed hardware setup.

TABLE I
INFLUENCE OF NUMBER OF SENSORS ON THE MEASUREMENT ERROR

n	measurement error (%)	n	measurement error (%)
1	9.23	8	6.00E-5
2	5.16	10	7.20E-6
4	2.07	12	5.30E-7
6	2.10E-1	16	2.70E-9

Misalignment of the primary conductor is the most common phenomenon taking place when measuring the current signal using a current transformer. Fig. 2 shows a schematic diagram when the primary conductor is shifted from O to O_1 position with Δl off-center distance. Due to this misalignment, the measurement error can be expressed as follows:

$$I_e = 1 - \frac{\pi r}{4} * \left(\frac{2r^2 - \sqrt{2}r\Delta l}{2\pi r[r^2 + (\Delta l)^2 - \sqrt{2}r\Delta l]} + \frac{2r^2 + \sqrt{2}r\Delta l}{2\pi r(r^2 + (\Delta l)^2 + \sqrt{2}r\Delta l)} + \frac{r}{\pi(r^2 + (\Delta l)^2)} + \frac{1}{2\pi(r - \Delta l)} + \frac{1}{2\pi(r + \Delta l)} \right) \quad (4)$$

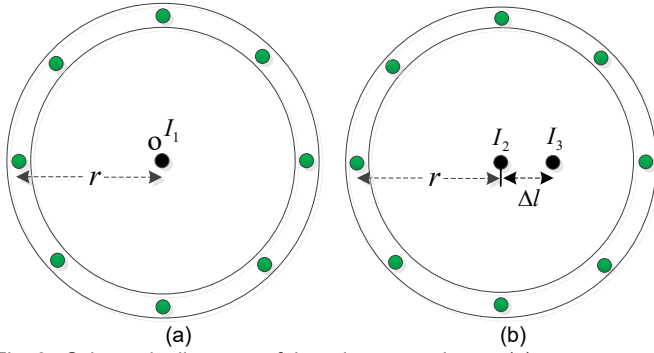


Fig. 3. Schematic diagrams of the primary conductor, (a) even current distribution. (b) uneven current distribution.

TABLE II

INFLUENCE OF UNEVEN CURRENT DISTRIBUTION ON MEASUREMENT ERROR

I_2 (A)	I_3 (A)	measurement error (%)
200	800	-0.008
400	600	-0.010
500	500	0.006
600	400	0.007
800	200	0.011

The above equation is analyzed when $r=0.1m$. Numerical analysis of (4) shows that the measurement error increases with the increase of the off-center distance where it exceeds 0.1% when Δl is 2.5mm. Therefore, the conductor off-center distance should be no more than 2.5mm to maintain the measurement accuracy standard. In practice, the off-center distance can be controlled by adding a fixed ring to maintain the position of the primary conductor.

In order to investigate the influence of uneven distribution of the conductor current on the measurement accuracy, the following analysis is carried out.

Fig. 3(a) shows a schematic diagram when the current is evenly distributed within the conductor while Fig. 3(b) shows two conductors A and B, separated by a distance Δl . For small value of Δl and when $I_1 = I_2 + I_3$, Fig. 3(b) can represent a situation when the current is not evenly distributed inside the conductor. For $I_1 = 1000A$ and $\Delta l = 1mm$, the variation of the measurement error with the uneven distribution of conductor current is shown in Table II. It can be seen from the table that the effect of uneven conductor current distribution on the measurement error is small and can be ignored.

According to the above analysis, the proposed ring sensor array features a strong anti-interference measurement ability and the current measurement accuracy is not significantly affected by the shape and position of the primary conductor.

B. DC Voltage Measurement Unit

The DC voltage measurement unit adopts a voltage divider concept using resistive and equalizing capacitive components. As shown in Fig.4, there is a H cascaded voltage divider circuits. The time constant which is correlated to the response time, is an important index to evaluate the performance of the voltage divider circuit. According to relevant technical conditions, the secondary output voltage of the divider needs to be stable within 5ms.

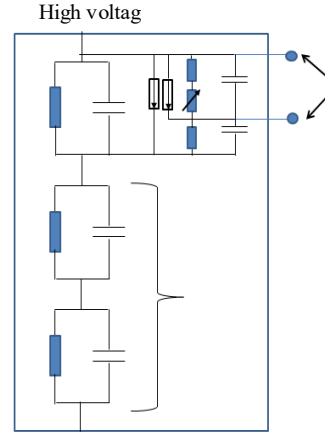


Fig. 4. Schematic of the DC voltage measurement unit.

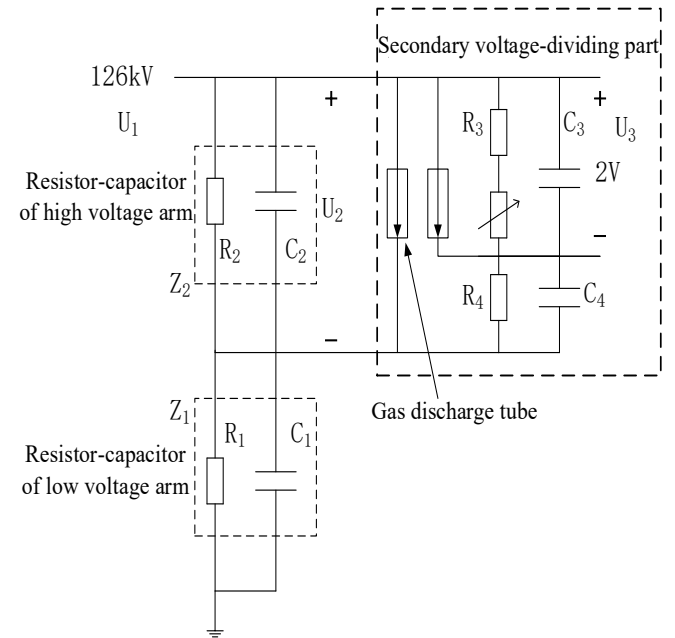


Fig. 5. Circuit diagram of the voltage divider.

Detailed circuit diagram of the DC voltage divider circuits is shown in Fig.5. For simplicity, the $H-I$ units of the low voltage arm in Fig.4 are combined into a single equivalent circuit comprising R_1 and C_1 as shown in Fig. 5.

To avoid the influence of uneven voltage distribution, parallel capacitors are utilized between the high and low voltage resistor arms to achieve voltage equalization. The ratio of the output voltage (U_2) to the input voltage (U_1) is:

$$\frac{U_2}{U_1} = \frac{Z_2}{Z_1 + Z_2} \quad (5)$$

Where the impedances of the high voltage (Z_1) and low voltage (Z_2) sides are given by:

$$\left\{ \begin{array}{l} Z_1 = \frac{R_1 \frac{1}{j\omega C_1}}{R_1 + \frac{1}{j\omega C_1}} \\ Z_2 = \frac{R_2 \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} \end{array} \right. \quad (6)$$

Using (5) and (6), the following equation can be derived:

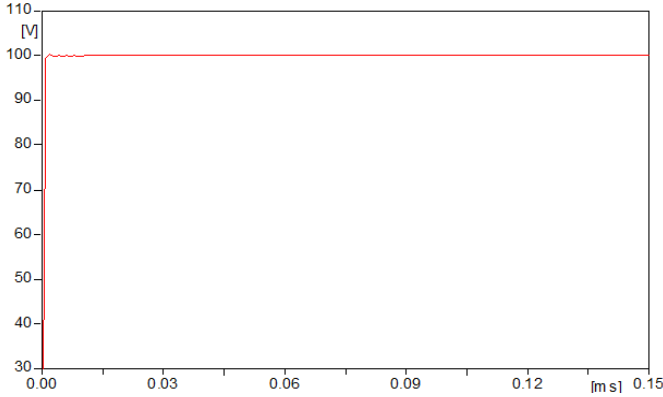


Fig. 6. Response time of the primary resistance and capacitance divider

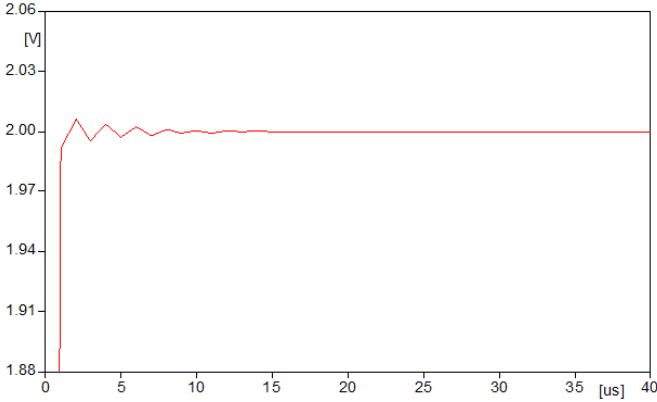


Fig. 7. Response time of the secondary resistance and capacitance divider.

$$\frac{U_2}{U_1} = \frac{(R_1 + R_2)R_2 + \omega^2 R_1^2 R_2^2 C_1 (C_1 + C_2)}{(R_1 + R_2)^2 + [\omega R_1 R_2 (C_1 + C_2)]^2} + j \frac{\omega(R_1 + R_2)R_1 R_2 C_1 - \omega R_1 R_2^2 (C_1 + C_2)}{(R_1 + R_2)^2 + [\omega R_1 R_2 (C_1 + C_2)]^2} \quad (7)$$

The output voltage varies in proportional to the input voltage when U_2/U_1 is a real number, and the waveform will not be distorted. Therefore, the imaginary part in (7) is to be eliminated by satisfying the following condition:

$$R_1 C_1 = R_2 C_2 \quad (8)$$

To improve the performance of the voltage divider circuit, the high and low voltage resistors and capacitors should be matched as much as possible to ensure the consistency of the time constants. Meanwhile, the time constant should be as small as possible for rapid measurement response time.

To calculate the response time of the voltage divider, the resistance of the low voltage arm R_1 is taken as 126M Ω , which is divided into 5 sections in series, the first four sections are of 25M Ω resistance each, and the last section is of 26M Ω resistance. C_1 is chosen to be 500pF, which is also divided into 5 sections in series, each section comprises 2500pF capacitance. The value of the high voltage arm resistance R_2 is 100k Ω . To ensure consistency of the time constants, C_2 is taken as 650nF. The overall response time of the output voltage measurement of this circuit is as shown in Fig.6. As can be seen, the transient time duration is less than 15 μ s after which the primary voltage reaches stable and constant level.

As shown in Fig. 5, a gas discharge tube is employed to protect the secondary voltage dividing circuit while a variable resistance is used to maintain the overall output voltage at 2V.

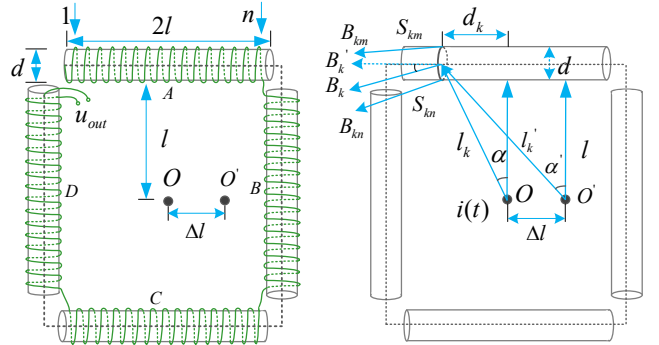


Fig. 8. Structure diagram of the proposed square Rogowski coil.

Considering the secondary voltage dividing, the ratio of the overall output voltage to the input voltage is:

$$\frac{U_3}{U_1} = \frac{R_2 R_3}{(1 + j\omega R_2 C_2)(1 + j\omega R_3 C_3)} \times \frac{1}{\left(\frac{R_2}{1 + j\omega R_2 C_2} + \frac{R_3}{1 + j\omega R_3 C_3} + \frac{R_4}{1 + j\omega R_4 C_4}\right)} \times \frac{1}{\left[\frac{R_1}{1 + j\omega R_1 C_1} + \frac{R_2 \left(\frac{R_3}{1 + j\omega R_3 C_3} + \frac{R_4}{1 + j\omega R_4 C_4}\right)}{(1 + j\omega R_2 C_2) \left(\frac{R_2}{1 + j\omega R_2 C_2} + \frac{R_3}{1 + j\omega R_3 C_3} + \frac{R_4}{1 + j\omega R_4 C_4}\right)}\right]} \quad (9)$$

In order to eliminate or reduce the imaginary part in (9), and by considering the design parameters mentioned above, the secondary voltage dividing resistance R_3 is set at 4.08k Ω with a 5 Ω variable resistance, C_3 is 16 μ F, R_4 is 100k Ω , and C_4 is 650nF. As shown in Fig.7, by using such design parameters, the overall output voltage is maintained at 2V, and the transient time duration is not more than 15 μ s, which meets the requirement of the time step response of secondary equipment.

C. Harmonic Measurement Unit

1) Sensor Design:

According to the national standard GB/T 26216.1-2019 [24], DC measurement unit needs to measure the DC current along with its harmonic contents. At present, optical and Rogowski coil sensors are commonly used for DC current harmonic measurement. However, the long-term measurement accuracy and stability of optical sensors are degraded due to the effect of environmental conditions such as temperature and humidity. Moreover, the cost of optical sensors is relatively high. On the other hand, Rogowski coil sensors are generally manufactured using PCB technology. Due to the limited size of the PCB, the number of coil turns is limited and hence the accuracy of measuring harmonic currents of low amplitudes is significantly reduced. To solve this problem, a Rogowski coil with a square skeleton is designed in this paper. The proposed Rogowski coil design consists of four straight bar coils as shown in Fig.8. The mathematical model of this design is analyzed below.

When the primary conductor current is in the center of the coil (point O in Fig. 8), the distances between the primary conductor current and the four sides of the square will be equal. Suppose $l \gg d$, the magnetic flux linkage on one side is:

$$\phi = \sum_{k=1}^N \phi_k = \frac{\mu_r \mu_0 d^2 N^2 (l + d/2) * i(t)}{8} * \sum_{k=1}^N \frac{1}{2l^2 (N^2 - 2Nk + 2k^2)} \quad (10)$$

where, ϕ_k is the magnetic flux of the k th turn coil, $\mu_r \mu_0$ is the magnetic permeability of the material and $i(t)$ is the current to be measured.

Considering the four straight bar coils, the final voltage output is:

$$u_{out} = -4 \frac{d\phi}{dt} = -\frac{\mu_r \mu_0 d^2 N^2 (l+d/2)}{2} * \sum_{k=1}^N \frac{1}{2l^2 (N^2 - 2Nk + 2k^2)} * \frac{di(t)}{dt} \quad (11)$$

The traditional Rogowski coil generally adopts a circular ring structure with inner and outer rings. While the inner ring can be fully wound up by coil turns, the outer ring cannot be fully wound, which makes the cross-sectional area of the coil turns uneven and thus the measurement accuracy is continuously affected by the misalignment of the primary conductor and other factors. The four straight bar coils in the square Rogowski coil proposed in this paper can be symmetrically wound to maintain consistent coil turns and hence improved measurement accuracy. Moreover, in contrary with the limited number of turns of the conventional Rogowski coil, the number of turns of the proposed square Rogowski coil can reach tens of thousands in a space of 20 cm diameter, which can realize accurate measurement of weak harmonic signals.

The design parameters of the proposed Rogowski coil shown in Fig. 8 are: $d=10\text{mm}$, $N=2000$ turns, and $l=80\text{mm}$. For 50 Hz, 100A current, the output voltage of the square Rogowski coil is about 60mV. When the primary conductor is Δl away from the coil center (as shown by point O' in Fig. 8), the distance between the primary conductor current and the four square sides is no longer equal. For the convenience of analysis, the square Rogowski coil is divided into four sides A , B , C and D , as shown in Fig.8. For A and C -side coils, the magnetic flux linkage is:

$$\phi_A = \phi_C = \sum_{k=1}^N \phi_k = \frac{\mu_r \mu_0 d^2 N^2 (l+d/2) * i(t)}{8} * \sum_{k=1}^N \frac{1}{2l^2 (N^2 - 2Nk + 2k^2) + 2lN\Delta l (N-2k) + (\Delta l)^2} \quad (12)$$

Similarly, for B -side coils, the magnetic flux linkage is:

$$\phi_B = \sum_{k=1}^N \phi_k = \frac{\mu_r \mu_0 d^2 N^2 (l+d/2-\Delta l) * i(t)}{8} * \sum_{k=1}^N \frac{1}{2l^2 (N^2 - 2Nk + 2k^2) - 2lN^2 \Delta l + N^2 (\Delta l)^2} \quad (13)$$

For D -side coils, the magnetic flux linkage is:

$$\phi_D = \sum_{k=1}^N \phi_k = \frac{\mu_r \mu_0 d^2 N^2 (l+d/2+\Delta l) * i(t)}{8} * \sum_{k=1}^N \frac{1}{2l^2 (N^2 - 2Nk + 2k^2) + 2lN^2 \Delta l + N^2 (\Delta l)^2} \quad (14)$$

Therefore, the total magnetic flux linkage is:

$$\phi_{\Sigma} = \phi_A + \phi_B + \phi_C + \phi_D \quad (15)$$

The measurement error is:

$$U_e = \left| \frac{4\phi - \phi_{\Sigma}}{4\phi} \right| = \left| 1 - \frac{\phi_{\Sigma}}{4\phi} \right| \quad (16)$$

The relationship between measurement error and the off-center distance is investigated when $d=10\text{mm}$, $N=2000$ turns, and $l=80\text{mm}$. The simulation results shown in Fig.9 reveal that the measurement error increases with the increase of the off-center distance, and the measurement error is less than 0.08% when the off-center distance is less than 2mm. Although the deviation of the installation position will have a certain impact on the measurement accuracy of the square Rogowski coil, the measurement error can be maintained less than 0.1% by improving the manufacturing process, fixing the installation and other measures, which meet the relevant requirements.

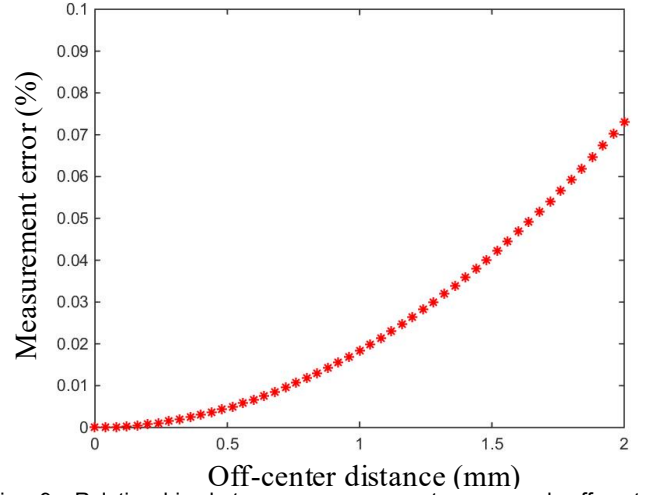


Fig. 9. Relationship between measurement error and off-center distance.

2) Digital Integration Algorithm Design:

It can be seen from (11) that the output voltage of the Rogowski coil is the differential of the measured current. If the output voltage of Rogowski coil is measured directly, it will be 10 times different than the power frequency and the 10-th harmonic component of the same amplitude, which brings difficulties to the design of the subsequent circuits. Meanwhile, the frequency fluctuation also affects the coil output, resulting in measurement errors, so the output voltage of the coil needs to be integrated in order to calculate the current. The commonly used analog integrators result in a large error due to the influence of dispersion of the analog devices, bias voltage and other factors [25]. Digital integrator on the other hand, does not exhibit these problems, so it has great application prospects. Rectangular integral, trapezoidal integral and Simpson integral algorithms are commonly used digital integration algorithms [26]. One of the main indicators for evaluating the performance of digital integration is its consistency with the ideal integral response curve. The integral algorithms mentioned above have a certain deviation from the ideal integral response curve. In view of this situation, an improved digital integration algorithm is proposed in this paper. The z -transform transfer function of this digital integration algorithm is as follows:

$$H_g(z) = \frac{T}{32} \frac{7 + 8z^{-1/4} + z^{-1/2}}{1 - z^{-1/2}} \quad (17)$$

The ideal integral transfer function in the frequency domain is:

$$H_I(j\omega) = \frac{1}{j\omega} \quad (18)$$

The amplitude and phase characteristics of the above-mentioned digital integrals along with the ideal integral are shown in Fig.10. It can be seen that the amplitude response of the proposed digital integral transfer function in (17) is consistent with the ideal integral, but the phase responses of the two integrals are a bit different. Therefore, it is necessary to add appropriate delay factor to improve the phase performance of the proposed integral. In Fig. 10(b), the phase response of the proposed integral is -72.72° when the normalized frequency is 1. Hence, the required delay factor λ should satisfy the equation $-72.72 + 180\lambda = -90$ which results in $\lambda = -0.096$. When this delay factor is considered, the transfer function in (17), is modified to:

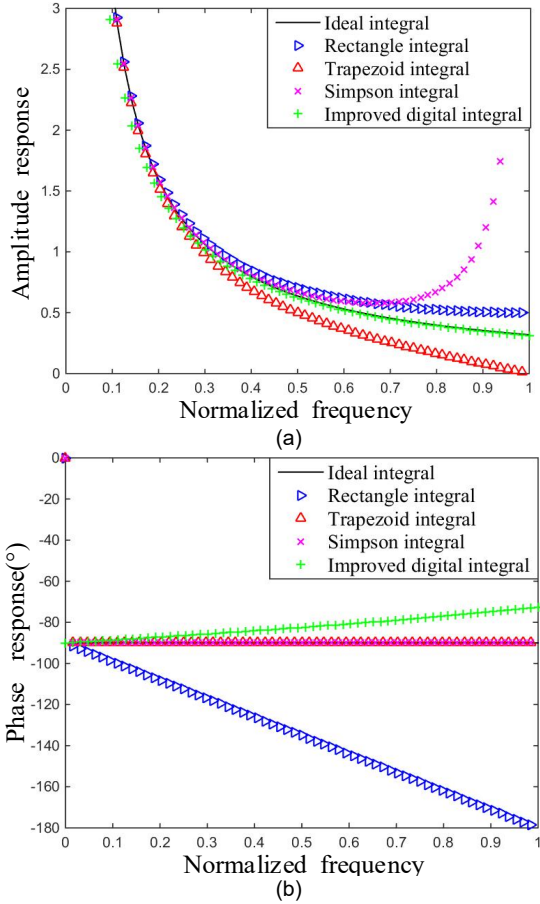


Fig. 10. Response curves of different digital integrals. (a) Amplitude response, (b) Phase response.

$$H_N(z) = \frac{T}{32} z^{-0.096} \frac{7 + 8z^{-1/4} + z^{-1/2}}{1 - z^{-1/2}} \quad (19)$$

The added delay factor won't affect the amplitude response of the proposed integral as can be seen from Fig. 11(a). On the other hand, Fig. 11(b) shows that the phase response of the improved digital integral with the added delay factor is consistent with that of the ideal integral, and thus the integral error is negligible. Since fractional part of (19) cannot be directly realized in practical applications, it can be converted into a series sum of integer approximate delays using finite impulse response (FIR) Lagrange interpolator filters and Thiran all pass infinite impulse response (IIR) filters [27].

The accuracy of the digital integration is affected by the sampling frequency. The errors at different sampling frequencies (4 kHz, 6.4 kHz and 12.8 kHz) are shown in Fig. 12. By comparing the amplitude error at three different sampling frequencies, it can be observed that the error can be effectively decreased by increasing the sampling frequency. In practical applications, the sampling frequency is usually set at 12.8 kHz, which results in an error of less than 0.001 which meets the accuracy requirement of the harmonic measurement.

D. Acquisition and transmission unit

The acquisition and transmission unit receives the signals from the measurement units, including DC voltage signal, DC current signal and harmonic signals as shown in the functional schematic diagram of Fig. 13.

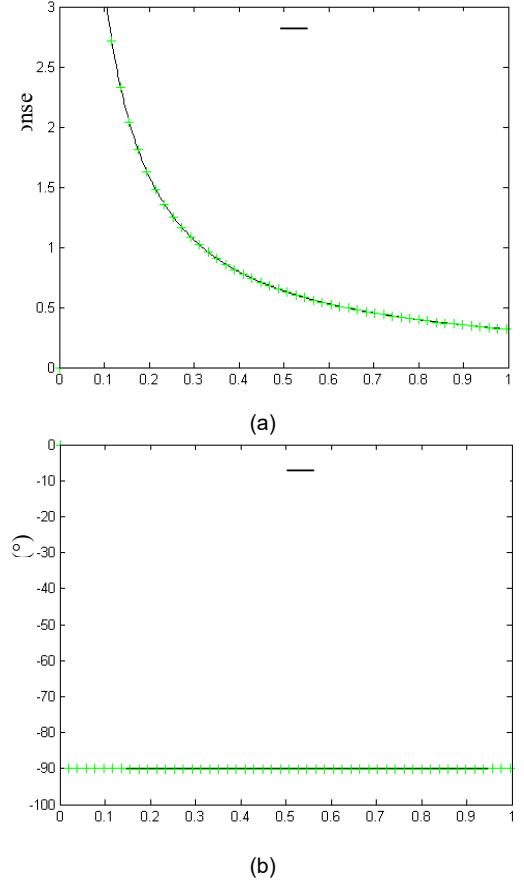


Fig. 11. Improved digital integral response curves with a delay factor. (a) Amplitude response, (b) Phase response.

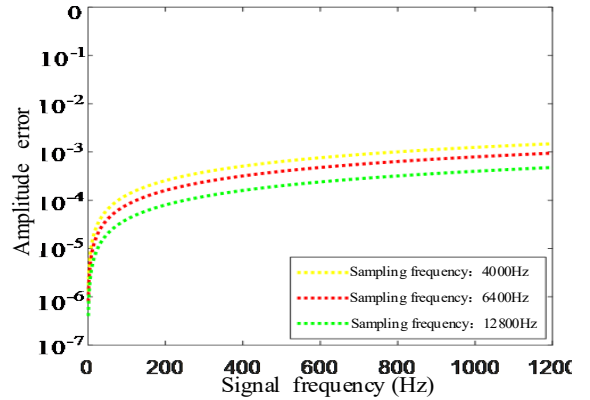


Fig. 12. Influence of sampling frequency on the digital integration amplitude error.

The output signals of the three channels, are transmitted to the signal processing and signal filtering circuits and then converted into digital signals through the analog to digital (A/D) circuit. The digital signals are then passed into a microprocessor (MCU) for frame processing after which the processed signals are transmitted to the merging unit in the low voltage side through optical fibers. The MCU receives the synchronized signals from the merging unit and controls the A/D converter. The circuits of high voltage side are energized by laser power. The power supply and communication between the high voltage side and the low voltage side are realized by optical fiber, which effectively ensures the isolation between the two sides and improves the anti-interference performance of the signal transmission.

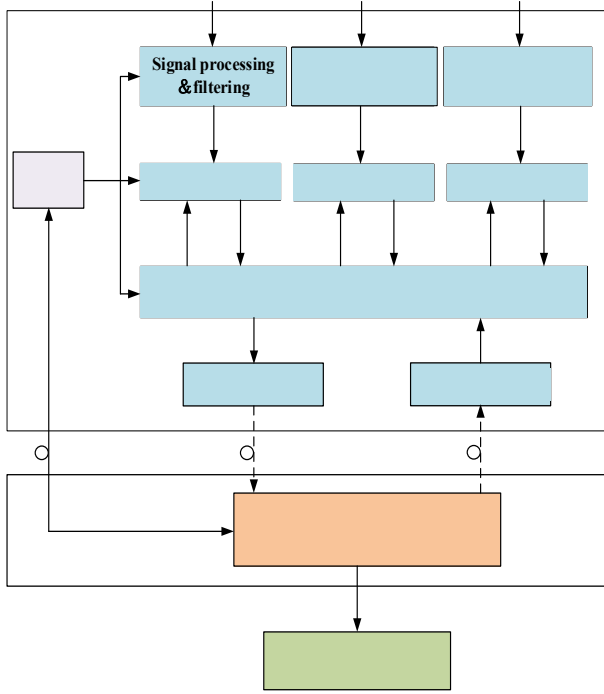


Fig. 13. Functional schematic diagram of the acquisition and transmission unit.

E. Measurement software algorithm

The merging unit frames the signals received from the acquisition and transmission unit according to IEC 61850-9-2 after which it transmits the processed data to a subsequent smart device or personal computer (PC) [28].

The developed PC software graphical user interface (GUI) is shown in Fig.14 This software can analyze, calculate, display and store data of DC voltage, DC current and harmonics. Meanwhile, pressure and early warning of SF₆ leakage used in the gas discharge protection tube can be monitored. The proposed algorithm along with simulation results are presented below.

1) Principle of four-spectral line interpolation based on trapezoidal self-convolution window:

In order to extract the DC and harmonic current signals accurately, windowed FFT algorithms are usually used [29]. To overcome the issue of spectrum leakage and fence effect caused by asynchronous sampling, the selection of a window function with good performance is a key for precise signal analysis [30]. In this paper, a four-spectral line interpolation FFT algorithm based on trapezoidal self-convolution window is adopted. The time-domain expression of the trapezoidal window is:

$$w_{\text{Tra}}(t) = \begin{cases} \frac{2ht}{T-l} & 0 \leq t < \frac{T-l}{2} \\ h & \frac{T-l}{2} \leq t < \frac{T+l}{2} \\ \frac{2(T-t)}{T-l} & \frac{T+l}{2} \leq t < T \end{cases} \quad (20)$$

where h is the trapezoidal window height, usually 1.

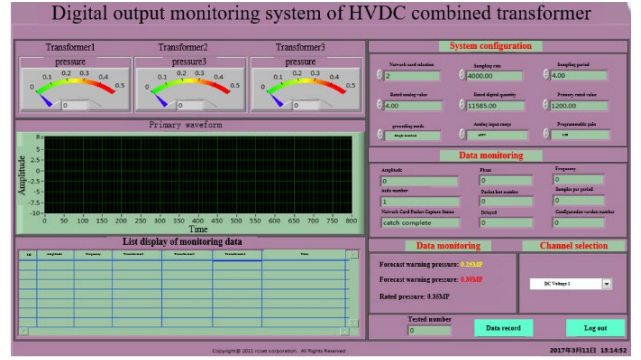


Fig. 14. Developed digital output GUI monitoring system.

By discretizing the trapezoidal window into a discrete trapezoidal window sequence with a length of M , equation (21) can be obtained:

$$w_{\text{Tra}}(t) = \begin{cases} \frac{2m}{M-L-1} & 0 \leq m < \frac{M-L-1}{2} \\ 1 & \frac{M-L-1}{2} \leq m < \frac{M+L-1}{2} \\ \frac{2(M-m-1)}{M-L-1} & \frac{M+L-1}{2} \leq m < M \end{cases} \quad (21)$$

where, M is the time domain length, and L is the upper length of the trapezoidal window.

In order to ensure that the trapezoid is an isosceles, the upper length of the trapezoidal window is generally even and is in the range of $0 < L < M - 2$.

When $M=128$ and $L=20$, the amplitude frequency response is as shown in Fig.15.

The trapezoidal convolution window is the result of time domain convolution of several trapezoidal windows. Suppose P is the order of convolution, then the P -order trapezoidal self-convolution window can be expressed as follows:

$$w_{\text{Tp}} = \underbrace{w_{\text{Tra}}(t) * w_{\text{Tra}}(t) * \dots * w_{\text{Tra}}(t)}_P$$

According to the convolution theorem, the convolution of trapezoidal windows in the time domain is equal to their multiplication in the frequency domain, so the expression of trapezoidal self-convolution window in frequency domain is:

$$W_{\text{Tra-p}}(\omega) = \underbrace{W_{\text{Tra}}(\omega) W_{\text{Tra}}(\omega) \dots W_{\text{Tra}}(\omega)}_P = [W_{\text{Tra}}(\omega)]^P \quad (23)$$

The sidelobe peak level and sidelobe attenuation rate of the trapezoidal self-convolution window depend on the convolution order. The higher the convolution order, the better the sidelobe performance of the trapezoidal window. The principal lobe width of the four order self-convolution window is $8\pi/(M-1+L)$. The peak level of the sidelobe is -128, and the attenuation rate is 48. In order to reduce the error caused by the fence effect, FFT harmonic detection method based on spectral line interpolation principle is often used. The four-spectral lines interpolation method takes full account of the spectrum information contained in the four spectral lines near the peak point. The correction value of the harmonic parameter can be obtained through weighted operation. The accuracy of this method is higher than the three- and the two-spectral lines interpolation methods.

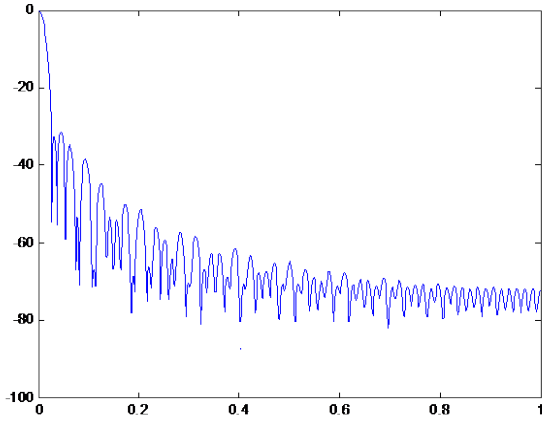


Fig. 15. Amplitude frequency response of trapezoidal window.

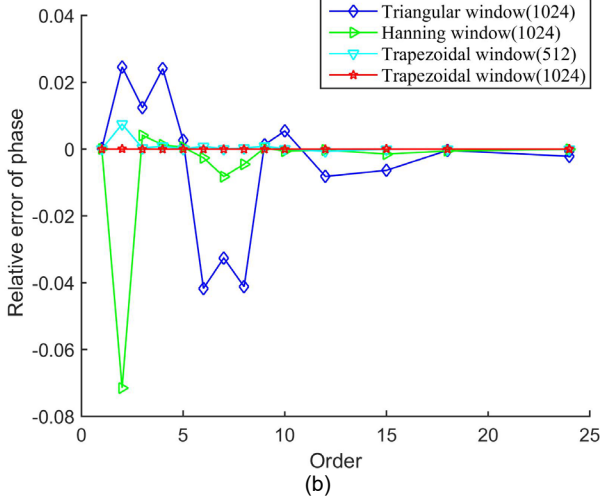
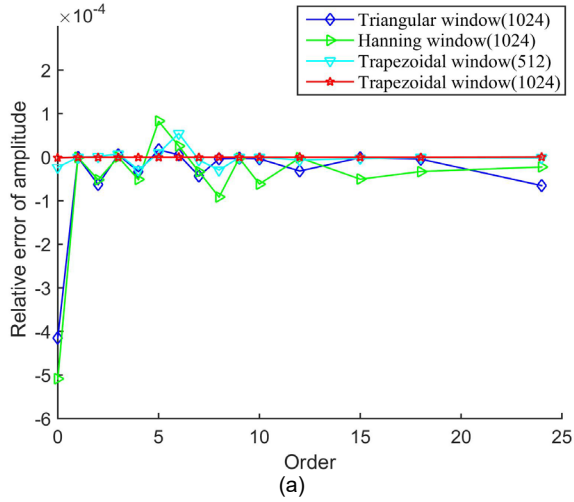


Fig. 16. Accuracy of various window functions in harmonic analysis. (a) Amplitude relative error, (b) Phase relative error.

2) Simulation analysis:

In order to verify the robustness of the trapezoidal window, the accuracy of the fourth order trapezoidal self-convolution window, fourth order triangular window and fourth order Hanning window are analyzed by Matlab. The results are shown in Fig. 16. It can be seen from the simulation results that when the number of sampling points is 512, the accuracy of the four-spectral line interpolation algorithm based on four order

trapezoidal self-convolution window used in this paper is higher than the Hanning self-convolution window with 1024 sampling points. When the number of sampling points of the four-line interpolation algorithm based on four order trapezoidal self-convolution window is 1024, the extraction accuracy of the DC current and harmonic components is higher than the other algorithms, which attests the accuracy of the proposed method in this paper.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Experimental Results

To validate the effectiveness of the proposed combined method for DC voltage and current measurements, a prototype of the proposed structure in Fig. 1 is built with design parameters: rated voltage (U_n), $\pm 126\text{kV}$ with error less than $\pm 0.2\%$ in the range of $10\%U_n$ to $120\%U_n$. Rated current (I_n), 3000A , with error less than $\pm 0.2\%$ in the range of $10\%I_n$ to $120\%I_n$. The measurement range for harmonics is 50 Hz to 1200 Hz . When the harmonic current is $20\%I_n$, the amplitude error for harmonic measurement is less than $\pm 0.5\%$, and the phase error is less than $500\mu\text{s}$.

A schematic diagram of the measurement experimental setup is shown in Fig. 17. In the developed setup, the error of the proposed combined measurement device is obtained by comparing its measurement results with that obtained using a standard transformer. In order to verify the performance and accuracy of the developed hardware, the below measurements were carried out.

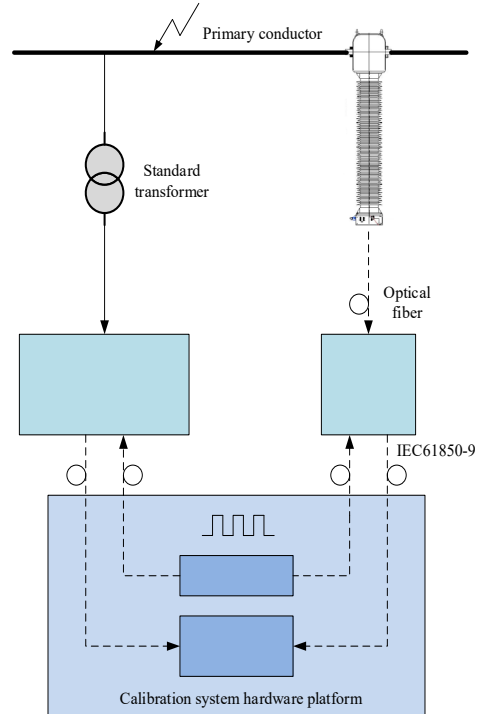


Fig. 17. Schematic diagram of the measurement experimental setup.

The accuracy of the DC current measurement is tested within the range 300A to 3600A , corresponding to 10% to 120% of the rated current, as listed in Table III. As can be seen, the error variation of the current measurement is less than 0.104% in the range of 10% to 120% of the rated current, and the error variation at the same test point is less than 0.012% in the

process of current rise and fall. This validates the high accuracy of the proposed method in measuring the DC current.

TABLE III
ACCURACY TEST FOR DC CURRENT MEASUREMENT

Percentage of rated current (%)	Ratio error (%)	Percentage of rated current (%)	Ratio error (%)
10	0.039	drop to 10	0.031
20	0.029	drop to 20	0.025
40	0.012	drop to 40	0.016
60	-0.042	drop to 60	-0.031
80	-0.051	drop to 80	-0.044
100	-0.062	drop to 100	-0.061
120	-0.065	/	/

To assess the accuracy of the voltage measurement, a rated voltage of $\pm 126\text{kV}$ is considered in the test. The rated digital output is 2D41H. The test results obtained by changing the applied DC voltage in the range 10% to 120% of the rated voltage as shown in Table IV. From the table, the error variation of the voltage measurement is less than 0.098% in the range of 10% to 120% of the rated voltage, and the error variation at the same test point is less than 0.010% in the process of voltage rise and fall. These results prove the high accuracy of the proposed method in measuring the DC voltage.

Based on the national standard GB/T 20840.8-2007 [31], the accuracy of the harmonic current measurement is tested within the range 1 to 24th harmonic orders with a fundamental component of 100 A. Measurements listed in Table V show that in this harmonic range, the ratio error of the harmonic current measurement unit is less than $\pm 0.2\%$, while the phase error is less than $\pm 8'$, and the phase deviation of each harmonic measurement is far less than the designed target of 500 μs .

The obtained measurement accuracy is higher than the non-contact voltage transformer method reported in [32] and the electronic current transformer method presented in [33]. It is worth mentioning that conventional devices can only perform one measurement task for either voltage or current which calls for two transformers and two insulating bushings to perform simultaneous voltage and current measurements. The proposed combined measurement device only needs one insulating bushing and one standard transformer. In addition, a ring hall sensor array is used for dc current measurement, which substantially reduces the volume, weight and cost of the proposed device compared with the conventional current transformer based on diverter principle. This makes the proposed device a cost-effective candidate for HVDC networks control and protection systems applications.

TABLE IV
ACCURACY TEST FOR DC VOLTAGE MEASUREMENT

Percentage of rated voltage (%)	Ratio error (%)	Percentage of rated voltage (%)	Ratio error (%)
10	0.041	drop to 10	0.049
50	-0.032	drop to 50	-0.039
80	0.027	drop to 80	0.018
100	0.035	drop to 100	0.033
120	0.059	/	/

TABLE V
ACCURACY TEST FOR HARMONIC MEASUREMENT

Harmonic orders	Ratio error (%)	Phase error (')	harmonic orders	Ratio error (%)	Phase error (')
1	-0.1126	-0.306	13	-0.0932	-4.031
2	-0.1096	-0.683	14	-0.0911	-4.170
3	-0.1112	-0.878	15	-0.1096	-5.683
4	-0.1061	-1.009	16	-0.1112	-5.878
5	-0.1045	-1.744	17	-0.1061	-6.009
6	-0.1332	-2.353	18	-0.1098	-6.594
7	-0.1675	-2.092	19	-0.1101	-6.789
8	-0.1446	-2.485	20	-0.1086	-7.736

B. Discussion

The proposed measuring device features several advantages when compared with the traditional single function measurement transformer in terms of reduced volume, weight and cost. The proposed device is expected to find wide applications in the protection and control of the HVDC networks. However, there still two key shortcomings call for further improvement; these are: 1) the use of new sensing technology such as the optical microelectromechanical systems to further decrease the device size and improve its reliability; 2) the proposed device utilizes two sensing units to realize simultaneous voltage and current measurements. Development of a new multi-parameter sensor will enable the device to perform such measurements using only one sensing unit and hence reducing its cost and complexity. While the current research on multi-parameter sensors mainly focuses on the simultaneous measurements of non-electrical signals such as temperature and humidity, a sensor for simultaneous voltage and current measurements is expected to receive much attention in the future research direction especially with the global trend to establish micro / smart grids and HVDC networks.

V. CONCLUSION

In this paper, a combined technique to simultaneously measure the DC voltage, current and harmonic current is proposed. The rated voltage of the DC voltage measurement unit is $\pm 126\text{kV}$, with a variation error less than 0.098% within the range of 10%~120% of the rated voltage. The rated current of the DC current measurement unit is 3000A, with a variation error less than 0.104% in the range of 10%~120% of the rated current. The frequency range for the harmonic current measurement is 50~1200Hz, the ratio error is less than 0.2%, and the phase error is less than 8'. This combined measurement technique features small size, low cost, high accuracy, wide frequency band and of is of reliable digital output, which is in line with the future development direction of digital substation automation systems.

APPENDIX

Influence of the number of sensors on measurement accuracy:

Fig.A-1 shows the influence of the number of array's sensors on the measurement accuracy. Conductor B is located at the center of the sensor array that comprises n -Hall sensors evenly distributed on a circle of radius r . In the figure, B_{Ak} and B_{Bk} are the magnetic field densities generated due to currents in two

adjacent conductors A and B that are measured by the k -th hall sensor, d is the distance between the two conductors and θ_k is the angle between the k -th Hall sensor and AB line. When the two conductors' currents are equal in magnitude and opposite in direction, the measurement error I_e as a function of the number of sensors and the physical dimensions of the ring Hall sensor array is:

$$I_e = -\frac{r}{n} \sum_{k=1}^n \frac{d \cos \theta_k + r}{d^2 + r^2 + 2dr \cos \theta_k} \quad (\text{A-1})$$

Equation (A-1) is used to obtain the results in Table I by assuming $r = 0.1\text{m}$ and $d = 1\text{m}$.

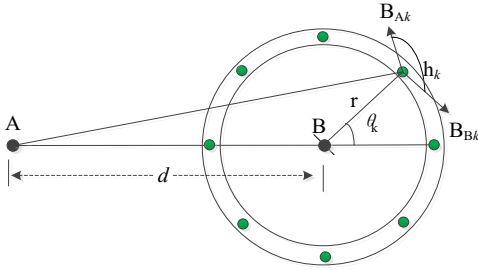


Fig. A-1. Influence of the number of sensors on the measurement accuracy.

REFERENCES

- [1] M. Mohan and K. P. Vittal, "DC Fault Protection in Multi-terminal VSC-Based HVDC Transmission Systems with Current Limiting Reactors," *J. of Electrical Engineering and Technology*, vol. 14, no. 1, pp. 1–12, 2019.
- [2] C. Yong, H. W. Yuan, X. Song, et al., "Model, design, and testing of field mill sensors for measuring electric fields under high-voltage direct-current power lines," *IEEE Trans. Industrial Electronics*, vol. 65, no. 1, pp. 608–615, Jun. 2017.
- [3] Q. Nguyen, G. Todeschini, S. Santoso, "Power Flow in a Multi-Frequency HVAC HVDC System: Formulation, Solution, & Validation," *IEEE Trans. Power Systems*, vol. 34, no. 4, pp. 2487–2497, 2019.
- [4] A. Elserougi, A. M. Massoud, and S. Ahmed, "A Grid-Connected Capacitor-Tapped Multi-Module Converter for HVDC Applications: Operational Concept and Control," *IEEE Trans. Industry Applications*, vol. 54, no. 5, pp. 5523–5535, Jan. 2018.
- [5] L. Callegaro, C. Cassiogo, and E. Gasparotto, "On the Calibration of Direct-Current Current Transformers," *IEEE Trans. Instrumentation and Measurement*, vol. 69, no. 3, pp. 723–727, Mar. 2015.
- [6] S. Shao, M. Jiang, J. Zhang, et al., "A Capacitor Voltage Balancing Method for a Modular Multilevel DC Transformer for DC Distribution System," *IEEE Trans. Power Elec.*, vol. 33, no. 4, pp. 3002–3011, 2018.
- [7] I. A. Gowaid, G. P. Adam, Ahmed M. Massoud, et al., "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability," *IEEE Trans. Power Electronics*, vol. 30, no. 1, pp. 108–123, Jan. 2015.
- [8] D. Jovicic and B. T. Ooi, "Developing DC Transmission Networks Using DC Transformers," *IEEE Trans. Power Delivery*, vol. 25, no. 4, pp. 2535–2543, Nov. 2010.
- [9] C. S. Li, H. M. Shao, W. Zhao, J. F. Wang, "Wide-frequency Measurement Characteristics of DC Fiber-optic Current Transformer," *Automation of Electric Power Systems*, vol. 41, no. 20, pp. 151–156, Oct. 2017.
- [10] S. Veinovic, M. Ponjavic, S. Milic, and R. Djuric, "Low-power design for DC current transformer using class-D compensating amplifier," *IET Circuits, Devices & Systems*, vol. 12, no. 3, pp. 215–220, May. 2018.
- [11] G. Montenero, P. Arpaia, A. Ballarino and L. Bottura, "Design, Assembly, and Commissioning of a Cryogenic DC Current Transformer Designed for Measuring Currents of up to 80 kA," *IEEE Trans. Applied Super.*, vol. 25, no. 3, pp. 1–6, Jun. 2015.
- [12] X. Xiao, H. L. Hu, Y. Xu, et al., "Research on the Error Characteristics of a 110 kV Optical Voltage Transformer under Three Conditions: In the Laboratory, Off-Line in the Field and During On-Line Operation," *Sensors*(14248220), vol. 16, no. 8, pp. 1303, Aug. 2016.
- [13] X. Cui and G. Q. Zhang, "Sensitivity analysis and automatic design of voltage ratio in an optical instrument voltage transformer," *IEEE Trans. Magnetics*, vol. 35, no. 3, pp. 1769–1772, May. 1999.
- [14] R. F. Xie, Q. F. XU, N. Xie, and C. Li, "A method for improving electric field distribution of OVTS electro-optical crystal," *Automation of Electric Power Systems*, vol. 40, no. 6, pp. 91–96, May. 2016.
- [15] H. X. Wang, G. Q. Zhang, X. G. Cai, et al., "Development of Precise Capacitive Voltage Divider for Optical Voltage Transformer," *Power system automation*, vol. 33, no. 8, pp. 72–76, Apr. 2009.
- [16] F. Rahmatian, P. P. Chavez, and N. A. F. Jaeger, "230 kV Optical Voltage Transducers Using Multiple Electric Field Sensors," *IEEE Trans. Power Delivery*, vol. 17, no. 2, pp. 417–422, Aug. 2002.
- [17] P. P. Zhu, G. X. Zhang, C. M. Luo, et al., "Application and error analysis of the quadrature methods in the voltage transformer," *High Voltage Engineering*, vol. 34, no. 5, pp. 919–924, May. 2002.
- [18] P. P. Chavez, N. A. F. Jaeger, and F. Rahmatian, "Accurate voltage measurement by the quadrature method," *IEEE Trans. Power Delivery*, vol. 18, no. 1, pp. 14–19, Feb. 2002.
- [19] A. Cataliotti, D. D. Cara, A. E. Emanue, and N. Salvatore, "Characterization and Error Compensation of a Rogowski Coil in the Presence of Harmonics," *IEEE Trans. Instrumentation and Measurement*, vol. 60, no. 4, pp. 1175–1181, May. 2011.
- [20] M. Gupta, B. Relan, R. Yadav, and V. Aggarwal, "Wideband digital integrators and differentiators designed using particle swarm optimization," *IET Signal Processing*, vol. 8, no. 6, pp. 668–679, 2014.
- [21] T. Mao, J. Le, Y. L. Huang, and H. W. Luo, "A novel AC side harmonic voltage measurement scheme of high-voltage DC power systems," *Proceedings of the Chinese Society of Electrical Engineering*, vol. 35, no. 4, pp. 796–803, Apr. 2015.
- [22] B. Zeng, Q. Tang, B. Y. Qin, et al., "Spectral analysis method based on improved FFT by Nuttall self-convolution window," *Transactions of China Electrotechnical Society*, vol. 29, no. 7, pp. 59–65, Jul. 2014.
- [23] H. Wen, et al., "Harmonic estimation using symmetrical interpolation FFT based on triangular self-convolution window," *IEEE Trans. Industrial Informatics*, vol. 11, no. 1, pp. 16–26, 2015.
- [24] *DC current measuring device for HVDC transmission system-Part 1: Electronic DC current measuring device*, Chinese National Standard GB/T 26216.1-2019, 2019.
- [25] Z. H. Li, X. Xiang, T. H. Hu, et al., "An improved digital integral algorithm to enhance the measurement accuracy of Rogowski coil-based electronic transformers," *International Journal of Electrical Power & Energy Systems*, vol. 118, no. 1, pp. 105806, Jun. 2020.
- [26] B. Zeng, Z. S. Teng, Y. Cai, and H. Wen, "Harmonic Phasor Analysis Based on Improved FFT Algorithm," *IEEE Trans. Smart Grid*, vol. 2, no. 1, pp. 51–59, Mar. 2011.
- [27] M. A. Al-Alaoui, "Using fractional delay to control the magnitudes and phases of integrators and differentiator," *IET Signal Processing*, vol. 1, no. 2, pp. 107–119, Jun. 2007.
- [28] *Communication networks and systems in substation-Part 9-2: Specific communication service mapping*, document IEC 61850-9-2, 2004.
- [29] H. Wen, J. Zhang, W. Yao, et al., "FFT-based amplitude estimation of power distribution systems signal distorted by harmonics and noise," *IEEE Trans. Industrial Informatics*, vol. 14, no. 4, pp. 1447–1455, 2017.
- [30] H. Wen, Z. S. Teng, Y. Wang, and H. G. Hu, "Spectral correction approach based on desirable sidelobe window for harmonic analysis of industrial power system," *IEEE Trans. Industrial Electronics*, vol. 60, no. 3, pp. 1001–1010, Feb. 2012.
- [31] *Instrument transformers-part 8: Electronic current transformers*, Chinese National Standard GB/T 20840. 8-2007, 2007.
- [32] Q. Zhou, H. Wei, S. N. Li, et al., "Experimental research of unipolar capacitive voltage transformer," *High Voltage Engineering*, vol. 42, no. 6, pp. 1781–1789, Jun. 2016.
- [33] G. Montenero, P. Arpaia, A. Ballarino, et al., "Design, assembly, and commissioning of a cryogenic DC current transformer designed for measuring currents of up to 80 kA," *IEEE Trans. Applied Superconductivity*, vol. 25, no. 3, pp. 1–6, Jun. 2015.