**School of Electrical Engineering, Computing and Mathematical Sciences**

# Mitigating Electromagnetic Interference in Power Converters for Radio Astronomy Applications

**James Buchan**
**0000-0002-4607-1205**

**This thesis is presented for the Degree of**
**Doctor of Philosophy**
**of**
**Curtin University**

**September 2021**

# Declaration

To the best of my knowledge and belief this thesis contains no material previously published by any other person except where due acknowledgement has been made.

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university

Signature: .....

Date: 17/09/2021

# Abstract

With electromagnetic compatibility (EMC) standards becoming increasingly rigorous, the requirement to improve electromagnetic interference (EMI) mitigation in power converters becomes essential during the design stage. Supplying and distributing power in radio astronomy applications is no exception. Strict EMC limits are specified to ensure the radio telescope will operate free from unwanted EMI. Although commercial and military EMC standards define strict compliance limits, future radio astronomy projects, such as the Square Kilometre Array (SKA) radio telescope, have more stringent EMC requirements, which ensure the performance of the radio telescope is not limited.

Power supply solutions for radio astronomy must be radio-quiet, and research efforts consider EMI mitigation techniques at the power or control stage of the power converter. Applications such as communications and defence also require adherence to strict EMC requirements. Furthermore, modern power converter design emphasises EMI mitigation and EMC compliance due to the proliferation of noisy and sensitive electronic equipment and the increasing demand for reliable electronic systems. One significant contribution is the desire for power converters to operate at higher switching frequencies to achieve miniaturisation and increase power density, inherently generating more EMI. The high-frequency EMI signals are generated within power converters by the rapid change in voltage and current levels when semiconductor devices undergo switching transitions.

Novel EMI mitigation techniques become critical to the power converter design process to ensure compliance with EMC standards of continually increasing stringency. Many technical and computational design considerations, including novel approaches, must be applied to power converters when considering EMC compliance for radio astronomy applications. A comprehensive understanding of power converter EMI generation mechanisms and mitigation techniques is required. This dissertation presents a comprehensive review of EMI mitigation techniques in power converters, identifying suitable techniques for radio astronomy applications. The summary concerns multiple

EMI mitigation techniques, including conventional design techniques, power circuitry specific mitigation approaches, and control system strategies. Additionally, the thesis contextualises the scope of EMI mitigation for radio-astronomy applications by presenting the SKA EMC requirements as an example.

EMI attenuation is not a straightforward process. Therefore, the review of EMI mitigation techniques provides a framework for designing low-EMI power converters. A systematic design methodology is presented, which provides an approach for developing low-noise power converters that target high-frequency EMI attenuation using novel techniques to produce shaped switching transitions. The systematic approach synthesises known strategies with new insights for achieving shaped switching transitions, providing valuable background information for radio astronomy design engineers and engineers facing similar technical challenges in other fields. Crucially, the design strategy presented helps identify and bridge the gap between power converter design and stringent EMI requirements for radio astronomy applications.

The logistic function introduced in this dissertation is another infinitely differentiable function with temporal characteristics that can be manipulated for low-EMI applications. Time and frequency-domain analysis are presented, including time-domain waveform synthesis and an analytical Fourier series derivation of a logistic shaped waveform. The analysis demonstrates that suitably defined temporal characteristics achieve significant spectral roll-off. Furthermore, an EMI performance comparison with trapezoidal, sinusoidal, and S-shaped transitions is presented to demonstrate the suitability of logistic-shaped functions for low-EMI applications where high-frequency EMI attenuation is required.

A simulation study and prototype of a low-EMI half-bridge capable of undergoing logistic-shaped switching transitions to achieve high-frequency EMI mitigation is presented. The research demonstrates that waveform shaping technology can be achieved using pulse width modulation switching control in a half-bridge converter. The computational modelling initially demonstrates the feasibility of the waveform shaping technology and the suitability of the control algorithm.

The half-bridge prototype is a novel topology that employs gate-drive control of both a power MOSFET and current injection MOSFET. The gate-drive control allows for the respective on-state drain-source resistance of the MOSFET to control the amount of current conducted, which allows the voltage across the capacitors connected in parallel to the power MOSFETs to generate a logistic shaped switching transition. The experimental and computational results demonstrate that a low-EMI half-bridge prototype

can produce logistic shaped switching transitions to verify the control system strategy and demonstrate EMI attenuation. The novel topology and approach improve research efforts provided in the literature by providing a shaped transition that is better suited for low-EMI applications and reducing output waveform quantisation and discontinuities.

Although there are notable improvements, there are still practical limitations that are identified and studied in this dissertation. The waveform modelling, circuit simulation, and prototyping have identified the precision required to achieve the steep spectral roll-off expected in the mathematical treatment of logistic-shaped switching transitions. The research has identified temporal characteristics of the logistic function that will provide the steep-roll off and what is required theoretically. However, practical limitations in the digital control circuity hinder the steep-roll off from being achieved. The shaped switching transitions still provide EMI mitigation, and the noise reduction is substantial compared to typical hard-switching power converter waveforms. The research outcomes provide a platform for continued investigation focusing on power converter design, including shaped switching transitions for high-frequency emissions attenuation.

# Acknowledgements

There are many people I would like to thank and acknowledge for their contributions to the research outcomes of this dissertation. Firstly, I would like to thank my supervisor Dr Adrian Sutinjo for providing vital guidance and facilitating my development throughout the research project.

The success of the research outcomes could not be made possible without the collaborative efforts of many involved. A collaboration agreement was formed in this dissertation between Curtin University and Balance Utility Solutions. The joint effort applies to developing a prototype novel half-bridge power converter capable of undergoing shaped switching transitions for low noise applications. I would like to thank Tom Booler, Rod Hayes, and Dr James Darbyshire for supporting the industry collaboration and making the prototyping project possible with industry-driven outcomes. Lastly, I want to thank Dr Lawrence Borle for your guidance throughout the prototype phase and for providing me with knowledge and insight into power converter design and implementation.

Furthermore, others have assisted with various technical aspects of the project. Firstly, I want to thank Professor Peter Hall for establishing my connection with Balance and playing a pivotal role during the early stages of the research project. Additionally, I want to thank Dr Budi Juswardy, Dr Franz Schlagenhaufer and David Kenney, who have been pivotal in expanding my knowledge and understanding of electromagnetic compatibility.

I would like to extend a massive thank you to my family Michael, Toni and Shaun Buchan, for their much-needed support over the years. Lastly, a huge thank you to my fiancé, Naomi Schlaepfer. Your love and support throughout this journey have been instrumental.

The research is supported by an Australian Government Research Training Program (RTP) Scholarship.

# Table of Contents

# Table of Figures

# Table of Tables

# Symbols

| Symbol | Description | Units |
|---|---|---|
| A | Waveform Amplitude | V |
| C | Capacitor | F |
| $C_b$ | Half-bridge bottom capacitor | F |
| $C_{ds}$ | drain-source capacitance | F |
| $C_{gd}$ | gate-drain capacitance | F |
| $C_{gs}$ | gate-source capacitance | F |
| $\|C_n\|$ | Harmonic amplitude | V or dB$\mu$V |
| $C_t$ | Half-bridge top capacitor | F |
| CF | Resolution bandwidth compensation factor | dB |
| d | Duty cycle | % |
| D | Diode | |
| $\Delta R$ | Spectral roll-off | dB/dec |
| $f_m$ | Modulation frequency | Hz |
| $f_c$ | Switching or carrier frequency | Hz |
| g | Gate-drive signal | |
| $g_{auxb}$ | Half-bridge bottom auxiliary MOSFET gate-drive signal | |
| $g_{auxt}$ | Half-bridge bottom auxiliary MOSFET gate-drive signal | |
| $g_b$ | Half-bridge bottom MOSFET gate-drive signal | |

( To be continued)

| Symbol | Description | Units |
|---|---|---|
| $g_{bi}$ | Half-bridge bottom injection MOSFET gate-drive signal | |
| $g_{fs}$ | MOSFET trans-conductance | ℧ |
| $g_t$ | Half-bridge top MOSFET gate-drive signal | |
| $g_{ti}$ | Half-bridge top injection MOSFET gate-drive signal | |
| $i_c$ | Capacitor current | A |
| $i_{Cb}$ | Half-bridge bottom capacitor current | A |
| $i_{Ct}$ | Half-bridge top capacitor current | A |
| $i_{ds}$ | drain-source current | A |
| $i_{gs}$ | gate-source current | A |
| $I_{aux}$ | Auxiliary current | A |
| $I_{DD}$ | Output current (constant) to model the load | V |
| $I_{load}$ | Load current | A |
| k | Logistic function growth rate | |
| L | Logistic function upper asymptote | |
| L | Inductor | H |
| $L_{aux}$ | Half-bridge auxiliary inductor | H |
| $L_d$ | Drain inductance | H |
| $L_g$ | Gate inductance | H |
| $L_s$ | Source inductance | H |
| $\lambda$ | Wavelength | m |
| n | Harmonic number | |
| $N$ | Ratio of carrier and modulation frequency | |
| $P_{tot}$ | EMI Metric | W or dBm |
| $Q_x$,$S_x$,$T_x$ | MOSFETs or IGBTs | |
| r | Separation distance | m |

( To be continued)

| Symbol | Description | Units |
|---|---|---|
| R | Resistor | Ω |
| $R_{ds(on)}$ | drain-source on resistance | Ω |
| $R_g$ | Gate resistor | Ω |
| t | time | s |
| $t_0$ | Time the logistic function is $A/2$ | s |
| $t_{di}$ | Randomised time delay of pulse i | s |
| T | Switching period | s |
| $T_{auxb}$ | Half-bridge bottom auxiliary MOSFET | |
| $T_{auxt}$ | Half-bridge bottom auxiliary MOSFET | |
| $T_b$ | Half-bridge bottom MOSFET | |
| $T_{bi}$ | Half-bridge bottom injection MOSFET | |
| $T_i$ | Switching period of pulse $i$ | s |
| $T_t$ | Half-bridge top MOSFET | |
| $T_{ti}$ | Half-bridge top injection MOSFET | |
| $\tau$ | Pulse-width | s |
| $\tau_f$ | Transition fall time | s |
| $\tau_{f'}$ or $\tau_{f(dv/dt)}$ | S-shaped derivative fall time | s |
| $\tau_i$ | Duration of pulse i | s |
| $\tau_r$ | Transition rise time | s |
| $\tau_{r'}$ or $\tau_{r(dv/dt)}$ | S-shaped derivative rise time | s |
| $\tau_t$ | Transition time | s |
| $v$ | Pulse v in a PWM waveform | |
| $V_{DD}$ | Input voltage (constant DC) | V |
| $v_g$ | Gate drive voltage | V |
| $v_{ds}$ | drain-source voltage | V |

( To be continued)

| Symbol | Description | Units |
|---|---|---|
| $V_{GH}$ | High gate voltage | V |
| $V_{GL}$ | Low gate voltage | V |
| $v_{gs}$ | gate-source voltage | V |
| $V_{th}$ | MOSFET threshold voltage | V |
| W | logistic function upper asymptote | |
| $\omega_0$ | Fundamental angular frequency | rad/s |

# Acronyms

| Acronyms | Definition |
|---|---|
| AVC | Active Voltage Control |
| AC | Alternating Current |
| ADC | Analogue to Digital Converters |
| CISPR | Comité International Spécial des Perturbations Radioélectriques |
| COTS | Commercial off the Shelf |
| CM | Common Mode |
| CMV | Common Mode Voltage |
| DUT | Device Under Test |
| DM | Differential Mode |
| DAC | Digital to Analogue Converters |
| DC | Direct Current |
| DFT | Discrete Fourier Transform |
| EIRP | Effective Isotropic Radiated Power |
| EMC | Electromagnetic Compatibility |
| EMI | Electromagnetic Interference |
| EoR | Epoch of Re-Ionisation |
| EUT | Equipment Under Test |
| FFT | Fast Fourier Transform |
| FPGA | Field-Programmable Gate Array |

( To be continued)

| Acronyms | Definition |
|---|---|
| ITU | International Telecommunications Union |
| LFAA | Low-Frequency Aperture Array |
| MOSFET | Metal-Oxide Semi-Conductor Field-Effect Transistor |
| $\mu$-processor | Microprocessor |
| MIL-STD | Military Standard |
| MRO | Murchison Radio-Astronomy Observatory |
| NPC | Neutral Point Clamped |
| PV | Photovoltaic |
| PaSD | Power and Signal Distribution |
| PSU | Power Supply Unit |
| PWM | Pulse Width Modulation |
| RPWM | Randomised Pulse Width Modulation |
| RBW | Resolution Bandwidth |
| SPWM | Sinusoidal Pulse Width Modulation |
| SKA-low | SKA Low-Frequency Aperture Array |
| SKA | Square Kilometre Array |
| SCADA | Supervisory Control and Data Acquisition |
| TPV | Transformer-less Photovoltaic |
| 2c | Two's Complement |
| ZCS | Zero-Current Switching |
| ZVS | Zero-Voltage Switching |

# Chapter 1

## Introduction

## 1.1 Introduction

The design of modern power electronic devices emphasises compliance with electromagnetic compatibility (EMC) standards for several reasons. One major contributing factor is that power electronics are beginning to operate at higher switching frequencies to achieve miniaturisation and increase the power density. Consequently, the high operational switching frequency generates considerable levels of electromagnetic interference (EMI), which increases the likelihood of failing to meet EMC standards. Although commercial standards such as CISPR [1] and MIL-STD-461F [2] place strict emission limits to ensure compliance, future radio astronomy applications, such as the Square Kilometre Array (SKA) radio telescope, have far more stringent EMC requirements [3], which stipulate the tolerable emission levels. Demonstrating compliance with the SKA EMC requirements ensures the performance of the radio telescope is not hindered [4, 5, 6].

With EMC standards becoming increasingly stringent, the need to further mitigate EMI in power electronic devices becomes a critical factor early in the design stage. Supplying and distributing power in radio astronomy applications such as the SKA project is no exception, with unprecedented sensitivity levels setting the EMC standard to ensure the radio telescope will operate free from unwanted EMI. The Murchison, in Western Australia, will be the host site of the SKA-low, where the environmental conditions and remote location make photovoltaic (PV) systems with battery energy storage a prospective power supply solution. Power electronic devices within PV-Battery systems and the power and signal distribution system of the SKA must be radio-quiet, and extensive research efforts focus on EMI mitigation techniques at either the power stage or control stage of the power converter.

The research project primarily targets power converter design and mitigating EMI at the source. Understanding how EMI is generated is a significant project driver, which seeks to understand the high-frequency behaviour of power converters. From a computational perspective, this dissertation extends on the shaped transition modelling presented in the literature and introduces a logistic shaped switching transition capable of producing steep spectral roll-off. Additionally, the temporal characteristics of the logistic function and shaped waveforms in general capable of producing steep spectral roll-off are identified. Furthermore, computer simulations and a prototype of a novel half-bridge power converter capable of producing logistic shaped switching transitions are presented. The novel topology and control strategy improves on techniques presented in the existing literature by reducing the quantisation and discontinuities present in the shaped waveforms, contributing to high-frequency spectral content. Additionally, the prototype extends the technology beyond implementation in a single semiconductor

device to a power converter using conventional Pulse Width Modulation (PWM) and operating under a constant load.

A primary objective of the research project is to mitigate high-frequency emissions generated by power converters between 50 MHz and 500 MHz, which encapsulates the SKA-low frequency range between 50 and 350 MHz. Power supply and distribution for the SKA-low require several design trade-off assessments between design requirements. Major project requirements include low antenna power levels distributed over a large site area, high energy availability, high efficiency, EMC compliance, 30-50 years project lifetime, increased system reliability and cost-effective solutions. All these major project requirements are not complementary, and a trade-off assessment will determine an optimised balance. The primary focus of this project is to provide power converter design recommendations and solutions considering the sensitive emissions requirements.

This research project presents computational studies and a prototype of a low-EMI half-bridge power converter that produces switching transitions capable of following a reference logistic function that targets high-frequency emissions attenuation. Compared to the EMI performance of trapezoidal, sinusoidal, and S-shaped transitions, the proposed logistic-shaped transitions presented in this project are expected, theoretically, to exhibit a steep roll-off in the spectral content, which is necessary for low-EMI outcomes. Conventionally used in population growth modelling [7], a logistic profile has been identified in this research project as a suitable candidate for low-EMI power converters. The temporal characteristics of the logistic function, such as the growth rate, can be selected for optimised EMI attenuation by maximising high-frequency spectral content roll-off.

A prototype half-bridge power converter capable of undergoing logistic shaped switching transitions is presented in this dissertation. The half-bridge prototype circuit consists of two n-channel power MOSFETs connected in series between a voltage source. Additionally, capacitors are placed in parallel with the MOSFETs since the inherent drain-source capacitance of the MOSFETs is insufficient to control the drain-source voltage. The proposed half-bridge utilises current injection circuitry to ensure a smooth transition in the MOSFET drain-source voltage during the second half of the transition. The injection circuits, consisting of a power supply and an added injection MOSFET, are connected in parallel to the added drain-source capacitance. Injected current is required to provide waveform shaping, which starts when the reference logistic profile reaches half the waveform amplitude. The injection circuit will divert current from the added drain-source capacitance, ensuring the voltage derivative of the MOSFET is identical to the voltage derivative of the reference logistic-shaped waveform. The combination of

the injection circuitry and parallel capacitors provides smooth shaped transitions that reduces signal quantisation.

An in-depth understanding of MOSFET transients during changes in the MOSFET gate-drive is required to understand the gate-drive initialisation, control command sequencing, and gate-drive profiles necessary to provide smooth low-EMI switching transitions. As such, the proposed control strategy can control the output voltage of a MOSFET to follow a logistic-shaped reference profile. Understanding the conditions that cause a MOSFET to operate within the cut-off, saturation, and ohmic regions and the expected transient response times of the MOSFET to applied gate voltages within the regions is crucial to the successful shaped switching control. The MOSFET operational regions assist with initialising the control, whereas the expectation of the transient response time determines when to apply the gate-drive signals.

The novel control system of the prototype system achieves waveform shaping by controlling the gate-drive of the MOSFET for the first half of the transition, combined with a current injection circuit to control the second half of the transition. The current injection is activated by a second MOSFET, allowing the same control strategy to be applied to both the power MOSFET and the current injection circuitry. Careful consideration of the timing of the gate-drive control and current injection allows for the switching transition of the prototype to follow a logistic-shaped reference.

This research project has demonstrated that power converters can undergo logistic-shaped switching transitions for applications where high-frequency electromagnetic disturbances are undesirable. Additionally, this is the first time the technology has been implemented using current injection technology. Furthermore, this novel technology has been prototyped using a half-bridge power converter, which has been designed and tested to operate under no-load and constant load conditions using a conventional Pulse Width Modulation (PWM) switching scheme. The improved novel control strategy combined with a half-bridge power circuit topology extends the capability of the shaped switching transition technology beyond a single semi-conductor switch, and it confirms the suitability of the technology for low-EMI power converter applications.

The critical considerations for a successful design approaching the theoretical spectral roll-off of a logistic transition are the parallel capacitors, injection circuitry and gate-drive control of the power MOSFETS and injection circuitry MOSFETS. The immediate application for low-EMI power converters is radio astronomy, and more specifically, the SKA-Low. However, low-EMI power systems are required more broadly in any radio-sensitive application where EMC non-compliance risks the safe, reliable, and

efficient operation of electrical and electronic systems. As such, applications can extend to military, communications, and medicine where strict EMC standards apply. Demonstrating that a power converter can be designed with controlled, shaped switching transitions is favourable for the SKA-low and other applications where stringent EMC standards are specified. The research project has produced the following key outcomes:

- **Identification of optimised shaped switching transitions for low-EMI applications:** Computational modelling and circuitry simulation has developed an understanding of the temporal characteristics of switching transitions, which has identified logistic-shaped transitions to be suitable for EMI attenuation. Furthermore, careful definition of the logistic reference profile removes signal discontinuities observed in the literature. Additionally, the circuit simulations have developed the control strategy required to ensure the prototype circuit will produce low-EMI switching waveforms.
- **Prototype development of a low-EMI power converter with a control strategy to shape switching transitions:** By developing a control strategy for logistic-shaped transitions, EMI is reduced at the source. Prototyping a low-EMI half-bridge has demonstrated the waveform shaping technology within power converters is possible. Additionally, the novel inclusion of the current injection circuitry and parallel capacitors reduces signal quantisation observed in the literature, which is a significant practical limitation in EMI attenuation for shaped transitions.
- **Analytical Fourier series for power converter PWM:** A set of Fourier series for power converter PWM switching undergoing shaped transitions has been derived. The set of Fourier series provides the analytical spectral content of both a DC-DC converter and a DC-AC converter considering both conventional PWM and randomised PWM. The derivations were verified by comparing the spectral content of a time-domain waveform using a discrete Fourier transform (DFT).
- **Power design for radio astronomy applications**: Crucially, the design strategy and prototype design and implementation presented in this dissertation help identify and bridge the gap between power converter design and stringent EMI requirements for radio astronomy applications.

This introductory chapter provides background context and justification for this research project. Initially, the project background of the SKA, mainly the SKA-low, with particular relevance to the power supply requirements and associated technological challenges in the context of EMC, is covered. Additionally, a chapter by chapter

breakdown of the thesis, and outline of the intellectual contributions are presented. Furthermore, the anticipated emission limits of the SKA-low are presented to provide context regards the stringency of the SKA-low EMC standard.

## 1.2 Thesis Structure

There are 6 chapters covering the research topics addressed in this dissertation.

Chapter 1 is the introductory thesis chapter, which justifies undertaking the research objectives and presents relevant background information. This chapter commences with the project introduction and intellectual contributions. Subsequently, the chapter introduces the research project, which is primarily motivated by the technological challenges faced by the SKA-low. The introductory chapter provides a project summary of the SKA-low and presents relevant background information, which provides context and a framework for the research presented in this dissertation.

Chapter 2 presents a literature review of EMI mitigation techniques in power electronic devices, considering radio astronomy applications. Firstly, the chapter summarises conventional EMC design techniques for power converters. Following this, a comprehensive review of EMI mitigation techniques applied to the power circuitry and control circuitry is presented. A review of EMI mitigation techniques in power converters considering radio-astronomy applications is presented. The chapter concludes with a design methodology for low-EMI power converters considering shaped switching transitions. The design methodology offers a systematic approach for developing low-noise power converter technologies for the SKA-low based on advancing and improving current research presented in the literature. The literature review identifies the intellectual contributions of previous studies, which is the research framework for this dissertation.

Chapter 3 presents a comprehensive numerical assessment of the spectral content of switching transitions in power electronic devices. The analytical Fourier series of hard switching waveforms for DC-DC converters is presented, providing a point of comparison for low-EMI shaped transitions, addressed in the remainder of the chapter. Initially, a summary of analytical spectral modelling in various literature sources is provided. Following this, an analytical derivation of trapezoidal, S-shaped, sinusoidal and logistic switching transitions is presented, which can be assessed for EMI mitigation. In addition to S-shaped switching transitions, infinitely differentiable switching transitions are identified as being best suited for EMI mitigation. Sinusoidal and logistic shaped switching transitions are studied in this chapter, and how their temporal characteris-

tics are critical for EMI mitigation. All the shaped transitions are numerically assessed using an EMI metric, spectral bounds and spectral roll-off to determine the EMI performance of each shaped switching transition.

How shaped switching transitions are accomplished in a half-bridge power converter is presented in Chapter 4. Firstly, a summary of the conventional hard-switching PWM half-bridge is presented to provide a basis for comparison to the half-bridged shaped transition prototype. The overview includes the device structure and physical operation of a MOSFET, which provides the fundamentals for the current-voltage characteristic and the modes of operation. Subsequently, the transient response of MOSFET during turn off is presented. Next, an overview of the prototype half-bridge circuit is presented alongside a simplified circuit, which explains the critical operational concepts without the detailed control considerations. Subsequently, a detailed breakdown of all the low-EMI half-bridge modes of operation and the essential control aspects for low-EMI applications is presented. Lastly, the chapter concludes with circuity simulations of shaped MOSFET switching transitions with the inclusion of MOSFET switching transients and parasitic components through the utilisation of component SPICE models. The MOSFET switching transients allow the circuit components to be modelled in the switching waveform transitions, consolidating the mathematical treatment of shaped switching transitions with a half-bridge power converter.

Chapter 5 presents the low-EMI prototype design and implementation. Initially, the detailed design of the half-bridge power circuit is presented. Next, the half-bridge control system implementation is presented, which explains the detail of the shaped waveform control strategy. An overview of the error detection and feedback control for the gate-drive is presented for the power and injection MOSFET control. Lastly, the chapter concludes with a section covering the laboratory assessment and performance verification. A measurement set-up and methodology is presented, followed by all laboratory measurements of the half-bridge low-EMI prototype producing an S-shaped, sinusoidal-shaped and logistic-shaped waveform for comparison. The hard-switching waveforms are also measured and included in the comparison. Additionally, a spectral comparison of all the generated shaped waveforms and hard-switching waveforms is presented.

Chapter 6 presents the prototype improvements and continued research works based on the outcomes of the prototype development. Firstly, all prototype improvements and ongoing research topics are presented, including improved circuitry efficiency, automated control of the auxiliary branch, improved control architecture, identifying the maximum switching frequency, and shortest transitions time achievable with the shaped

transitions technology. The chapter also presents continued modelling, including computational spectral content modelling for DC-AC inverters and randomised PWM with logistic shaped transitions for DC-DC converters and DC-AC inverters. Lastly, the discussion and conclusion sections for the thesis is presented.

## 1.3 Intellectual Contributions

The intellectual contributions of this research project are identified in this section. A high-level description of the intellectual contributions are itemized as follows:

- Identification of optimised shaped switching transitions for low-EMI applications, which include logistic-shaped switching transitions.
- EMI modelling of shaped switching transitions of DC-DC converters for a detailed comparison of EMI mitigation.
- Analytical Fourier series derivations of a generic shaped transition function for both DC-DC converter and DC-AC inverter PWM and randomised PWM.
- Modelling, designing and prototyping of a novel low EMI half-bridge power converter with a control strategy to produce shaped switching transitions.
- The development of EMI design strategies for low-EMI power converters considering radio astronomy applications.

The modelling, designing and prototyping of low-EMI power converters capable of producing shaped switching transitions lends itself to numerous intellectual contributions. Detailed computational modelling of shaped transitions and circuit simulations of a low-EMI half-bridge power converter provides the generation mechanisms of EMI, in particular how the temporal characteristics of switch transitions can influence high-frequency EMI. Understanding the switching nature of semiconductor switches and the time-domain properties that affect high-frequency EMI mitigation is sought through an analytically derived Fourier series. A more in-depth understanding is obtained by developing computational modelling of S-shaped, sinusoidal-shaped and logistic-shaped switching transitions and the associated harmonic content.

The consolidation of MOSFET switching transient models with the numerical shaped transitions provides practical design aspects of the half-bridge prototype design for EMI attenuation. Identifying the operational regions of the MOSFETs and the key parasitic components that dominate the transient response of a MOSFET are key constituents in defining the expected transient response times when the gate-drive of a MOSFET

is being controlled. Understanding the operational regions is pivotal for initialising the control, where the anticipated transient response times based on major parasitic components determine when to apply the gate-drive signals.

Furthermore, the research project has developed EMI attenuation strategies intended for radio astronomy applications. The levels of sensitivity and the operational frequency band of the telescope (50 – 350 MHz) create technical challenges that are not conventionally addressed by power converter design and power converter EMI mitigation. The significance and innovation of this research project stem from the development of a low-EMI half-bridge power converter with a novel shaped switching transitions control strategy. Additionally, the prototype outcomes present new insights for achieving shaped switching transitions in power converters, which has the potential for steep spectral content roll-off and, therefore, high-frequency EMI mitigation. The prototype efforts provide valuable background information for SKA-low design engineers and engineers facing similar technical challenges in other fields. Therefore, this research project provides a comprehensive theoretical and practical understanding of mitigating EMI at the source of emissions generated by power converters. Crucially, the design strategy presented helps identify and bridge the gap between power converter design and stringent EMI requirements for radio astronomy applications.

## 1.4 List of Publications

A collaboration agreement was formed as part of this dissertation between Curtin University and Balance Utility Solutions. A licence agreements between both parties has been executed and the research outcomes of this dissertation contain patentable concepts. Therefore, journal articles have not been published since the intellectual property will be released into the public domain. However, journal articles have been drafted, which will be published once the license agreement permits. An overview of the two drafted articles is presented as follows:

**Journal Article 1:** Electromagnetic Interference Mitigation in Power Electronic Devices and Considerations for Radio Astronomy

- This manuscript presents a review of EMI mitigation techniques in power converters considering radio-astronomy applications, followed by a design methodology for low-EMI power converters considering shaped switching transitions. The design methodology presents a systematic approach for developing low-noise power converter technologies for the SKA-low. While this article presents a high-level design approach for low-EMI power converters, the methodology synthesises known strategies with new insights for achieving shaped switching transitions, provid-

ing valuable background information for SKA-low design engineers and engineers facing similar technical challenges in other fields.

**Journal Article 2:** Reducing Electromagnetic Interference in Half-Bridge DC-DC Converters for Radio Astronomy Applications

- This manuscript presents a computational study and prototype of a low-EMI half-bridge capable of undergoing logistic-shaped switching transitions to achieve high-frequency EMI mitigation. Compared to the EMI performance of trapezoidal, sinusoidal and S-shaped transitions, the proposed logistic-shaped transitions provide steep roll-off, necessary for low-EMI outcomes. Both computational and laboratory results demonstrate that the proposed half-bridge circuit with logistic shaped transitions achieves EMI attenuation.

## 1.5 Providing Power to the Square Kilometre Array

The SKA will be the world's largest and most sensitive radio telescope, with the technology and capability to make discoveries in many areas of radio astronomy [4]. The SKA project will revolutionise radio telescope technology and deepen humanity's understanding of the Universe. Developing a state of the art radio astronomy facility will ensure the SKA plays a significant role in the progression and advancement of critical areas of astrophysics and cosmology. The capabilities of the SKA allows for a large number of many important and new astrophysical observations to be made. The primary scientific drivers of the SKA include the cradle of life, pulsar and black hole surveys, cosmic magnetism, galaxy evolution and cosmology, Epoch of Re-Ionisation (EoR), the dark ages, and will have the capabilities to explore the unknown and make new scientific discoveries [4, 8, 9, 10, 11].

The host site of the SKA Low-Frequency Aperture Array (SKA-low) is the Murchison Radio-Astronomy Observatory (MRO) in Western Australia is shown in Figure 1.1, which provides a radio-quiet location free from artificial electromagnetic disturbances. The radio telescope will operate between 50 MHz and 350 MHz and comprise approximately 128,000 radio antennas during Phase 1 of construction. Power supply considerations based on EMI impact will be limited by the availability and cost of the technology required [12, 13], which is necessary to ensure the radio antennas do not become susceptible to generated EMI. Furthermore, the remote location and environmental conditions of the Murchison make renewable energy systems a prospective power supply solution for the SKA-low. DC-DC converters and DC-AC inverters are major power conversion constituents of renewable energy systems and must not generate undesirable electromagnetic disturbances. Furthermore, EMC compliant power converters are required to provide power at suitable voltages to the radio-antennas.

Power supplies will be installed as close as 1 m to the nearest antenna, which requires a comprehensive understanding of EMI generation mechanisms within power converters.

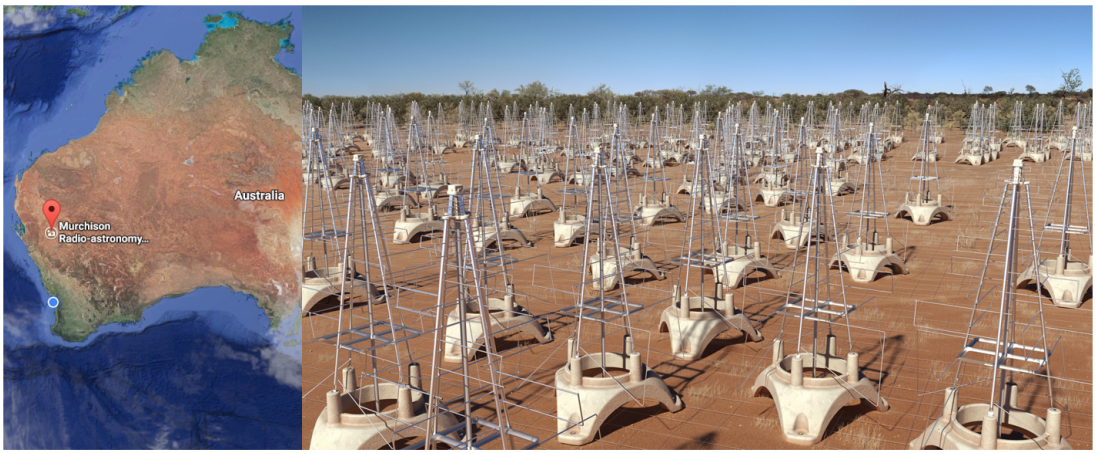



Figure 1.1: Geogrpahical location of the SKA-low site at the MRO.

The majority of the collecting area of the SKA-low will be situated within a dense core approximately 5 km wide. However, the entire array will span a much more extensive region. SKA-low Phase 1 will extend roughly 100 km in width, whereas Phase 2 is anticipated to extend as far as ∼3000 km considering the furthest baselines [11]. A representation of the SKA-low layout is depicted in Figure 1.2, where a single dot represents 256 antennas, referred to as a Field Node. The core of the SKA-low consists of a dense array of antennas approximately 3 km in diameter, connected to sparse antenna spiral arms extending up to 50 km from the centre of the core. The sparsity of the spiral arms increases proportionally with distance from the core, making Field Nodes become increasingly more remote the further they are from the centre.

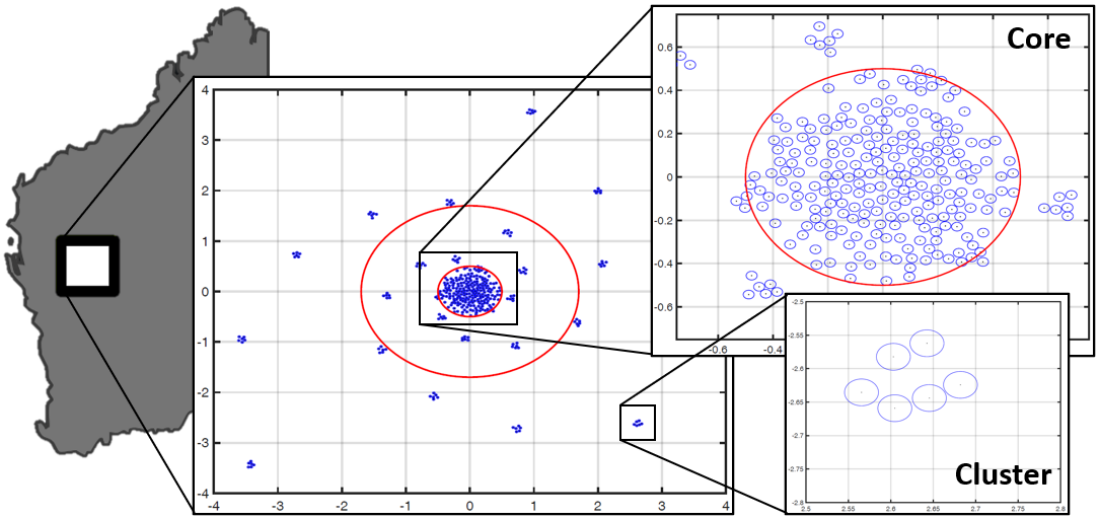



Figure 1.2: SKA-Low Radio Telescope topology.

The power supply considerations for the SKA-low faces numerous technical challenges, requiring the power system design to meet stringent EMC, availability and reliability requirements. Low EMI systems are vital in radio-astronomy applications, where radio-antennas cannot become susceptible to electromagnetic noise, which impacts the performance of the antennas trying to detect faint radio signals in the distant Universe. The main power supply requirements that are pivotal to the success of the SKA-low are:

- Identify a cost-effective power supply and distribution solution [14].
- Supply low voltage power to the antennas over the large SKA-low site area [14].
- Maintaining high energy availability above 99.5% [15, 16].
- SKA-low reliability and maintainability requirements [15, 16].
- Generating low levels of EMI that the radio antennas cannot detect [3].
- Adherence to the SKA-low power quality standards [17].
- Ensuring the power generation and distribution solution operates over the entire 50-year project lifetime [14].

A detailed trade-off assessment of the above-listed requirements will provide the optimised outcome since not all requirements complement each other. For example, meeting EMI and energy availability requirements can be achieved with additional system costs. PV arrays with energy storage have been identified as a possible power supply solution for the SKA-low remote Field Nodes along the spiral arms of the radio telescope.

The remote location of the MRO is not dissimilar from rural or remote settlements, making PV technologies viable candidates for a stand-alone solar power supply. PV panels need to be characterised considering the radiated emissions generated by solar modules to become a feasible power supply for the SKA-low. Although it is not a research objective for this project, PV panels are known to exhibit antenna characteristics [18, 19, 20, 21, 22, 23, 24, 25, 26, 27]. Furthermore, the power supply and distribution solution include rectifiers and DC-DC converters that are required to convert power to suitable voltage levels needed to power all the radio antennas. All power converters must be carefully designed to mitigate EMI since the high-frequency semiconductor switching components generate electromagnetic noise.

The SKA is currently in the precursor prototyping phase and the system-level design, focusing on solar power generation and the power and signal distribution (PaSD) to the antennas. The solar power generation investigation considers a stand-alone PV system with battery energy storage and AC distribution to the point of connection to the PaSD system for a single Field Node. An overview of the power system topology is shown in Figure 1.3. The system topology identifies where power conversion is required throughout the PV battery and PaSD system with indicative voltage levels and distance to the nearest antenna.

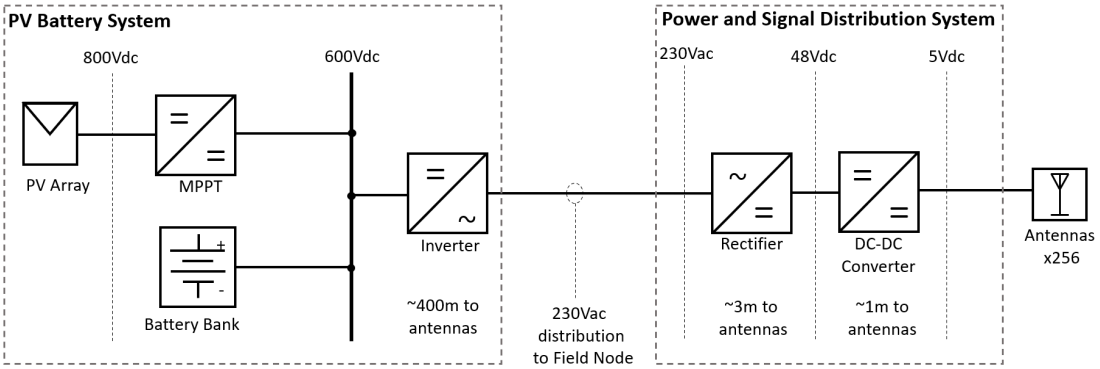



Figure 1.3: PV-Battery system and PaSD overview.

Prototyping and testing of the PV system rely on EMI filtering and shielding technologies, both having cost implications. Similarly, the PaSD prototyping efforts explored the feasibility of a commercial off the shelf (COTS) power supply, combined with a custom-designed supervisory control and data acquisition (SCADA) system capable of monitoring and controlling groups of eight antennas. The prototyping efforts for the PV battery system and PaSD system showcase the numerous trade-off assessments made with each prototype. The EMI design and control methodologies within the PaSD and PV battery systems consider technological and cost challenges associated with EMI

attenuation. Therefore, extensive EMI mitigation and characterisation are the critical research areas of this project and are further discussed in the remainder of this thesis.

## 1.6 SKA-Low Electromagnetic Compatibility Standards

### 1.6.1 Electromagnetic Interference

This section presents an overview of EMI generated by electrical and electronic devices, particularly power converters. EMI is the adverse effect of noisy circuitry on nearby electronic components, and modern electronic design emphasises mitigating EMI due to the proliferation of noisy and sensitive electronic equipment and increasing demand for reliable electronic systems. Additionally, circuitry design should ensure minimal electrical noise contribution and immunity to the surrounding electromagnetic environment, which is known as EMC and is a crucial design objective for the SKA-low. An electronic device satisfies EMC requirements if it does not cause interference to other systems, is immune to emissions generated by other systems, and does not interfere with itself.

Emissions are defined as conductive or radiative signals. Conventionally, conducted and radiated emissions are categorised by frequency bands where conducted emissions are usually generated between 10 kHz and 30 MHz and radiated emissions are generated beyond 30 MHz. Furthermore, conducted emissions are classed as either differential-mode (DM) or common-mode (CM) emissions. DM emissions conduct through a power converter through interconnecting leads connected to the source or load in the power converters. CM emissions flow in the same direction into and out of a power supply, returning to the source through a common ground. Radiated emissions are generated by the interconnecting leads and power converter circuitry, which act as transmitting antennas. The radiated emissions generated by power converters are created by the switching frequency, and the electrical length of the radiating element in the circuit, loop area created by any conducting paths, and the operating circuit voltages. The electrical length of the conducting path and the loop area can be minimised to mitigate radiated emissions generated by power converters. Considering the control of power converters, switching schemes and control strategies can be developed to mitigate emissions at the source of noise, which is the focal point for this dissertation.

### 1.6.2 Unprecedented levels of Sensitivity: SKA-Low EMC Requirements

All electrical and electronic equipment must meet stringent EMC requirements to be deployed on-site for the SKA-low. Mitigating EMI is crucial to the success of the SKA and will strongly influence the design of electrical equipment to prevent the SKA

radio telescope making false detections. Currently, the SKA-low EMC compliance requirements are not comprehensive and lack clarity regarding verifiable and repeatable test methods that will demonstrate that the emissions generated by a device under test (DUT) comply with the emission limits. The SKA-low EMC standards are established to set the threshold limit values where the required sensitivity performance is maintained to ensure no EMI will disrupt the performance of the telescope. The SKA-low EMC standard adopts the ITU-R.769.2 International Telecommunications Union (ITU) Recommendation [28] to determine the emission protection levels for the radio telescope, based on the interference power that would cause errors in the signals expected to be detected by the SKA-low. The emission protection levels limits are also expressed as an equivalent electric field strength since EMC test facilities are calibrated to either commercial or military EMC standards to detect emissions as electric fields.

The SKA-low EMC standard adopts the CISPR 22 class B [1] and MIL-STD-461F [2] standard test procedures and limit values, which provide accepted test methods. The adopted EMC standard procedures are not entirely sufficient as the measurement resolution bandwidths (RBW) and measurement distances specified in the EMC standard differ from the SKA-low EMC standard. Therefore, conversion factors account for differences in the RBWs and measurement distances. The SKA-low EMC limits are 80-100 dB less than MIL-STD-461F RE102 emission limits at a 1 m distance to the nearest antenna, presenting a worst-case. The level of sensitivity is below the noise floor of EMC test facilities, which makes testing and verification per the SKA-low EMC standard difficult. It is expected that multiple stages of shielding and filtering are required, which will add size and cost to the system design. In addition to quantifying shielding effectiveness, other power converter EMI mitigation techniques should be similarly assessed.

Developing novel test methods and new technologies to satisfy the SKA-low EMC requirements should also be considered. The frequency range of the SKA-low provides an onerous challenge for power converters since the switching behaviour of power converters generates broadband emissions caused by switching harmonics, which can span the entire frequency range of the SKA-low. If considerations are not made to the design of the power electronic devices, there will be difficulties adhering to the stringent SKA-low EMC standards. Conventional solutions such as lowering the switching frequency and increasing switching transition times reduce EMI but can have detrimental effects on converter efficiency, size and cost.

### 1.6.3 Proposed SKA-low EMC Standards

For the telescope to perform a specific measurement, it is calibrated to a particular measurement bandwidth and sweep time. These measurements are categorised as a

narrow band or broadband measurement and set a sensitivity requirement, which are determined based on the most sensitive measurement at each frequency. This section provides a numerical assessment of the proposed SKA-low EMC requirements and represents the limit values as an electric field strength compared to the MIL-STD-461F RE102 limit lines and measurement procedure. Major power supply components for antennas will generate EMI within proximity to the radio receivers. Therefore, identified sources of EMI are assessed assuming a 1 m distance from the antennas. For devices such as PV-battery systems, correction factors for 100 m, and 400 m distances can be applied to consider the adjusted emission limits for installations at a greater distance from the nearest antenna. As specified in the SKA-low EMC requirements [3], the PSD of broadband signals using a bandwidth of 1% of the central frequency, and the PSD of narrow band signals using a 0.001% of the centre frequency is shown in Figure 1.4.

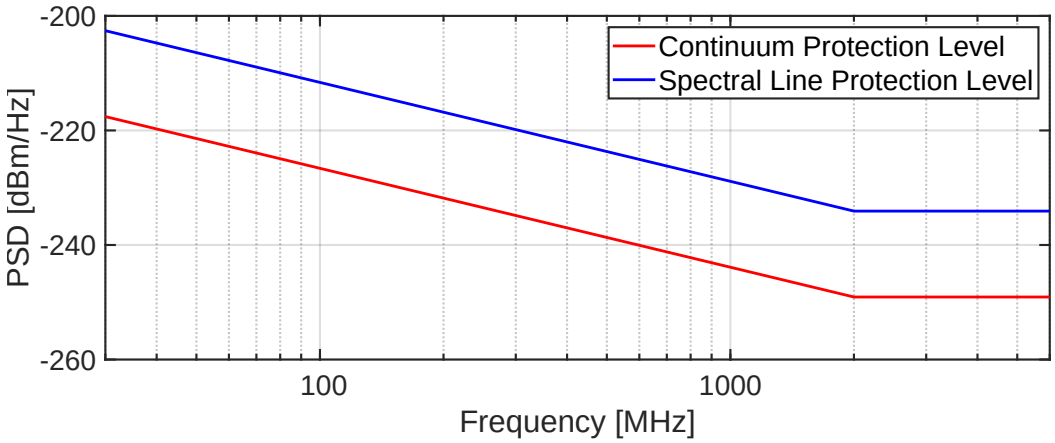



Figure 1.4: SKA-Low continuum and spectral line PSD protection levels.

The threshold level of a radiating device at a distance $r$ to the nearest antenna is defined as the maximum effective isotropic radiated power (EIRP) at the RBW set by the central frequency. The EIRP assumes the emissions are detected by the antenna through a 0 dBi side-lobe gain, given by:

$$\mathrm{EIRP} = \mathrm{PSD} + \log_{10}(\mathrm{RBW}) + 10\log_{10}\left(\frac{\lambda}{4\pi r}\right)^2 \tag{1.1}$$

Where the last term in the equation is the free space path loss, $r$ is the distance between the emissions culprit and receiving antenna, and $\lambda$ is the wavelength of the transmitted signal. The following equation calculates the electric field strength limit at a distance, $d$, between the emission culprit and the measuring antenna:

$$E_{dB\mu V/m} = \text{EIRP} - 20\log_{10}(d) + 104.8 \tag{1.2}$$

Lastly, when the RBW of the receiver, $\text{RBW}_{\text{ref}}$, is greater than the RBW of the transmitted signal, $\text{RBW}_{\text{act}}$, a compensation factor is applied, which is given as:

$$\text{CF} = 10\log_{10}\left(\frac{\text{RBW}_{\text{ref}}}{\text{RBW}_{\text{act}}}\right) \tag{1.3}$$

When the detected emissions are narrowband, the RBW of the receiver is narrower than the transmitted signal, and a correction factor is not required. One emission limit is considered for simplicity, which is the minimum permitted transmitted power from either the broadband or narrowband signals at each frequency. The correction factors that are applied to compare the SKA limits to MIL-STD-461F is shown in Fig. 1.5. Since the SKA-low emission limits are defined considering the distance between the EMI culprit and the nearest antenna, the worst-case SKA-low electric field strength limit values at 1 m are shown and compared MIL-STD-461F RE102 limit less 80 dB to demonstrate the stringent emission limits defined by the SKA-low EMC standard. The approach for EMC compliance is cumbersome since multiple stages of shielding and filtering are required, adding size and cost to the system design, which advocates for novel power converter EMI mitigation techniques to be considered.

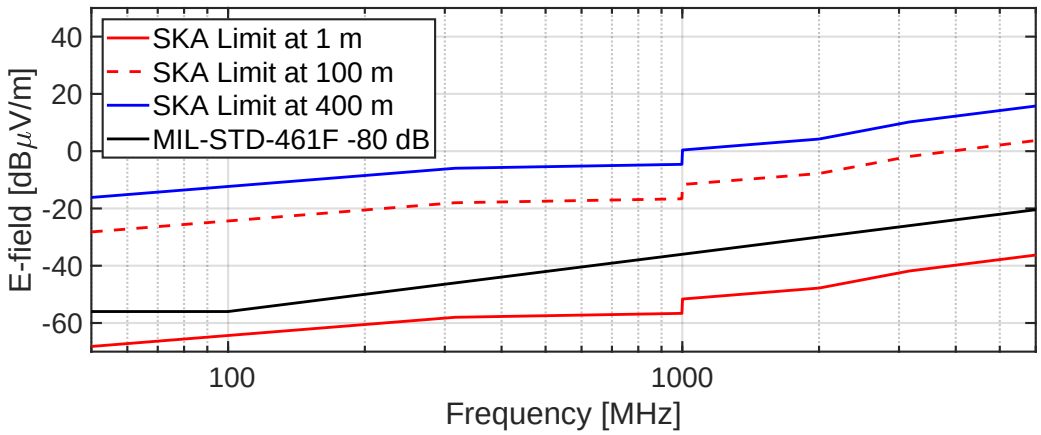



Figure 1.5: SKA-Low EMC emission limits considering a 1 m, 100 m and 400 m distance from the nearest antenna. The MIL-STD-461F RE102 limit less 80 dB is included for comparison.

## 1.7 Power Converter EMI Mitigation

The proposed SKA-low EMC limit values presented in Figure 1.5 outline the stringent sensitivity levels required to maintain the sensitivity of the radio telescope. The emission limits advocate for power converter EMI mitigation techniques that provide emissions attenuation beyond 50 MHz. The semiconductor switches within power converters generate considerable levels of conducted and radiated EMI due to the high-frequency content of the rapidly changing voltage and current waveforms. The sharp edges on the switching waveforms generate high $dv/dt$ and $di/dt$ and, when analysed in the frequency domain, show the harmonics that contribute to the conducted and radiated emissions generated. Understanding the generation mechanisms of EMI is an essential aspect of this project since it will provide a fast and accurate prediction tool. There is no universal approach to predict the EMI in power converters since an accurate description of the propagation path is complex and challenging. Focusing on the source of the generated EMI has merits since reducing electromagnetic disturbances at the source will reduce the EMI regardless of the propagation path.

The switching scheme significantly contributes to the conducted EMI, which can be exacerbated by the frequency-dependent parasitic components that resonate. In typical EMI studies of power converters, the frequency range of interest does not often extend past 10 MHz. In standard applications, the EMI issues with power converters can be constrained to a conducted emissions problem, where the frequency range of interest is below 30 MHz. Additionally, although power converters beyond 30 MHz generate detectable radiated emissions, there often is not a desire for novel technologies to be developed to achieve compliance as only a small amount of attenuation is required, if any, to meet commercial EMC standards such as CISPR. However, in the context of the SKA-low EMI requirements, these emissions are a significant issue that must be addressed for the telescope to operate as intended.

Novel methods must be applied in conjunction with traditional methods such as filtering and shielding to achieve significant EMI mitigation within power converters. Novel techniques to mitigate EMI generated by power converters include topology design [29, 30], randomised or spread spectrum switching [31], soft-switching [32] and shaped pulse transitions [33]. These techniques reduce EMI and, therefore, the dependency on filtering and shielding, reducing the size and cost of the COTS EMC solutions required to meet the SKA-low EMC standard. Generated noise can be suppressed if the switching transitions times of the semiconductor switches within the power converters are increased [34]. However, this is detrimental to the power converter efficiency, and low EMI should be ascertained without considerable losses. Shaped transitions achieve low-

EMI by mitigating high-frequency harmonics without increasing the transition times of the switching waveform. Therefore, switching losses are reduced compared to slowed switching transitions that are implemented to mitigate EMI. The following chapter presents a comprehensive review of EMI mitigation techniques, particularly methods that are suitable for radio astronomy applications.

## 1.8 References

[1] *Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement*, Standards Australia / Standards New Zealand Std. AZ/NZS CISPR 22:2009, 2009.

[2] *Department of Defence Interface Standard: Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment*, Department of Defense Std. MIL-STD-461F, 2007.

[3] *SKA RFI/EMC Standard*, Square Kilometre Array Organisation Std. SKA-TEL-SKO-0 000 202, 2021.

[4] P. E. Dewdney, P. J. Hall, R. T. Schilizzi, and T. J. L. W. Lazio, "The Square Kilometre Array," *Proc. IEEE*, vol. 97, no. 8, pp. 1482–1496, 2009.

[5] C. Jackson, A. R. Forsyth, L. Li, M. J. Kesteven, and S. Mickle, "Emc considerations for the askap dish antennas," in *Proc Asia-Pacific Symp. Electromagn. Compat.*, 2013, pp. 1–4.

[6] R. Millenaar, "Considerations for the optimal radio astronomy site featuring the Square Kilometre Array as an example," in *AFRICON, 2013*, 2013, pp. 1–5.

[7] P. S. Meyer and J. H. Ausubel, "Carrying capacity: A model with logistically varying limits," *Technological Forecasting and Social Change*, vol. 61, no. 3, pp. 209 – 214, 1999.

[8] D. L. Jones, "Technology challenges for the Square Kilometre Array," *IEEE Aerosp. Electron. Syst. Mag.*, vol. 28, no. 2, pp. 18–23, 2013.

[9] Carilli, C. L. and Rawlings, S., "Science with the Square Kilometre Array: Motivation, Key Science Projects, Standards and Assumptions," *New Astronomy Reviews*, vol. 48, p. 979–984, 2004.

[10] Carilli, C. L., "Square Kilometre Array Key Science: a Progressive Retrospective," in *Proc. Sci.*, 2014.

[11] Schilizzi, R. T., Alexander, P., Cordes, J. M, Dewdney, P. E., Ekers, R. D., Faulkner, A. J., Gaensler, B. M., Hall, P. J., Jonas, J. L., and Kellermann, K. I., "Preliminary Specifications for the Square Kilometre Array," in *SKA Memo*, 2007.

[12] P. J. Hall, "Power considerations for the Square Kilometre Array (SKA) radio telescope," in *General Assembly and Scientific Symp.*, 2011, pp. 1–4.

[13] A. V. Ardenne, A. J. Faulkner, and J. G. D. Vaate, *The Square Kilometre Array: Paving the way for the new 21st century radio astronomy paradigm*, ser. Astrophysics and Space Science Proceedings. Berlin, Heidelberg: Springer Berlin Heidelberg, 2012. [Online]. Available: http://link.springer.com/10.1007/978-3-642-22795-0

[14] *Power and Signal Distribution (PaSD) Requirements Specification*, Square Kilometre Array Organisation Std. SKA-TEL-SKO-0 001 073, 2021.

[15] *Reliability Availability and Maintainability Predictions*, Square Kilometre Array Organisation Std. SKA-TEL-LFAA-0 200 008, 2015.

[16] *SKA RAM Allocation*, Square Kilometre Array Organisation Std. SKA-TEL-SKO-0 000 102, 2016.

[17] *SKA1 Power Quality Standard*, Square Kilometre Array Organisation Std.

[18] N. Henze and T. Degner, "Radio interference of photovoltaic power systems," in *16th Int. Symp. and Exhibition on EMC,*, 2002, pp. 1–6.

[19] M. Tomisawa and M. Tokuda, "Induction characteristics of a solar cell to radiated electromagnetic disturbances," in *19th Int. Symp. Electromagnetic Compatibility*, 2008, pp. 538–541.

[20] T. Wada, T. Mori, M. Tokuda, S. Suenaga, and H. Igarashi, "Radiated electromagnetic field from a solar cell for CISPR radiated emission measurement method," in *Int. Symp. Electromagnetic Compatibility*, vol. 1, 2005, pp. 112–117.

[21] M. Tomisawa and M. Tokuda, "Induction characteristics of a solar cell on the ground plane from radiated electromagnetic disturbances," in *20th Int. Symp. Electromagnetic Compatibility*, 2009, pp. 81–84.

[22] G. Andrieu, A. Reineix, and J. Panh, "A numerical methodology for the prediction of the near-field parasitic electromagnetic emissions of solar panels," *IEEE Trans. Electromagn. Compat.*, vol. 51, no. 4, pp. 919–927, 2009.

[23] G. Andrieu, J. Panh, A. Reineix, P. Pelissou, P. Delannoy, C. Girard, X. Romeuf, and D. Schmitt, "Improvements of a numerical methodology for computing near-field parasitic electromagnetic emissions of solar panels," *IEEE Trans. Electromagn. Compat.*, vol. 56, pp. 792–799, Aug 2014.

[24] B. Juswardy, F. Schlagenhaufer, S. Padhi, and P. Hall, "Radiated EMI emission study on photovoltaic module for radio astronomy receiver front-end," in *Electromagnetic Compatibility Symp.*, Nov 2011, pp. 1–4.

[25] M. C. Di Piazza, C. Seaport, G. Tine, and G. Vitale, "Electromagnetic compatibility characterisation of the DC side in a low power photovoltaic plant," in *IEEE Int. Conf. on Industrial Technology.*, vol. 2, 2004, pp. 672–677.

[26] I. Wu, T. Shinozuka, and S. Ishigami, "Evaluation of electromagnetic radiation from the dc side of photovoltaic power generation system," *IEEE Electromagn. Compat. Mag.*, pp. 73–81, 2015.

[27] G. Chen, Y. Deng, Y. Tao, X. He, Y. Wang, and Y. Hu, "Topology derivation and generalized analysis of zero-voltage-switching synchronous dc converters with coupled inductors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4805–4815, Aug 2016.

[28] *Protection Criteria Used for Radio Astronomical Measurements*, International Telecommunication Union Std. RA.769-2, 2003.

[29] D. Dong, F. Luo, D. Boroyevich, and P. Mattavelli, "Leakage current reduction in a single-phase bidirectional AC-DC full-bridge inverter," *IEEE Trans. Power Electron.*, vol. 27, pp. 4281–4291, 2012.

[30] J. W. Shin, H. Shin, G. S. Seo, J. I. Ha, and B. H. Cho, "Low-common mode voltage H-bridge converter with additional switch legs," *IEEE Trans. Power Electron.*, vol. 28, pp. 1773–1782, 2013.

[31] H. Li, Y. Liu, J. Lu, T. Zheng, and X. Yu, "Suppressing emi in power converters via chaotic spwm control based on spectrum analysis approach," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 6128–6137, 2014.

[32] H. Chung, S. Hui, and K. Tse, "Reduction of power converter EMI emission using soft-switching technique," *IEEE Trans. Electromagn. Compat.*, vol. 40, pp. 282–287, 1998.

[33] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 47, pp. 2154–2165, 2011.

[34] M. Vilathgamuwa, J. Deng, and K. J. Tseng, "Emi suppression with switching frequency modulated DC-DC converters," *IEEE Ind. Appl. Mag.*, vol. 5, pp. 27–33, 1999.

# Chapter 2

## EMI Reduction Techniques in Power Converters

## 2.1 Introduction

This Chapter presents a comprehensive review of EMI mitigation techniques and design recommendations for power converter designs considering radio astronomy applications, which are also applicable in communications and defence requiring low-EMI power converters. EMI mitigation techniques for power converters are categorised as conventional, power circuitry techniques, and control techniques and are shown in Figure 2.1.

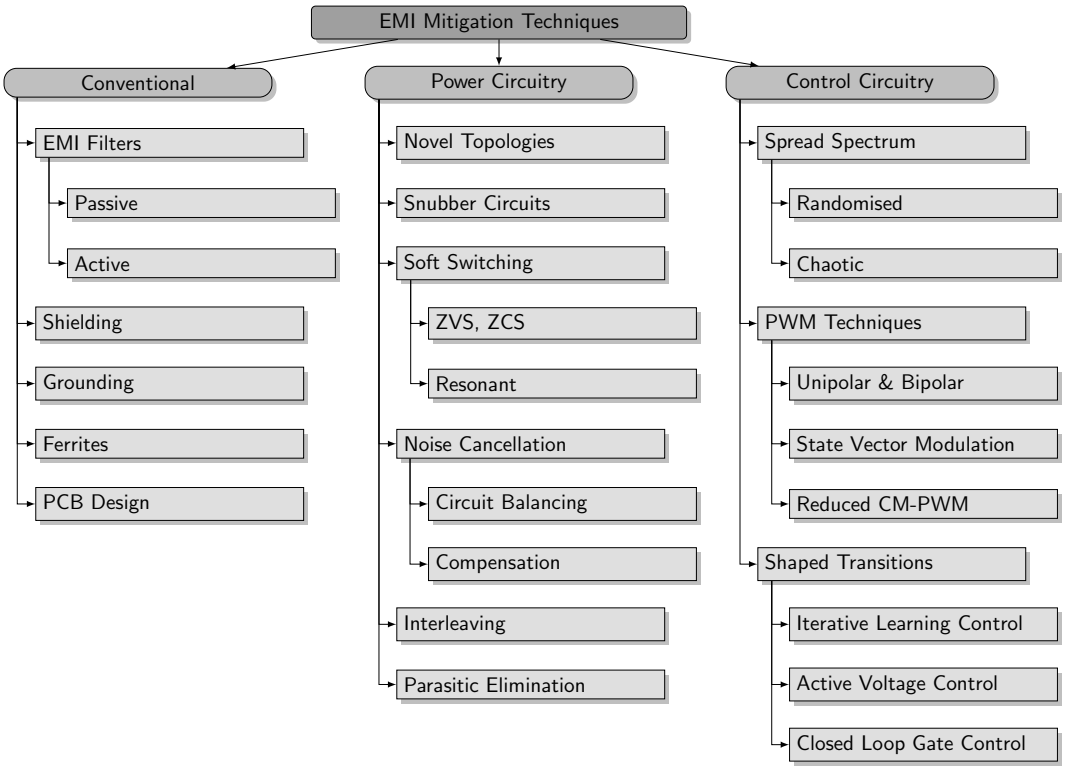
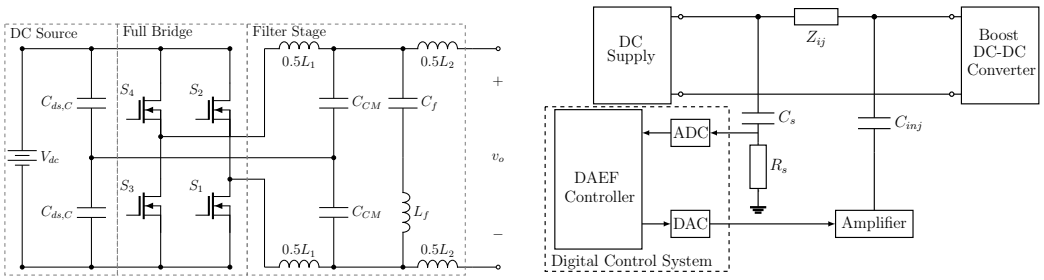



Figure 2.1: EMI mitigation techniques for power converters.

Typically, aspects of a power converter, which are significant sources of EMI and inhibit the power electronic device from complying with emissions standards, can broadly be categorised as either an emission generated during switching transients or due to parasitic components that are an artefact of non-ideal circuitry components. Conventionally, IGBTs and MOSFETs are semiconductor devices and generate harmonics that contribute to the conducted and radiated emissions generated by power converters. During switching instances, rapid $dv/dt$ and $di/dt$ are generated, caused by the sharp edges of the switching waveforms. Additionally, parasitic components form resonant frequencies contributing to significant peaks in EMI and ringing during switching. Of particular interest to the SKA-low are the high-frequency emissions generated beyond

30 MHz, which are considered a hindrance to the performance of the SKA-low and must not exceed the emission limit values set by the SKA-low EMC requirements. Additionally, emissions below 30 MHz are still considered to ensure the equipment under test (EUT) is EMC compliant across all frequency ranges.

Conventional techniques applied to mitigate EMI include electromagnetic shielding, EMI filtering, grounding, ferrites and PCB layout optimisation. EMI filtering techniques mitigate conducted EMI and are categorised as either passive [1, 2, 3, 4] as shown in Figure 2.2(a), or active [5, 6, 7] as shown in Figure 2.2(b). Similarly, conducted emissions are mitigated by ferrites and chokes [8, 9]. Lastly, PCB design techniques are applied to reduce radiated emissions in power converters by adopting layout optimisation techniques [10], reducing switching loop inductance [11], reducing loop area size [12], loop area orientation [13], and electric field propagation [14]. Although these techniques are well documented and effectively mitigate EMI, multiple stages of attenuation using conventional techniques, or a combination of conventional and novel techniques are expected to be required to comply with the SKA-low EMC standards.




(a) (b)

Figure 2.2: EMI filters, including (a) A novel LLCL filter topology used in a single phase grid connected PV inverter [3], and (b) Active EMI filter implemented using sensing circuits, injection circuitry, ADC sampling, DAC output circuitry and digital control [7].

Firstly, a summary of power circuitry EMI mitigation techniques of power converters, including snubber circuitry, parasitic elimination, paralleling techniques, noise cancellation, and novel power converter topologies, is presented. Following this, an overview of power converter control techniques for EMI mitigation is presented, including unique inverter PWM techniques. Afterwards, the Chapter discusses power converter EMI mitigation techniques suitable for radio astronomy applications, including soft-switching, novel power converter topologies, spread-spectrum switching strategies, and shaped switching transitions targeting high-frequency emissions attenuation. The two latter methods target EMI mitigation at the source with power converter control techniques. Furthermore, conduction losses must be reduced during low-EMI switching transitions,

requiring soft-switching techniques and high-efficiency topologies. Lastly, a strategic approach outlining novel mitigation strategies for power converters for shaping switching transition, which achieves high-frequency spectral roll-off, is presented. The design approach presented provides the framework for the research objectives presented in this dissertation and helps identify and bridge the gap between power converter design and EMI requirements for radio astronomy applications.

## 2.2 Novel EMI Mitigation Strategies

Novel techniques to mitigate EMI in power converters are categorised as techniques applied to the power circuitry or control circuitry. Power circuitry techniques to attenuate EMI include modifying the circuitry topology or adding auxiliary branches. In addition to common approaches such as PCB layout, EMI filters and ferrites, power circuitry design considerations such as adding snubbers and clamps can also reduce EMI. Emissions generated by power converters are reduced by including noise compensation schemes in the circuit or eliminating parasitic effects. Similarly, balancing techniques are implemented to cancel out CM generated noise. Paralleling approaches such as interleaving can be implemented to reduce ripple current and, therefore, DM emissions. Control circuitry techniques are categorised as either a PWM scheme or a gate drive control strategy.

Snubber circuits limit switching stresses and overshoot, which reduces EMI by allowing semiconductor switches to operate under zero-current or zero-voltage conditions and are classified as passive [15, 16, 17, 18, 19, 20] or active [21]. An example of a lossless passive snubber circuit implemented in a boost DC-DC converter is presented in Figure 2.3. Furthermore, computational modelling of snubber designs further improves EMI mitigation by identifying causes of EMI in the design process [22, 23].

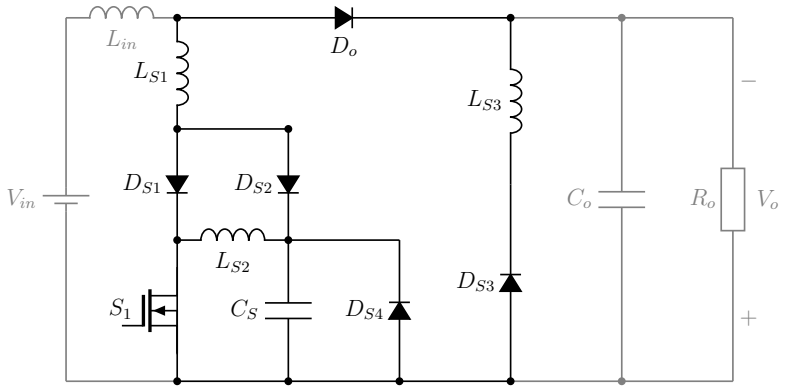
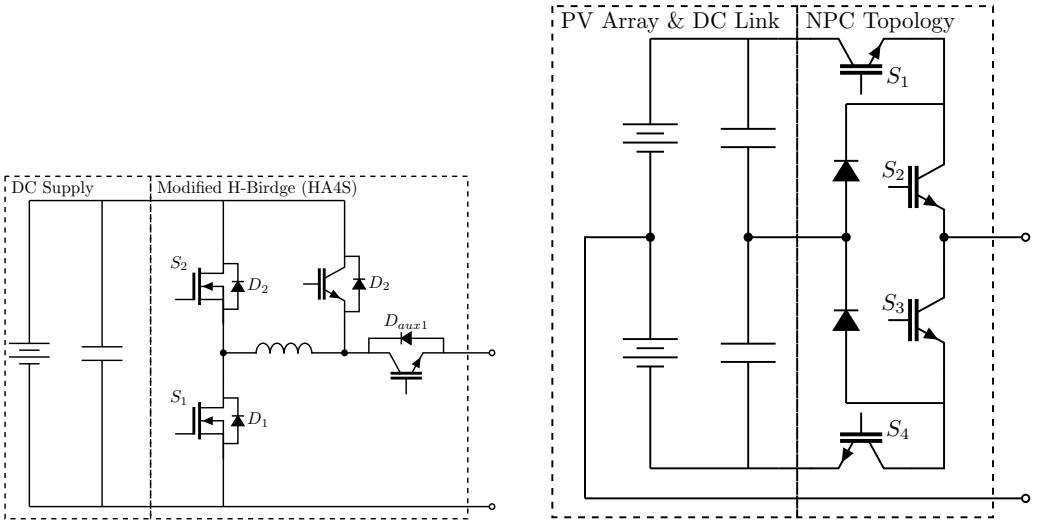



Figure 2.3: Lossless passive snubber circuit implemented in a boost DC-DC converter [19].

Parasitic components introduce resonant frequencies, which can be attenuated using a coupled inductor and capacitor circuit [24] or split leakage inductor windings [25]. Alternatively, common-mode (CM) noise signals are mitigated using cancellation techniques, which is achieved by either creating symmetrical circuits with balancing techniques [26, 27, 28], or with active techniques that measure CM noise currents and inject out of phase noise signals to mitigate CM emissions [29, 30].

Power converter topologies have been investigated to understand their impact on generated EMI, which typically involves modifying the circuitry by changing the number of active switching and auxiliary components, which are applied to the full-bridge [31, 32, 33], multi-level [34, 35], and neutral point clamped (NPC) inverters [36]. Low-EMI studies by means of modifying the H-bridge topology [33], and alleviating CMV with the NPC inverter used in PV applications [37], is presented in Figure 2.4(a) and Figure 2.4(b), respectively. Similarly, circuitry modifications are also applied to various DC-DC converter topologies, including the multi-level buck converter [38], buck-buck-boost (B3) [39] and the CukZeta [40].




(a) (b)

Figure 2.4: Low-EMI studies by (a) modifying the H-bridge topology [33], and (b) alleviating CMV with the NPC inverter used in PV applications [37].

Control circuitry EMI mitigation techniques are pulse width modulation (PWM) techniques or gate drive control strategies. Various PWM switching scheme studies perform quantitative comparisons between PWM techniques to assess EMI performance [41, 42, 43]. Additionally, novel strategies are implemented, which target reducing CM emissions by eliminating CM voltage variations and reducing CM leakage currents [44, 45, 46, 47, 48, 49, 50].

The EMI mitigation techniques previously discussed have various drawbacks when considering applications for the SKA-low. For instance, the PWM techniques are hard-switching approaches, which are undesirable for high-frequency emissions. Furthermore, filtering, shielding, snubbers, cancellation and elimination strategies acknowledge that EMI is already generated and attempts to attenuate the existing noise signals. Therefore, it is necessary to consider EMI mitigation techniques such as shaped pulse transitions and randomised PWM, which mitigates EMI at the source. Furthermore, conduction losses must be reduced, supporting the implementation of soft-switching strategies and high-efficiency topologies. Hence, attempts made to achieve EMI mitigation whilst maintaining adequate converter efficiency is desirable.

## 2.3 EMI Mitigation Techniques for Radio Astronomy Applications

### 2.3.1 Soft-Switching

Conventional power converter switching schemes are hard switched, which produce rapid changes in voltage and current, and as power converters are operated at higher frequencies, switching losses and high-frequency emissions are increased. The drawbacks of hard switching techniques are circumvented by implementing soft-switching techniques, which simultaneously improves the operating efficiency of power converters and mitigates EMI by reducing $dv/dt$ and $di/dt$ during switching transitions. The inherent reductions in switching conduction losses are only applicable to high power applications since extra auxiliary components that enable soft-switching also increase the overall conduction losses. Another drawback to soft-switching is the inclusion of additional auxiliary components, making the design and control strategy more complicated.

One common approach to soft switching is resonant switching, where resonance is invoked in the switching transition by including resonant inductors and resonant capacitors in the circuitry. Although resonant switching power converters can reduce switching losses and EMI, high-value voltage and current peaks are generated, which increases conductive losses and requires components to have higher voltage and current ratings. Resonant converters also require variable frequency control, which involves complex control circuitry. Furthermore, the auxiliary branches responsible for ZCS or ZVS switching remain in the circuit continuously and contribute to system losses.

Resonant switches combined with PWM are quasi-resonant power converters that avoid frequency modulation and are categorised as either zero-voltage switching (ZVS) or zero-current switching (ZCS) converters. Soft-switched PWM converters have similar waveforms to conventional PWM, with the main difference being reduced EMI during switching transitions. Soft-switched PWM converters will invoke resonance in a controlled manner, which is only required just before and during a switching transition to create the ZCS or ZVS condition.

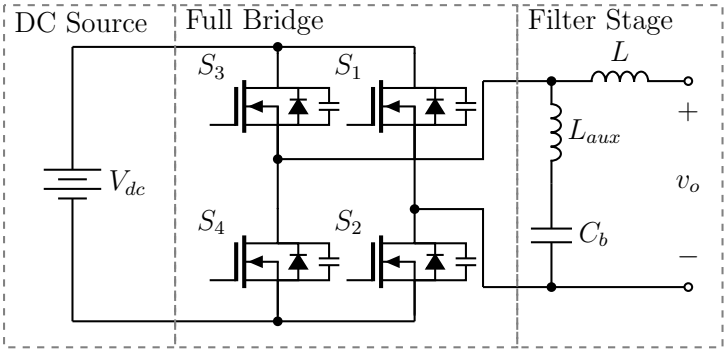



Figure 2.5: Soft-switching full-bridge inverter with an LC auxiliary circuit [51].

ZCS techniques combined with snubber circuits demonstrate that the EMI of a single-phase inverter is reduced whilst also increasing efficiency through a straightforward configuration requiring fewer active switching devices and passive components [52]. Additionally, a novel technique for a full-bridge single phase inverter using an LC auxiliary circuit to generate resonance is proposed, which charges and discharges the snubber capacitor under ZVS conditions to demonstrate high efficiency and a simpler EMI filter design [51], shown in Figure 2.5. Similarly, an auxiliary soft-switching boost converter that allows the inverter to operate under ZVS is added to a full-bridge inverter providing improved efficiency, reduced EMI and low voltage stress [53], shown in Figure 2.6. Resonant circuits can be placed on the output of full-bridge inverters to provide ZVS and improved efficiency [54]. ZCS conditions are also met using the full-bridge topology to provide improved efficiency and reduced EMI where the control methodology allows zero crossings of the resonant current by introducing a phase shift between inverter arms [55].

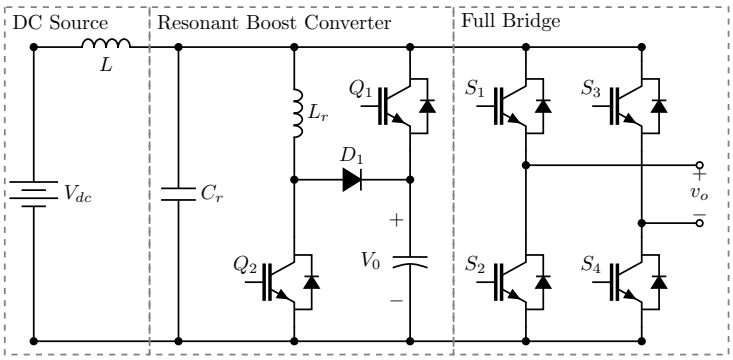



Figure 2.6: Soft-switching full-bridge inverter with an auxiliary soft-switching boost converter [53].

Aside from conventional topologies such as the full-bridge, numerous studies have been performed on the Transformer-less Photovoltaic (TPV) inverters. A novel soft-switching TPV combining traditional PWM with pulse-amplitude modulation is proposed, which improves efficiency and reduces EMI by implementing a ZCS turn-on through a resonant bridge and turn-off via a snubber circuit [56]. ZVT-TPV inverters have been studied, with the main focus being on the H6-I topology using resonant tanks as shown in Figure 2.7 and a comparative study between the hard switching equivalent [57]. It outperforms the ZVT-HERIC, ZVT-H5 and ZVT-H6-II considering efficiency and EMI by achieving zero CM leakage current under ZVS conditions with two resonant tanks and clamping the free-wheeling paths to maintain a constant CMV [57].

Similar to the ZVT literature presented by Xiao et al. [57], ZCT-TPV inverters have been studied, with the main focus being on the ZCT-H6-I topology [58]. ZCT resonant tanks are added to the main high-frequency switches, consisting of an auxiliary switch, resonant inductor and capacitor, which allows the ZCS and TPV topology to reduce EMI. As with [57], additional topologies are introduced, including the ZCT-HERIC, ZCT-H5 and ZCT-H6-II [58].

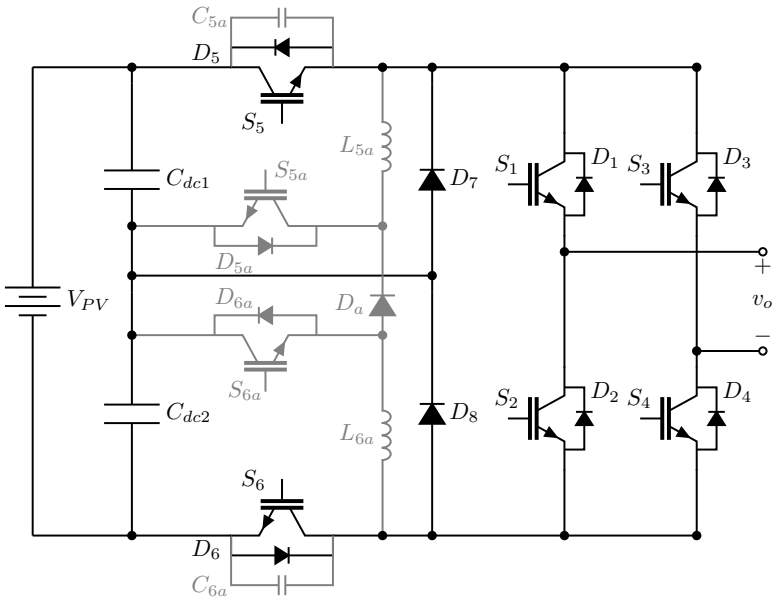



Figure 2.7: Soft switching techniques applied to the H6-TPV inverter topology utilising ZVT [57]. The main power circuitry is shown in black and the auxiliary circuitry to provide soft-switching conditions is shown in grey.

Although ZVS and ZCS can circumvent the drawbacks associated with hard-switching, soft-switching techniques have their performance shortcomings such as high voltage and current stress, circulating energy, parasitic ringing and hard switching auxiliary branches, where the two latter drawbacks are detrimental to EMI performance [59]. Comparative assessments of hard switching and soft switching techniques demonstrate the reduction in high frequency conducted emissions [60]. However, EMI reduction is marginal, as shown in studies performed on the ZCT fly-back converter [61]. Soft-switching techniques combined with shaped switching transitions presented in Section 2.3.3 are expected to provide a trade-off between the two techniques, where soft-switching will improve switching losses, and shaped transitions will provide high-frequency EMI mitigation. A preliminary study comparing the ideal transition of a logistic shaped transitions with logistic shaped transitions, where a portion of the transitions undergoes soft-switching, is presented in Chapter 6. The spectral comparison provides insight into the expected trade-off in performance considering continued research efforts and the shaped waveform technology applications.

### 2.3.2 Spread Spectrum Modulation Techniques

Novel methods applied in conjunction with traditional methods achieve the best EMI suppression outcomes, which are achieved by implementing a switching control strategy. For instance, controlling how and when the switch is operated can have a desired outcome for EMI reduction. Frequency domain analysis of fixed frequency PWM determines the harmonic spectral peaks that significantly contribute to EMI. Random frequency modulation achieves EMI reduction, whereby the switching frequency is varied according to a randomised signal. EMI mitigation is achieved since the switching instances are no longer occurring periodically, which do not generate peaks in the emissions when analysed in the frequency domain. The randomised switching frequency spreads the emission over the entire frequency range, therefore reducing EMI. One drawback to the randomised approach is that the random switching frequency adds complexity to the design since the component selection is frequency-dependent. Although randomised modulation strategies are favourable for EMI mitigation, design drawbacks include complexities associated with sizing inductors and capacitors with randomised switching frequencies.

In addition to random frequency modulation, the duty cycle and pulse position can also be randomised to reduce EMI in buck converters, as shown in Figure 2.8. Implementing the randomised modulation strategies with a field-programmable gate array (FPGA) shows that the randomised duty ratio significantly reduces conducted emissions [62]. Similarly, a computational study performed up to 108 MHz on randomised PWM tech-

niques such as randomised duty ratio, random carrier frequency modulation with fixed duty or variable duty cycles, demonstrated the two former strategies are preferred for low EMI applications in DC-DC converters [63]. When tested per EN55011 Class B, a chaotic switched-mode power converter reduced peak emissions by 25 dB and 22 dB for conducted and radiated emissions respectively [64].

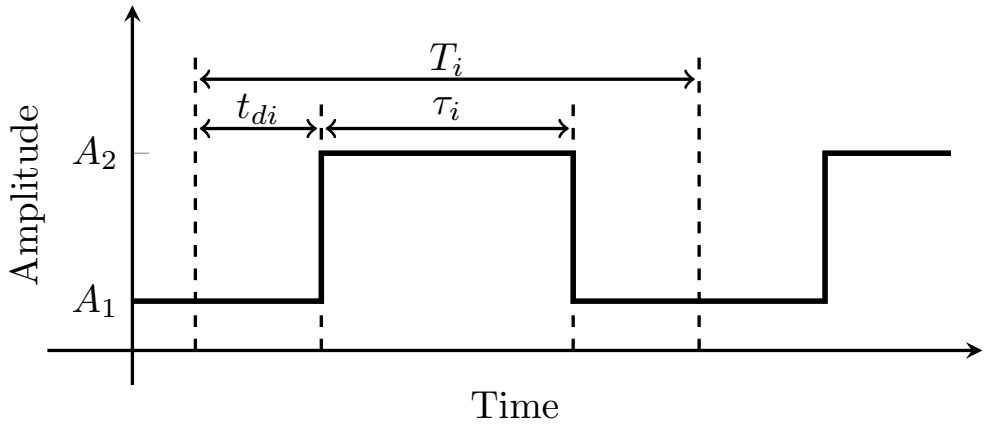



Figure 2.8: Randomised modulation strategy [63].

Similar to randomised PWM strategies, spread-spectrum harmonics are achieved from chaos control modulation schemes, known as chaos control with parameter modulation and chaotic PWM control. The latter is typically favourable since it adopts the well-known PWM strategy implemented with additional programmable chaotic signals. The ripple magnitudes are also programmable, providing the desired outcome that circumvents one of the significant drawbacks of chaotic parameter modulation. Additionally, chaotic switching using a logistic-map PWM is shown to reduce emissions compared to a hard-switched counterpart [65]. Furthermore, the EMI performance of various chaotic mapping approaches, including the circle, logistic and tent maps, was assessed by comparing with the PSD of each approach, demonstrating that a chaotic map with a kurtosis closest to a uniform distribution provides the best outcome for EMI reduction [66].

A novel chaotic switching scheme for a boost converter has been developed to reduce EMI, which uses two reference currents to create an upper and lower bound reference signal, where increasing the lower bound reference reduced ripple [67]. Additionally, EMI is reduced up to 23 dB by adopting a pseudo-random clock generation scheme, which varies the switching frequency between 1.74 MHz to 2.84 MHz in 128 steps [68]. Furthermore, both analogue [69] and digital [70] chaotic modulation strategies are shown to reduce emissions when compared to hard switching.

A chaotic sinusoidal-PWM (SPWM) switching scheme that chaotically alters the switching frequency within a predetermined range considerably reduces the EMI [71]. The chaotic SPWM technique is utilised in TPV full-bridge inverters, experimentally observing the THD and EMI reduction [72]. Multi-level inverters are known to generate low levels of EMI, which are further reduced by implementing a pseudo-random carrier modulation scheme [73]. Furthermore, a novel randomised modulation technique is implemented using a digital signal processor where a saw-tooth waveform acts as the reference, and a randomly varied high-frequency triangular waveform is the carrier is implemented to study reductions in generated EMI [74].

Lastly, spread-spectrum switching schemes and soft-switching techniques are combined by implementing a soft-switched auxiliary circuit branch and a chaotic carrier on a PWM boost converter, as shown in Figure 2.9, to fine-tune the output ripple, which significantly reduced EMI compared to hard switching [75]. Pseudo-random modulation and ZCT are combined in the ZCT flyback isolated DC-DC converter topology, demonstrating a reduction in EMI [76].

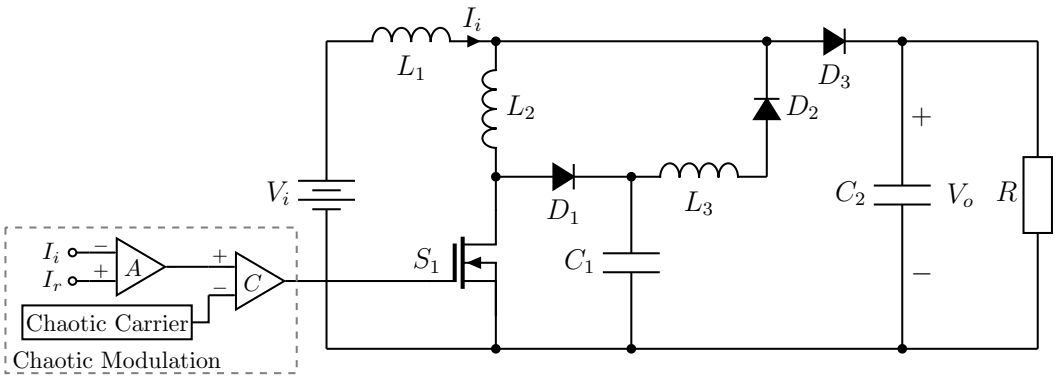



Figure 2.9: Chaotic modulation of a soft-switching DC-DC converter [75].

Although spread spectrum techniques demonstrate EMI mitigation through reduced harmonic spectral peaks, the techniques have an inherent drawback since each switching instant is still hard-switched, which is undesirable for high-frequency EMI mitigation. Randomised PWM (R-PWM) strategies should be combined with shaped switching transitions to reduce further the spectral contribution of a switching waveform. Both techniques are complementary since the R-PWM will produce a spread spectrum outcome, whereas the shape transition will produce high-EMI mitigation, and in the case of a logistic shaped switching transition, substantial high-frequency roll-off. A preliminary study comparing the ideal transition of a logistic shaped switching transition with randomised logistic shaped switching transitions is presented in Chapter 6. Furthermore, the following section presents a literature review of shaped switching transitions.

### 2.3.3 Shaped Switching Transitions

EMI mitigation is achieved by shaping the switching transition of a semiconductor switch with precise gate-drive circuitry. Rather than adjusting the amplitude and frequency of the PWM carrier signal, a control strategy is implemented to precisely shape the switching transitions of a semiconductor switch to achieve desirable EMI attenuation. These control strategies can be combined with conventional PWM switching techniques, with the additional transition shaping control initiated during each switching transition.

Conventionally, EMI is suppressed in power converters when the transition times of the semiconductor switches are increased [77]. However, it is detrimental to the power converter efficiency, and EMI attenuation should be achieved without considerable power losses. Shaping waveforms is beneficial for efficiency and EMI mitigation since EMI is reduced without increasing the transition times of the switching scheme [78]. This section provides a summary of studies presented in journal articles considering shaped switching transitions and EMI mitigation.

The switching transitions summarised in this section include trapezoidal, S-shaped, sinusoidal and Gaussian-shaped transitions. Naturally, the progressions presented in the literature seek to further reduce EMI by finding ideal shaped transitions with the temporal characteristics that favour EMI mitigation, which progress towards shaped pulse transitions that are infinitely differentiable. These waveforms are ideal for applications where a trade-off between efficiency and low-EMI is necessary. Shaped transitions achieve low-EMI outcomes through high-frequency harmonic mitigation without considerably increasing the switching waveform transition times. Therefore, the switching losses are reduced compared to hard switching applications, which achieve EMI mitigation with significantly longer switching transitions.

The basis of the analytical modelling provided for EMI at the source is obtained in [79] and [78], which provide analytical Fourier series to predict the harmonic spectra of hard-switching and S-shaped waveforms, respectively. The theory behind the S-shaped pulse transition describes the third derivative of the waveform as a pulse train, which allows for the spectral content to be analytically derived from time-shifting and differentiation properties of the Fourier series [80]. A switching transition with a fixed transition time can have many unique S-shaped transitions, which are synthesised from temporal characteristics of the S-shaped function and the first, second and third-order derivatives, which is inherently beneficial for reducing switching losses and EMI mitigation [78]. Naturally, subsequent research efforts expanded on the concept of exploring higher-order derivative pulse trains, which can further reduce EMI [81, 82].

Features from the first to the fourth derivative were studied to investigate the effects time-domain characteristics of the switching waveform have on the harmonic spectra [81]. The harmonics can reduce by $20n$ dB per decade, where $n$ is the highest derivative. Although the roll-off is only verified up to the fourth derivative of a switching transition, there will be a limit to the roll-off that higher-order derivative pulses can achieve. Computational results of infinitely differentiable waveforms such as a Gaussian-shaped transition is presented in [82, 83], which provide significant harmonic spectral roll-off and, therefore, high-frequency EMI attenuation. Infinitely differentiable waveforms can provide maximum EMI mitigation at the source since the waveform and all of its derivatives are smooth. However, only specific shaping of the waveform will yield the desired low-EMI outcome.

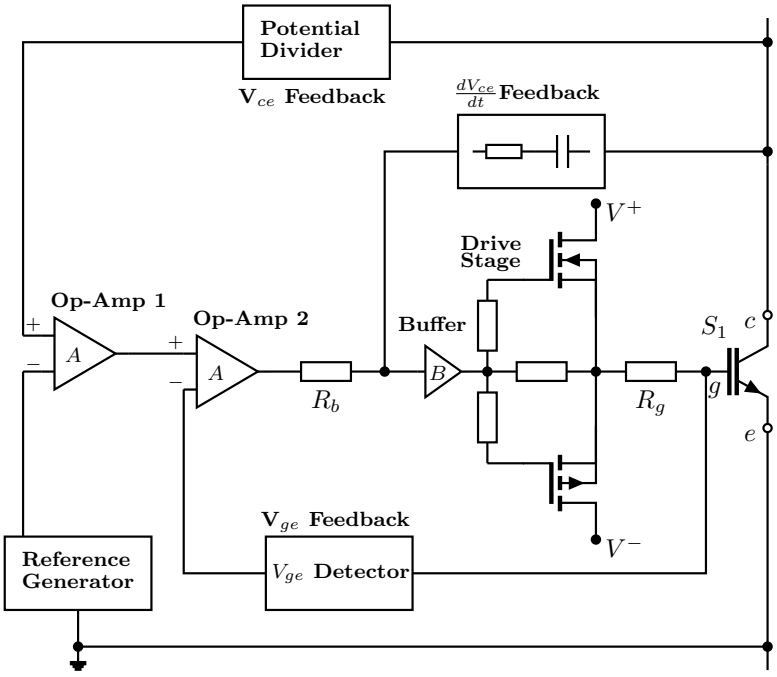



Figure 2.10: Feedback control for shaped transition applying AVC [82].

The most recent literature on low-EMI switching transitions summarises research outcomes, which primarily focus on control system development and circuitry design to achieve shaped transitions to mitigate high-frequency harmonics. Implementation of shaped pulse transitions has been demonstrated through iterative learning control via active control of the first and second derivatives [84], shaped transition modelling applied to resonant circuitry [85, 86], active voltage control (AVC) of Gaussian-shaped waveforms [82, 87] shown in Figure 2.10, and closed-loop gate control with on-state resistance compensation [88] shown in Figure 2.11. One drawback when implementing

the gate-drive control to shape transitions is the signal quantisation observed in [82, 88] by digitising the control system. The gate-drive control system adds high-frequency harmonics generated by the clock signal of the digital processor used, which is an undesirable result when high-frequency emission reduction is required for the SKA-low.

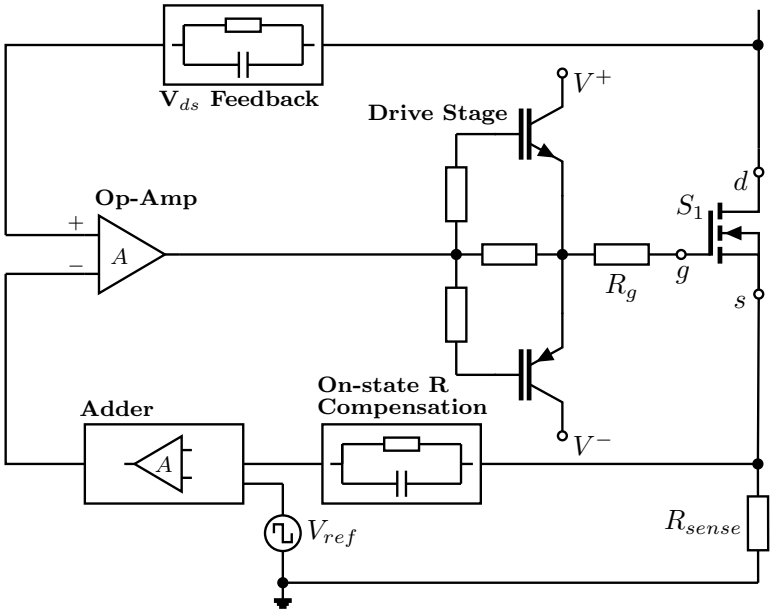



Figure 2.11: Feedback control for shaped transition applying closed-loop gate control with on-state resistance compensation [88].

Low-EMI shaped transition should be identified, such as Gaussian-shaped waveforms that provide steep spectral content roll-off, which is desirable for high-frequency EMI mitigation [82, 83, 87, 88]. However, there are limitations in the modelling and implementation, such as high-frequency spectral content caused by waveform discontinuities [82, 83, 87], or signal quantisation generated by the digital gate-drive control system utilising on-state resistance compensation [88]. Logistic pulse transitions are studied, extending the ideas of infinitely differentiable shaped switching transitions and the appropriate control circuitry. Although these functions, like Gaussian waveforms, are asymptotic, they are derived such that the waveforms equate to the desired amplitude for shaped rising transitions, which circumvents waveform discontinuities. The mathematical treatment of the logistic waveform and assessment of the harmonic content to analyse EMI is provided in the following Chapter.

## 2.4 EMC Design Strategy Recommendations for the SKA-Low

Although the techniques summarised seek to reduce EMI in power converters, novel mitigation strategies should be selected based on the amount of attenuation required to meet the SKA-low EMC limits. Typically, the outcomes presented in the literature demonstrate EMI mitigation compared to a worst-case switching noise scenario like hard-switching. The mitigation strategies, whether applied to the power circuitry or control strategy, will seek to demonstrate compliance with CISPR22 Class A or Class B limits and compare emissions to hard-switching. Given that the SKA-low emission limits are approximately 100 dB less than MIL-STD-461F RE102, compliance will be achieved with multiple levels of shielding and filtering with a device that is CISPR22 compliant. A mitigation strategy must be adopted to comply with the SKA-low EMC standard, such as logistic-shaped switching transitions targetted at achieving considerable attenuation beyond 30 MHz

The modelling and prototype design presented in subsequent chapters achieves logistic shaped transitions capable of producing high-frequency spectral content roll-off within a power converter. The novel design approach primarily addresses actual circuit implementation concerning logistic shaped waveform realisation. The modelling and prototype design improves signal quantisation and waveform discontinuities to reduce high-frequency EMI. Signal quantisation and waveform discontinuities are the primary impairments preventing the theoretical roll-off observed in Gaussian and logistic-shaped transitions. Additionally, measurement techniques are presented to reduce noise in the measured waveforms. The design and measurement recommendation presented in the remainder of this section defines a staged approach to achieve the steep spectral content roll-off observed in the theoretical mathematical treatment of shaped switching transitions.

### 2.4.1 Logistic Shaped Switching Transitions

Infinitely differentiable shaped transitions presented in the literature, like Gaussian-shaped switching transitions, provide excellent spectral content roll-off, which is desirable for high-frequency EMI mitigation. Firstly, additional mathematical functions suitable for EMI mitigation are identified to understand better the time-domain characteristics that influence high-frequency spectral content roll-off. The logistic functions belong to a class of Sigmoid functions and are typically used in population growth predictive models [89]. The logistic function is defined by its growth rate, a temporal characteristic selected for optimised EMI mitigation through steep spectral content roll-off. Gaussian and logistic functions are asymptotic, and therefore introduce discontinuities when used to synthesise shaped reference waveforms, which are not favourable for high-

frequency EMI mitigation. The transitions should have suitably defined asymptotes to ensure the reference waveforms are created to avoid discontinuities. Expanding on the set of infinitely differentiable waveforms suitable for EMI mitigation, a more in-depth understanding of the time-domain characteristics that yield optimised emissions attenuation is ascertained.

In the case of a shaped rising transition, the logistic function asymptotes are defined so the transition will start at zero and reach the signal amplitude at the end of the transition. Furthermore, signal quantisation effects should be avoided where possible, and a more in-depth understanding of MOSFET transients can be applied, which avoids introducing unwanted high-frequency harmonics caused by digital clock signals. A comprehensive understanding of the MOSFET output drain-source voltage transient response to precisely controlled gate-drive will produce smoother transitions. Considering the noise introduced to the power circuitry through signal quantisation generated by digital control circuitry, the amount of attenuation achieved will be limited. Additionally, other factors such as parasitic components and propagation paths will limit the amount of practically achieved attenuation. The analysis of the spectral content provides a basis for making informed estimates considering the expected emission levels.

### 2.4.2 Proposed Power Converter Topology

Next, a circuit topology and control strategy is presented to reduce signal quantisation effects where possible. Additionally, a more in-depth understanding of MOSFET transients during changes in the MOSFET gate-drive is required to understand the gate-drive initialisation, control command sequencing, and gate-drive profiles required to provide smooth low-EMI switching transitions. The proposed half-bridge utilises current injection circuitry to ensure a smooth transition in the MOSFET drain-source voltage during the second half of the transition. Additionally, capacitors are placed in parallel with the MOSFETs since the inherent drain-source capacitance of the MOSFETs is insufficient to control the drain-source voltage. The combination of the injection circuitry and parallel capacitors provides smooth shaped transitions that reduce signal quantisation. The circuit topology and control strategy is presented in Chapter 4.

### 2.4.3 Circuit Simulation Approach

Simulations of the proposed half-bridge circuit identify what is required to produce shaped transitions. Additionally, the simulations identify the MOSFET characteristics that are pertinent to the shaped waveform control. SPICE models of the intended MOSFETs to be used in the power converter should be modelled to define the expected transient response of the MOSFET accurately. Feedback control can be simulated us-

ing MATLAB and LTSPICE to determine the gate-drive signals and the precise timing of each MOSFET that will produce a logistic-shaped switching transition. The critical information expected to be obtained from the MATLAB and LTSPICE modelling will be the expected gate-drive profiles, the timing and sequencing of each MOSFET, and the requirements for initialising each MOSFET. The latter is essential when preparing the injection MOSFETs to reduce any transients and delay the injection circuit. Therefore, a smooth transition between the power MOSFET and injection MOSFET control ensures the waveform control remains as smooth as possible at the mid-point. The circuit simulations are presented in Chapter 4.

### 2.4.4 Prototype Development

A prototype of the half-bridge is required to verify the waveform shaping technology. Additionally, the technology will be integrated with an operational power converter, demonstrating suitability for PWM switching schemes and operability under constant load. Additionally, the selection of analogue to digital converters (ADC), digital to analogue converters (DAC), and microprocessors ($\mu$-processors) is critical. Selecting ADC, DAC, and $\mu$-processors must ensure onerous high-frequency noise is not generated. However, ADC and DAC resolution and the $\mu$-processor clock speed are critical for control accuracy. Therefore, a trade-off exists between the control system accuracy and the noise floor introduced by the digital circuitry, which depends on the intended application. Additionally, analogue circuitry control would mitigate signal quantisation effects. However, the digital control circuit is initially required since the $\mu$-processor is programmable, which offers flexibility during prototype development. The prototype design and implementation are presented in Chapter 5.

### 2.4.5 Measurement and Verification Challenges

Lastly, measurement approaches are required to verify the low-EMI performance of the shaped switching transitions. The approach should reduce noise that is introduced during the measurement of the shaped transitions. Since oscilloscopes are used to perform time-domain measurements and frequency domain measurements, it is difficult to verify the steep roll-off of a logistic shaped transition since the oscilloscope bandwidth is limited by the measurement signal-to-noise ratio created by the quantisation of the ADC in the oscilloscope [90]. Since MOSFET switching is periodic and random noise is present in measurements, time-domain averaging is a suitable technique to reduce noise introduced by the measuring equipment.

Although averaging techniques are necessary to remove measurement equipment noise, the time-step required to perform frequency domain analysis on the shaped transi-

tion switching signals will be less than 100 ns to reach frequencies beyond 100 MHz. A shaped switching transition occurs over microseconds, whereas switching frequencies of power converters occur over 10-100ms. Therefore, measurement approaches are time-consuming and relatively data-intensive to sample the waveform with <100ns time-steps and average the switching waveform over an entire switching period. Additionally, oscilloscopes that simultaneously perform both time and frequency domain measurements may be cost-prohibitive at the level of accuracy required. The prototype laboratory measurement is presented in Chapter 5.

## 2.5 References

[1] W. Wu, Y. Sun, Z. Lin, T. Tang, F. Blaabjerg, and H. S. H. Chung, "A new LCL-filter with in-series parallel resonant circuit for single-phase grid-tied inverter," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 4640–4644, 2014.

[2] M. H. Hedayati and V. John, "Filter configuration and PWM method for single phase inverters with reduced conducted EMI noise," *IEEE Trans. Ind. Appl.*, pp. 1–6, 2015.

[3] W. Wu, Y. Sun, Z. Lin, Y. He, M. Huang, F. Blaabjerg, and H. S. H. Chung, "A modified LLCL filter with the reduced conducted EMI noise," *IEEE Trans. Power Electron.*, vol. 29, pp. 3393–3402, 2014.

[4] J. Ji, W. Wu, Y. He, Z. Lin, F. Blaabjerg, and H. Chung, "A simple differential mode EMI suppressor for the LLCL-filter based single phase grid-tied transformerless inverter," *IEEE Trans. Ind. Electron.*, vol. 62, pp. 4141–4147, 2015.

[5] D. Hamza, Q. Mei, and P. K. Jain, "Implementation of an EMI active filter in grid-tied PV micro-inverter controller and stability verification ," in *38th Annu. Conf. IEEE Industrial*, 2012, pp. 477–482.

[6] X. Chang, Y. Yang, W. Chen, and X. Yang, "Implementation of a novel active common-mode filter used in DC-DC converters," in *URSI General Assembly and Scientific Symp.*, 2014, pp. 1–4.

[7] J. Ji, W. Chen, Z. Gu, X. Yang, and X. Zhang, "A control method of digital active EMI filter," in *IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1141–1145.

[8] P. Chen and Y. Lai, "Effective EMI filter design method for three-phase inverter based upon software noise separation," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2797–2806, 2010.

[9] D. Xu, C. K. Lee, S. Kiratipongvoot, and W. M. Ng, "An active EMI choke for both common- and differential-mode noise suppression," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4640–4649, 2018.

[10] J. L. Schanen, L. Jourdan, and J. Roudet, "Layout optimization to reduce EMI of a switched mode power supply," in *IEEE 33rd Annu. IEEE Power Electron. Spec. Conf. Proc.*, vol. 4, 2002.

[11] K. Koo, J. Kim, M. Kim, and J. Kim, "Impact of PCB design on switching noise and EMI of synchronous DC-DC buck converter," in *IEEE Int. Symp. Electromagn. Compat.*, 2010, pp. 67–71.

[12] R. Blecic, J. Bacmaga, R. Gillon, B. Nauwelaers, and A. Baric, "EMC-oriented design of output stage of synchronous buck converter," in *11th Int. Workshop Electromagn. Compat. Integr. Circuits*, 2017, pp. 91–96.

[13] A. Bhargava, D. Pommerenke, K. W. Kam, F. Centola, and C. W. Lam, "DC-DC buck converter EMI reduction using PCB layout modification," *IEEE Trans. Electromagn. Compat.*, vol. 53, no. 3, pp. 806–813, 2011.

[14] A. Nejadpak and O. A. Mohammed, "Physics-based optimization of EMI performance in frequency modulated switch mode power converters," in *6th Int. Conf. Electromagn. Field Problems Applicat.*, 2012, pp. 1–4.

[15] K. Ogura, S. Chandhaket, T. Ahmed, and M. Nakaoka, "Non-isolated ZVS-PWM boost chopper-fed dc-dc converter with auxiliary edge resonant snubber," in *29th Annu. Conf. IEEE Industrial Electronics Soc.*, vol. 3, 2003, pp. 2356–2362.

[16] Y. Tang, H. Zhu, B. Song, J. S. Lai, and C. Chen, "EMI experimental comparison of PWM inverters between hard- and soft-switching techniques," in *Power Electron. Transportation*, 1998, pp. 71–77.

[17] H. Zhang, B. Kou, Y. Jin, and H. Zhang, "Analysis of MOSFETs switching performance in auxiliary resonant snubber inverter," in *8th IEEE Int. Power Electron. Motion Control Conf.*, 2016, pp. 1230–1235.

[18] C. U-Yaisom, W. Khanngern, and S. Nitta, "The study and analysis of the conducted EMI suppression on power MOSFET using passive snubber circuits," in *3rd Int. Symp. on Electromagn. Compat.*, 2002, pp. 561–564.

[19] M. Mohammadi, E. Adib, and M. R. Yazdani, "Family of soft-switching single-switch PWM converters with lossless passive snubber," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3473–3481, 2015.

[20] H. S. Shin, H. A. Huynh, and S. Kim, "Design and optimization of inductive snubber for DC-DC converter," in *Int. Symp. Electromagn. Compat.*, 2017, pp. 148–150.

[21] R. T. Li and C. N. Ho, "An active snubber cell for$n$-phase interleaved DC–DC converters," *IEEE J. Emerging and Selected Topics Power Electron.*, vol. 4, no. 2, pp. 344–351, 2016.

[22] M. Rucinski, P. Musznicki, and P. J. Chrzan, "Electromagnetic interference frequencies prediction model of flyback converter for snubber design," *IET Power Electron.*, vol. 8, no. 6, pp. 994–999, 2015.

[23] A. Nejadpak and O. A. Mohammed, "Performance analysis of planar inductor based snubbing circuit on EMI effects generated by switching action in DC/DC boost converter," in *Int. Symp. Electromagn. Compat.*, 2012, pp. 1–6.

[24] H. Zhang and A. Wu, "Common-mode noise reduction by parasitic capacitance cancellation in the three-phase inverter," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 1, pp. 295–300, 2019.

[25] K. Nomura, T. Kojima, A. Takahashi, Y. Hattori, and K. Torii, "Conducted common mode noise reduction for boost converters using leakage inductance of coupled inductor," in *IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 294–299.

[26] M. Shoyama, T. Okunaga, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," in *IEEE 32nd Annu. Power Electronics Spec.Conf.*, vol. 1, 2001, pp. 451–456.

[27] M. Shoyama, M. Ohba, and T. Ninomiya, "Balanced buck-boost switching converter to reduce common-mode conducted noise," in *IEEE 33rd Annu. Power Electronics Spec. Conf.*, vol. 4, 2002, pp. 2056–2061.

[28] M. Shoyama, T. Tsumura, and T. Ninomiya, "Mechanism of common-mode noise reduction in balanced boost switching converter," in *IEEE 35th Annual Power Electronics Spec. Conf.*, vol. 2, 2004, pp. 1115–1120.

[29] Z. Ning, Z. Yan, Y. Zhang, N. Wang, J. Tang, and Z. Min, "DM EMI reduction using the gate drive signal in a flyback converter," in *2th Int. Symp. Antennas, Propag. and EM Theory*, 2018, pp. 1–5.

[30] S. Ohara, S. Ogasawara, T. Masatsugu, K. Orikawa, and Y. Yamamoto, "A novel active common-noise canceler combining feedforward and feedback control," in *IEEE Energy Convers. Congr. Expo.*, 2017, pp. 2469–2475.

[31] A. Rao, T. A. Lipo, and A. L. Julian, "A modified single phase inverter topology with active common mode voltage cancellation," in *30th Annu. IEEE Power Electronics Specialists Conf.*, vol. 2, 1999, pp. 850–854.

[32] D. Dong, F. Luo, D. Boroyevich, and P. Mattavelli, "Leakage current reduction in a single-phase bidirectional AC-DC full-bridge inverter," *IEEE Trans. Power Electron.*, vol. 27, pp. 4281–4291, 2012.

[33] J. W. Shin, H. Shin, G. S. Seo, J. I. Ha, and B. H. Cho, "Low-common mode voltage H-bridge converter with additional switch legs," *IEEE Trans. Power Electron.*, vol. 28, pp. 1773–1782, 2013.

[34] N. Karnik, D. Singla, and P. R. Sharma, "Comparative analysis of harmonic reduction in multilevel inverter," in *5th IEEE Power India Conf.*, 2012, pp. 1–5.

[35] L. M. A. Beigi, N. A. Azli, F. Khosravi, E. Najafi, and A. Kaykhosravi, "A new multilevel inverter topology with reduced number of power switches," in *IEEE Int. Conf. Power Energy*, 2012, pp. 55–59.

[36] M. J. Ferdous, S. Kabir, M. R. A. Siddique, and U. Salma, "Split inductor based neutral point clamped inverter using improved modulation technique to reduce common mode voltage," in *Int. Conf. on Electrical and Computer Engineering*, 2014, pp. 623–626.

[37] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless photovoltaic inverters connected to the grid," in *IEEE Appl. Power Electron. Conf. Expo.*, 2007, pp. 1733–1737.

[38] I. Grobler and M. N. Gitau, "Common mode noise in three-level DC-DC converters," in *AFRICON*, 2009, pp. 1–6.

[39] J. W. Shin, H. Shin, J. I. Ha, and B. H. Cho, "A low-common mode noise and high-efficiency buck-buck-boost inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 2259–2265.

[40] M. Islam and L. Czarnecki, "Design and simulation of a single phase grid connected photovoltaic CukZeta inverter," in *IEEE 39th Photovoltaic Spec. Conf.*, 2013, pp. 2896–2901.

[41] K. Karanun, W. Khanngern, and S. Nitta, "The characteristics of conducted EMI emission on PWM inverters with various PWM patterns," in *3rd Int. Symp. on Electromagnetic Compatibility*, vol. 1, 2002, pp. 533–536.

[42] M. Salem, M. Hamouda, J. Ben, and H. Slama, "Performance assessment of conventional modulation schemes in terms of conducted EMI egnerated by PWM inverters," in *Int. Conf. on Green Energy*, 2014, pp. 207–212.

[43] C. C. Hou, C. C. Shih, P. T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, pp. 1971–1979, 2013.

[44] T. Kato, L. Inoue, and K. Akimasa, "EMI Reduction Method for a Single-Phase PWM Inverter by Suppressing Common-Mode Currents with Complementary Switching," in *CES/IEEE 5th Int. Power Electronics and Motion Control Conf.*, vol. 3, 2006, pp. 1–5.

[45] M. Cacciato, A. Consoli, G. Scarcely, G. Scelba, and T. A., "A novel space-vector modulation technique for common mode emissions reduction," in *Int. Aegean Conf. on Electrical Machines and Power Electronics*, vol. 1, 2007, pp. 199–204.

[46] M. F. N. Tajuddin, N. H. Ghazali, T. C. Siong, and N. Ghazali, "Modelling and simulation of modified unipolar PWM scheme on a single phase DC-AC converter using PSIM," in *2009 IEEE Student Conf. on Research and Development*, vol. 1, 2009, pp. 328–331.

[47] N. Ozturk, R. Canbaz, and E. Celik, "Constant voltage constant frequency control for single phase three level inverter," in *Int. Conf. Renewable Energy Research and Applications*, 2012, pp. 1–5.

[48] A. M. Hava and E. Ün, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 24, pp. 241–252, 2009.

[49] M. C. Cavalcanti, K. C. De Oliveira, A. M. De Farias, F. a. S. Neves, G. M. S. Azevedo, and F. C. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 1360–1368, 2010.

[50] W. Cui, B. Yang, Y. Zhao, W. Li, and X. He, "A novel single-phase transformerless grid-connected inverter," in *37th Annu. Conf. IEEE Industrial Electronics Soc.*, 2011, pp. 1126–1130.

[51] B. Koushki, S. A. Khajehoddin, A. Safaee, P. Jain, and A. Bakhshai, "A high power density grid connected soft switched inverter," in *IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 2264–2270.

[52] X. He, J. Kong, Z. Qian, and W. B. W, "Analysis and design of composite soft switching single phase inverters with PWM control," in *Proc. IEEE Int. Conf. Power Electronics and Drive Systems*, vol. 2, 1999, pp. 1102–1107.

[53] D. jo Won, C.-Y. Won, S. won Lee, Y.-C. Jung, and D.-S. Oh, "A novel DC-AC single phase resonant inverter using soft switching boost converter," in *IEEE 6th Int. Power Electronics and Motion Control Conf.*, 2009, pp. 1483–1487.

[54] I. Colak and E. Kabalci, "Implementation of energy-efficient inverter for renewable energy sources," *Electr. Pow. Compo. Sys.*, vol. 41, pp. 31–46, 2012.

[55] H. Matsuo, H. Yonemori, and Y. Yasaka, "Phase-shift controlled zero current switching high frequency inverter in the MHz frequency range," in *Int. Power Electronics Conf.*, 2010, pp. 2830–2835.

[56] I. Pecelj, S. de Haan, and J. Ferreira, "Analytical modelling of modulation of soft-switched partial-resonant link inverter suitable for PV," 2013, pp. 5363–5368.

[57] H. F. Xiao, X. P. Liu, and K. Lan, "Zero-voltage-transition full-bridge topologies for transformerless photovoltaic grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 5393–5401, 2014.

[58] H. F. Xiao, K. Lan, B. Zhou, L. Zhang, and Z. Wu, "A family of zero-current-transition transformerless photovoltaic grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3156–3165, 2015.

[59] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," in *19th Annu. Conf. IEEE Ind. Electron.*, vol. 42, 1993, pp. 637–643.

[60] J. Shao, R. L. Lin, F. C. Lee, and D. Y. Chen, "Characterization of EMI performance for hard and soft-switched inverters," in *15th Annu. IEEE Appl. Power Electron. Conf. Expo.*, vol. 2, 2000, pp. 1009–1014.

[61] M. R. Yazdani, H. Farzanehfard, and J. Faiz, "EMI analysis and evaluation of an improved ZCT flyback converter," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2326–2334, 2011.

[62] G. M. Dousoky, M. Shoyama, and T. Ninomiya, "Fpga-based spread-spectrum schemes for conducted-noise mitigation in DC-DC power converters: Design, implementation, and experimental investigation," *IEEE Trans. Ind. Electron.*, vol. 58, pp. 429–435, 2011.

[63] F. Mihalic and D. Kos, "Reduced conductive EMI in switched-mode DC-DC power converters without EMI filters: PWM versus randomized PWM," *IEEE Trans. Power Electron.*, vol. 21, pp. 1783–1794, 2011.

[64] H. Wong, Y. Chan, and S. W. Ma, "Electromagnetic interference of switching mode power regulator with chaotic frequency modulation," in *23rd Int. Conf. Microelectron.. Proc.*, vol. 2, 2002, pp. 577–580.

[65] R. Gamoudi, D. Chariag, and L. Sbita, "Electromagnetic interference reduction in boost converter using logistic PWM," in *Int. Conf. Green Energy Convers. Syst.*, 2017, pp. 1–4.

[66] R. Gamoudi, D. Chariag, and L. Sbita, "Impact of the used chaotic map on the EMI reduction level," in *Int. Conf. Elect. Sci. and Technol.*, 2018, pp. 1–5.

[67] H. Li, W. K. S. Tang, Z. Li, and W. A. Halang, "A chaotic peak current-mode boost converter for EMI reduction and ripple suppression," in *IEEE Trans. Circuits and Syst. II, Exp. Briefs.*, vol. 55, 2008, pp. 763–767.

[68] O. Trescases, G. Wei, and W. T. Ng, "A low-power DC-DC converter with digital spread spectrum for reduced EMI," in *37th IEEE Power Electronics Spec. Conf.*, 2006, pp. 1–7.

[69] H. Li, Z. Li, B. Zhang, F. Wang, N. Tan, and W. A. Halang, "Design of analogue chaotic PWM for EMI suppression," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 1001–1007, 2010.

[70] L. Premalatha and A. Thanuja, "Generation of chaos and EMI reduction in current controlled boost converter using random modulation," in *Int. Conf. advancements Electr. Electron. control Eng.*, 2011, pp. 211–215.

[71] H. Li, T. Q. Zheng, Z. Li, and F. Wang, "EMI suppression for single-phase grid-connected inverter based on chaotic SPWM control," in *Proc Asia-Pacific Symp. Electromagn. Compat.*, 2012, pp. 125–128.

[72] H. Li, Y. Liu, J. Lu, T. Zheng, and X. Yu, "Suppressing emi in power converters via chaotic spwm control based on spectrum analysis approach," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 6128–6137, 2014.

[73] T. Ramanathan, R. Ramesh, C. Subramaniam, and K. Ganesan, "Pseudorandom carrier based subharmonic PWM for cascaded multilevel inverters," in *IEEE Int. Symp. on Circuits and Systems*, 2014, pp. 117–120.

[74] W. R. Liou, H. M. Villaruza, L. Yeh, M, and P. Roblin, "A digitally controlled low-EMI SPWM generation method for inverter applications," *IEEE Trans. Ind. Informatics*, vol. 10, pp. 73–83, 2014.

[75] H. Li, Z. Li, W. A. Halang, and W. K. S. Tang, "A chaotic soft switching PWM Boost converter for EMI reduction," in *IEEE Int. Symp. Industrial Electronics*, 2008, pp. 341–346.

[76] M. R. Yazdani and H. Farzanehfard, "Conducted electromagnetic interference analysis and mitigation using zero-current transition soft switching and spread spectrum techniques," *IET Power Electron.*, vol. 5, no. 7, pp. 1034–1041, 2012.

[77] M. Vilathgamuwa, J. Deng, and K. J. Tseng, "Emi suppression with switching frequency modulated DC-DC converters," *IEEE Ind. Appl. Mag.*, vol. 5, pp. 27–33, 1999.

[78] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 47, pp. 2154–2165, 2011.

[79] A. Nagel and R. W. De Doncker, "Analytical approximations of interference spectra generated by power converters," in *IEEE Ind. Appl. Conf.*, vol. 2, 1997, pp. 1564–1570.

[80] C. R. Paul, *Introduction to Electromagnetic Compatability.* United States of America: Wiley-Interscience John Wiley & Sons, 2006.

[81] S. Walder, X. Yuan, I. Laird, and J. J. O. Dalton, "Identification of the temporal source of frequency domain characteristics of SiC MOSFET based power converter waveforms," in *IEEE Energy Convers. Congr. and Expo.*, Sept 2016, pp. 1–8.

[82] X. Yang, Y. Yuan, X. Zhang, and P. R. Palmer, "Shaping high-power IGBT switching transitions by active voltage control for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1669–1677, March 2015.

[83] X. Yang, Z. Long, Y. Wen, H. Huang, and P. R. Palmer, "Investigation of the trade-off between switching losses and EMI generation in gaussian S-shaping for high-power IGBT switching transients by active voltage control," *IET Power Electron.*, vol. 9, no. 9, pp. 1979–1984, 2016.

[84] M. Blank, T. Glück, A. Kugi, and H. P. Kreuter, "Digital slew rate and S-shape control for smart power switches to reduce EMI generation," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5170–5180, Sept 2015.

[85] A. Charalambous, X. Yuan, N. McNeill, S. Walder, Q. Yan, and C. Frederickson, "Controlling the output voltage frequency response of the auxiliary commutated pole inverter," in *IEEE Ind. Electron. Soc. Conf.*, Oct 2016, pp. 3305–3310.

[86] A. Charalambous, X. Yuan, and N. McNeill, "High-frequency EMI attenuation at source with the auxiliary commutated pole inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5660–5676, 2018.

[87] J. Yang, J. Shi, and T. Cui, "An active voltage controller of SiC MOSFET for reduced EMI generation," in *3rd IEEE Advanced Inf. Technol., Electron. Autom. Control Conf. (IAEAC)*, 2018, pp. 979–983.

[88] T. Cui, Q. Ma, P. Xu, and Y. Wang, "Analysis and optimization of power MOSFETs shaped switching transients for reduced EMI generation," *IEEE Access*, vol. 5, pp. 20 440–20 448, 2017.

[89] P. S. Meyer and J. H. Ausubel, "Carrying capacity: A model with logistically varying limits," *Technological Forecasting and Social Change*, vol. 61, no. 3, pp. 209 – 214, 1999.

[90] N. Oswald,and B. H. Stark, and N. McNeill, and D Holliday, "High-bandwidth, high-fidelity in-circuit measurement of power electronic switching waveforms for emi generation analysis," in *IEEE Energy Conv. Cong. and Expo.*, 2011, pp. 3886–3893.

# Chapter 3

## Spectral Content of Switching Transitions

## 3.1 Introduction

This Chapter provides the theoretical background and spectral content analysis of various hard switching and shaped switching transitions. The progression from hard-switching waveforms, shaped waveforms presented in the literature, and eventually logistic shaped transitions to show the improvements in EMI reduction at high frequencies is presented. Analytical techniques are explored and developed to model the interference spectra generated by DC-DC converter PWM waveforms undergoing logistic shaped switching transitions. Additionally, analytical expressions of various waveform Fourier series are summarised from various literature sources to provide a basis for comparison.

Furthermore, this Chapter summarises the methodology developed to numerically assess the harmonic spectra and identify the ideal switching transition shapes for EMI mitigation. The literature review on shaped switching transitions has identified that infinitely differentiable pulse shapes are best suited for low-EMI applications, typically for high-frequency EMI mitigation. However, not all infinitely differentiable shaped transitions are well suited for low EMI applications, as demonstrated in this Chapter, such as sinusoidal-shaped transitions. As presented in the literature and extended upon in this dissertation, infinitely differentiable Sigmoid functions appear best suited for EMI mitigation as steep spectral content roll-off is observed at high frequencies. Infinitely differentiable pulse shapes, namely the logistic transition, is identified to be best suited for EMI mitigation at the source. One key time-domain characteristic of the logistic function is the growth rate, which produces a steep spectral roll-off essential for high-frequency EMI mitigation. Throughout this dissertation, the growth rate is also interchangeably referred to as the steepness parameter or the k-value. Key EMI performance metrics, which are used to analyse the spectra of various waveforms, is the EMI metric [1], spectral bound (or spectral envelope) and the roll-off of the harmonic spectra.

An overview of the numerical assessment of the spectral content produced by hard-switching and shaped switching transitions, including the Fourier series, EMI metric, spectral bound, and roll-off, is initially presented. Next, the spectral modelling of various shaped switching transitions undergoing typical PWM switching schemes in DC-DC converters is presented. The modelling provides an overview of the temporal characteristics and analytical Fourier series of all hard-switching and shaped switching transitions considered for comparison, including the logistic-shaped transition. Lastly, numerical spectral comparison of hard-switching and shaped switching transitions, including the harmonic spectra, EMI metric, spectral bound, and roll-off, is presented.

## 3.2 Numerical Assessment of Shaped Switching Transitions

### 3.2.1 Fourier Series Techniques

The Fourier series coefficients in the complex form is given by:

$$C_n = \frac{1}{T}\int_0^T f(t)\mathrm{e}^{-i2\pi nt/T}dt \tag{3.1}$$

Where, $f(t)$ is the switching waveform over the interval $[0,T]$. The amplitude of spectral content is determined by taking the magnitude of $C_n$. Conversion to dB$\mu$V, is performed as follows:

$$C_{n(dB\mu V)} = 20\log_{10}|C_n| + 120 \tag{3.2}$$

The waveforms analysed in this section can be categorised into either finitely differentiable or infinitely differentiable, which determined the analytical Fourier series method adopted to derive the harmonic contribution of the waveform. Firstly, the approach to determine the analytical Fourier series of a finitely differential waveform is discussed. If the n-th derivative of the switching waveform is expressed as a pulse train, then specific properties of the Fourier series can be utilized to determine the spectral content of the waveform [2]. For example, the second derivative of the trapezoidal shaped switching waveform and the third derivative of the S-shaped switching waveform produce pulse trains. The Fourier series properties considered include the impulse function, linearity, time-scaling, and differentiation. The Fourier series of a time-shifted impulse function is given by:

$$C_n = \frac{1}{T}\int_{-T/2}^{T/2}\delta(t-\tau)e^{-j2n\pi ft}dt = \frac{1}{T}e^{-2jn\pi f\tau} \tag{3.3}$$

The differentiation property of the Fourier series is given by:

$$\frac{d^{(k)}f(t)}{dt^{(k)}} = \sum_{n=-\infty}^{\infty}(j2n\pi f)^k c_n e^{2jn\pi ft} \tag{3.4}$$

The first step to determine the analytical Fourier series of a finitely differentiable waveform is to continue differentiating until a pulse train is produced. Following which, the Fourier series of pulse train can be calculated with the time-shifting, linearity, and impulse properties of the Fourier series. For the best outcome considering low-EMI, the waveform should be symmetrical, which will allow for the Fourier series of the pulse train to be simplified. After the expression is simplified, the differentiation property is used to compute the Fourier series of the waveform. Section 3.3.1 and Section 3.3.2

present an example for a hard-switching square wave and a trapezoidal waveform, respectively.

Lastly, the approach to determine the analytical Fourier series of an infinitely differentiable shaped transition is presented, which is derived for this dissertation. The methodology utilizes the piecewise representation of the waveform presented in this Section. Note that care must be taken when defining the shaped transition to ensure the piecewise representation of the waveform remains continuous, which is necessary for EMI mitigation. In this case, the linearity and time-shifting properties are applied to the piecewise representation of the waveform to determine the analytical Fourier series. The piecewise representation of a switching waveform with an arbitrarily shaped switching transition $r(t)$, is expressed as:

$$\begin{aligned} f(t) &= r(t), && 0 \leq t < \tau_t \\ f(t) &= A, && \tau_t \leq t < \tau \\ f(t) &= A - r(t-\tau), && \tau \leq t < \tau + \tau_t \\ f(t) &= 0, && \tau + \tau_t \leq t < T \end{aligned} \tag{3.5}$$

Where $\tau$ is the pulse-width, $T$ is the waveform period, and $\tau_t$ is the waveform transition time. For a piecewise function, consisting of an arbitrarily shaped function $r(t)$, during each transition, the Fourier series of each piecewise function is expressed as:

$$\begin{aligned} A(t) &= \frac{1}{T}\int_0^{\tau_t} r(t)\mathrm{e}^{-i2\pi nt/T}dt \\ B(t) &= \frac{1}{T}\int_{\tau_t}^{\tau} A\mathrm{e}^{-i2\pi nt/T}dt \\ C(t) &= \frac{1}{T}\int_{\tau}^{\tau+\tau_t} (A - r(t-\tau))\,\mathrm{e}^{-i2\pi nt/T}dt \\ D(t) &= \frac{1}{T}\int_{\tau+\tau_t}^{T} 0\mathrm{e}^{-i2\pi nt/T}dt \end{aligned} \tag{3.6}$$

The total expression is given by:

$$\begin{aligned} S(t) &= A(t) + B(t) + C(t) + D(t) \\ &= \frac{1}{T}\int_0^{\tau_t} r(t)\mathrm{e}^{-i2\pi nt/T}dt + \frac{1}{T}\int_{\tau_t}^{\tau} A\mathrm{e}^{-i2\pi nt/T}dt \\ &+ \frac{1}{T}\int_{\tau}^{\tau+\tau_t} A\mathrm{e}^{-i2\pi nt/T}dt - \frac{1}{T}\int_{\tau}^{\tau+\tau_t} r(t-\tau)\mathrm{e}^{-i2\pi nt/T}dt \end{aligned} \tag{3.7}$$

The time-shifting and linearity properties can be applied to each individual term in the Fourier series expression. Note that $D(t)$ is $A(t)$, which has been y-axis inverted and time-shifted. Therefore the Fourier series properties can be applied such that:

$$D(t) = -\mathrm{e}^{-i2\pi\tau/T}A(t) \tag{3.8}$$

Additionally, $B(t)$ and $C(t)$ can be combined since they are both integrals of the amplitude, $A$:

$$\begin{aligned} B(t)+C(t) &= \frac{1}{T}\int_{\tau_t}^{\tau} A\mathrm{e}^{-i2\pi nt/T}dt + \frac{1}{T}\int_{\tau}^{\tau+\tau_t} A\mathrm{e}^{-i2\pi nt/T}dt \\ &= \frac{1}{T}\int_{\tau_t}^{\tau+\tau_t} A\mathrm{e}^{-i2\pi nt/T} \end{aligned} \tag{3.9}$$

Similarly, the time-shifting property can be applied to $B(t)+C(t)$:

$$\begin{aligned} \frac{1}{T}\int_{\tau_t}^{\tau+\tau_t} (B(t)+C(t))\,dt &= \frac{1}{T}\int_{\tau_t}^{\tau+\tau_t} A\mathrm{e}^{-i2\pi nt/T}dt \\ &= \mathrm{e}^{-i2\pi\tau_t/T}\frac{1}{T}\int_{0}^{\tau} A\mathrm{e}^{-i2\pi nt/T}dt \end{aligned} \tag{3.10}$$

The result is defined as $E(t)$:

$$E(t) = \frac{1}{T}\int_{0}^{\tau} A\mathrm{e}^{-i2\pi nt/T}dt \tag{3.11}$$

Therefore, the simplified representation of $C_n$ becomes:

$$C_n = \left(1-\mathrm{e}^{-i2\pi\tau/T}\right)A(t) + \mathrm{e}^{-i2\pi\tau_t/T}E(t) \tag{3.12}$$

Where:

$$\begin{aligned} A(t) &= \frac{1}{T}\int_{0}^{\tau_t} r(t)\mathrm{e}^{-i2\pi nt/T}dt \\ E(t) &= \frac{1}{T}\int_{0}^{\tau} A\mathrm{e}^{-i2\pi nt/T}dt \end{aligned} \tag{3.13}$$

Therefore, the analytical Fourier series representation of the piecewise arbitrarily shaped switching transition is expressed as two terms: the shaped function, $r(t)$, and amplitude terms. An example of this approach is presented in Section 3.3.4 and Section 3.3.5.

Additionally, a discrete Fourier transform (DFT) can be utilised if the waveform synthesis is discretised with equally spaced time-steps and a sufficient sampling rate to compute the spectral content at the upper-frequency limit. In MATLAB, the DFT is computed using the fast Fourier transform (FFT) algorithm.

### 3.2.2 EMI Metric for Harmonic Spectra Comparison

The EMI metric originally defined in [1] is adopted to assess the harmonic spectra of numerous shaped pulse transitions. The EMI metric calculates the total power dissipated in a 50 Ω impedance for a given frequency range, or equivalently, harmonic numbers. The total power dissipation is calculated using the following equation:

$$P_{tot} = \sum_{i=n_1}^{n_2} \frac{|V_i|^2}{R}$$
$$n_1 = \frac{f_1}{f_c},\ n_2 = \frac{f_2}{f_c} \tag{3.14}$$

Where $V_i$ is the harmonic voltage, $R$ is 50Ω, and $f_c$ is the switching frequency. The frequency range over which the total dissipated power is calculated is set by $f_1$ and $f_2$. Note that the EMI metric depends on the selected bandwidth and, therefore, can be used for particular applications if required. For instance, the frequency ranges used in this analysis align with the frequency range of the SKA-low.

### 3.2.3 Spectral Bounds and Roll-Off

In addition to calculating the harmonic spectra and EMI metric, spectral bounds and roll-off of the shaped transitions offers a more in-depth and comprehensive comparison between shaped transitions when considering EMI. The peak envelope of the spectral content is determined to ascertain the spectral bound of the harmonic spectra. The signal envelope in MATLAB is used to determine the peak envelope. The signal roll-off of the spectral bound is determined by:

$$\Delta R = \frac{A_2 - A_1}{\log\left(\frac{f_2}{f_1}\right)} \tag{3.15}$$

Where $A_1$ and $A_2$ are subsequent spectral bound amplitudes, which occur at $f_1$ and $f_2$, respectively. Note, the frequency points $f_1$ and $f_2$ differ from the frequencies defined in Equation 3.14.

## 3.3 Spectral Modelling of DC-DC Converter Switching Transitions

This section provides the theoretical background and spectral content analysis of various hard switching and shaped switching transitions. A progression from hard-switching waveforms, shaped waveforms presented in the literature, and eventually logistic shaped transitions to demonstrate EMI mitigation improvements, particularly at high frequencies, is presented. Analytical techniques are explored and developed to model the interference spectra generated by DC-DC converter PWM waveforms. Where possible, analytical expressions of various waveform Fourier series are presented and provide a basis for comparison.

### 3.3.1 Hard Switching Harmonic Spectra Approximations of Switching Transitions

In DC-DC converter applications, the commonly used PWM waveform is the asymmetric square wave. An example of the square wave with a 50% duty cycle, $d$, is shown in Figure 3.1.

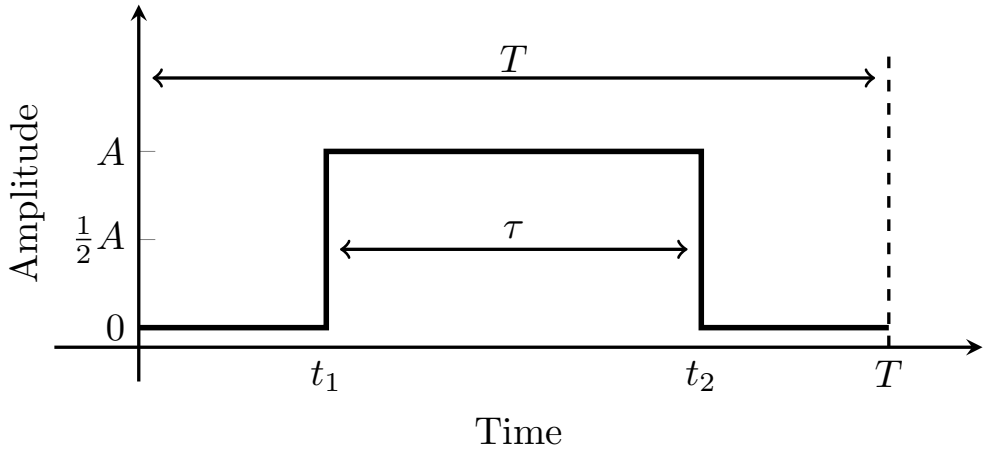



Figure 3.1: Square waveform.

Since the first derivative of the square wave is two impulse functions, the Fourier series of the derivative of the square wave is the sum of both impulses. The first impulse occurs at $t = 0$ with amplitude $A$, and the second impulse occurs at $t = \tau$ with amplitude $-A$, therefore:

$$c_n^{(1)} = A\frac{1}{T} - A\frac{1}{T}\mathrm{e}^{-jn\omega_0\tau} = jn\omega_0\frac{A\tau}{T}\frac{\sin\left(\frac{1}{2}n\omega_0\tau\right)}{\frac{1}{2}n\omega_0\tau}\mathrm{e}^{\frac{-jn\omega_0\tau}{2}} \tag{3.16}$$

Applying the differentiation property of the Fourier series, $c_n = \frac{1}{jn\omega_0}c_n^{(1)}$ , the magnitude spectrum becomes:

$$C_n = \frac{A\tau}{T}\frac{\sin\left(\frac{1}{2}n\omega_0\tau\right)}{\frac{1}{2}n\omega_0\tau}\mathrm{e}^{\frac{-jn\omega_0\tau}{2}} \tag{3.17}$$

Where A is the signal amplitude, $\tau$ is the pulse-width, $T$ is the waveform period, $\omega_0$ is the fundamental angular frequency, and $n$ is the harmonic number. The harmonic spectrum of an example square wave is provided in Figure 3.2. The waveform is synthesized using the following parameters: $f_c = 10$ kHz, $A = 1$ V, $d = 50\%$. The harmonic spectrum of a trapezoidal, sinusoidal, logistic and S-shaped transitions are presented in the remainder of this sub-section. Following this, the spectral content of the various shaped transitions are compared in Section 3.4.2 and Section 3.4.3.

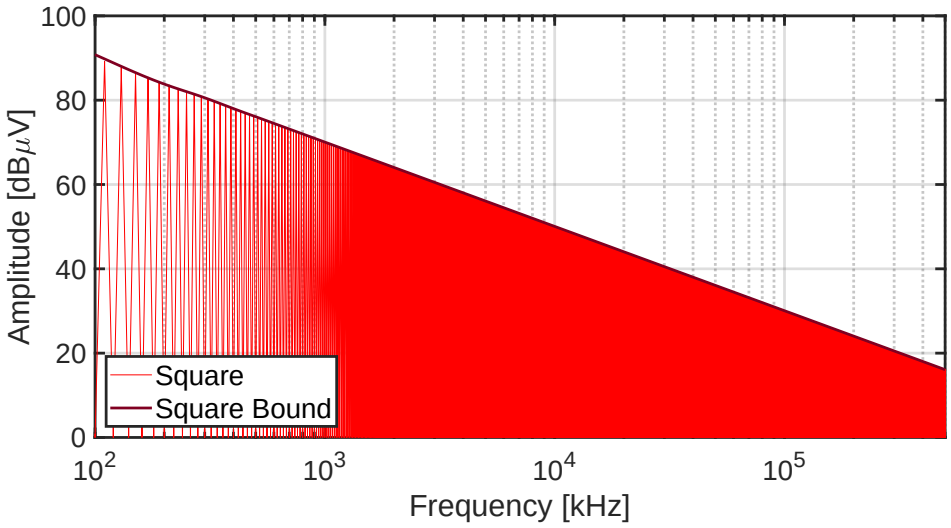



Figure 3.2: Harmonic spectra and spectral bound of a square waveform.

### 3.3.2 Trapezoidal Switching Transitions

When considering the realistic behaviour of switching transitions, slew rates can be considered. The slew rates approximate transient behaviour of switching transitions, where the resultant behaviour is trapezoidal. Moreover, the trapezoidal waveforms are used to reduce EMI, where the switching transition time is controlled to reduce unwanted EMI [3]. For hard-switched DC-DC converters, the transition time of the waveform is short relative to a controlled trapezoidal-shaped switching transition. An example of a trapezoidal waveform is shown in Figure 3.3.

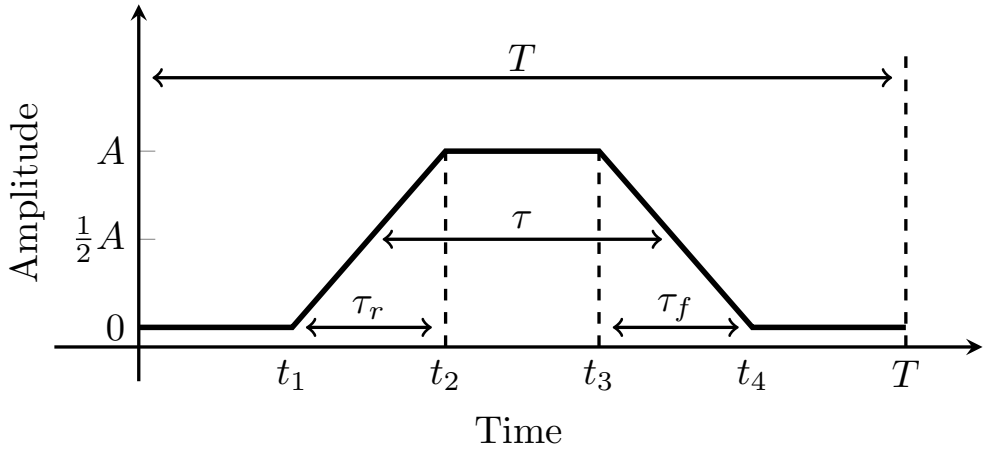



Figure 3.3: Trapezoidal waveform.

The remainder of this section provides an example of the calculation approach for the trapezoidal pulse train with a unique rise ($\tau_r$) and fall time ($\tau_f$). The second derivative can be expressed as a series of impulses, therefore:

$$c_n^{(2)} = \frac{1}{T}\frac{A}{\tau_r} - \frac{1}{T}\frac{A}{\tau_r}e^{-jn\omega_0\tau_r} - \frac{1}{T}\frac{A}{\tau_f}e^{-jn\omega_0[\tau+(\tau_r-\tau_f)/2]} + \frac{1}{T}\frac{A}{\tau_f}e^{-jn\omega_0[\tau+(\tau_r+\tau_f)/2]} \tag{3.18}$$

By considering Euler's equation:

$$\begin{aligned} e^{j\theta} &= \cos\theta + j\sin\theta \\ e^{-j\theta} &= \cos\theta - j\sin\theta \\ e^{j\theta} - e^{-j\theta} &= (\cos\theta + j\sin\theta) - (\cos\theta - j\sin\theta) = 2j\sin\theta \end{aligned} \tag{3.19}$$

The expressions can be simplified and expressed in terms of $\mathrm{sinc}(x)$ functions:

$$c_n^{(2)} = j\frac{A}{\pi n}(n\omega_0)^2 e^{-jn\omega_0\tau_r/2}e^{-jn\omega_0\tau/2}\left(\mathrm{sinc}\left(\frac{1}{2}n\omega_0\tau_r\right)e^{jn\omega_0\tau/2} - \mathrm{sinc}\left(\frac{1}{2}n\omega_0\tau_f\right)e^{-jn\omega_0\tau/2}\right) \tag{3.20}$$

Applying the Fourier series differentiation property, the impulse train can be transformed to the Fourier series of the trapezoidal switching waveform. Recalling:

$$c_n = \frac{1}{(jn\omega_0)^2}c_n^{(2)} = -\frac{c_n^{(2)}}{(jn\omega_0)^2} \tag{3.21}$$

Therefore:

$$c_n = -j\frac{A}{\pi n}e^{-jn\omega_0\tau_r/2}e^{-jn\omega_0\tau/2}\left(\mathrm{sinc}\left(\frac{1}{2}n\omega_0\tau_r\right)e^{jn\omega_0\tau/2} - \mathrm{sinc}\left(\frac{1}{2}n\omega_0\tau_f\right)e^{-jn\omega_0\tau/2}\right) \tag{3.22}$$

Considering the magnitude spectrum of the Fourier Series and re-calling that $|e^{i\theta}| = 1$:

$$c_n = \left|\frac{A}{\pi n}\right|\left|\left(\mathrm{sinc}\left(\frac{1}{2}n\omega_0\tau_r\right)e^{jn\omega_0\tau/2} - \mathrm{sinc}\left(\frac{1}{2}n\omega_0\tau_f\right)e^{-jn\omega_0\tau/2}\right)\right| \tag{3.23}$$

Where A is the signal amplitude, $\tau$ is the pulse-width, $T$ is the waveform period, $\omega_0$ is the fundamental angular frequency, and $n$ is the harmonic number. The harmonic spectrum of an example trapezoidal waveform is provided in Figure 3.4. The waveform is synthesized using the following parameters: $f_c = 10$ kHz, $A = 1$ V, $d = 50\%$, $\tau_r = \tau_f = \tau_t = 5$ $\mu$s.

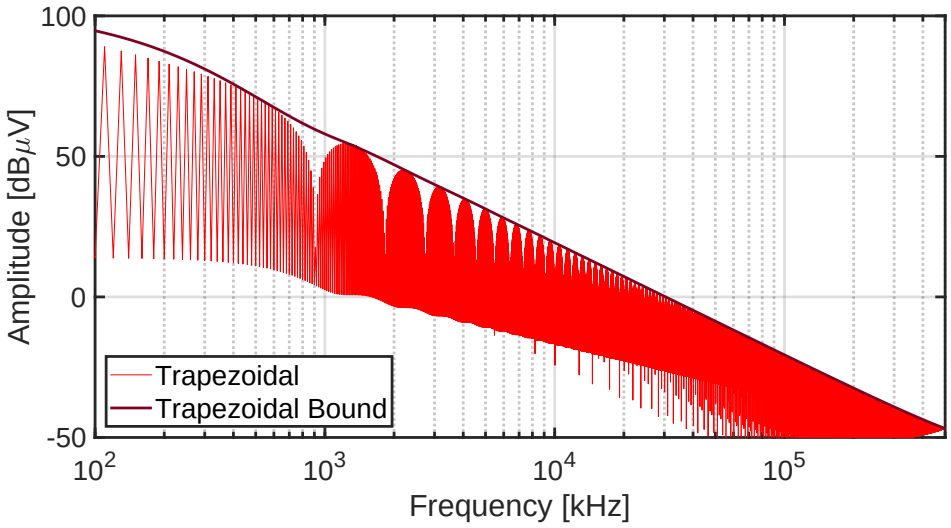



Figure 3.4: Harmonic spectra and spectral bound of a trapezoidal waveform.

### 3.3.3 S-Shaped Switching Transitions

S-shaped pulse transitions can be derived analytically since the waveform is finitely differentiable and can be represented mathematically as a pulse train. Properties of the Fourier series can be applied to derive the analytical Fourier series of the S-shaped waveform, including linearity, time-shifting, and differentiation. An example of an S-shaped waveform is shown in Figure 3.5.

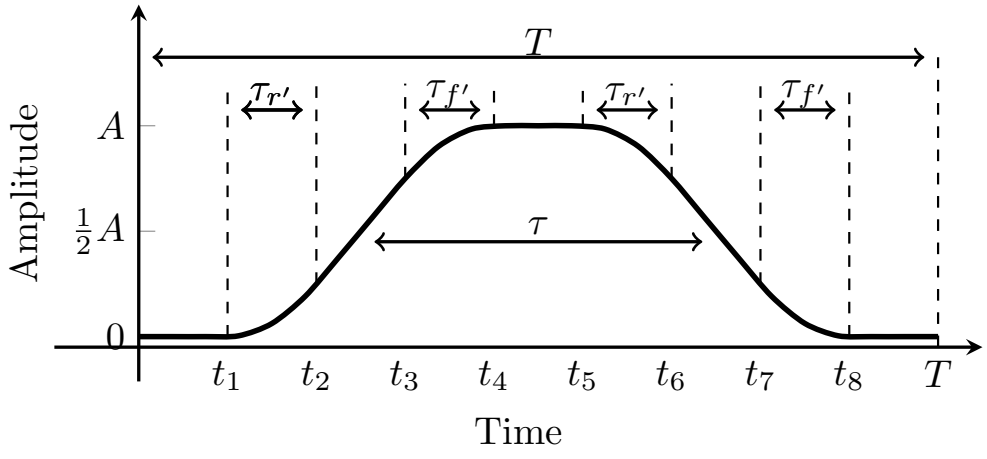



Figure 3.5: S-shaped waveform.

Since the third derivative of the S-shaped waveform consists of eight time-shifted impulses, the analytical Fourier series for the S-shaped, as provided in [1] is given as:

$$c_n = A\frac{\tau}{T}\text{sinc}\left(n\omega_0\frac{\tau}{2}\right)\text{sinc}\left(n\omega_0\frac{\tau_r - \tau_{r(dv/dt)}}{2}\right)\text{sinc}\left(n\omega_0\frac{\tau_{r(dv/dt)}}{2}\right)\left(e^{jn\omega_0\frac{\tau_r+\tau_{r(dv/dt)}}{2}}\right) \tag{3.24}$$

Where A is the signal amplitude, $\tau$ is the pulse-width, $T$ is the waveform period, $\omega_0$ is the fundamental angular frequency, $\tau_r$ is the waveform rise time, $\tau_{r(dv/dt)}$ is the derivative rise-time, and $\text{sinc}(x)$ denotes $\sin(x)/x$. Note that the Fourier series assumes symmetry therefore therefore $\tau_r = \tau_f$ and $\tau_{r(dv/dt)} = \tau_{f(dv/dt)}$.

Similarly, higher-order shaped transitions that are finitely differentiable to yield a pulse train can also be analytically represented in this manner [4]. Only S-shaped waveforms are included in this dissertations as a point of comparison to a sample of infinitely differentiable waveforms such as the sinusoidal waveforms, which represents soft-switching power converter waveforms and logistic-shaped transitions. The logistic waveforms significantly improves EMI mitigation and spectral content roll-off compared to S-shaped transitions and soft-switching waveforms. Additionally, logistic shaped transitions are comparable to Gaussian-shaped transitions presented in the literature.

The harmonic spectrum of an example S-shaped waveform is provided in Figure 3.6. The waveform is synthesized using the following parameters: $f_c = 10$ kHz, $A = 1$ V, $d = 50\%$, $\tau_t = 5$ $\mu$s.

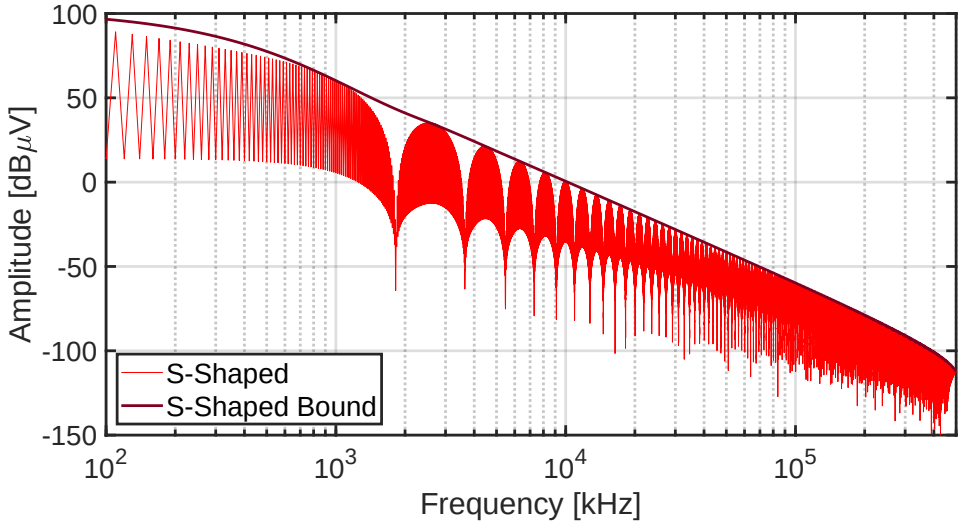



Figure 3.6: Harmonic spectra and spectral bound of a S-shaped waveform.

### 3.3.4 Sinusoidal Switching Transitions

Sinusoidal-shaped switching transitions are included in this thesis for two major reasons. Firstly, they are representative of soft-switching resonant waveforms. Secondly, they demonstrate a class of infinitely differentiable waveforms that are not adequate for high-frequency EMI mitigation. Although a sinusoidal-shaped waveform is infinitely differentiable, the temporal characteristics are like an S-shaped waveform (see Figure 3.5) and, therefore, does not provide additional EMI attenuation. An example of a Sinusoidal-shaped waveform is shown in Figure 3.7.

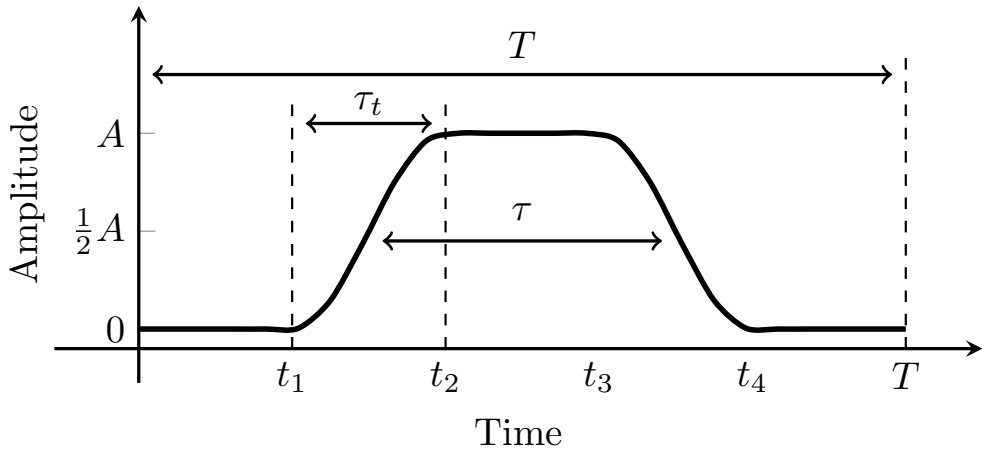



Figure 3.7: Sinusoidal-shaped waveform.

Since the waveform is infinitely differentiable, the method to determine magnitude spectrum is given by Eq. 3.12 and Eq. 3.13. The equation for a sinusoidal shaped transitions is given by:

$$r(t) = \frac{1}{2}A\left(1 - \sin\left(\frac{\pi}{\tau_t}t - \frac{\pi}{2}\right)\right) \tag{3.25}$$

The complete Fourier series expression is therefore:

$$\begin{aligned} S(t) = \left(1 - \mathrm{e}^{\left(-\frac{i2\pi n\tau}{T}\right)}\right)\frac{1}{T}\int_0^{\tau_t}\left(\frac{1}{2}A - \frac{1}{2}A\sin\left(\frac{\pi}{\tau_t}t - \frac{\pi}{2}\right)\right)\mathrm{e}^{\left(-\frac{i2\pi nt}{T}\right)}dt \\ + \frac{1}{T}\int_0^{\tau} A\mathrm{e}^{\left(-\frac{i2\pi nt}{T}\right)}dt \end{aligned} \tag{3.26}$$

Solving for $A(t)$:

$$A(t) = \frac{A}{2T}\left[\frac{iT\mathrm{e}^{\frac{-i2\pi nt}{T}}}{2\pi n}\bigg|_0^{\tau_t} + \frac{\mathrm{e}^{\frac{-i2\pi nt}{T}}\left(\frac{\pi}{\tau_t}\cos\left(\frac{\pi}{2} - \frac{\pi}{\tau_t}t\right) - i\frac{2\pi n}{T}\sin\left(\frac{\pi}{2} - \frac{\pi}{\tau_t}t\right)\right)}{\left(\frac{\pi}{\tau_t} - \frac{2\pi n}{T}\right)\left(\frac{\pi}{\tau_t} + \frac{2\pi n}{T}\right)}\bigg|_0^{\tau_t}\right] \tag{3.27}$$

Solving for $E(t)$:

$$E(t) = \frac{iA}{2\pi n} \mathrm{e}^{\frac{-i2\pi nt}{T}} \Big|_0^{\tau} \tag{3.28}$$

The harmonic spectrum of an example sinusoidal-shaped waveform is provided in Figure 3.8. The waveform is synthesized using the following parameters: $f_c$ = 10 kHz, $A$ = 1 V, $d$ = 50%, $\tau_t$ = 5 $\mu$s.

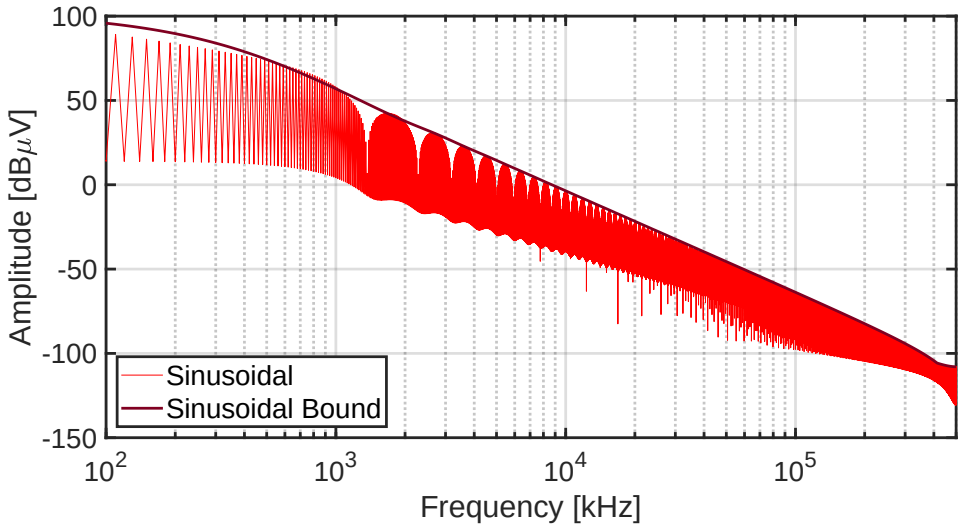



Figure 3.8: Harmonic spectra and spectral bound of a Sinusoidal-shaped waveform.

### 3.3.5 Logistic Transition to Mitigate High Frequency Harmonics

The following equation defines the generalised logistic function:

$$f(t) = W + \frac{L - W}{\left(C + Qe^{-k(t-t_0)}\right)^{1/\nu}} \tag{3.29}$$

Where $W$ is the value of the lower asymptote, $L$ is the value of the upper asymptote, $k$ is the steepness parameter or growth-rate, $t_0$ is the time the logistic function reaches the mid-point of the function, $C$ is typically a value of 1, $Q$ is related to f(0), and $\nu$ impacts the point where maximum growth occurs. The growth rate, $k$, of the logistic function is a key temporal characteristic for EMI mitigation. Appropriate selection of the growth-rate can achieve the desired spectral roll-off. Additionally, symmetrical waveforms are desirable for low-EMI, therefore $C$, $Q$ and $\nu$ take the value of 1. Additionally, $t_0$ is defined as half the transition time $\tau_t/2$. The simplified logistic equation is therefore:

$$f(t) = W + \frac{L - W}{1 + e^{-k(t-\tau_t/2)}} \tag{3.30}$$

The upper and lower asymptotes of the logistic function must be determined from initial conditions to circumvent discontinuities in the switching waveform. The logistic function must be zero at the start of the transition and reach the waveform amplitude, $A$, at the end of the transition considering a waveform undergoing a rising transition. Therefore, the logistic transition must reach equate to $f(t) = 0$ V and $f(\tau_t) = $ A V, which is determined by equating the upper and lower asymptotes of the waveform from initial conditions. By making the substitutions of $\alpha = 1 + e^{-\frac{k\tau_t}{2}}$, $\beta = 1 + e^{\frac{k\tau_t}{2}}$, the asymptotes,$W$ and $L$, can be solved for:

$$L = \frac{\alpha A(\beta - 1)}{\beta - \alpha} \tag{3.31}$$

$$W = -\frac{\alpha A}{\beta - \alpha} \tag{3.32}$$

Substituting and simplifying gives:

$$f(t) = \frac{\alpha A}{\beta - \alpha}\left[\frac{\beta}{\left(1 + e^{-k(t-\tau_r/2)}\right)} - 1\right] \tag{3.33}$$

The falling transition is similar to the rising transition, except the logistic shaped transition is reflected about the y-axis. Therefore, the expression for the falling logistic-shaped transition is:

$$f(t) = \frac{\alpha A}{\beta - \alpha}\left[\frac{\beta}{1 + e^{k(t-\tau_r/2)}} - 1\right] \tag{3.34}$$

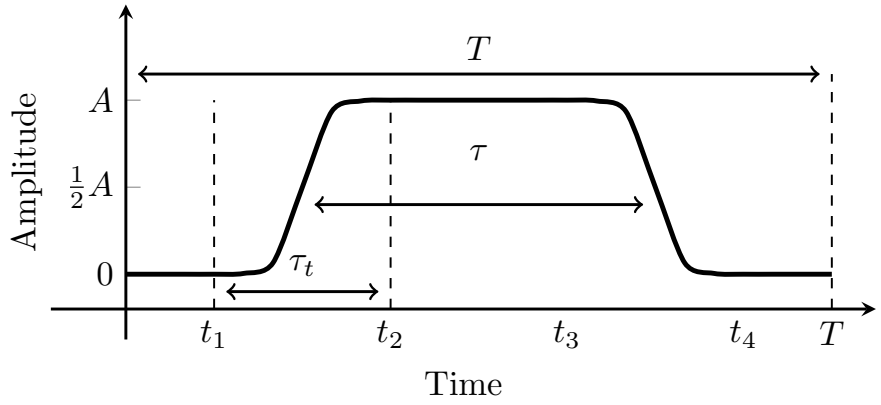



Figure 3.9: Logistic-shaped waveform.

An example of a logistic shaped switching waveform is shown in Figure 3.9. Since the waveform is infinitely differentiable, the method to determine the magnitude spectrum is as follows. Considering $r(t)$ as a logistic equation:

$$r(t) = \frac{\alpha A}{\beta - \alpha}\left[\frac{\beta}{1+\mathrm{e}^{-k(t-\tau_t/2)}} - 1\right] \tag{3.35}$$

$A(t)$ and $E(t)$ are therefore given by:

$$\begin{aligned} A(t) &= \frac{A\alpha}{T(\beta-\alpha)}\int_0^{\tau_t}\left[\frac{\beta}{1+\mathrm{e}^{-k(t-\tau_t/2)}} - 1\right]\mathrm{e}^{-i2\pi nt/T}dt \\ E(t) &= \frac{A}{T}\int_0^{\tau_i} A\mathrm{e}^{-i2\pi t/T} \end{aligned} \tag{3.36}$$

Firstly, re-writing $A(t)$ gives:

$$A(t) = \frac{A\alpha}{T(\beta-\alpha)}\left[\int_0^{\tau_t}\frac{\beta\mathrm{e}^{-i2\pi nt/T}}{1+\mathrm{e}^{-k(t-\tau_t/2)}}dt - \int_0^{\tau_t}\mathrm{e}^{-i2\pi nt/T}dt\right] \tag{3.37}$$

Solving for the integral terms only, the terms inside the square brackets become:

$$\frac{-i\beta T\mathrm{e}^{-i2\pi nt/T}}{2\pi n}\left[-1 + {}_2F_1\left(\left[1, \frac{i2\pi n/T}{k}\right]; 1 - \frac{i2\pi n/T}{k}; -\mathrm{e}^{k(t-\tau_t/2)}\right)\right]\Bigg|_0^{\tau_t} - \frac{iT\mathrm{e}^{-i2\pi nt/T}}{2\pi n}\Bigg|_0^{\tau_t} \tag{3.38}$$

Where ${}_2F_1\left(\left[1, 1-\frac{i2\pi n}{kT}\right]; 2-\frac{i2\pi n}{kT}; -\mathrm{e}^{k(t-\tau_t/2)}\right)$ is a hyper-geometric series. Similarly, $E(t)$ can be solved for the integral limits:

$$E(t) = \frac{A}{T}\int_0^{\tau_i} A\mathrm{e}^{-i2\pi nt/T} = \frac{A}{T}\frac{iT\mathrm{e}^{-i2\pi nt/T}}{2\pi}\Bigg|_0^{\tau_i} \tag{3.39}$$

Therefore, expressions for $A(t)$ and $E(t)$ are given as:

$$\begin{aligned} A(t) = -\frac{iA\alpha}{2\pi n(\beta-\alpha)}\Bigg(&\beta\mathrm{e}^{-i2\pi nt/T}\left[-1 + {}_2F_1\left(\left[1, \frac{i2\pi n/T}{k}\right]; 1 - \frac{i2\pi n/T}{k}; -\mathrm{e}^{k(t-\tau_t/2)}\right)\right]\Bigg|_0^{\tau_t} \\ &- \mathrm{e}^{-i2\pi nt/T}\Bigg|_0^{\tau_t}\Bigg) \\ E(t) = \frac{iA}{2\pi n}&\mathrm{e}^{-i2\pi nt/T}\Bigg|_0^{\tau_i} \end{aligned} \tag{3.40}$$

The harmonic spectrum of an example logistic-shaped waveform is provided in Figure 3.10. The waveform is synthesized using the following parameters: $f_c = 10$ kHz, $A = 1$ V, $d = 50\%$, $\tau_t = 5$ $\mu$s.

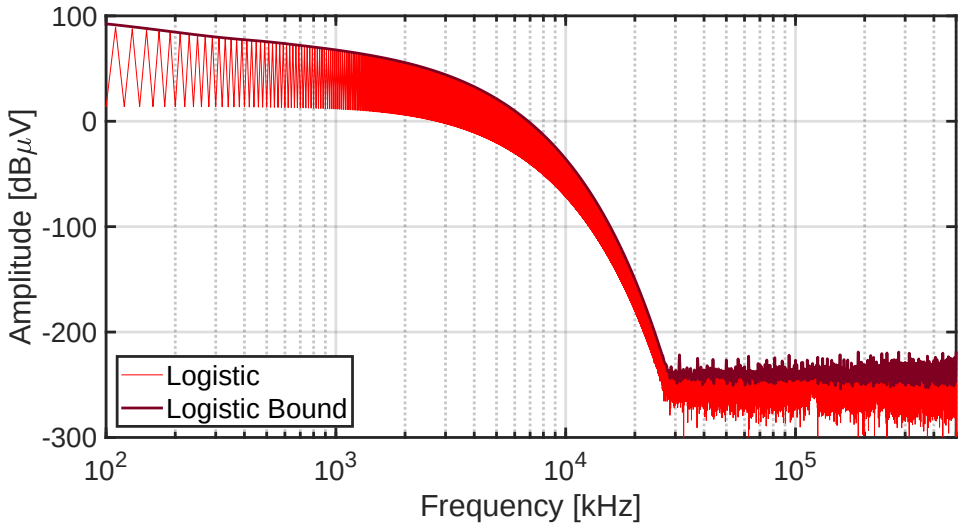



Figure 3.10: Harmonic spectra and spectral bound of a logistic-shaped waveform.

When considering the logistic waveform, one observable characteristic is the steep roll-off that can be achieved with appropriately selected growth rates. The growth rate parameter, when varied, creates a noticeable difference in spectral characteristics. The roll-off will peak for a particular k-value that is influenced by the transition time and amplitude of the waveform. The roll-off is not steep for low k-values as the waveform becomes more comparable to S-shaped transitions or even trapezoidal shaped transitions if the k-value is low enough. Higher k-values are not favourable for EMI-mitigation as the $dv/dt$ in the logistic region increases and closely resembles a square wave. Selecting the right k-value will ensure the best roll-off and high-frequency spectral content mitigation is achieved.

Lastly, higher k-values increases the low-frequency EMI and causes the steep roll-off to occurs at higher frequencies. Increasing low-frequency content is not desirable as the total harmonic distortion is increased, which is a power quality issue that needs to be addressed. Therefore the growth-rate must be suitably selected considering both low and high-frequency impacts. The effects of the growth-rate on the spectral content of logistic shaped transitions is presented in Section 3.4.3.

## 3.4 Comparing the EMI of Shaped Switching Transitions

### 3.4.1 Modelling Methodology Overview

This section outlines the computational modelling approach that was developed to compare the harmonic content of various-shaped transitions. The modelling approach

demonstrates the capability of a logistic-shaped transition to mitigate EMI and achieve steep spectral roll-off. The intended outcome of the modelling approach is to recommend typical waveform shapes that mitigate EMI and is properly-suited for the SKA-low radio telescope. The modelling performed is aligned with the half-bridge switch leg circuit design, which considers transition times and capacitor sizes intended to be implemented in the prototype development. Previous modelling studies presented in the literature on shaped transitions identified that infinitely differentiable switching transitions are best suited EMI mitigation, typically at high frequencies due to well suited temporal characteristics.

An outline of the modelling methodology developed to compare the spectral content of numerous shaped transitions is presented. Shaped transitions are synthesised and analysed using comparable transitions times, waveform amplitudes, and switching frequencies. The computational study allows for a comparison of different shaped waveforms such as the trapezoidal, sinusoidal, S-shaped, and logistic shaped switching transitions. Additionally, the analysis allows temporal characteristics, such as the growth rate of the logistic waveform, to be studied to ascertain the best EMI attenuation considering the SKA-low.

A MATLAB script has been developed, which computes the harmonic spectra, spectral bound, roll-off and EMI metric of a shaped transition. Firstly, all modelling parameters are defined, which includes all common time and frequency domain modelling parameters such as switching frequency, waveform duty cycle, maximum harmonic frequency, waveform amplitude and transition time. Additionally, shaped transition specific parameters such as the logistic growth rate the S-shaped derivative transition times are also defined. The rise and fall transitions are calculated and combined into a single PWM waveform following the initialisation of the computational script. Lastly, the harmonic spectra for each transition are computed, then the EMI metric, spectral bound and roll-off are calculated. All modelling results are provided in the following section for comparison. A complete overview of the modelling approach is provided as follows:

- Set-up all modelling parameters
- Synthesise all shaped waveforms for a given switching frequency and duty cycle
- Compute the harmonic spectra for each waveform
- Determine the spectral bound and compute the roll-off for each transition
- Calculate the EMI metric for each predefined frequency range

### 3.4.2 Spectral Comparison of Shaped Switching Transitions

The synthesis of an S-shaped waveform is described in [1], where the third derivative of the waveform can be represented as a pulse train, which provides the basis for deriving the Fourier series. The study utilised time-shifting and the derivative properties of the Fourier series [2] to ascertain the spectral content of an S-shaped waveform. Additionally, the S-shaped function can be determined by continually integrating the third-derivative pulse train until the function is provided. Alternatively, the Fourier series is dependent on the transition times of the S-shaped waveform and the transition times of the derivative of the waveform. The trapezoidal, sinusoidal and S-shaped transitions are shown in Figure 3.11, as depicted by the black, red, and blue traces, respectively. For representation, the transition times are exaggerated to demonstrate the waveform shaping.

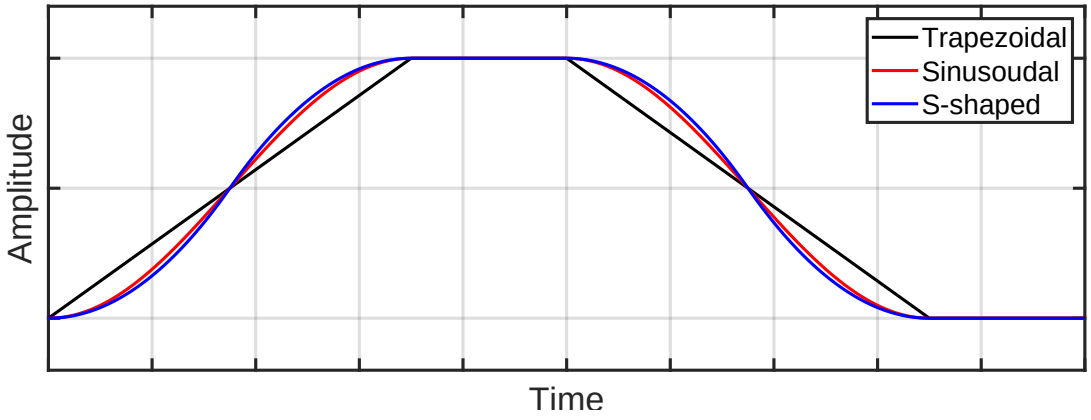



Figure 3.11: Time-domain waveform synthesis of trapezoidal- sinusoidal- and S-shaped transitions.

A spectral comparison between the square wave, trapezoidal, sinusoidal, and S-shaped switching transitions is presented in Figure 3.12. Each transition is synthesised using the following parameters: $f_c$ = 10 kHz, $A$ =1 V, $d$ = 50%, $\tau_t$ = 5 $\mu$s. For each waveform plotted, the EMI metric from 100 kHz-1 MHz, 1-30 MHz, 30-500 MHz, and the SKA-low frequency range of 50-350 MHz is presented in Table 3.1. Additionally, the minimum amplitude and corresponding frequency and maximum spectral roll-off and corresponding frequency is resented in Table 3.2.

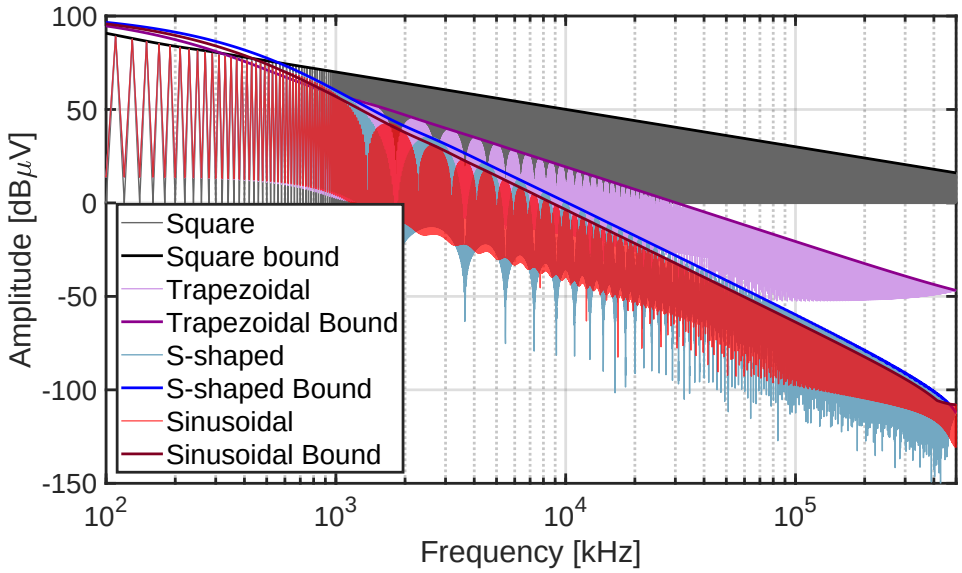



Figure 3.12: Spectral comparison between the square wave, trapezoidal, sinusoidal, and S-shaped transitions. The spectral bound of each switching transitions is also shown.

Table 3.1: EMI Metric and of the square, trapezoidal, sinusoidal, logistic and S-shaped transitions for various frequency bands.

| | **0.1-1 MHz** | **1-30 MHz** | **30-500 MHz** | **50-350 MHz** |
|---|---|---|---|---|
| **Unit** | dBm | dBm | dBm | dBm |
| **Square** | -10.42 | -20.09 | -34.98 | -37.60 |
| **Trapezoidal** | -11.66 | -38.27 | -82.74 | -89.29 |
| **S-shaped** | -11.12 | -38.59 | -114.46 | -125.63 |
| **Sinusoidal** | -11.21 | -41.90 | -117.38 | -128.48 |
| **Logistic** | -10.65 | -26.84 | -306.78 | -308.69 |

Table 3.2: Minimum spectral amplitude and maximum spectral roll-off of a square, trapezoidal, sinusoidal, logistic and S-shaped transition.

| | **Frequency** | **Minimum Amplitude** | **Frequency** | **Maximum Roll-off** |
|---|---|---|---|---|
| **Unit** | MHz | dB$\mu$V | MHz | dB/dec |
| **Square** | 500 | 16.08 | 0.12 | 24.76 |
| **Trapezoidal** | 500 | -46.82 | 0.56 | 49.85 |
| **S-shaped** | 500 | -112.34 | 1.21 | 67.27 |
| **Sinusoidal** | 499.97 | -107.91 | 1.30 | 66.44 |
| **Logistic** | 377.48 | -242.09 | 24.05 | 611.69 |

### 3.4.3 Logistic-Shaped Switching Transitions

Logistic-shaped transitions with varying growth rate parameters are shown in Figure 3.13. The plot demonstrates how the shape of the logistic profile can be changed with the growth-rate parameter. The growth rate is a critical temporal characteristic of the logistic function, which can be utilised for high-frequency spectral content mitigation. Note that as the steepness parameter approaches zero, the logistic transition represents a trapezoidal waveform, and as the steepness parameter approaches infinity, the logistic transitions represent a square wave.

Figure 3.13 provides a sample of logistic shaped transitions with two extreme cases of a trapezoidal and square-wave-like transition being produced from low and high growth rates selected for a transition time of 5 $\mu$s. The intended application influences the desired growth rate, and considerations to the amount of high-frequency signal attenuation and the targeted frequency range should be considered. For the SKA-low, frequencies beyond 30 MHz are most important, and therefore the logistic waveforms should be shaped to ensure emissions beyond 30 MHz generated by switching waveforms are alleviated.

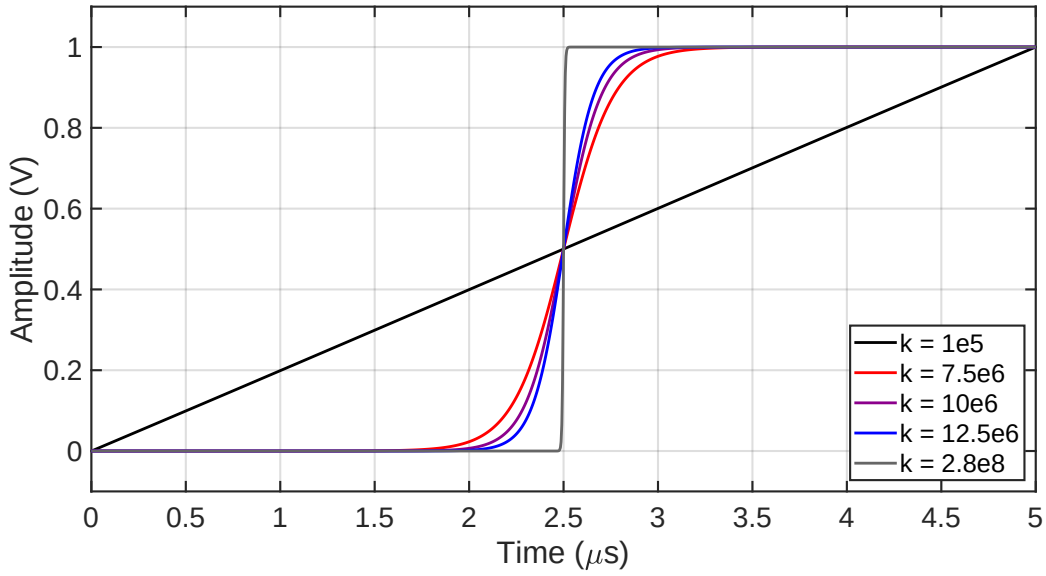



Figure 3.13: Logistic-shaped transitions with varying growth-rate parameters. Waveforms like the trapezoidal (black trace) and a square wave (grey trace) are produced by using growth rates of $1 \times 10^5$ and $2.8 \times 10^8$, respectively.

The harmonic spectral content of a logistic-shaped transition for varied growth rates is shown in Figure 3.14. Each logistic shaped waveform is synthesised with $\tau_t = 5$ $\mu$s, $f_c = 10$ kHz and 50% duty cycle. As shown in the plot Figure 3.14, the growth rate can be selected to provide a required amount of roll-off and for the roll-off to be achieved before a particular frequency. For example, a growth rate of $10 \times 10^6$ will achieve maximum roll-off before 10 MHz, where as a growth rate of $2.8 \times 10^8$ achieves maximum roll-off around 200 MHz.

Analysis of the spectral bound ascertains the ideal logistic waveform shaping by quantifying the minimum harmonic amplitude and the maximum signal roll-off. The minimum spectral amplitude, maximum roll-off and frequency where maximum roll-off occurs are characterised as a function of the logistic growth rate as shown in Figure 3.15(a), Figure 3.15(b), and Figure 3.15(c) respectively. As shown in Fig. 3.15, the minimum spectral amplitude is obtained between $1.2 \times 10^7$ and $1.6 \times 10^7$. Furthermore, growth rates ranging between $1.5 \times 10^7$ and $2 \times 10^7$ achieve maximum spectral content roll-off. A growth-rate of $1.5 \times 10^7$ is best suited for high frequency mitigation below 30 MHz, since the spectral content is minimised and the steepest roll-off is achieved at the lowest frequency compared to other suitable growth-rates.

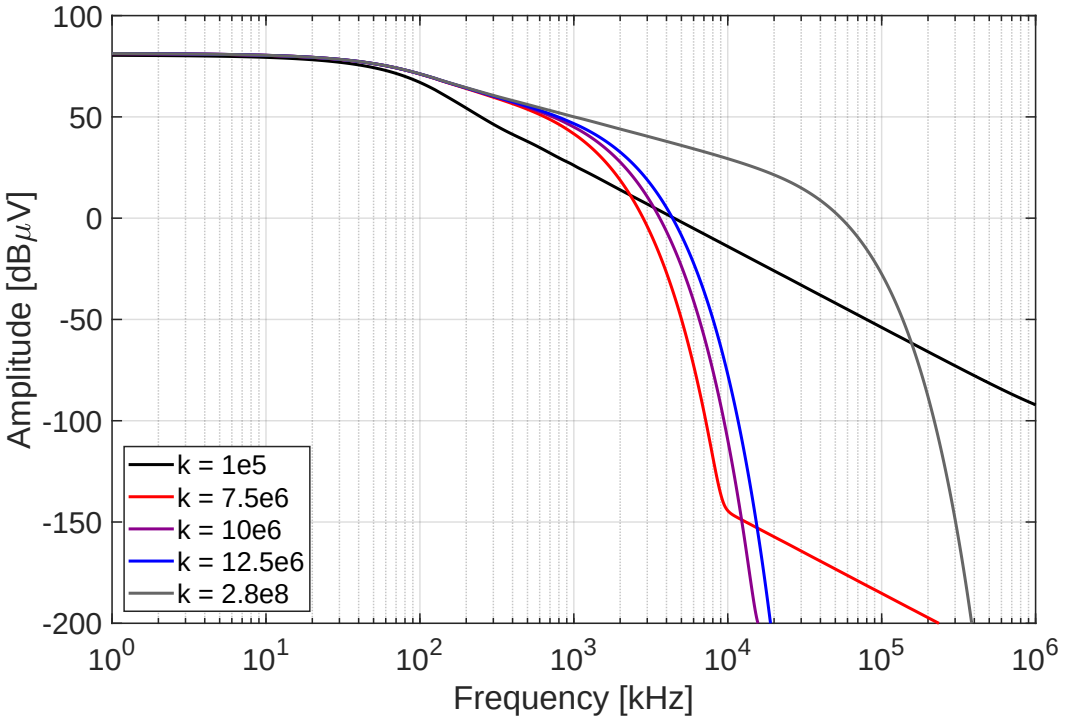
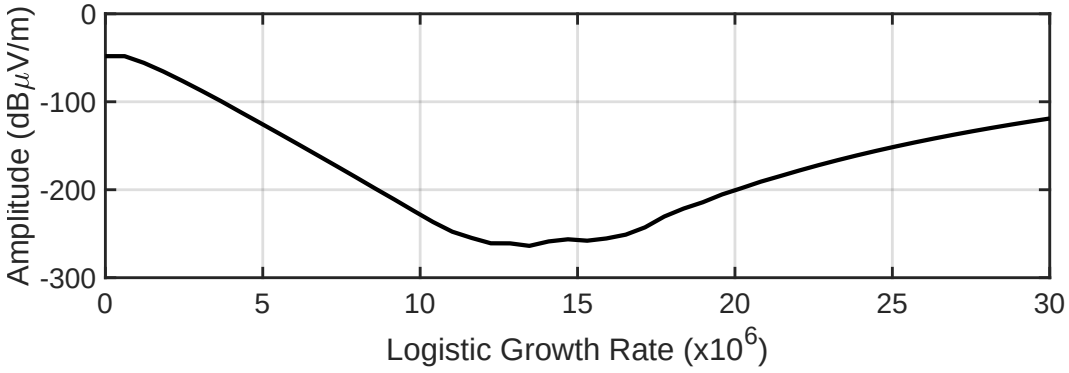
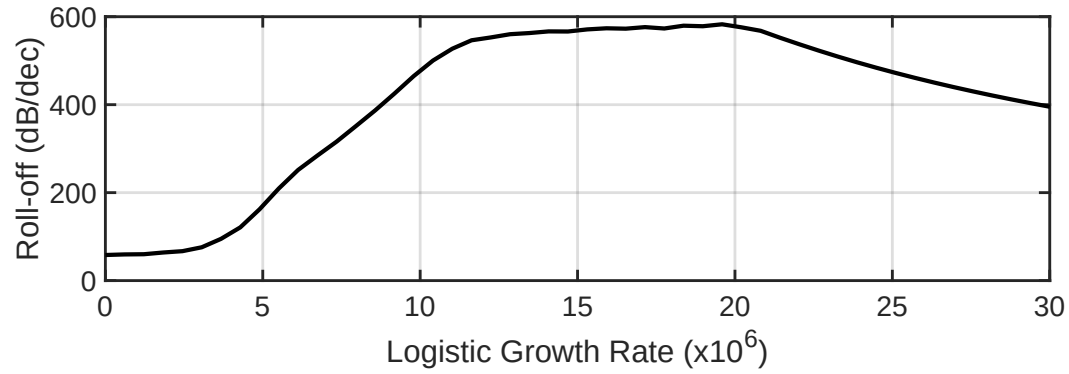


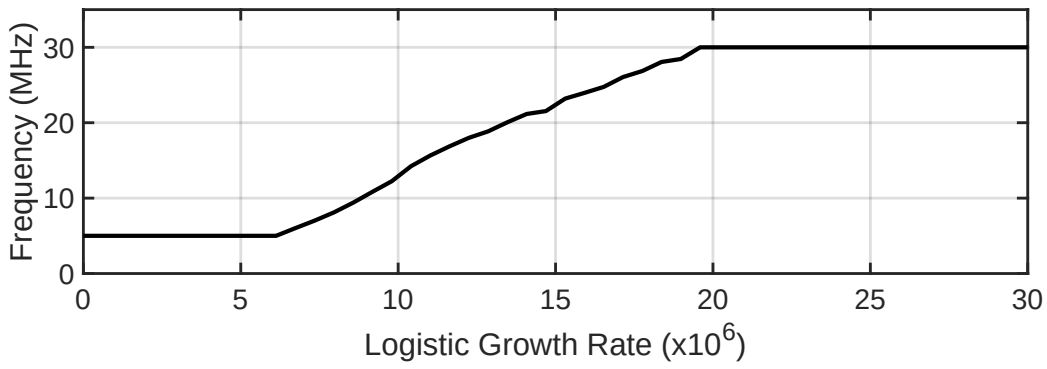

Figure 3.14: Harmonic spectral comparison of logistic-shaped transitions with different growth rates. Waveforms like the trapezoidal (black trace) and a square wave (grey trace) are produced by using growth rates of $1 \times 10^5$ and $2.8 \times 10^8$, respectively.




(a)




(b)




(c)

Figure 3.15: Logistic waveform spectral content analysis showing (a) minimum spectral amplitude, (b) the maximum roll-off, (c) frequency occurrence of the maximum roll-off.

A spectral comparison between the trapezoidal, S-shaped, and logistic-shaped transitions is presented in Figure 3.16. Each transition is synthesised using the following parameters: $f_c = 10$ kHz, $A = 1$ V, $d = 50\%$, $\tau_t = 5$ $\mu$s. Table 3.1 presents the EMI metric in various frequency bands for each waveform. Additionally, refer to Table 3.2 for the minimum amplitude and maximum spectral roll-off of each shaped waveform.

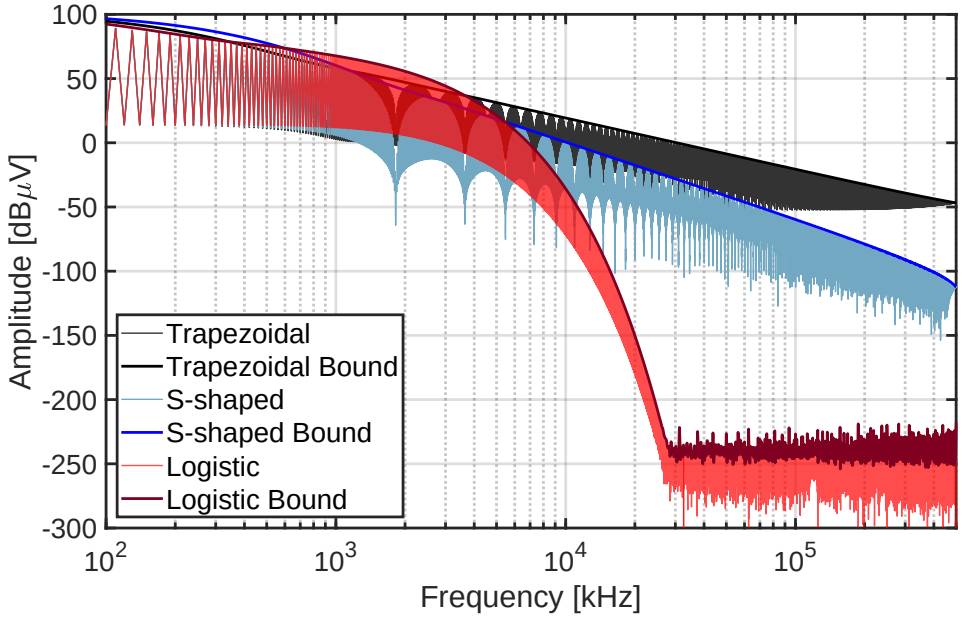
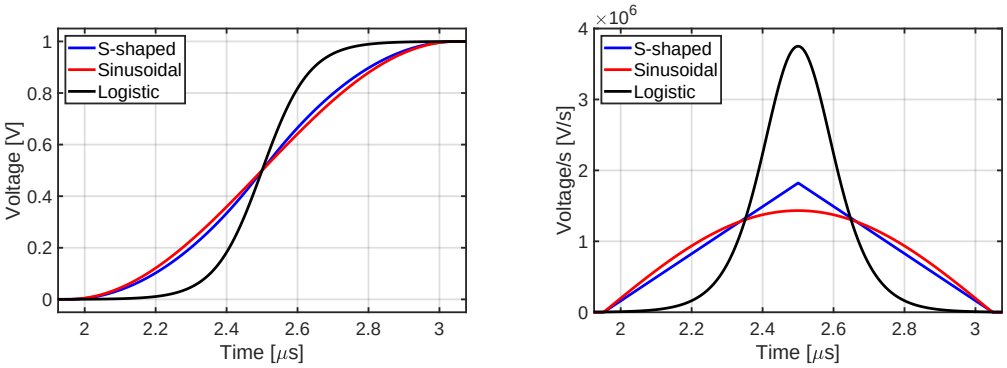



Figure 3.16: Spectral content and the spectral bound of a trapezoidal, logistic and S-shaped switching transition.

Although a sinusoidal shaped transition is infinitely differentiable, the shaped transitions do not achieve steep spectral roll-off as observed with a logistic shaped switching transition. Figure 3.17 presents the switching transitions and the derivatives of an S-shaped, sinusoidal and logistic transition. Notably, the derivative of the sinusoidal and S-shaped switching transitions are similar. Of particular importance is that the derivative is not smooth at the start and end of the sinusoidal and S-shaped switching transitions. Therefore, the second derivative of the entire waveform for both the sinusoidal and S-shaped switching transitions are discontinuous at the start and end of the sinusoidal and S-shaped switching transitions. Conversely, the derivative of the logistic shaped switching transition is smooth. The smoothness of the entire waveform is a critical feature for achieving steep spectral content roll-off. Therefore, the number of continuous derivatives necessary to achieve roll-off or EMI attenuation can be defined depending on the EMI mitigation requirements.

Figure 3.17 demonstrates that it is not only sufficient for the shaped transition to be infinitely differentiable, but the entire waveform also needs to be smooth. Therefore, it is crucial to ensure the shaped switching transition function is defined such that it is smooth at the start and end of the shaped switching transition. As presented in Section 3.3.5, defining the upper and lower asymptotes of the logistic function based on the initial condition to ensure the function is smooth at the beginning and end of the shaped transition is necessary for achieving steep spectral roll-off. Therefore, the ideal theoretical best outcome for steep spectral content roll-off is a smooth waveform with infinitely continuous derivatives. However, there are practical limitations, such as waveform discontinuities and signal quantisation, restricting the amount of spectral content roll-off that can be practically achieved.




(a) (b)

Figure 3.17: (a) Shaped switching transitions and (b) the corresponding derivatives of a sinusoidal, logistic, and S-shaped switching transition.

## 3.5 Practical Limitations of Waveform Shaping

Currently, the modelling presented in this Chapter provides the spectral content of idealised logistic shaped switching transitions, which are expected to provide steep spectral roll-off in theory. However, there are practical limitations, which will hinder the amount of EMI mitigation that is achieved. Two significant limitations which introduce high-frequency spectral content are signal quantisation and waveform discontinuities. These limitations are observed in the literature with high-frequency spectral content was caused by waveform discontinuities [5, 6, 7], and signal quantisation generated by the digital gate-drive control system utilising on-state resistance compensation [8]. Signal quantisation persists where digital control circuitry is required. Waveform discontinuities exist when there are errors between the shaped reference waveform and output shaped waveform of the circuit, or the shaped transition is not smooth.

### 3.5.1 Signal Quantisation and Waveform Discontinuities

The spectral content of an ideal logistic shaped switching transition and a logistic shaped transition that is quantised with 12-bit, 16-bit and 20-bit resolution is presented in Figure 3.18. The resolution of the quantised waveform introduces a noise floor, which limits the EMI mitigation at high frequencies. High-resolution is preferred for low-EMI applications, but it may be cost-prohibitive. Worth noting is Figure 3.18 presents a worst-case scenario where the digital control applies signal quantisation directly to the output waveform, similar to the outcomes presented in [8]. For each waveform plotted, the EMI metric from 100 kHz-1 MHz, 1-30 MHz, 30-500 MHz, and the SKA-low frequency range of 50-350 MHz is presented in Table 3.3. Additionally, the minimum amplitude and corresponding frequency and maximum spectral roll-off and corresponding frequency is resented in Table 3.4.

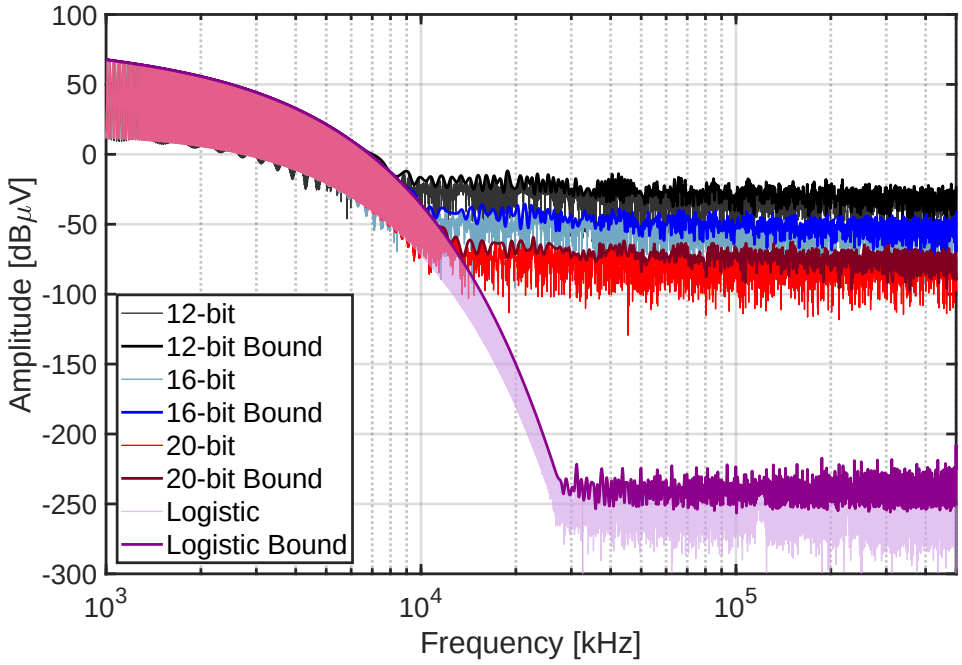



Figure 3.18: Harmonic spectra of a logistic shaped transition that is quantised with 12-, 16- and 20-bit resolution.

Table 3.3: EMI Metric and of an ideal logistic transition and a logistic shaped transition that is quantised with 12-, 16- and 20-bit resolution.

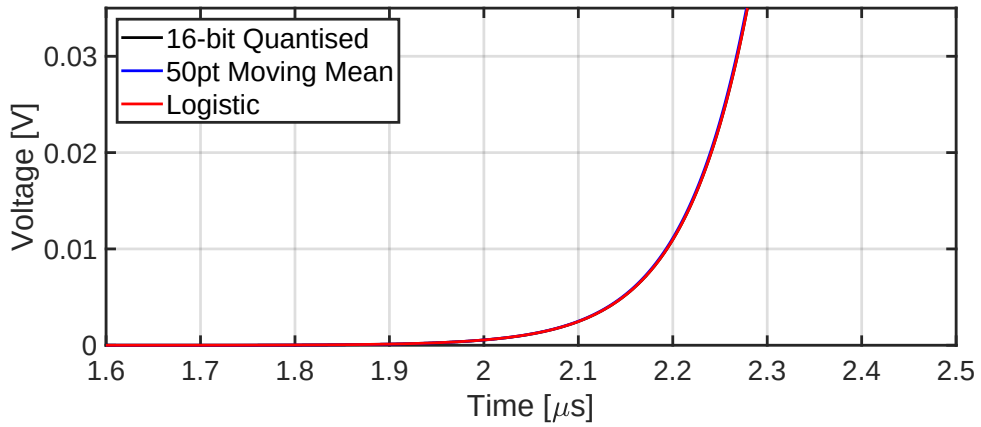
| | **0.1-1 MHz** | **1-30 MHz** | **30-500 MHz** | **50-350 MHz** |
|---|---|---|---|---|
| **Unit** | dBm | dBm | dBm | dBm |
| **Ideal** | -10.65 | -26.84 | -306.78 | -308.69 |
| **12-bit** | -10.65 | -26.85 | -89.84 | -91.57 |
| **16-bit** | -10.65 | -26.85 | -112.63 | -114.55 |
| **20-bit** | -10.65 | -26.84 | -135.81 | -137.57 |

Table 3.4: Minimum spectral amplitude and maximum spectral roll-off of an ideal logistic transition and a logistic shaped transition that is quantised with 12-, 16- and 20-bit resolution.

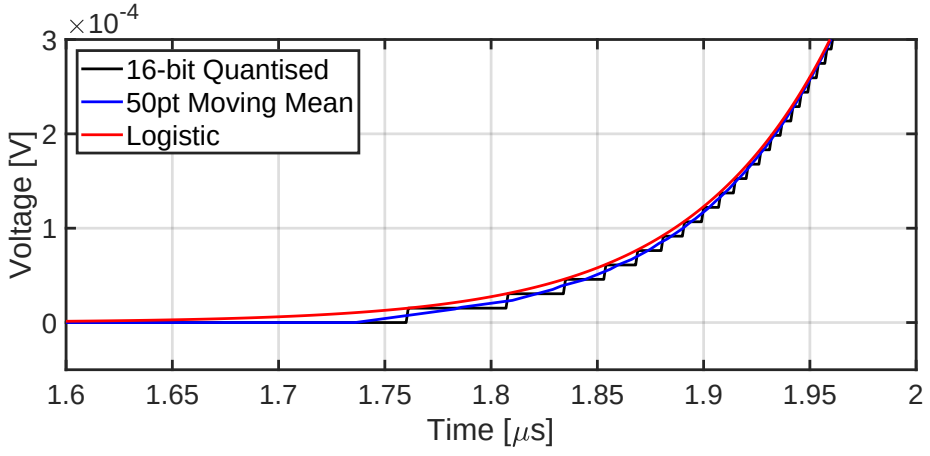
| | **Frequency** | **Minimum Amplitude** | **Frequency** | **Maximum Roll-off** |
|---|---|---|---|---|
| **Unit** | MHz | dB$\mu$V | MHz | dB/dec |
| **Ideal** | 365.98 | -241.93 | 23.48 | 608.70 |
| **12-bit** | 497.78 | -36.01 | 6.34 | 139.51 |
| **16-bit** | 420.06 | -58.25 | 8.18 | 187.37 |
| **20-bit** | 466.18 | -81.46 | 10.08 | 236.16 |

The prototype presented in this dissertation seeks to limit the effects of signal quantisation, where the output of the digital control is only applied to the gate drive, which is quantised. Therefore, the transient response of the controlled MOSFETs and the parallel capacitor will smooth the output waveform, limiting the quantisation impacts of digital circuity. More details of the prototype design are presented in Chapter 4 and Chapter 5.

A computational investigation was performed to determine the expected improved EMI mitigation, when the impacts of the quantisation caused by digital circuity are reduced. A logistic shaped transitions during the first 30 mV and 300$\mu V$ of a 1 V transition is presented in Figure 3.19(a) and Figure 3.19(b) respectively. The initial portions of the transition present an ideal logistic transition, 16-bit quantised logistic transition, and a smoothed transition. The smoothed transition provides a high-level estimate of the expected smoothing of the gate-drive quantisation as the MOSFET undergoes a transient response. The smoothed transitions is created by applying a fifty-point moving average filter to the 16-bit quantised waveform. Figure 3.19(b) shows the smoothed transition does not differ significantly from the ideal logistic transition.

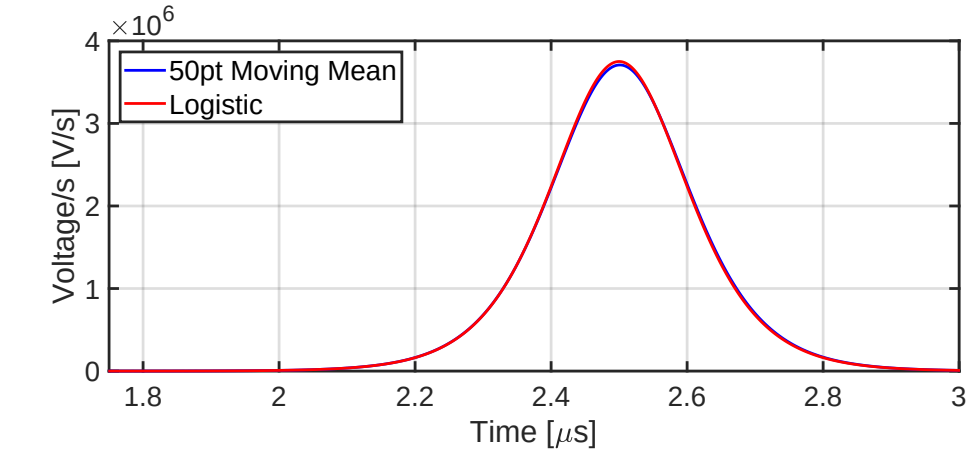



(a)

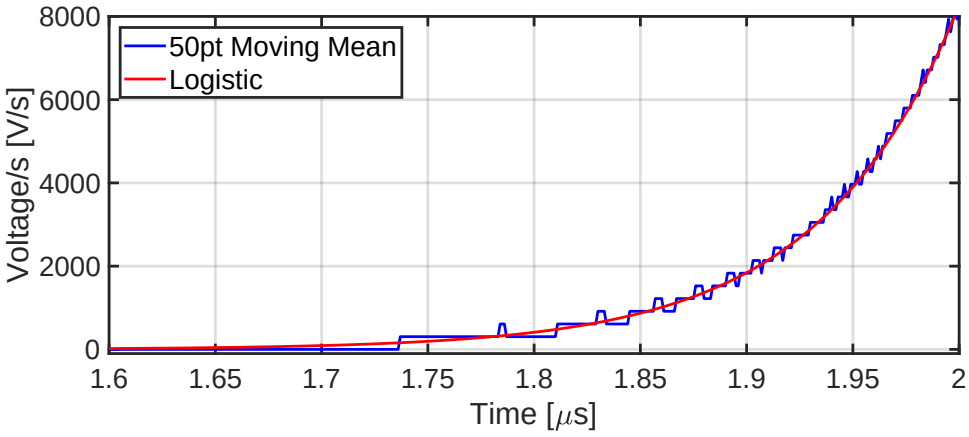



(b)

Figure 3.19: A logistic shaped transitions during the first (a) 30 mV and (b) 300$\mu V$ of a 1 V transition.




(a)




(b)

Figure 3.20: Derivative of a logistic shaped transitions during a (a) complete rising transition and (b) during the first 400ns of the shaped logistic transitions when the transition is starting to increase.

Additionally, the derivative of the ideal logistic and fifty-point moving average logistic transitions is presented in Figure 3.20. The entire derivative during a rising transition in Figure 3.20(a) shows the derivatives are similar in value during the entire transition. However, Figure 3.20(b) shows the derivative of the fifty-point moving average logistic transition is not smooth. The fifty-point moving average logistic transition is representative of actual circuitry implementation, which is expected to have practical limitations caused by digital control circuity, errors in the control system caused by resolution of digital-to-analogue and analogue-to-digital converters, and measurement noise introduced by oscilloscopes.

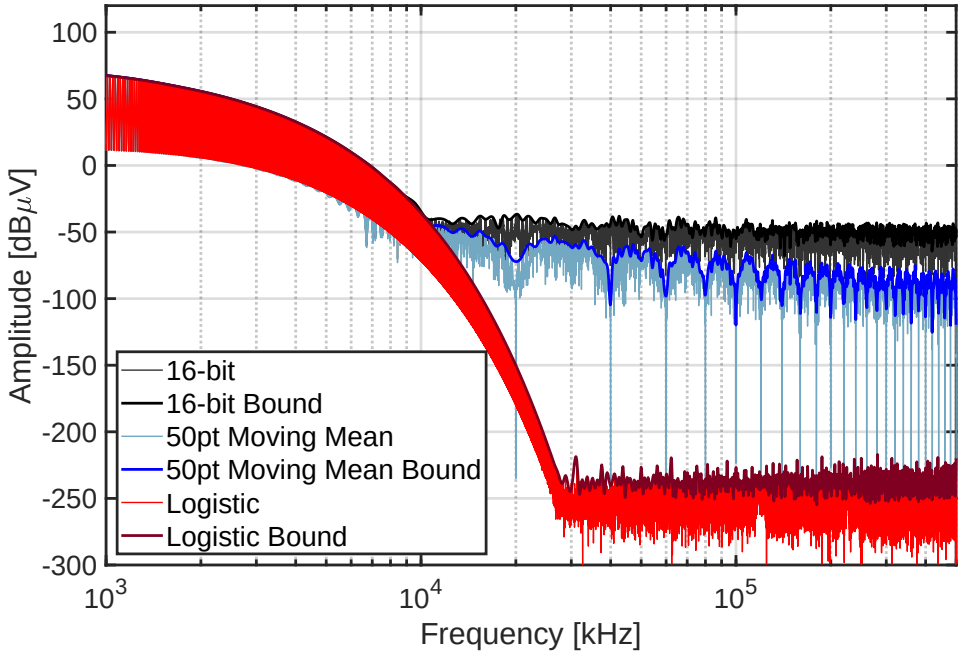



Figure 3.21: Harmonic spectral estimate of a logistic shaped transition with a quantised gate-drive signal (blue) compared to an ideal logistic shaped transition (red) and 16-bit quantised logistic waveform (black).

The spectral content comparison between the ideal logistic shaped transition, 16-bit quantised logistic transition and fifty point moving average logistic transition is presented in Figure 3.21. Although the fifty point moving average logistic transition presents an improvement compared to the 16-bit quantised waveform, the impairments and limitations in achieving the desired spectral roll-off is attributed to the derivative of the fifty point moving average logistic transition not being smooth. Although smooth waveform with infinitely continuous derivatives are desired, the computational estimate of the expected circuit implementation demonstrates the limitations that exist, which hinder the spectral roll-off from being achieved.

Additionally, the impacts of signal discontinuities on the harmonic spectra of a logistic shaped waveform is presented in Figure 3.22. An ideal logistic shaped switching transition and logistic shaped transitions with a 1 mV, 1 $\mu$V and 1 nV discontinuity are presented. For each waveform plotted, the EMI metric from 100 kHz-1 MHz, 1-30 MHz, 30-500 MHz, and the SKA-low frequency range of 50-350 MHz is presented in Table 3.5.

Furthermore, the minimum amplitude and corresponding frequency and maximum spectral roll-off and corresponding frequency is resented in Table 3.6. The discontinuities provide insight into the amount of precision that is required to achieve the spectral roll-off that is observed in an ideal logistic-shaped transition. A small discontinuity of 1 nV is anticipated to provide a 100 dB difference from the ideal logistic shaped transition. Note that the noise floor provided by the ideal logistic shaped transition is a MATLAB limitation caused by standard double-precision floating-point arithmetic, which is limited to 16 significant digits.

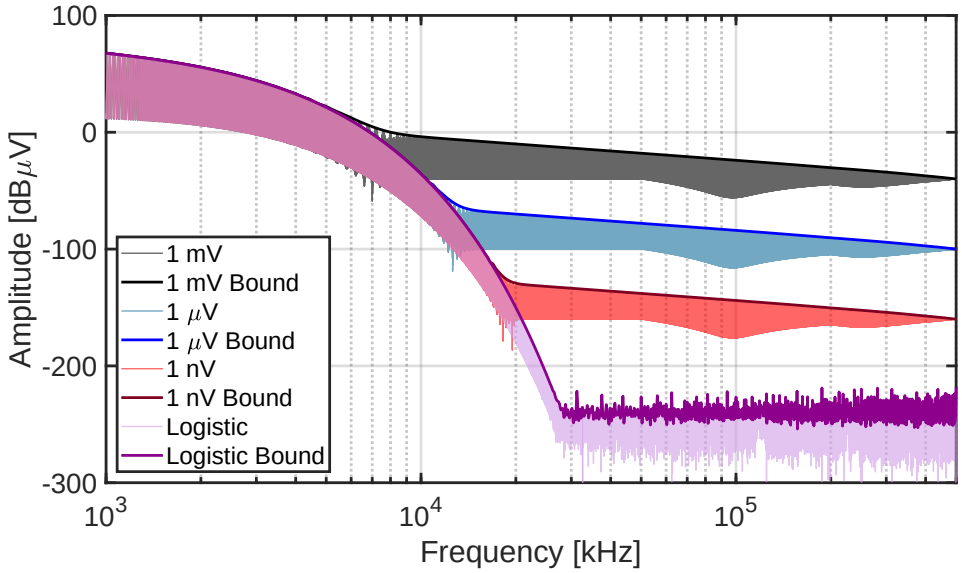



Figure 3.22: Harmonic spectra of a logistic shaped transition with discontinuities introduced.

Table 3.5: EMI Metric and of an ideal logistic transition and a logistic shaped transition with 1 mV, 1 $\mu$V and 1 nV discontinuities.

| | **0.1-1 MHz** | **1-30 MHz** | **30-500 MHz** | **50-350 MHz** |
|---|---|---|---|---|
| **Unit** | dBm | dBm | dBm | dBm |
| **Ideal** | -10.65 | -26.84 | -306.78 | -308.69 |
| **1mV** | -10.65 | -26.85 | -91.72 | -94.32 |
| **1uV** | -10.65 | -26.84 | -151.72 | -154.32 |
| **1nV** | -10.65 | -26.84 | -211.72 | -214.32 |

Table 3.6: Minimum spectral amplitude and maximum spectral roll-off of an ideal logistic transition and a logistic shaped transition with 1 mV, 1 $\mu$V and 1 nV discontinuities.

| | **Frequency** | **Minimum Amplitude** | **Frequency** | **Maximum Roll-off** |
|---|---|---|---|---|
| **Unit** | MHz | dB$\mu$V | MHz | dB/dec |
| **Ideal** | 377.48 | -242.09 | 24.05 | 611.69 |
| **1mV** | 500 | -40 | 6.02 | 120.98 |
| **1uV** | 500 | -100 | 10.40 | 278.30 |
| **1nV** | 500 | -159.96 | 14.83 | 361.33 |

Furthermore, the impacts of signal discontinuities on the harmonic spectra of a sinusoidal shaped and trapezoidal shaped waveform is presented in Figure 3.23 and Figure 3.24, respectively. Given that both the sinusoidal shaped and trapezoidal shaped waveform do not achieve steep spectral roll-off like the logistic shaped switching transitions, the magnitude of the discontinuities are larger before the spectral content is hindered by introducing a noise floor to the spectral content. For the sinusoidal shaped switching transitions, the harmonic spectra considering a 1 mV, 100 $\mu$V and 10 $\mu$V discontinuities are presented. Additionally, 100 mV, 10 mV and 1 mV discontinuities are considered for the trapezoidal shaped waveform.

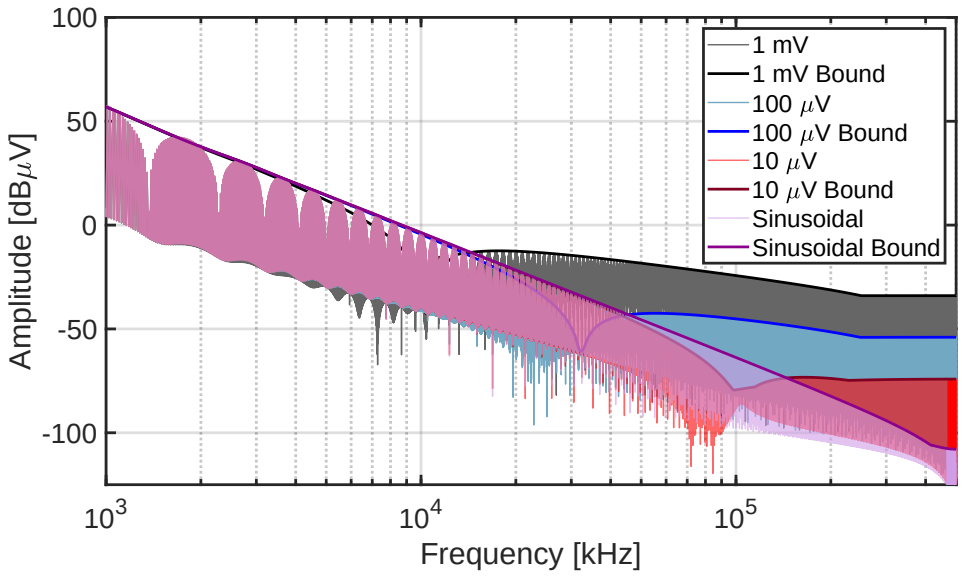



Figure 3.23: Harmonic spectra of a sinusoidal shaped transition with discontinuities introduced.

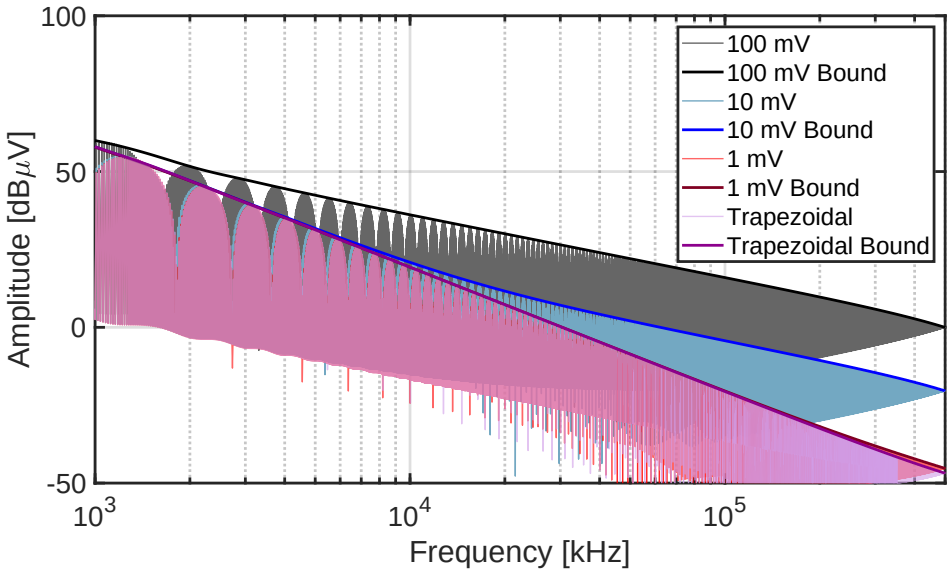



Figure 3.24: Harmonic spectra of a trapezoidal shaped transition with discontinuities introduced.

For each ideal and discontinuous waveform plotted, the EMI metric from 100 kHz-1 MHz, 1-30 MHz, 30-500 MHz, and the SKA-low frequency range of 50-350 MHz is presented in Table 3.7 and Table 3.8 for the sinusoidal and trapezoidal shaped transitions, respectively. Additionally, the minimum amplitude and corresponding frequency and maximum spectral roll-off and corresponding frequency is resented in Table 3.9 and Table 3.10 for the sinusoidal and trapezoidal shaped transitions, respectively.

Table 3.7: EMI Metric and of an ideal sinusoidal transition and a sinusoidal transition with 1 mV, 100 $\mu$V and 10 $\mu$V discontinuities.

| | **0.1-1 MHz** | **1-30 MHz** | **30-500 MHz** | **50-350 MHz** |
|---|---|---|---|---|
| **Unit** | dBm | dBm | dBm | dBm |
| **Ideal** | -11.205 | -41.902 | -117.38 | -128.48 |
| **1mV** | -11.192 | -42.007 | -92.042 | -94.444 |
| **100uV** | -11.203 | -41.913 | -114.74 | -115.64 |
| **10uV** | -11.204 | -41.903 | -118.62 | -131.73 |

Table 3.8: EMI Metric and of an ideal trapezoidal transition and a trapezoidal transition with 100 mV, 10 mV and 1 mV discontinuities.

| | **0.1-1 MHz** | **1-30 MHz** | **30-500 MHz** | **50-350 MHz** |
|---|---|---|---|---|
| **Unit** | dBm | dBm | dBm | dBm |
| **Ideal** | -11.657 | -38.267 | -82.744 | -89.289 |
| **100mV** | -10.364 | -33.896 | -51.742 | -54.352 |
| **10mV** | -11.521 | -38.01 | -71.743 | -74.574 |
| **1mV** | -11.644 | -38.246 | -82.674 | -89.154 |

Table 3.9: Minimum spectral amplitude and maximum spectral roll-off of an ideal sinusoidal transition and a sinusoidal transition with 1 mV, 100 $\mu$V and 10 $\mu$V discontinuities.

| | **Frequency** | **Minimum Amplitude** | **Frequency** | **Maximum Roll-off** |
|---|---|---|---|---|
| **Unit** | MHz | dB$\mu$V | MHz | dB/dec |
| **Ideal** | 499.97 | -107.91 | 1.30 | 66.44 |
| **1mV** | 254.28 | -33.99 | 9.06 | 207.57 |
| **100uV** | 98.56 | -79.45 | 1.30 | 66.45 |
| **10uV** | 32.41 | -57.98 | 30.01 | 306.79 |

Table 3.10: Minimum spectral amplitude and maximum spectral roll-off of an ideal trapezoidal transition and a trapezoidal transition with 100 mV, 10 mV and 1 mV discontinuities.

| | **Frequency** | **Minimum Amplitude** | **Frequency** | **Maximum Roll-off** |
|---|---|---|---|---|
| **Unit** | MHz | dB$\mu$V | MHz | dB/dec |
| **Ideal** | 500 | -46.82 | 0.56 | 49.85 |
| **100mV** | 500 | -45.28 | 0.57 | 50.10 |
| **10mV** | 500 | -20.40 | 0.56 | 50.00 |
| **1mV** | 500 | -0.04 | 0.52 | 46.99 |

Regardless, the level of precision from hardware implementation is speculated to be hindered by the selection of ADCs, DACs, and $\mu$-processors used in the power converter prototype. Although the theorised roll-off is not expected to be achieved, the waveform shaping is improved compared to hard switching and provides additional attenuation compared to the shaped switching transition implementations presented in the literature. Selecting ADC, DAC, and $\mu$-processors must ensure onerous high-frequency noise is not generated. However, ADC and DAC resolution and the $\mu$-processor clock speed are critical for control accuracy. Therefore, a trade-off exists between the control system accuracy and the noise floor introduced by the digital circuitry, which depends on the intended application. Additionally, analogue circuitry control would mitigate signal quantisation effects. However, the digital control circuit is initially required since the $\mu$-processor is programmable, which offers flexibility during prototype development.

### 3.5.2 Considerations for Circuitry Implementation

The gate drive control of the half-bridge prototype will allow for the drain-source voltage of the MOSFET to track a logistic waveform. A capacitor is connected in parallel to the power MOSFETs, which is sized based on the load demand of the system. For a transition targeted at achieving low-EMI, the entire transition is controlled. Therefore, the current is completely transferred to the capacitors. For a logistic shaped transition, this is when the derivative reaches a maximum, which occurs when the voltage has reached half of the waveform amplitude. Therefore a relationship exists between the maximum derivative and the maximum current diverted through the capacitor. Available capacitor values and their expected tolerances place a design constraint on the allowable logistic shaped reference profiles. At the point where all current is transferred to the capacitor, the voltage profile is linear and the waveform derivative has reached a maximum. Therefore:

$$i_C = C\max\left(\frac{dv_{ds}}{dt}\right) \tag{3.41}$$

Where:

$$\frac{dv_{ds}}{dt} = \frac{d}{dt}r(t) = \frac{\alpha A}{\beta-\alpha}\left(\frac{\beta k e^{k(t-\tau_r/2)}}{\left(e^{k(t-\tau_r/2)}+1\right)^2}\right) \tag{3.42}$$

The logistic modelling must be performed in accordance with the operating conditions and circuitry component selection of the half-bridge prototype. Although theoretical modelling should be performed to identify the ideal shaped switching conditions for low-EMI, it is unlikely that the circuit can be designed to be shaped exactly per the logistic reference function and the desired growth rate.

It may not be possible to have a manufactured capacitor sized exactly to match the desired k-value. Additionally, there are also error tolerances of the capacitor to consider. Instead, capacitor values should be selected and the k-values should be calculated. For example, capacitor values of 68 nF, 47 nF and 33 nF correspond to k-values of $6.12 \times 10^6$, $8.86 \times 10^6$, and $12.26 \times 10^6$, respectively.

The critical design information required for the modelling process regarding ideal waveform shaping is the size of the capacitor to ensure all current transfers at the middle of the drain-source voltage transition. In later chapters of this dissertation, the auxiliary branch sequencing and gate-drive profiles for the power MOSFETs and current injection MOSFETs is presented for ideal transitions both computationally in Chapter 4 and for an FPGA presented in Chapter 5 for the prototype implementation.

## 3.6 References

[1] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 47, pp. 2154–2165, 2011.

[2] C. R. Paul, *Introduction to Electromagnetic Compatability.* United States of America: Wiley-Interscience John Wiley & Sons, 2006.

[3] M. Vilathgamuwa, J. Deng, and K. J. Tseng, "Emi suppression with switching frequency modulated DC-DC converters," *IEEE Ind. Appl. Mag.*, vol. 5, pp. 27–33, 1999.

[4] S. Walder, X. Yuan, I. Laird, and J. J. O. Dalton, "Identification of the temporal source of frequency domain characteristics of SiC MOSFET based power converter waveforms," in *IEEE Energy Convers. Congr. and Expo.*, Sept 2016, pp. 1–8.

[5] X. Yang, Y. Yuan, X. Zhang, and P. R. Palmer, "Shaping high-power IGBT switching transitions by active voltage control for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1669–1677, March 2015.

[6] X. Yang, Z. Long, Y. Wen, H. Huang, and P. R. Palmer, "Investigation of the trade-off between switching losses and EMI generation in gaussian S-shaping for high-power IGBT switching transients by active voltage control," *IET Power Electron.*, vol. 9, no. 9, pp. 1979–1984, 2016.

[7] J. Yang, J. Shi, and T. Cui, "An active voltage controller of SiC MOSFET for reduced EMI generation," in *3rd IEEE Advanced Inf. Technol., Electron. Autom. Control Conf. (IAEAC)*, 2018, pp. 979–983.

[8] T. Cui, Q. Ma, P. Xu, and Y. Wang, "Analysis and optimization of power MOSFETs shaped switching transients for reduced EMI generation," *IEEE Access*, vol. 5, pp. 20 440–20 448, 2017.

# Chapter 4

## Shaped Switching Transitions in MOSFETs

## 4.1 Introduction

This Chapter presents the theoretical framework and systematic approach to achieving shaped switching transitions in a half-bridge power converter. Firstly, an overview of a half-bridge DC-DC converter utilising hard-switching PWM is presented, which provides a comparison to the half-bridge prototype capable of undergoing a shaped switching transition. The intent is to present how MOSFETs are typically used as switches in power converters, compared to a carefully controlled approach to produce shaped switching transitions. Furthermore, an overview of the device structure and physical operation is presented, which provides the fundamentals for the current-voltage characteristic and the operational modes of a MOSFET. Following this, the turn-off transients of the MOSFET is presented, with simulation outcomes using the same MOSFET included in the low-EMI half-bridge prototype.

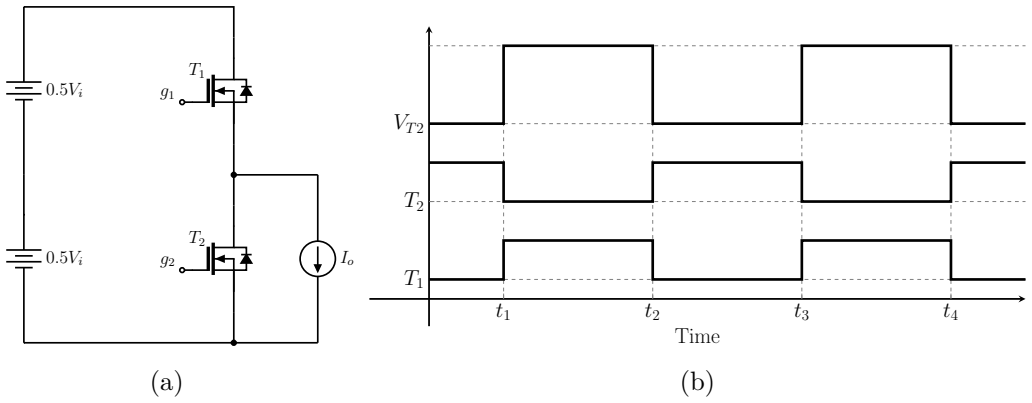
Next, an overview of the half-bridge circuit is presented alongside the sequence of gate-drive signals, which provides an overview of the control philosophy without detailed control considerations. Following this, an overview of all the low-EMI half-bridge modes of operation and critical control aspects is presented, outlining how the circuit can produce shaped switching waveforms. Additionally, the control algorithm is presented, which details how the error signal between the expected output voltage and the actual voltage is used as feedback to correct the gate-drives of the power and injection MOSFETs to follow the desired shaped switching transition. Lastly, the chapter concludes with simulations of a half-bridge DC-DC converter capable of undergoing shaped switching transitions. The simulation modelling uses MOSFET SPICE models to simulate the MOSFET switching transients, allowing the circuit components to be accurately modelled during shaped switching transitions. The circuit simulations of a half-bridge DC-DC converter using MOSFET SPICE models and the presented control algorithm consolidates the mathematical treatment of shaped switching transitions presented in Chapter 3.

## 4.2 Half-Bridge DC-DC Converter and MOSFET Transients

### 4.2.1 Overview

The half-bridge topology is utilised in DC-DC power converter applications [1, 2]. A circuit schematic of a half-bridge DC-DC converter connected to a constant load $I_o$ is shown in Figure 4.1(a). The switching sequence of the switching MOSFETs and the idealised drain source voltage, $v_{ds}$, waveform of the bottom switching MOSFET, $T_2$ is shown in Figure 4.1(b). Note that the output MOSFET waveform is presented in Figure 4.1(b) instead of the converter output voltage and current waveforms to provide

a comparison to the prototype half-bridge presented in later sections of this Chapter. The typical hard-switching approach invokes a rapid change in the gate-drive voltage to allow the MOSFET to be quickly turned off or on, which is desirable for reducing conduction losses. When turning a MOSFET off, typically, the gate-drive voltage is rapidly changed from a high on-state voltage $V_{GH}$ to a low off-state voltage $V_{GL}$, which can be zero or negative. The drain-source resistance of the MOSFET is, therefore, increased as quickly as possible to turn the MOSFET off. The switching and control strategy is the opposite approach to the low-EMI prototype, where the gate drive is slowly and carefully controlled to produce a shaped drain-source voltage, $v_{ds}$, of the MOSFET. Therefore, the drain-source resistance of the MOSFET is slowly varied to obtain the desired shaped waveform.




(a) (b)

Figure 4.1: Half-Bridge DC-DC (a) circuit topology and (b) control signal sequencing.

### 4.2.2 MOSFET Transients

#### 4.2.2.1 Overview

The basic principle of a MOSFET is that the gate-source voltage, $v_{gs}$, can control the drain-source current, $i_{ds}$, to be operated as a controlled source or a switch. MOSFETs are used in power converters as a switch. However, when designing power converters for low-EMI applications, the MOSFET is used as a controlled source and a switch. As such, a fundamental understanding of the MOSFET characteristics is required. Initially, the structure of the MOSFET and the physical operation is presented. Following this, the transient and high-frequency behaviour of a MOSFET during a turn-off transition is presented.

The characteristics of a MOSFET play a critical role in controlling a MOSFET to following a reference profile for shaped switching transitions, where knowledge of the structure, physical operation and transient response of the MOSFET is required to

determine the gate-source voltage, $v_{gs}$, and gate-source current, $i_{gs}$, that is required to generate the required output voltage waveform. This section presents an overview of the MOSFET, including the physical structure, simple operation, terminal characteristics, circuit models, transient response, and high-frequency behaviour. The information provides the framework for the circuit modelling and control strategy discussed in later sections.

#### 4.2.2.2 Device Structure

As an overview, the structure of the n-type MOSFET will be discussed. The n-type MOSFET is manufactured on a wafer of silicon, which is a p-type substrate [3]. Furthermore, two heavily doped n-type substrates are synthesised, creating the source and drain regions of the MOSFET in the p-type substrate. An insulating silicon dioxide layer is grown on the substrate surface between the source and drain, and a metal layer is placed over the top to form the MOSFET gate. Additionally, metal contacts are placed on the source, drain and substrate regions. As such, the MOSFET can be treated as a three-terminal device: the gate, source, and drain. A voltage is applied to the gate to control the drain-source current, if the circuit is permitting. A cross-sectional diagram of an n-type MOSFET physical structure is shown in Figure 4.2.

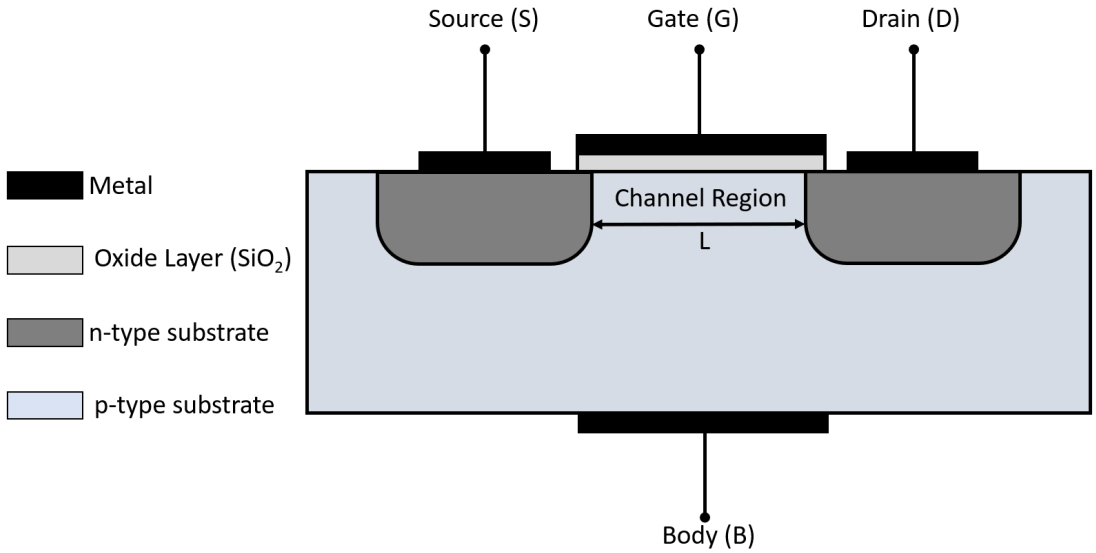



Figure 4.2: Cross-section of an n-type MOSFET physical structure.

#### 4.2.2.3 Physical Operation and Current-Voltage Characteristics

When a positive $v_{gs}$ is applied across the gate, a depletion region is formed, which is filled with the negative charge of the acceptor atoms and attracted electrons of the drain and source regions. An applied $v_{gs}$ which exceeds the MOSFET threshold voltage, $V_{th}$, causes a sufficient negative charge to build up, causing current to conduct if a sufficient voltage is applied across the drain-source of the MOSFET, $V_{DD}$. Furthermore, the gate and channel region create a parallel-plate capacitor, producing an electric field that controls the amount of charge in the channel. The charge accumulation determines the channel conductivity and, therefore, the current flowing through the channel for an applied $V_{DD}$.

The current is negligibly small for instances where $v_{gs}$ equals $V_{th}$ since the channel is only just formed. As $v_{gs}$ begins to exceed $V_{th}$, more electrons are attracted into the channel, which is analogous to an increase in channel depth, resulting in a reduced channel resistance. For a small $v_{ds}$, proportionality exists between $v_{ds}$ and $i_{ds}$, and current will conduct for any $v_{gs}$–$V_{th}$, which is known as the ohmic region.

When $v_{gs}$ is held constant such that $v_{gs} > V_{th}$, a voltage drop is present along the channel, increasing from 0 to $v_{ds}$. The channel depth is varied, being thicker at the source end and thinner at the drain end. As $v_{ds}$ is increased further to a point where $v_{ds} = v_{gs}$–$V_{th}$, the channel depth at the drain approaches zero and is tapered, and the relationship between $v_{ds}$ and $i_{ds}$ is non-linear. At this point, for any increase in $v_{ds}$, $i_{ds}$ does not increase further, and the MOSFET has entered the saturation region. Therefore, for instances where $v_{ds} > v_{gs}$–$V_{th}$, the MOSFET is in the saturation region, and for instances where $v_{ds} < v_{gs}$–$V_{th}$, the MOSFET is in the ohmic region. For any value of $v_{gs}$, where $v_{gs} > V_{th}$, there is a unique $v_{ds}$ at the boundary between the ohmic and saturation regions.

Understanding the MOSFET terminal characteristics is essential for the design of power converters and is of particular importance for low-EMI circuit design. The MOSFET is operated in the cut-off and saturation regions in power converter applications, moving quickly through the ohmic region while switching as quickly as possible. A MOSFET will operate in either the cut-off, ohmic or saturation region under the following conditions:

- Cut-off: $v_{gs} < V_{th}$
- Ohmic: $v_{ds} < v_{gs}$–$V_{th}$
- Saturation: $v_{ds} \geq v_{gs}$–$V_{th}$

An in-depth understanding of the ohmic region is important for the half-bridge prototype design presented in this Chapter. In the ohmic region, an applied $v_{gs}$ and $v_{ds}$ will give a unique drain-source voltage/current characteristic. Alternatively, this can be considered as a unique resistance for each $v_{gs}$ and $v_{ds}$ combination. To operate a MOSFET in the ohmic region $v_{gs}$ must be greater than $V_{th}$, and $v_{ds} < v_{gs}–V_{th}$.

To characterise the MOSFET $i_{ds}$, a portion of the gate is considered as an infinitesimal strip distance, $x$, from the source. The effective voltage between the gate at the point $x$, forms a strip of gate capacitance with stored electron charge. The voltage, $v_{ds}$, produces an electric field along the channel, causing the electron charge to drift towards the drain, forming a resultant drift current, $i$, where $i = -i_{ds}$. Performing an integral over the length of the channel gives the following equation for $i_{ds}$ in the ohmic region [3]:

$$i_{ds} = \frac{g_{fs}W}{L}\left[(v_{gs} - V_t)\, v_{ds} - \frac{1}{2}v_{ds}^2\right] \tag{4.1}$$

For the MOSFET in the saturation region, $i_{ds}$ becomes [3]:

$$i_{ds} = \frac{g_{fs}W}{2L}\,(v_{gs} - V_t)^2 \tag{4.2}$$

Where $g_{fs}$ is the transconductance of the MOSFET, $L$ is the channel length, and $W$ is the channel width. In the ohmic region, the quadratic term can be ignored if $v_{ds}$ is sufficiently small, giving a linear relationship for the resistance of the MOSFET [3]:

$$r_{ds} = \frac{v_{ds}}{i_{ds}} = \frac{L}{[gW\,(v_{gs} - V_t)\, v_{ds}]} \tag{4.3}$$

The n-channel MOSFET current-voltage characteristic for various curves of $i_{ds}$ as a function of $v_{ds}$ is presented in Figure 4.3.

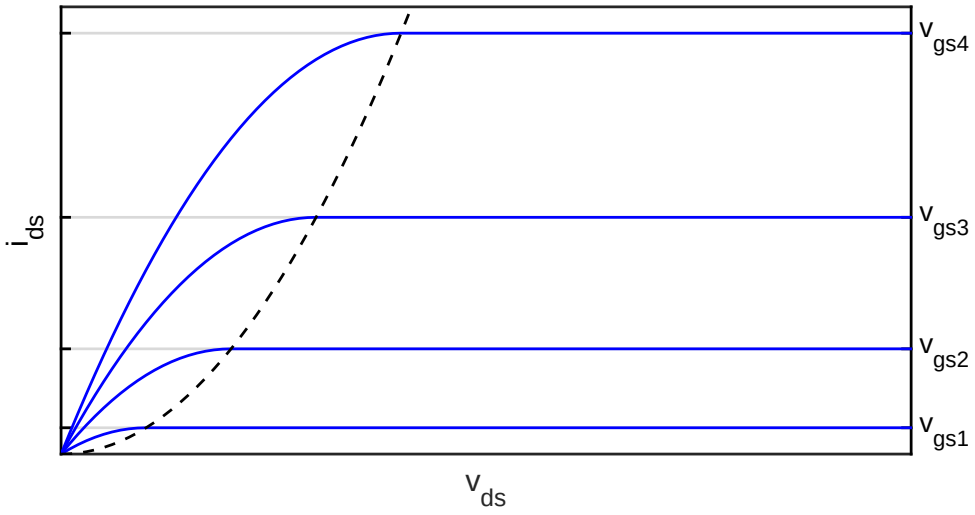



Figure 4.3: $i_{ds}$ as a function of $v_{ds}$ curves of an n-channel MOSFET. Note $v_{gs1} > V_{th}$.

The conditions for the linear resistance equation requires $v_{gs}$ to be constant and $v_{ds}$ to be sufficiently small. The device structure, physical operation and drain-source current-voltage characteristics provide a basic understanding of how the MOSFET operational characteristics vary depending on the $v_{gs}$ and $v_{ds}$ that is applied. The key characteristics are the combination of applied $v_{gs}$ and $v_{ds}$ set the $r_{ds}$ of the MOSFET. Essentially, the MOSFET operates as a variable resistor. Therefore, applying the correct voltage profile to the gate of a MOSFET will allow for $v_{ds}$ to be controlled given a certain $i_{ds}$. To accurately define the behaviour of the MOSFET, an understanding of the transient response and high-frequency behaviour of the MOSFET is required.

The operational requirement of the low-EMI prototype is to control the output $v_{ds}$ of a MOSFET to follow the desired reference profile. Knowing the MOSFET can operate as a variable resistor identifies one part of the solution to the problem. The next critical aspect is to understand how the MOSFET responds to changes in $v_{gs}$. The transient response, and more importantly, the time delay between applying the gate signal and getting the desired output $v_{ds}$, needs to be understood. The delays in the transient response will differ depending on whether the MOSFET is in the cut-off, ohmic or the saturation region. The following sections address the transient and high-frequency behaviour of a MOSFET, using an equivalent circuit to explain the response of the MOSFET to changes in gate voltages.

#### 4.2.2.4 Transient Behaviour: Parasitic Components and Equivalent Circuit

Due to the physical structure of the MOSFET, parasitic components inherently exist. The major parasitic components of a MOSFET include the resistances of the bulk material and the contacts. Additionally, the inductances of the leads and capacitance of junctions and connections should also be considered. The parasitic components of a MOSFET are essential when considering the transient response and high-frequency behaviour of the MOSFET. Correctly identifying the parasitic components of a MOSFET is critical for waveform shaping since the control of a power converter to achieve a desired shaped switching transition relies on a relatively slow and controlled transient response of a MOSFET.

This Section presents a simplified analytical solution to the turn-off transients response of a MOSFET. The key equations to explain the gate-source current $i_{gs}$, gate-source voltage $v_{gs}$, drain-source voltage $v_{ds}$, and drain-source current $i_{ds}$ throughout various stages of the transient responses are presented. The key equations identify the major parasitic components that dominate the transient response of a MOSFET during turn-off.

The major parasitic components include the gate-source capacitance, gate-drain capacitance, drain-source capacitance, source lead inductance, drain lead inductance and the internal gate resistance. During turn-off, energy in the lead inductances is dissipated. The MOSFET equivalent circuit with the major parasitic components is presented in Figure 4.4. Each major component included in the equivalent circuit is described in Table 4.1.

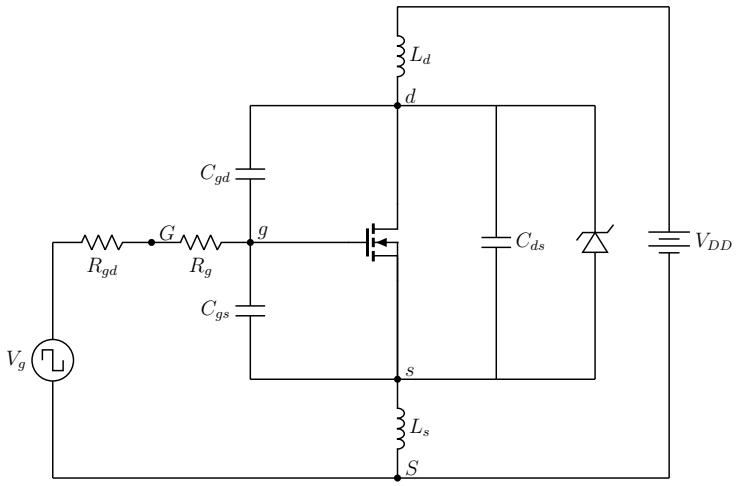



Figure 4.4: MOSFET equivalent circuit.

Table 4.1: Description of major parasitic components in the MOSFET equivalent circuit.

| **Symbol ID** | **Description** |
|---|---|
| $V_{DD}$ | Input voltage (constant DC) |
| $V_g$ | Gate drive voltage |
| $L_s$ | Source inductance |
| $L_d$ | Drain inductance |
| $R_g$ | Internal gate drive resistance |
| $R_{gd}$ | External gate drive resistance |
| $C_{gs}$ | Gate-source capacitance |
| $C_{gd}$ | Gate-drain capacitance |
| $C_{ds}$ | Drain-source capacitance |
| $C_{iss}$ | $C_{gs}+C_{gd}$ |
| $C_{oss}$ | $C_{gs}+C_{gd}$ |

The basic operation of a MOSFET is achieved by controlling the drain current with the gate voltage. The time taken for $v_{ds}$ to respond to a change in $v_{gs}$ is depends on the time taken to establish a change in the number of carriers in the inversion layer and the transition time of the carriers along the length of the channel [4].

The transient response of a circuit is typically performed by solving the physical equations describing the behaviour of the device alongside an equivalent circuit model [5, 6, 7, 8]. However, considering the transient response of a MOSFET, matching the non-linear device characteristics [9, 10] to the terminal characteristics of the equivalent circuit is complicated [11, 12, 13, 14, 15]. For power MOSFETs, this typically is not an issue since the applications are low frequency, and the parasitic components limit the operation of the MOSFET at high frequencies. The typical transient response of a power MOSFET occurs over 10s of nanoseconds compared to a switching frequency occurring over 10s to 100s of microseconds. The dominant parasitic components and the transient response provides some general context for realising shaped switching transitions.

The transient response discussed in the remainder of this section outlines the turn-off sequence of the MOSFET. An analytical solution to the turn-off transients is presented, making simplified assumptions and considering only the major parasitic components of the MOSFET that dominate the transient response. Accurate and detailed solutions require computational resources, as is the case with this research which utilises SPICE simulation software and MOSFET SPICE models to simulate the transient response of a MOSFET with a controlled gate-drive.

#### 4.2.2.5 Turn-off Transients

The sequence of events for a MOSFET turn-off for a hard switching scenario is presented in this section. The intent is to explain the natural transient response of the MOSFET to a rapid drop in $v_{gs}$, which initiates the turn-off sequence. When achieving low-EMI, the turn-off sequence is still initiated. However, precise control is implemented to manipulate the transient response of the MOSFET where necessary. The turn-off sequence identifies the key parasitic components that influence the transient response of a MOSFET, which are required to be understood when controlling the gate-drive of the MOSFET for shaped transitions. The turn-off sequence can be described in four stages:

1. Initial turn-off sequence and delay time
2. Increasing drain-source voltage
3. Decreasing drain-source current
4. Voltage turn-off ring.

During the initial turn-off sequence, when the gate voltage is dropped towards the MOSFET $V_{th}$, the gate-source and gate-drain capacitances are discharged. The gate voltage remains greater than $V_{th}$, and $i_{ds}$ continues to flow through the MOSFET and is therefore still on. This initial stage is the delay stage, where $v_{gs}$ and can be modelled as a discharging capacitor. The time constant is characterised by the external and internal gate resistances and the internal gate-source and gate-drain capacitances. Initially, the MOSFET is assumed to be on where $v_{gs} = V_{GH},\ i_d = I_o,\ v_{ds} = 0$. To initiate the transition, the gate-drive voltage is rapidly changed from $V_{GH}$ to $V_{LH}$, causing $C_{gs}$ and $C_{gd}$ to start discharging. The time taken for $v_{gs}$ to reduce from $V_{GH}$ to $V_{th} + I_o/g_{fs}$ is the turn-off delay time $\tau_d$. The gate-source voltage decays according to [4]:

$$v_{gs} = (V_{GH} - V_{GL})\exp(-t/\tau_g) + V_{GL} \tag{4.4}$$

Where:

$$\tau_g = (R_{gd} + R_g)(C_{gd} + C_{gs}) \tag{4.5}$$

This phase ends when $v_{gs} = V_{th} + I_o/g_{fs}$:

$$\tau_d = \tau_g \ln\left[\frac{V_{GH} - V_{GL}}{V_{th} + I_o/g_{fs} - V_{GL}}\right] \tag{4.6}$$

Once the gate voltage falls to the Miller voltage of the MOSFET, $v_{ds}$ begins to increase. During this stage, $v_{ds}$ will begin to increase while $v_{gs}$ remains fairly constant at the Miller voltage, which also known as the plateau region of the MOSFET. During this stage of the transition, the MOSFET is depleting its stored charge to turn off, and $v_{ds}$ starts to increase. During this portion of the turn-off sequence, $C_{gd}$ is non-linear and will begin to decrease as the MOSFET $v_{ds}$ increases. During the next phase of the turn-off transients, once $v_{gs}$ reaches $V_{th} + I_o/g_{fs}$, it remains constant and $v_{ds}$ increases towards $V_{DD}$. While $v_{ds}$ is below $V_{DD}$, the full load current flows through the MOSFET. Therefore $i_{ds}$ and $v_{gs}$ remain constant. The increase in $v_{ds}$ can be described using [4]:

$$v_{ds} = \frac{I_o + g_{fs}(V_T - V_{GL})}{C_{ds} + [1 + g_{fs}(R_s + R_g)]C_{gd}}t \tag{4.7}$$

After a certain amount of time, the next stage of the turn-off sequence will begin, where $i_{ds}$ will begin to decrease, after $v_{ds}$ has reached $V_{DD}$. During this stage, $v_{ds}$ will overshoot $V_{DD}$ to a value $V_d$. By the end of this stage, $i_{ds}$ is zero, and $v_{gs}$ is below $V_{th}$. The equations for $i_{ds}$ is [14]:

$$i_{ds} = g_{fs}(v_{gs} - V_{th}) \tag{4.8}$$

In this stage, the gate capacitance discharges and $v_{gs}$ approaches $V_{GL}$ exponentially with the time constant $\tau_g$ [7]:

$$v_{gs} = \left(\frac{I_o}{g_{fs}} + V_{th}\right) \mathrm{e}^{-(t-t_2)/\tau_g} \tag{4.9}$$

Where $t_2$ is when $i_{ds}$ begins to decrease. During the final stage of the turn-off transient response, the gate voltage has fallen to $V_{GL}$, and $v_{ds}$ will typically oscillate. The major components contributing to the oscillations are $R_d$, $L_d$, $C_{ds}$, and $C_{gd}$. At the beginning of this stage, $v_{ds}$ is equal to $V_d$, which occurred at at $\tau_2$ during the previous stage. $v_{ds}$ defined by [4]:

$$v_{ds} = V_{DD} + [V_d - V_{DD}]\exp(-t/\tau_d)\cos\omega_d t \tag{4.10}$$

Where:

$$\tau_d = \frac{2L_d}{R_d} \tag{4.11}$$

and

$$\omega_d = \sqrt{\frac{1}{L_d C_d} - \left(\frac{R_d}{2L_d}\right)^2} \tag{4.12}$$

To demonstrate the turn-off transients of a MOSFET undergoing hard-switching, a half-bridge DC-DC converter is simulated using LTSPICE. The half-bridge includes two n-channel Infineon irfp150n power MOSFETs and a constant 10 A load. The irfp150n MOSFETs are imported into the simulation as SPICE models, which are analytical MOSFET models used to describe the behaviour of the semiconductor device in circuit simulations [16]. The major parasitic components included in the MOSFET model are summarised in Table 4.2. The turn-off transient response of an n-channel irfp150n power MOSFET is presented in Figure 4.5, which demonstrates the first three stages of the turn-off transients, which are the initial delay when $v_{gs}$ is reduced, increase in $v_{ds}$, and decrease in $i_{ds}$.

Table 4.2: MOSFET equivalent circuit description of major parasitic components.

| **Parameter** | **Value** | **Unit** | **Parameter** | **Value** | **Unit** |
|---|---|---|---|---|---|
| $V_{DD}$ | 100 | V | $g_{fs}$ | 14 | ℧ |
| $I_{ds}$ | 42 | A | $C_{iss}$ | 1900 | pF |
| $R_{DS(on)}$ | 36 | mΩ | $C_{oss}$ | 450 | pF |
| $V_g$ | ±20 | V | $L_s$ | 5.0 | nH |
| $V_{th}$ | 2.0 | V | $L_d$ | 13 | nH |

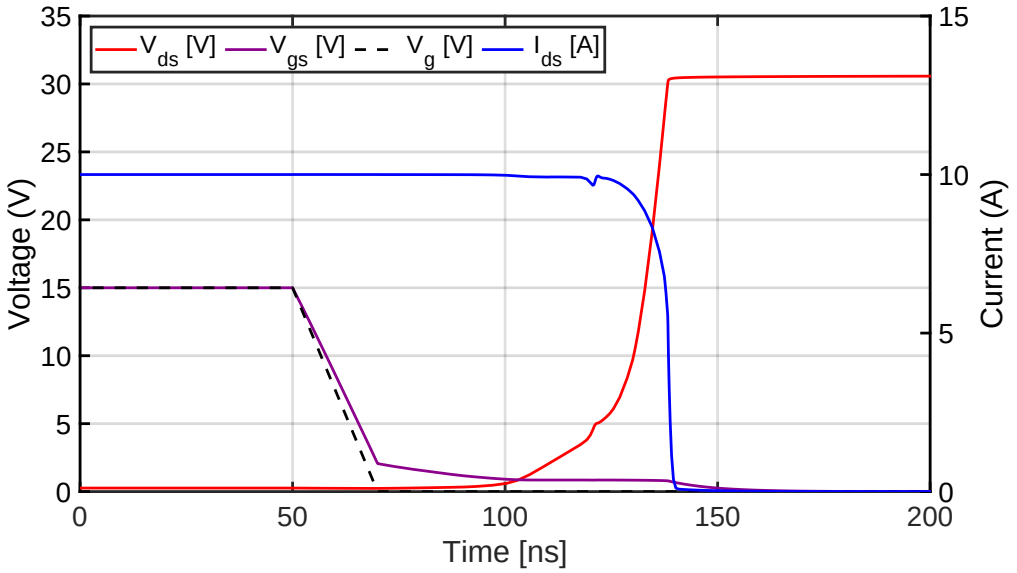



Figure 4.5: LTSPICE simulation results of MOSFET $v_{ds}$,$i_{ds}$,$v_{gs}$ waveforms during turn-off in a half-bridge DC-DC converter using irfp150n SPICE models.

The remainder of this Section presents the prototype half-bridge that is designed to generate shaped switching transitions. The gate-drive control strategy is outlined and compared to the hard-switching half-bridge discussed in this section, to identify how MOSFETs are controlled differently to conventional power converter switching strategies.

## 4.3 Shaped Switching Transitions in a Half-Bridge DC-DC Converter

### 4.3.1 Half-Bridge Circuit Overview

A prototype design and control philosophy of a half-bridge power converter capable of producing logistic-shaped switching transitions is presented in this section. The half-bridge shaped switching transition process intends to force the half-bridge midpoint voltage to follow a shaped low-EMI voltage reference waveform. The additional circuitry required to deliver the low-EMI logistic shaped switching transitions includes the current injection circuits for the top and bottom MOSFETs, the auxiliary branch, and the gate current injection circuit for each half-bridge MOSFET.

An overview of the half-bridge circuit is presented in Fig. 4.6, which includes two n-channel power MOSFETs with parallel capacitors connected in series between a voltage source. The injection circuits are connected in parallel to each power MOSFET, which consists of a power supply capable of delivering up to 10 A, and a MOSFET that

includes gate-drive control circuity to provide the required amount injection current for waveform shaping. Additionally, the half-bridge circuit includes an auxiliary branch with a smoothing inductor, $L_{aux}$, that is connected to the mid-point of the half-bridge. When the auxiliary branch is operated, the current will begin to ramp such that the $i_{ds}$ of the MOSFET undergoing waveform shaping is compensated. Correct timing and operation of the auxiliary branch will ensure the $I_o + I_{aux} = 1$ pu criteria is met.

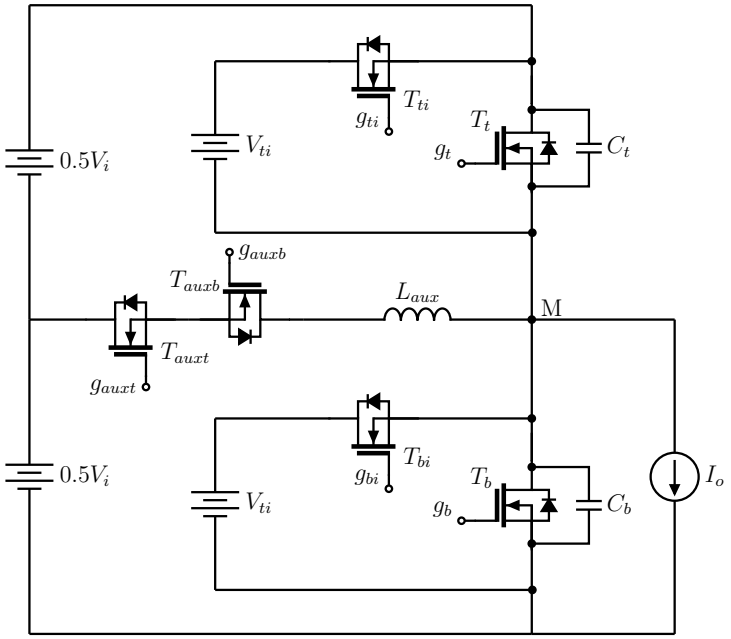



Figure 4.6: Half-bridge prototype equivalent circuit.

The half-bridge differs from the AVC for IGBTs [17], and closed-loop gate control with on-state resistance compensation [18] approaches presented in the literature by including current injection circuitry to provide waveform shaping and parallel capacitors. The capacitors ensure the MOSFET $v_{ds}$ is controlled since the current in the capacitors controls the MOSFET $dv_{ds}/dt$. The on-state resistance compensation approach introduces quantisation in the $v_{ds}$ that causes high-frequency EMI, which the injection circuity and parallel capacitors circumvent.

The injection circuit will draw current away from the capacitors, such that $dv_{ds}/dt$ is identical to the reference logistic-shaped waveform. At $0.5V_i$, the current in the capacitors reaches a maximum, which is $0.5I_o$. The injection circuit must be capable of diverting current away from both capacitors and therefore compensating $v_{ds}$ as required. The following equation describes the injection current:

$$i_{injection} = I_o - 2C\frac{dv_{ds}}{dt} \tag{4.13}$$

The intention is to get $v_{gs}$ to fall to a value that is slightly larger than the Miller plateau region of the MOSFET and over a time scale that is longer than the natural transient response time to invoke slower transients for low-EMI applications. A controlled fall in $v_{gs}$ will cause the $C_{gd}$ and $C_{gs}$ to discharge, and the change is significant enough to cause enough stored charge in the MOSFET to be depleted to cause the $v_{ds}$ to increase slowly.

In addition to slowing the initial turn-off stages, the intermediate stage of the MOSFET turn-off can also be precisely controlled. As previously discussed, the $v_{ds}$ will begin to increase when $v_{gs}$ decreases below the Miller plateau region in response to a rapid drop in the gate drive voltage. The rapid decrease in $v_{gs}$ is from a predefined high-state ($V_{GH}$) to a predefined low-state ($V_{GL}$), where the MOSFET is known to be off. In the intermediate regions where the MOSFET $v_{ds}$ increases and the $i_{ds}$ decreases, controlling the $v_{gs}$ between the Miller plateau region and $V_{th}$ is critical for shaping the $v_{ds}$ of a MOSFET.

For gate voltages above the Miller plateau region, the MOSFET is on, and $v_{ds}$ and $i_{ds}$ do not change. Similarly, for a $v_{gs}$ below $V_{th}$, the MOSFET is off, and $v_{ds}$ and $i_{ds}$ do not change either. When controlling $v_{ds}$ during turn-off, it is important to note the following characteristics:

- A slow $dv_{gs}/dt$ where $v_{gs}$ is just below the Miller plateau region will invoke a slow transient response. In other words, the $dv_{ds}/dt$ will be slow.
- A fast $dv_{gs}/dt$ where $v_{gs}$ is reduced to below or near $V_{th}$ will invoke a fast transient response. In other words, the $dv_{ds}/dt$ will be fast.
- A slow $dv_{gs}/dt$ for changes in $v_{gs}$ values ranging between the Miller plateau region and $V_{th}$ will invoke a slow transient response. However, there is a point where all the MOSFET charge becomes entirely depleted, and the MOSFET will be OFF.
- Conversely, a fast $dv_{gs}/dt$ for changes in $v_{gs}$ values ranging between the Miller plateau region and $V_{th}$ will invoke a fast transient response.

All modes of operation are discussed throughout the remainder of this section. In the operation of the switching half-bridge with added drain-source capacitance on the power MOSFETs, in each switching transition, one power MOSFET is gradually turned off, and then the other power MOSFET is eventually turned on at the end of the transition. The power MOSFET undergoing a controlled turn-off from the beginning of the transition is the $\alpha$-MOSFET. The power MOSFET turned on at the end of the transition is called the $\beta$-MOSFET. To designate which MOSFETs are being controlled, the controlled power MOSFET is the $\alpha$-MOSFET, and the controlled injection MOSFET

is the $\beta$-injection MOSFET since it is connected in parallel to the $\beta$-MOSFET. The $\alpha$- and $\beta$-MOSFET identification is used throughout the remainder of this dissertation to explain the various modes of operation, discuss the simulation results, explain the control system implementation using the FPGA and discuss the laboratory results. To summarise, the $\alpha$-MOSFET is:

- The bottom MOSFET in a rising transition of the half-bridge mid-point voltage.
- The top MOSFET in a falling transition of the half-bridge mid-point voltage.

Similarly, the $\beta$-MOSFET is:

- The top MOSFET in a rising transition of the half-bridge mid-point voltage.
- The bottom MOSFET in a falling transition of the half-bridge mid-point voltage.

In this control implementation, the injection circuit is only used to inject current to displace current in the $\beta$-MOSFET, and so is called $\beta$-injection MOSFET. There is no $\alpha$-injection occurring in this control implementation.

### 4.3.2 Demonstrating Performance with a Simplified Circuit

A simplified circuit is used to illustrate the desired behaviour of the half-bridge switching. Although this circuit does not take into account the transient responses of the power and injection MOSFETs, it assists in identifying the timing required of the various elements in the circuit. The simplified circuit is shown in Figure 4.7, which replaces the power MOSFETs with variable resistors and the injection circuit with ideal current sources. Additionally, the auxiliary branch MOSFETs are replaced with an ideal switch.

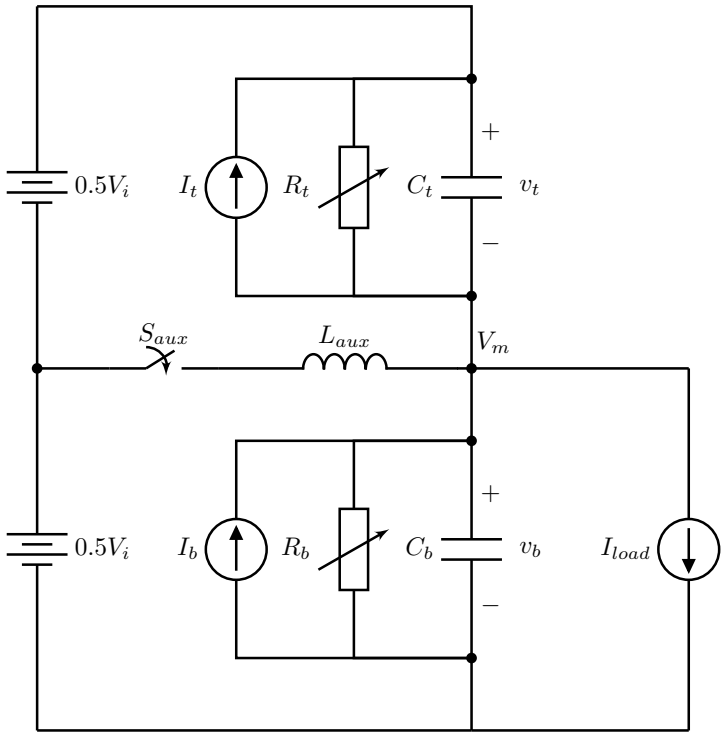



Figure 4.7: Simplified half-bridge circuit.

Considering a falling transition of the midpoint voltage, the simplified circuit undergoes a shaped transition by varying $R_t$, which causes $V_m$ to start decreasing. The transition commences with the following initial conditions: $I_{Rt} = I_{load}$, $I_{Rb} = 0$ A, $R_t = 10$ m$\Omega$, $I_t = 0$ A, $V_t = 0$ V, $I_b = 0$ A, $R_b =$ huge, $V_b = V_i$, $I_{aux} = 0$ A, $S_{aux} =$ off. Note that $R_b$ is denoted as a 'huge' resistance, which is substantially large enough to cause negligible current to conduct, which represents a MOSFET being off. Following which, $R_t$ is increased such that the voltage waveform $V_t$ changes to follow a reference profile. As $R_t$ is increased, $C_t$ begins to charge, while $C_b$ begins to discharge.

For an ideal logistic transition, which considers that the maximum derivative of the logistic transition that is limited by the value of $C_t$ and $C_b$, will increase $R_t$ such that all the current has diverted to both capacitors by the time $V_t$ reaches half the waveform amplitude, $0.5V_i$. Once all the current has transferred to the capacitors ($0.5I_{load}$ downwards in $C_t$ and $0.5I_{load}$ upwards in $C_b$), at the mid-point voltage $V_m$, the injection circuit will commence to offset the current in $C_t$ and $C_b$, allowing $V_b$ to start reducing its slope to follow the desired logistic-shaped transition. It is imperative that the injected current $I_b$ should allow the voltages across the capacitors to be shaped. Once $I_b$ reaches $I_{load}$, the switching transition is complete and $V_b$ has reached 0 V, and $V_t$ has

reached $V_i$. At this stage the $R_b$ can be set to 10 m$\Omega$, and $I_b$ can be set to 0 A, which represents the bottom MOSFET being turned on the the bottom injection circuit being turned off, respectively. A while later, the next switching transition can begin, which determined by the duty cycle of the power converter PWM switching strategy.

The next transition undergoes a shaped transition by controlling $R_b$, which causes the midpoint voltage ($V_m$) to undergo a rising transition. The transition commences with the following initial conditions: $I_{Rt} = 0$ A, $I_{Rb} = I_{load}$, with $R_t =$ huge, $I_t = 0$ A, $V_t = V_i$, $I_b = 0$ A, $R_b = 10$ m$\Omega$, $V_b = 10$ mV, $I_{aux} = 0$ A, $S_{aux} =$ off. Before the shaped transition commences, the auxiliary branch is switched on via $S_{aux}$ causing $I_{aux}$ to ramp at rate set by $L_{aux}$. When $I_{aux} < -I_{load}$, $I_{load}$ is completely compensated and the current in $R_b$ is now downwards and can begin to be increased to control the shape of $V_b$. $R_b$ continues to be increased to provide a logistic shaped transition, with the intent that $V_b$ reaches $0.5V_i$ at the point when $I_{aux} = -2I_{load}$. At this point, $R_b$ should be huge and the current in $C_b$ should be $0.5I_{load}$ downwards (and $0.5I_{load}$ upwards in $C_t$). Once the voltage reaches $0.5V_i$, the top injection current is initiated to offset current in $C_t$ and $C_b$ to allow $V_t$ to start reducing its slope and continue to follow the shaped reference profile. When $I_t$ reaches $I_o$, the switching transition is complete and $V_t = 0$ V. $R_t$ can be set to 10 m$\Omega$, and then $I_t$ can be set to 0 A.

Illustrative waveforms of the simplified half-bridge circuit are provided considering $R_t$ being varied to produce a logistic shaped switching transition. The calculation considers a voltage amplitude of $V_i = 30$ V and $I_{load} = 10$ A. The logistic reference is synthesised with $\tau_t = 5$ $\mu$s, and a growth rate of $3 \times 10^6$. Note the growth-rate was selected to provide observable shaped transitions throughout the entire transition time, which corresponds to ideal capacitor values of $C_t = C_b = 222$ nF. The voltage waveforms of $R_t$ and $R_b$ are presented in Figure 4.8. Figure 4.9 shows the current in $R_t$, $C_t$, $C_b$ and $I_b$ during the entire transition. Lastly, Figure 4.10 shows $R_t$ being varied between 1 $\mu$s to 2.4 $\mu$s, which is just before $0.5V_i$ is reached. Note that $R_t$ begins to increase rapidly to ensure the current in $R_t$ approaches zero and the mid-point circuit voltage $V_m$ approaches $0.5V_i$. Additionally, at the mid-point $R_t$ becomes huge, which is representative of a MOSFET being off. Additionally, once $I_b$ reaches 10 A at the end of the transition $R_b$ is made very small, which is representative of a MOSFET being on. Once waveform shaping is complete $I_b$ will stop injecting current.

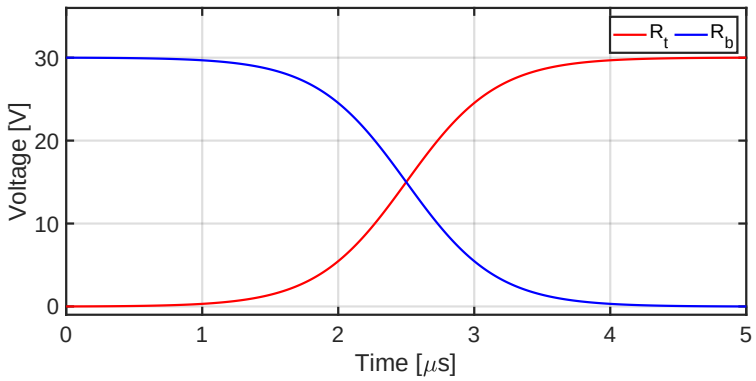



Figure 4.8: Illustrative voltage waveforms of the simplified circuit.

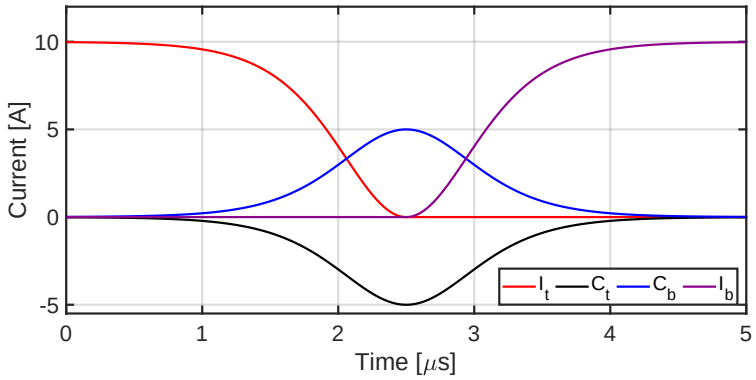



Figure 4.9: Illustrative current waveforms of the simplified circuit.

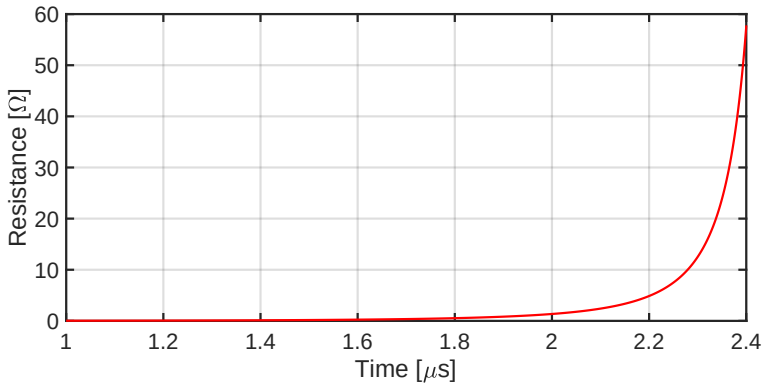



Figure 4.10: Illustrative variable resistance of the simplified circuit.

#### 4.3.2.1 Half-Bridge Prototype Control Signal Sequencing

The half-bridge prototype circuit during a shaped switching transition for both power MOSFETs is presented in Fig. 4.11, where each MOSFET coloured in Fig. 4.11(a) corresponds to the control signal in Fig. 4.11(b). The waveform shaping is achieved by controlling a power MOSFET ($T_t/T_b$ in Fig. 4.11(a)) during the first half of the shaped transition and an injection MOSFET ($T_{ti}/T_{bi}$ in Fig. 4.11(a)) for the second half of the transition. The power MOSFETs $T_b/T_t$ and injection MOSFETs $T_{bi}/T_{ti}$ are labelled in Fig. 4.11(b) to show when they are designated the $\alpha$-MOSFET and $\beta$-injection MOSFET during the control sequence of the half-bridge DC-DC converter. Note that, for simplicity, a controlled portion of a power or injection MOSFET is shown as a downward ramp to designate when the MOSFET is undergoing gate-drive control.

All modes of operation are discussed throughout the remainder of this section, considering the control of the $T_b/T_{ti}$ MOSFET pair, which are the $\alpha$-MOSFET ($\alpha$) and $\beta$-injection MOSFET ($\beta i$), respectively. Note, the control strategy of the $T_t/T_{bi}$ is identical since the MOSFET pairing is complimentary. When subsequently shaped transitions occur, the designation of the $\alpha$-MOSFET and $\beta$-injection will swap to the $T_t/T_{bi}$ MOSFET pairing. Additionally, an illustrative example of the half-bridge circuit during the various modes of operation is presented in Figure 4.12 to facilitate the discussion of each mode of operation discussed throughout the remainder of this section. Figure 4.12(a) presents the half-bridge mid-point voltage, and Figure 4.12(b) presents the power MOSFET, injection-MOSFET, and parallel capacitor currents. Lastly, Figure 4.12(c) presents the power MOSFET and injection MOSFET gate-drive voltages.

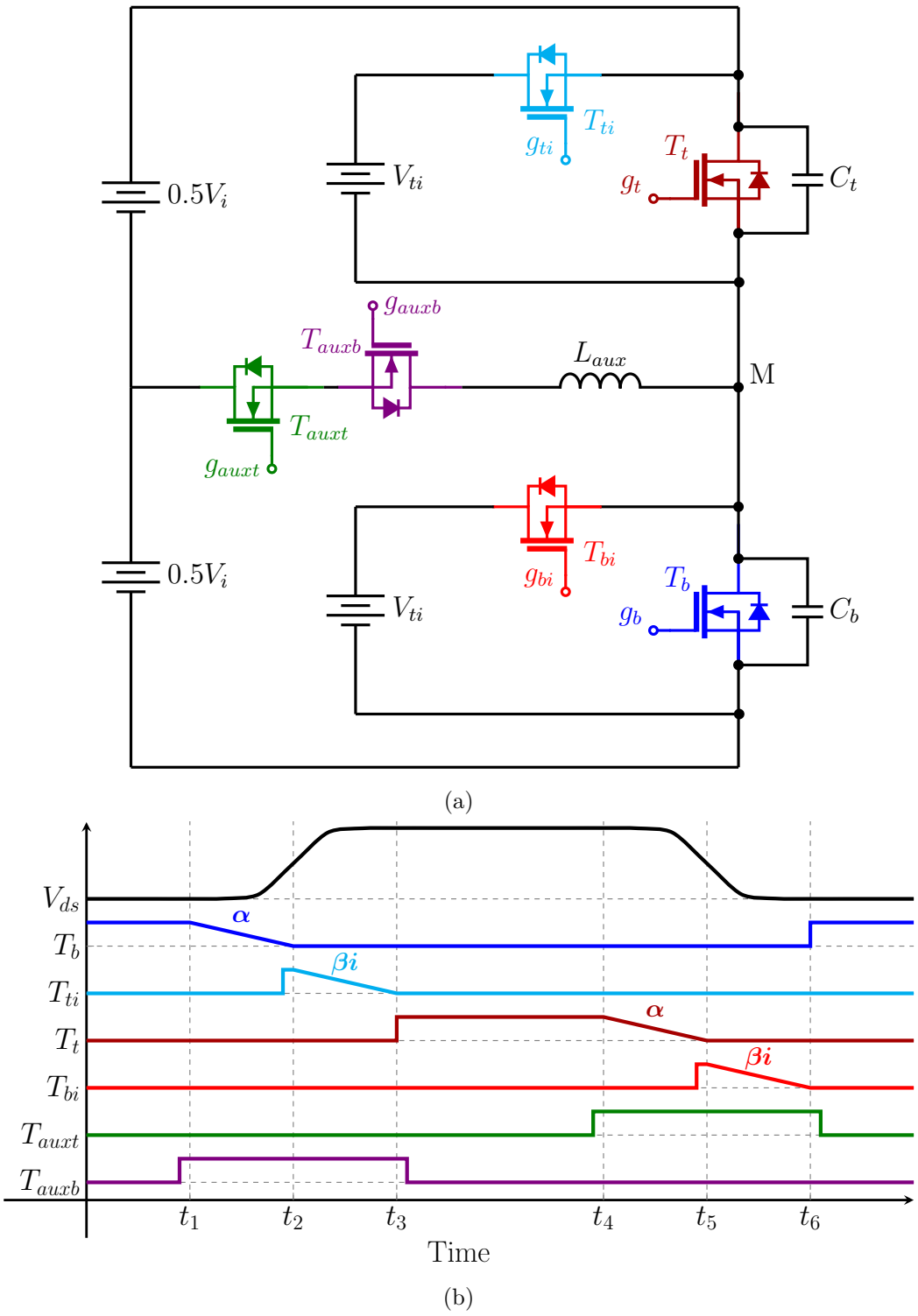



Figure 4.11: Half-bridge prototype control signal sequencing.

#### 4.3.2.2 Waveform Overview

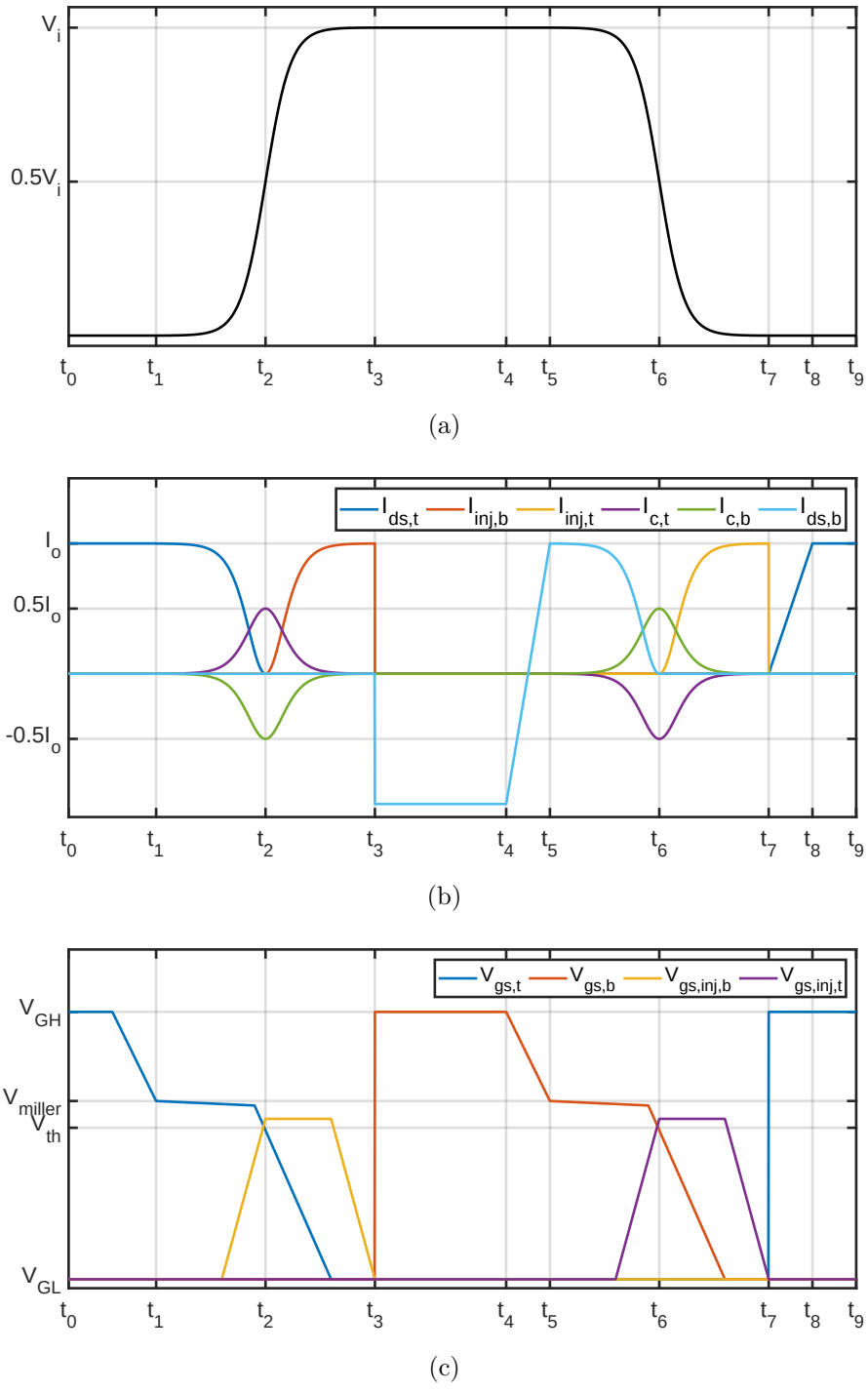



Figure 4.12: Illustrative example of the waveforms during the various modes of operation for the half-bridge circuit.

### 4.3.3 Low-EMI Half-Bridge: Modes of Operation

#### 4.3.3.1 Overview

This section provides an overview of the modes of operation of the half-bridge circuitry. For each mode, a half-bridge circuit is included where only the conducting parts of the circuitry are shown in black. All inactive parts of the circuitry are coloured grey. Note that the modes of operation describe the scenario where the half-bridge power converter supplies maximum load current, and the auxiliary branch can deliver up to twice the load current. This mode is referred to as full-load operation, and the auxiliary branch current is required to provide current in only one direction (i.e. $T_{auxb}$ only). There are other modes where the half-bridge does not supply full-load current. Therefore the auxiliary branch is required to provide current in both directions where both $T_{auxt}$ and $T_{auxb}$ are operated.

Lastly, the circuit can operate under no-load. In this mode, the auxiliary branch must provide current in both directions and reach a large enough current magnitude to allow the capacitors to charge and discharge fully. In the case of the hardware implementation, this current magnitude is 10 A. Under no-load conditions, the auxiliary branch is required to supply $I_{aux} = \pm$ 1 pu for both the top and bottom power MOSFETs undergoing a controlled, shaped transition.

Figure 4.12 in Section 4.3.2.2 provides a waveform overview for the prototype half-bridge topology undergoing a rising and falling transitions at the mid-point of the power converter. The illustrative example presented the expected behaviour of the mid-point voltage, all power and injection MOSFET $i_{ds}$, all power and injection MOSFET $v_{gs}$, and the parallel capacitor currents. Generalised timing instances are presented so each stage discussed throughout the remainder of this section can be referred to Figure 4.12. Furthermore, since the timing instances are generalised, the auxiliary current is not included. Instead, $i_{ds}$ of the the bottom MOSFET is ramped during the time interval $[t_4, t_5]$ and the $i_{ds}$ of the the top MOSFET is ramped in the time interval $[t_7, t_8]$ to illustrate the effects of the auxiliary branch current on the $i_{ds}$ of the power MOSFETs.

#### 4.3.3.2 Stage 1 $[\mathbf{t_0}, \mathbf{t_1}]$:

Stage 1 is the initialisation stage for the modes of operation and is where the $\alpha$-MOSFET is on, and the $\beta$-MOSFET is off. Since the half-bridge is designed to operate the MOSFETs as complementary pairs, the MOSFETs are only controlled to form a shaped rising transition during turn off. For this discussion, the top MOSFET $v_{ds}$ is initially undergoing a shaped rising transition. Therefore the controlled voltage $V_m$ will undergo a shaped falling transition. Note that the gate-drive voltage is sufficiently large, $V_{GH}$, to ensure the $\alpha$-MOSFET is on and conducting.

The operational modes will commence by causing the $\alpha$-MOSFET $v_{ds}$ to undergo a rising transition, which causes the $\beta$-MOSFET $v_{ds}$ to undergo a falling transition. The $\alpha$-MOSFET $v_{ds}$ undergoing a shaped rising transition will commence with the following initial conditions. Load current is $I_o$, $\alpha$-MOSFET $v_{ds} = V_i$, $\beta$-MOSFET $v_{ds} = 0$ V, $\alpha$-MOSFET $v_{gs} = V_{GH}$, $\beta$-MOSFET $v_{gs} = V_{GL}$, both injection circuits are off, and the auxiliary branch is off.

The half-bridge prototype circuit during the initialisation stage is presented in Figure 4.13. All of the conducting paths of the circuit are coloured black, and all non-conducting paths are coloured grey. The half-bridge circuit designates the top power MOSFET as the $\alpha$-MOSFET ($\alpha$) and the bottom injection MOSFET as the $\beta$-injection MOSFET ($\beta i$). Note that when the subsequently shaped transitions take place, the designation of the $\alpha$-MOSFET and $\beta$-injection will swap to the bottom power MOSFET and top injection MOSFET, respectively. The half-bridge circuits for the modes of operation beyond Stage 7 demonstrate the change in $\alpha$-MOSFET and $\beta$-injection designation.

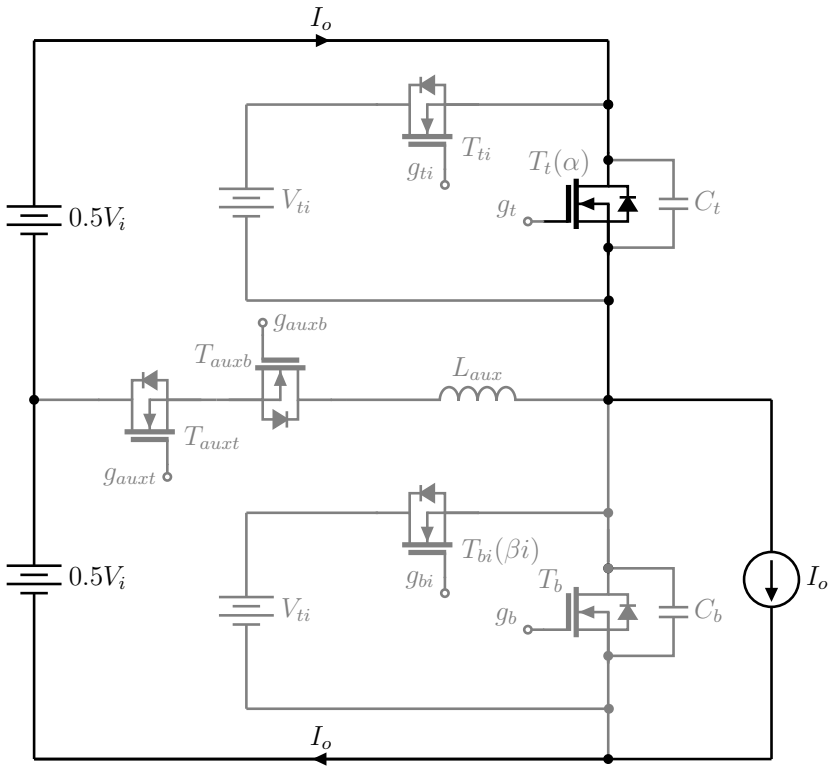



Figure 4.13: Stage 1 of the half-bridge prototype circuit.

#### 4.3.3.3 Stage 2 $[\mathbf{t_1}, \mathbf{t_2}]$:

The gate drive voltage profile of the $\alpha$-MOSFET commences and is required to get $v_{ds}$ to follow the $v_{ds}$ reference profile to $0.5V_i$ of the shaped transition. During the control of the gate drive, the current is diverted to the capacitors, $C_t$ and $C_b$. Once the gate-drive stage of the $\alpha$-MOSFET is complete, all the current has diverted to the capacitors ($|I_{C_t}| = |I_{C_b}| = 0.5I_o$) and the $\alpha$-MOSFET is turned off by the time $v_{ds}$ has reached $0.5V_i$. The mid-point defines the point where the load current $I_o$ is diverted to the capacitors, which is desired for ideal shaped transitions considering low-EMI outcomes. However, in applications where greater efficiency is required, the target voltage can be set lower, which is explored further in Chapter 6 of this dissertation.

During this stage, the half-bridge control system will control the $\alpha$-MOSFET gate voltage to shape the $\alpha$-MOSFET $v_{ds}$ as defined by the reference profile. The half-bridge prototype circuit during Stage 2 is presented in Figure 4.14. All conducting paths of the circuit are coloured black.

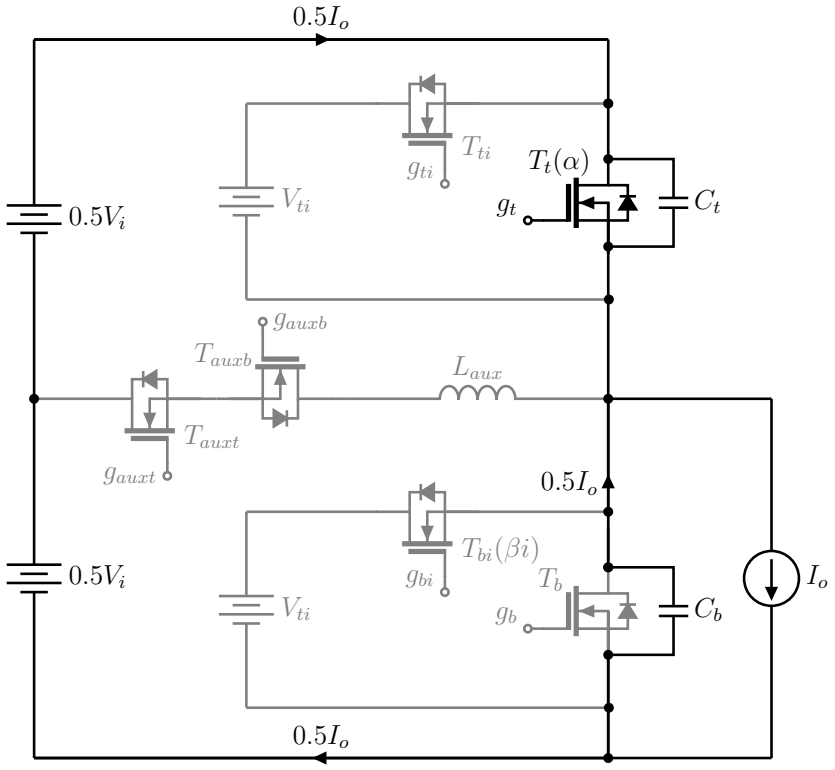



Figure 4.14: Stage 2 of the half-bridge prototype circuit.

#### 4.3.3.4 Stage 3 $[\mathbf{t_2}, \mathbf{t_3}]$:

The current injection profile of the $\beta$-injection MOSFET circuit is switched on once the $\alpha$-MOSFET $v_{ds}$ reaches $0.5V_i$. The $\beta$-injection MOSFET will inject current to offset the current in the parallel capacitors allowing the slope of the $\alpha$-MOSFET $v_{ds}$ to reduce, ensuring the $\alpha$-MOSFET $v_{ds}$ is shaped as per the reference profile. Essentially, the $\alpha$-MOSFET response is slowed by the current injection, which allows the $\alpha$-MOSFET $v_{ds}$ to follow the reference profile. By the end of the $\beta$-injection MOSFET gate-drive stage, $C_t$ is completely charged, and $C_b$ is completely discharged. Both the capacitor currents have reached $I_{C_t} = I_{C_b} = 0$ A by the time the $\alpha$-MOSFET $v_{ds}$ has reached $V_i$.

During this stage, the half-bridge control system will control the $\beta$-injection MOSFET gate voltage to shape the half-bridge mid-point voltage as defined by the reference profile. As previously discussed, the $\beta$-injection MOSFET gate-drive seeks to inject a current that will compensate the inherent transient response of the $\alpha$-MOSFET allowing the half-bridge mid-point voltage to be shaped. The half-bridge prototype circuit during Stage 3 is presented in Figure 4.15. All conducting paths of the circuit are coloured black.

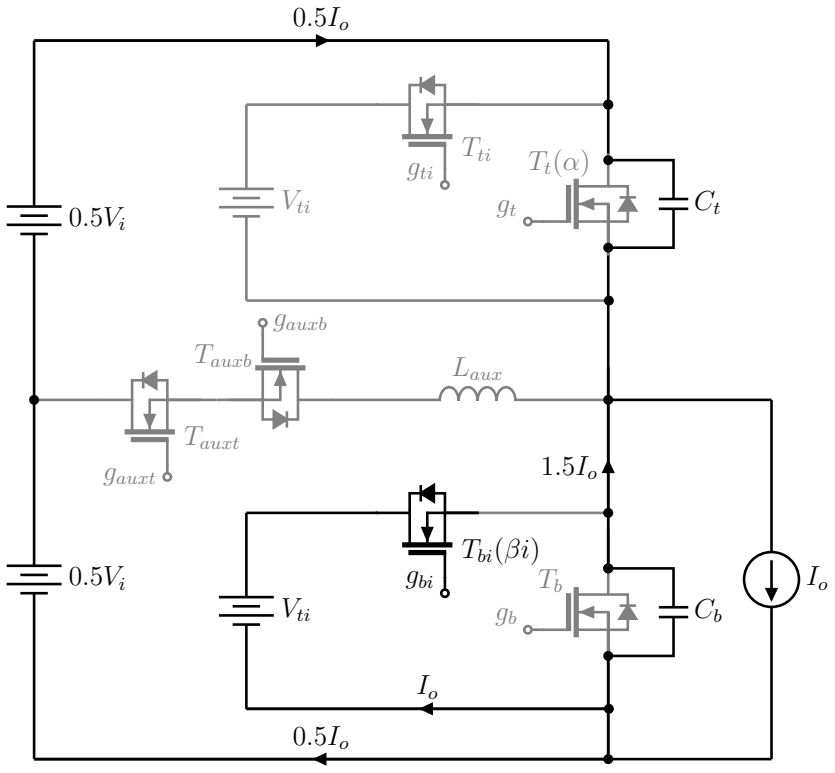



Figure 4.15: Stage 3 of the half-bridge prototype circuit.

#### 4.3.3.5 Stage 4 $[\mathbf{t_3}, \mathbf{t_4}]$:

The circuit has completed the current injection stage by the time the $\alpha$-MOSFET $v_{ds}$ has reached $V_i$, denoting the end of the shaped transition control. The $\beta$-injection MOSFET circuit is switched off, and the $\beta$-MOSFET $v_{gs}$ is ramped to $V_{GH}$ at the beginning of the stage, which is required to ensure the $\alpha$-MOSFET $v_{ds}$ remains at the waveform amplitude of $V_i$. $v_{ds} = V_i$ occurs when the injection current reaches $I_o$, which indicates that the switching transition is complete. Turning on the $\beta$-MOSFET at this stage is essential to minimise conduction losses as the on-state resistance of the MOSFET should be reduced as current starts to be diverted into the MOSFET branch. Once the current in the $\beta$-MOSFET switching branch reaches $I_o$, the switching transition is complete.

Note that the modes of operation represent an ideal scenario, and during prototype implementation, there will be overlap between the various modes of operation. For example, the gate-drive of the $\beta$-injection MOSFET starts before the $\alpha$-injection gate-drive is complete, and all current is diverted to the parallel capacitors at half the waveform amplitude, $0.5V_i$. This allows for the $\beta$-injection circuit to be prepared by providing sufficient charge build up across the gate such that the $\beta$-injection MOSFET will begin conduction with minimal delay, which is desirable for achieving the best practical shaping.

Additionally, this stage allows the circuit to reach steady-state conditions before commencing the subsequent controlled, shaped transition for the bottom power MOSFET and top injection MOSFET. The steady-state conditions that must be met before the next transition can occur is that $I_o$ is entirely conducting through the $\beta$-MOSFET, $\alpha$-MOSFET $v_{gs} = V_{GL}$, $\beta$-MOSFET $v_{gs} = V_{GH}$, $\alpha$-MOSFET $v_{ds} = V_i$, $\beta$-MOSFET $v_{ds}$ = 0 V, and the auxiliary branch is switched off. Note, in practice, the $\beta$-MOSFET $v_{ds}$ will not be precisely 0 V due to the on-state resistance of the MOSFET. However, for discussion purposes, the on-state resistance is assumed to be negligible. The half-bridge prototype circuit during Stage 4 is presented in Figure 4.16. All conducting paths of the circuit are coloured black.

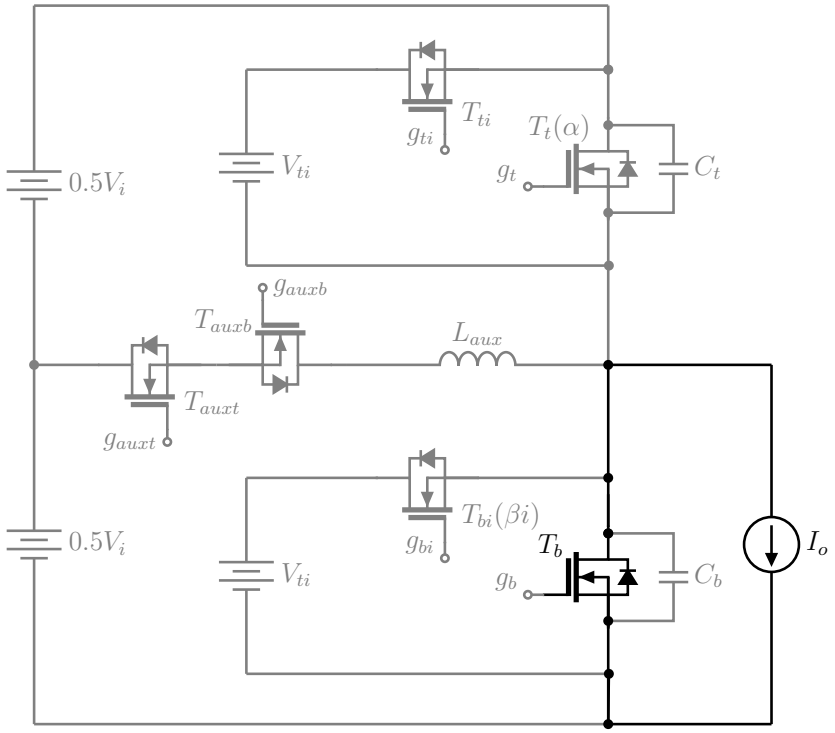



Figure 4.16: Stage 4 of the half-bridge prototype circuit.

#### 4.3.3.6 Stage 5 $[\mathbf{t_4}, \mathbf{t_5}]$:

Note at this stage of the half-bridge operation, and the bottom power MOSFET becomes the $\alpha$-MOSFET, and the top injection MOSFET becomes the $\beta$-injection MOSFET. Figure 4.17 shows the designation of $\alpha$ and $\beta i$ for the bottom power MOSFET and the top injection MOSFET, respectively. The auxiliary branch is turned on, which causes the auxiliary branch inductor to start ramping up to $2I_o$ by the time the half-bridge mid-point voltages reaches $0.5V_i$. Additionally, the auxiliary branch current is required to ensure the $\alpha$-MOSFET $i_{ds}$ reaches $I_o$ before the $\alpha$-MOSFET gate-drive control commences. Therefore, the direction of current flow in each MOSFET is $I_o$ and the same control strategy to achieve waveform shaping can be implemented. Once the bottom MOSFET current is compensated for, the $\alpha$-MOSFET can commence the controlled turn-off. Note that the timing of the auxiliary branch must ensure the auxiliary branch current reaches $2I_o$. The half-bridge prototype circuit during Stage 5 is presented in Figure 4.17. All conducting paths of the circuit are coloured black.

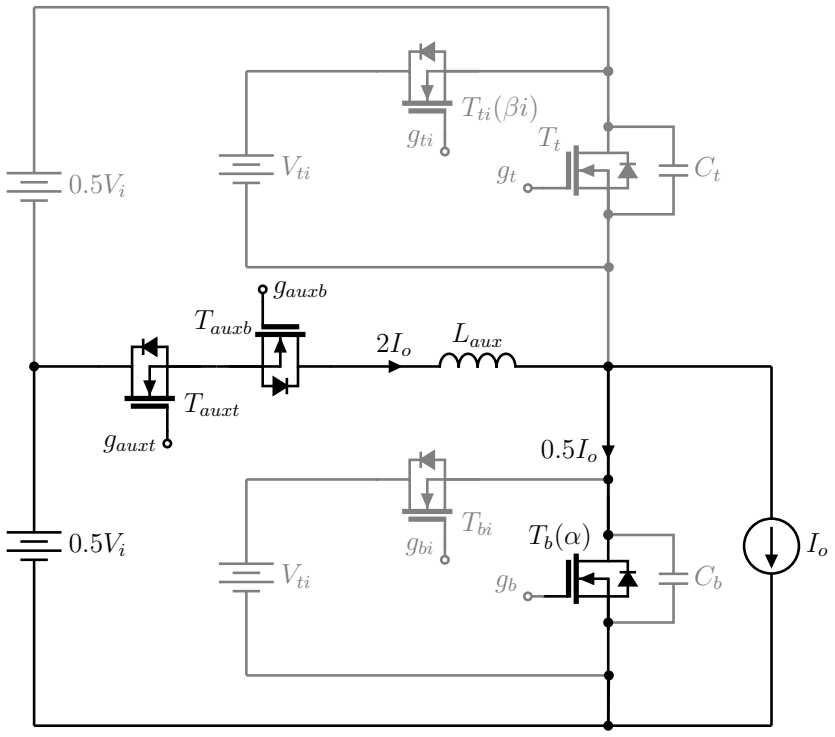



Figure 4.17: Stage 5 of the half-bridge prototype circuit.

#### 4.3.3.7 Stage 6 $[\mathbf{t_5}, \mathbf{t_6}]$:

The gate drive voltage profile of the $\alpha$-MOSFET commences and is required to ensure $v_{ds}$ is follows the $v_{ds}$ reference voltage until $0.5V_i$ is reached. More detail regarding the gate-drive stage can be found in Section 4.3.3.3 - Stage 2. The half-bridge prototype circuit during Stage 6 is presented in Figure 4.18. All conducting paths of the circuit are coloured black.

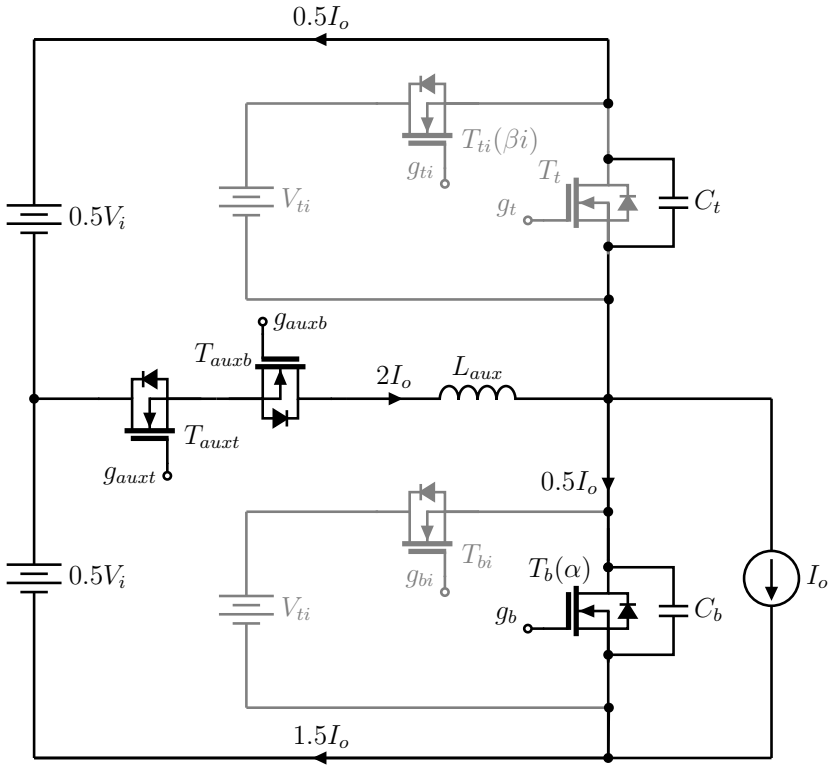



Figure 4.18: Stage 6 of the half-bridge prototype circuit.

#### 4.3.3.8 Stage 7 $[\mathbf{t_6}, \mathbf{t_7}]$:

The current injection profile of the $\beta$-injection MOSFET circuit is switched on until $V_i$ is reached. More detail regarding the current injection stage can be found in Section 4.3.3.4 - Stage 3. Note that the current injection magnitude for the $\beta$-injection MOSFET circuit does not need to reach $I_o$, which is required for the $\beta$-injection MOSFET in the previous transition. There is also some compensation being provided by the auxiliary branch, as the current magnitude is ramping down from $2I_o$ to 0 A. By the and of Stage 7, the circuit has completed the current injection stage, $C_b$ is completely charged, and $C_t$ is completely discharged when the half-bridge mid-point voltage has reached $V_i$. The half-bridge prototype circuit during Stage 7 is presented in Figure 4.19. All conducting paths of the circuit are coloured black.

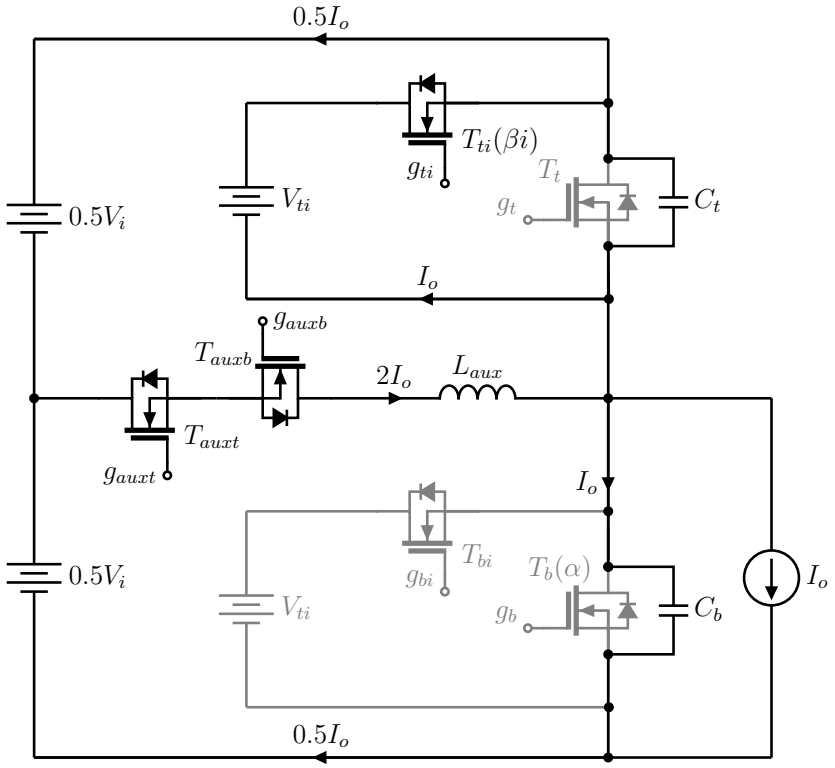



Figure 4.19: Stage 7 of the half-bridge prototype circuit.

#### 4.3.3.9 Stage 8 $[\mathbf{t_7}, \mathbf{t_8}]$:

The $\beta$-injection MOSFET circuit is switched off, and the $\beta$-MOSFET gate-drive is ramped to $V_{GH}$, to ensure the $\alpha$-MOSFET $v_{ds}$ remains at $V_i$. Note that to handle the compensation effects of the auxiliary branch, the timing between turning the $\beta$-injection MOSFET off and the $\beta$ MOSFET on is slightly different to the timing that is required for Section 4.3.3.5 - Stage 4. The half-bridge prototype circuit during Stage 8 is presented in Figure 4.20. All conducting paths of the circuit are coloured black.

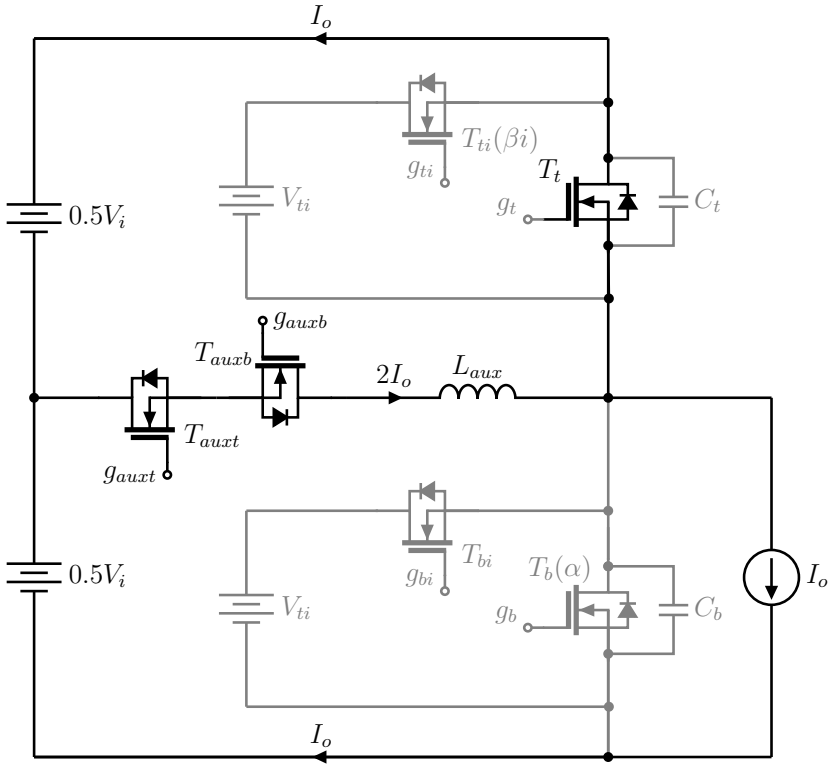



Figure 4.20: Stage 8 of the half-bridge prototype circuit.

#### 4.3.3.10 Stage 9 $[t_8, t_9]$:

Lastly, the auxiliary branch is switched off. By this stage, the current in the $\beta$-MOSFET reaches $I_o$, and the switching transition is complete. The circuit will remain in this state until the next switching transition, governed by the switching frequency of the PWM control. The modes of operation describe how the waveform shaping is integrated with a power converter that works under load, which is the next progression beyond shaping transitions of just MOSFETs and IGBTs. At this point, the steady-state conditions should be the same as Section 4.3.3.2, and the process can be repeated.

The steady-state conditions that must be met before the next transition can occur is $I_o$ is entirely conducting through the $\beta$-MOSFET, $\alpha$-MOSFET $v_{gs} = V_{GL}$, $\beta$-MOSFET $v_{gs} = V_{GH}$, $\alpha$-MOSFET $v_{ds} = V_i$, $\beta$-MOSFET $v_{ds} = 0$ V, and the auxiliary branch is switched off. The half-bridge prototype circuit during Stage 9 is presented in Figure 4.21. All conducting paths of the circuit are coloured black.

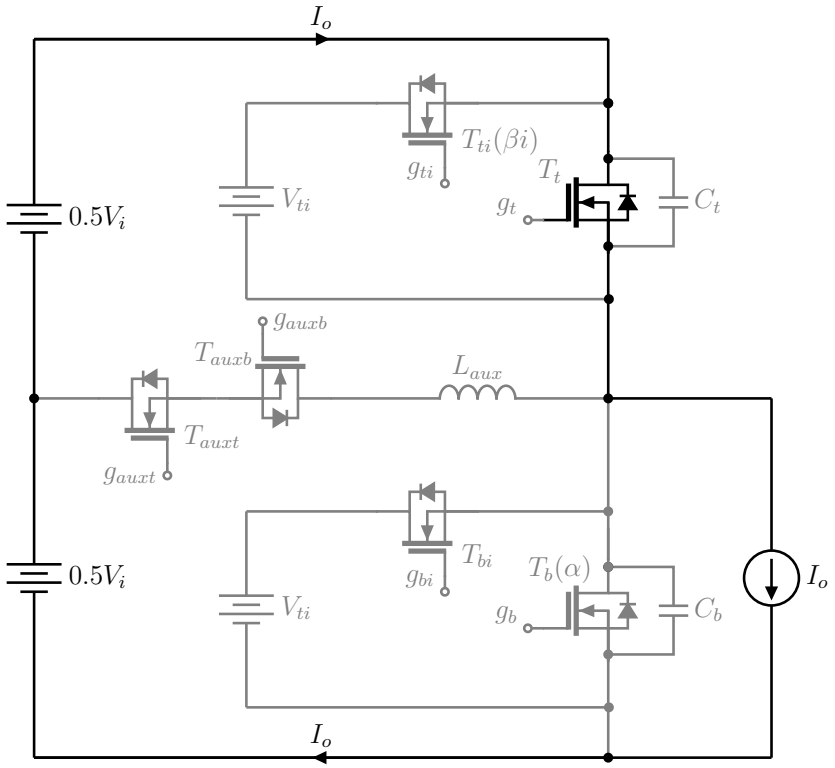



Figure 4.21: Stage 9 of the half-bridge prototype circuit.

## 4.4 Half-Bridge Control Algorithm

The power MOSFET gate-drive and injection MOSFET gate-drive utilise the same control algorithm to shape their respective half of the shaped switching transitions. An illustrative example of the gate-drive control algorithm is presented in Figure 4.22. The reference logistic profile used in the illustrative plot is offset to provide a distinct error between the reference and measured logistic transitions to demonstrate the approach of the algorithm. Additionally, the $\alpha$-MOSFET $v_{gs}$ and $\beta$-injection MOSFET $v_{gs}$ signals are both scaled by a factor of four to provide clarity.

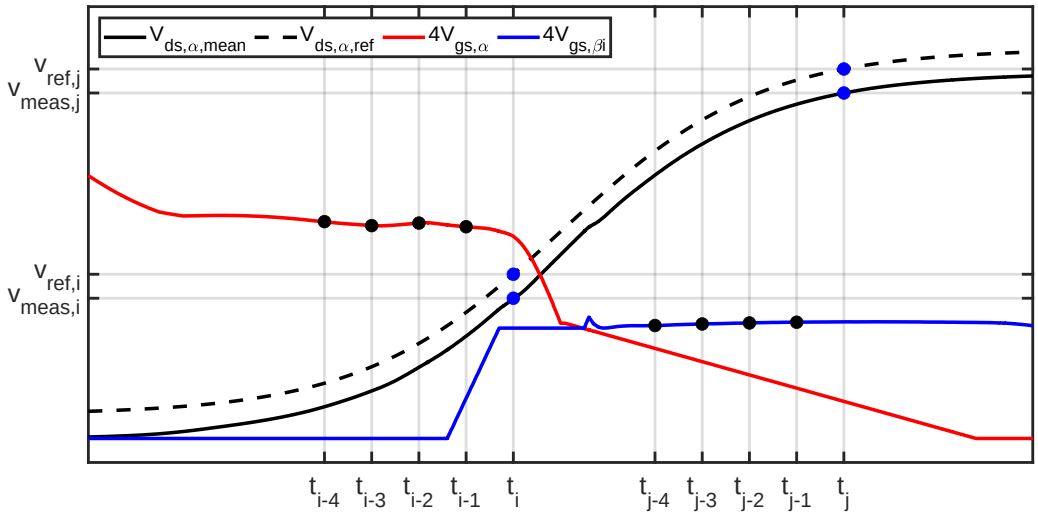



Figure 4.22: Half-bridge gate-drive control algorithm illustrative example.

The primary objective of the algorithm is to provide a form of corrective feedback that accounts for the varying transient delay of the power and injection MOSFETs throughout the shaped switching transition. The example provided in Figure 4.22 presents the gate-drive control algorithm being applied to both the $\alpha$-MOSFET $v_{gs}$ and $\beta$-injection MOSFET $v_{gs}$. At any point, $t_i$, in the first half of the shaped switching transition, the measured $v_{ds}$ is compared to the reference $v_{ds}$ and an error is calculated. To account for the transient delay of the MOSFET throughout the shaped switching transition, the error signal, multiplied by a small gain, is applied to $v_{gs}$ $n$-time-steps before $t_i$. In the case of the $\alpha$-MOSFET example presented in Figure 4.22, the error compensation is applied to 4 time-steps before $t_i$, which are denoted $t_{i-1}$, $t_{i-2}$, $t_{i-3}$, and $t_{i-4}$, which creates a window where the error compensation signal is applied. The error signal at any point in time is given by:

$$\text{err} = v_{ds,ref} - v_{ds,meas} \tag{4.14}$$

Therefore, the error compensation applied to $v_{gs}$ is:

$$\text{CF}_{\text{err}} = G\text{err} \tag{4.15}$$

Where $G$ is the gain applied to the error. As illustrated in Figure 4.22, the compensation factor will then be applied to $v_{gs}$ four time-steps before when the error signal was calculated. Therefore, the total compensation signal applied to $v_{gs}$ each time-step is the sum of four subsequent error compensations, which is calculated using:

$$\text{CF}_{\text{tot}} = \sum_{i=1}^{N} G\text{err}_{i+1} \tag{4.16}$$

Where $N$ is the total number of compensation terms applied. For the control strategy implemented in the LTSPICE and MATLAB simulations, the $\alpha$-MOSFET applies error compensation to $v_{gs}$ sixteen time-steps before $t_i$, and the $\beta$-injection MOSFET applies error compensation to $v_{gs}$ four time-steps before $t_j$. The simulation considers 20 ns time-steps per the FPGA clock-speed, which provides a 320 ns and 80 ns delay window for the $\alpha$-MOSFET and $\beta$-injection MOSFET, respectively. A longer delay window is required for the $\alpha$-MOSFET, as a slower and more gradual control of $v_{ds}$ is required during the first half of the shaped switching transition.

## 4.5 Half-Bridge Shaped Switching Transition Modelling

### 4.5.1 Complete Half-Bridge Operations - Full Load

The entire half-bridge was simulated to test the robustness of the gate voltage profile and the current injection profiles. This section presents the LTSPICE and MATLAB circuit simulations for the low-EMI half-bridge circuit operating under constant load. The schematic uses the irfp150n and PSMN038-100YL SPICE models for the power and injection MOSFETs, respectively. Additionally, the AP9465GEM selected from the LTSPICE component library was used for the auxiliary branch MOSFETs. The major parasitic components of the irfp150n are presented in Table 4.2 when discussing the turn-off transients of a hard-switching half-bridge DC-DC converter. The major parasitic components of the PSMN038-100YL are presented in Table 4.3. The LTSPICE low-EMI half-bridge circuit is operated under a constant load of 10 A, modelled using a constant current source. The schematic for the low-EMI half-bridge circuit operating under constant full load conditions is presented in Figure 4.23.

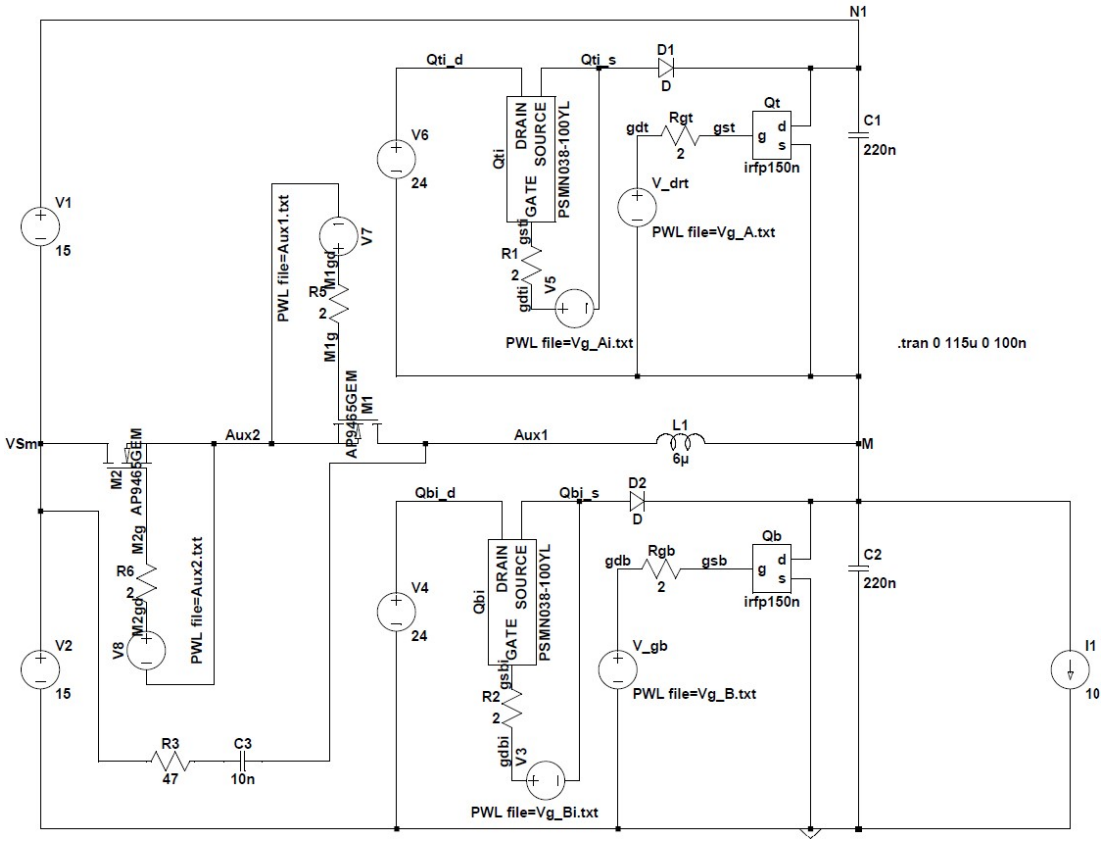



Figure 4.23: LTSPICE schematic for the low-EMI half-bridge circuit configured to operate under full-load.

Table 4.3: MOSFET equivalent circuit description of major parasitic components.

| **Parameter** | **Value** | **Unit** | **Parameter** | **Value** | **Unit** |
|---|---|---|---|---|---|
| $V_{DD}$ | 100 | V | g | 45 | Ʊ |
| $I_{ds}$ | 30 | A | $C_{iss}$ | 1905 | pF |
| $R_{DS(on)}$ | 37.5 | mΩ | $C_{oss}$ | 137 | pF |
| $V_g$ | ±20 | V | $V_{th}$ | 1.7 | V |

The simulation starts by designating the top power MOSFET as the $\alpha$-MOSFET and the bottom injection MOSFET as the $\beta$-injection MOSFET, then changing the designation to the bottom MOSFET and the top injection MOSFET for the next shaped switching transition. The complete sequence of events for the half-bridge modelling is summarised as follows.

- **Stage 1:** Initially, the simulation starts with a delay stage, which gives the circuit time to reach steady state conditions. The top MOSFET is controlled to undergo a rising transition, which commences with the following initial conditions: Load current, $I_o = 10$ A, $\alpha$-MOSFET $v_{ds} = 30$ V, $\beta$-MOSFET $v_{ds} = 0$ V, $\alpha$-MOSFET $v_{gs} = 15$ V, $\beta$-MOSFET $v_{gs} = 0$ V, and the auxiliary branch is off.

- **Stage 2:** The gate drive voltage profile of the $\alpha$-MOSFET commences and is required to get the $\alpha$-MOSFET $v_{ds}$ to follow the $v_{ds}$ reference profile. As the gate-drive voltage decreases, the drain-source resistance increases, causing current to be diverted to the capacitors. At the end of the $\alpha$-MOSFET gate-drive stage, the current has completely diverted to the capacitors when the $v_{ds}$ reaches 15 V.

- **Stage 3:** Just prior to $v_{ds}$ reaching 15 V, the $\beta$-injection MOSFET $v_{gs}$ is increased to below $V_{th}$ to ensure the MOSFET can allow for the injection current to conduct as soon as 15 V is reached. The current injection profile of the $\beta$-injection MOSFET is switched on when 15 V is reached, which offsets the current in the parallel capacitors allowing $v_{ds}$ of the MOSFET to reduce its slope.

- **Stage 4:** The $\beta$-injection MOSFET is switched off, and the $\beta$-MOSFET $v_{gs}$ is ramped to 15V, which ensures the $\alpha$-MOSFET $v_{ds}$ remains at the target voltage of 30 V. The $\beta$-injection MOSFET is turned off when the injection circuit reaches 10A, indicating a complete switching transition. Turning on the $\beta$-MOSFET at this stage is important to reduce the on-state resistance of the $\beta$-MOSFET and minimise losses as current is diverted into the MOSFET branch.

- **Stage 5:** This is a delay stage allowing the circuit to reach steady-state conditions prior to the bottom MOSFET, which is now the $\alpha$-MOSFET, undergoing a shaped rising transition. The steady-state conditions that must be met before the $\alpha$-MOSFET shaped transition can occur is the same for Stage 1.

- **Stage 6:** The auxiliary branch is turned on, which allows the magnitude of the current in the auxiliary branch to ramp up to 20 A as required prior to commencing the controlled $\alpha$-MOSFET turn-off sequence. The auxiliary branch is negative, and increases in magnitude to 20 A, which is required to completely compensate the current in the $\alpha$-MOSFET before the $\alpha$-MOSFET can commence the rising transition.

- **Stage 7:** The gate drive voltage profile of the $\alpha$-MOSFET shapes $v_{ds}$ until 15 V is reached, similar to Stage 2.
- **Stage 8:** The $\beta$-injection MOSFET is controlled until 30 V is reached, similar to Stage 3. Note that the current injection magnitude for the top injection circuit does not need to be 10 A since there is some compensation being provided by the auxiliary branch, which is ramping down from 20 A to 0 A.
- **Stage 9:** The $\beta$-injection MOSFET is switched off and the $\beta$-MOSFET $v_{gs}$ is ramped to 15 V to ensure the $\beta$-MOSFET $v_{ds}$ remains at 30 V. Note that the timing between turning $\beta$-injection MOSFET off and the $\beta$-MOSFET on is slightly different to Stage 4 since there is current in the auxiliary branch.
- **Stage 10:** The auxiliary branch is switched off. By this stage, the current in the $\beta$-MOSFET is 10 A, and the switching transition is complete.
- **Stage 11:** A delay stage to allow the circuit to reach steady-state conditions prior to commencing the next shaped switching transition. At this point, the steady-state conditions are the same as Stage 1, and the process can be repeated.

Figure 4.24 presents the LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the $\alpha$-MOSFET $v_{ds}$ (orange), $\alpha$-MOSFET $v_{ds}$ reference profile (black-dashed), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and the $\beta$-MOSFET $v_{gs}$ (purple). For clarity, the $\beta$-injection MOSFET $v_{gs}$ is scaled by a factor of 10. Firstly, the plot shows that the $\alpha$-MOSFET $v_{ds}$ accurately follows the reference logistic-shaped waveform. Concurrently, the $\beta$-MOSFET $v_{ds}$ also produces a logistic shaped switching transition since it is complementary to the $\alpha$-MOSFET. Lastly, the gate voltages of the $\alpha$-MOSFET, $\beta$-injection MOSFET, and $\beta$-MOSFET are presented, which indicates the control sequence of the low-EMI half-bridge. Initially, the $\alpha$-MOSFET is controlled from 10 $\mu$s to 20 $\mu$s, to provide $\alpha$-MOSFET $v_{ds}$ shaping up to $0.5V_i$.

The $\beta$-injection MOSFET $v_{gs}$ is ramped from 0 V to 2.3 V between 19 $\mu$s and 19.5 $\mu$s, and then held constant at 2.3 V from 19.5 $\mu$s to 20 $\mu$s. Preparing the $\beta$-injection MOSFET is required to ensure there is sufficient charge in the MOSFET to reduce the transient response time when the MOSFET is expected to start conducting to allow the injection current to flow into the circuit to shape the $\alpha$-MOSFET $v_{ds}$. From 20 $\mu$s to 22.5 $\mu$s, the $\beta$-injection MOSFET $v_{gs}$ is controlled to allow the required amount injected current to be provided. Finally, the $\beta$-injection MOSFET $v_{gs}$ is ramped from the value of the gate-voltage at 22.5 $\mu$s to 0 V at 23 $\mu$s. Once the transition is complete and the reference waveform transition time is reached, the $\beta$-MOSFET $v_{gs}$ is slowly

ramped from 0 V to 15 V over 6 $\mu$s, which turns on the MOSFET. In the next switching cycle, the $\beta$-MOSFET will become the $\alpha$-MOSFET and undergoes a controlled turn-off sequence.

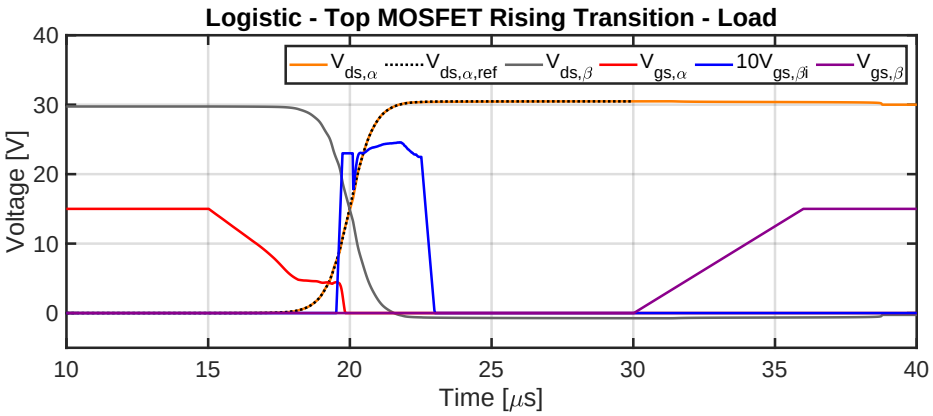



Figure 4.24: LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the $\alpha$-MOSFET $v_{ds}$ (orange), $\alpha$-MOSFET $v_{ds}$ reference profile (black-dashed), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ scaled by a factor for 10 (blue), and the $\beta$-MOSFET $v_{gs}$ (purple). The half-bridge circuit is operating under constant load.

Figure 4.25 presents the LTSPICE and MATLAB simulation results of the $\alpha$-MOSFET $i_{gs}$ (blue), and $\beta$-injection MOSFET $i_{gs}$ (red) during a shaped transition. The $\alpha$-MOSFET $v_{ds}$ (orange), $\alpha$-MOSFET $v_{ds}$ reference profile (black-dashed) are also included as a point of reference for timing throughout the shaped transition.

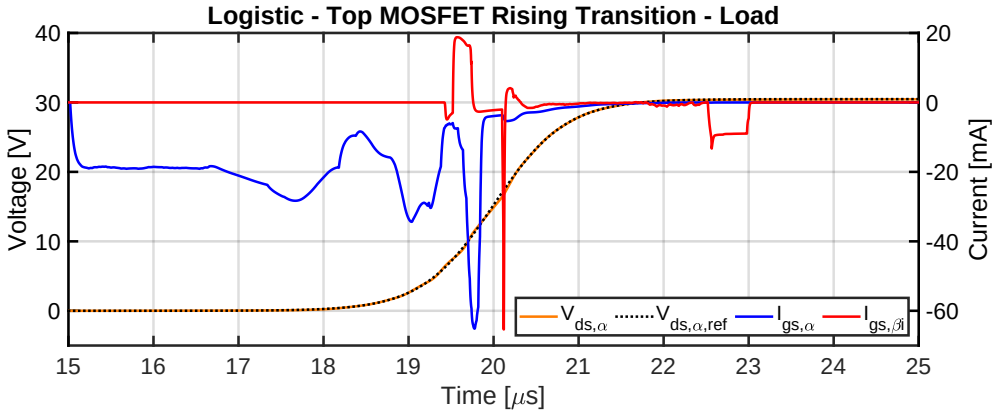



Figure 4.25: LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the $\alpha$-MOSFET $v_{ds}$ (orange), $\alpha$-MOSFET $v_{ds}$ reference profile (black-dashed), $\alpha$-MOSFET $i_{gs}$ (blue), and $\beta$-injection MOSFET $i_{gs}$ (red). The half-bridge circuit is operating under constant load.

Figure 4.26 presents the LTSPICE and MATLAB simulation results of the $\alpha$-MOSFET $i_{ds}$ (grey), $\beta$-MOSFET $i_{ds}$ (red), $\beta$-injection MOSFET $i_{ds}$ (light-blue), top capacitor current $i_{Ct}$ (blue), bottom capacitor current $i_{Cb}$ (purple) and the auxiliary branch current $i_{aux}$ (black). Since the top MOSFET is the $\alpha$-MOSFET, the auxiliary branch is not required for the shaped rising transition of $v_{ds}$. During the first half of the transition, both the $i_{C_t}$ and $i_{C_b}$ are both increasing in current magnitude. Subsequently, the $\beta$-injection MOSFET injects current just before 15 V, which diverts current away from the capacitors, allowing the second half of the MOSFET transition to be controlled and shaped.

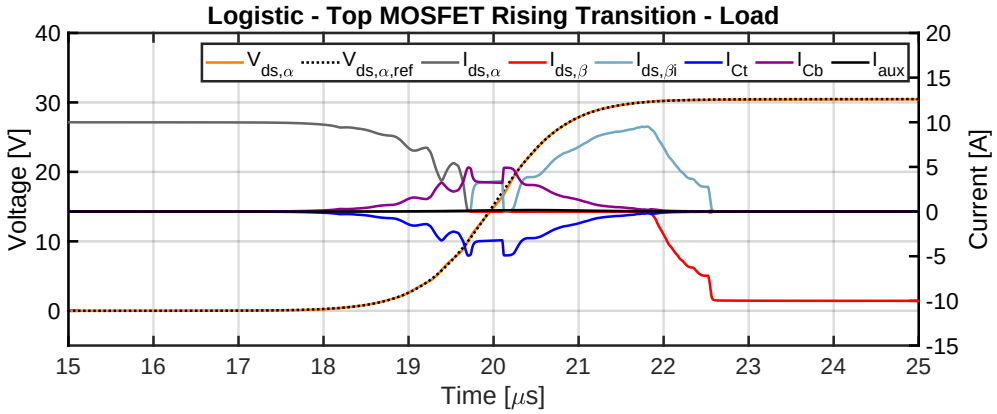



Figure 4.26: LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the $\alpha$-MOSFET $v_{ds}$ (orange), $\alpha$-MOSFET $v_{ds}$ reference profile (black-dashed), $\alpha$-MOSFET $i_{ds}$ (grey), $\beta$-MOSFET $i_{ds}$ (red), $\beta$-injection MOSFET $i_{ds}$ (light-blue), top capacitor current $i_{Ct}$ (blue), bottom capacitor current $i_{Cb}$ (purple), and the auxiliary branch current $i_{aux}$ (black). The half-bridge circuit is operating under load.

Figure 4.27 presents the LTSPICE and MATLAB simulation results of the half-bridge auxiliary branch control during a complete rising and falling logistic-shaped switching transition of the half-bridge circuit. Note that auxiliary MOSFET 1 ($T_{auxt}$) $v_{gs}$ is not controlled since it is not required when $\alpha$-MOSFET is the top power MOSFET and the load current is 10 A. Auxiliary MOSFET 2 ($T_{auxb}$) is turned on when the $\alpha$-MOSFET is the bottom power MOSFET to allow the current in the auxiliary branch to reach 20 A once the $\alpha$-MOSFET $v_{ds}$ has reached the 15 V.

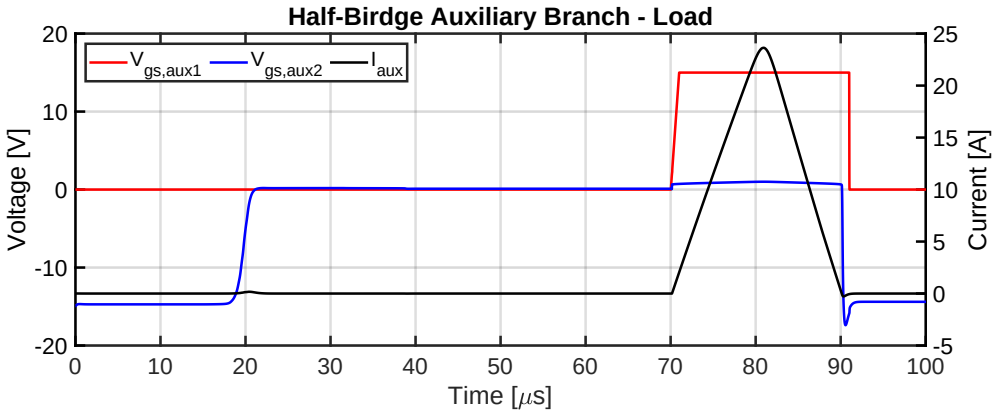



Figure 4.27: LTSPICE and MATLAB simulation results of the half-bridge auxiliary branch control during a complete rising and falling transition for a logistic reference waveform. The plot shows the auxiliary MOSFET 1 ($T_{auxt}$) $v_{gs}$, auxiliary MOSFET 2 ($T_{auxb}$) $v_{gs}$, and the auxiliary branch current $i_aux$ (black). The half-bridge circuit is operating under load.

Figure 4.28 presents the error signal, which is the absolute difference between the $\alpha$-MOSFET $v_{ds}$ and the $\alpha$-MOSFET $v_{ds}$ reference profile. The error at the beginning and end of the transitions are the MOSFET on and off-state voltages differing marginally from the desired reference profile. During the controlled portion, the errors are primarily present during the first half of the transitions, which is caused by the transient response of the $\alpha$-MOSFET during the first half of the control sequence being relatively slow and requiring precise control of the gate-drive with an ever-changing transient response as the charge is gradually depleted from the gate. Additionally, a relatively significant error at approximately 240 mV is present near when $v_{ds}$ reaches 15 V, caused by the $\alpha$-MOSFET gate-drive control finishing, and the $\beta$-injection MOSFET control commencing.

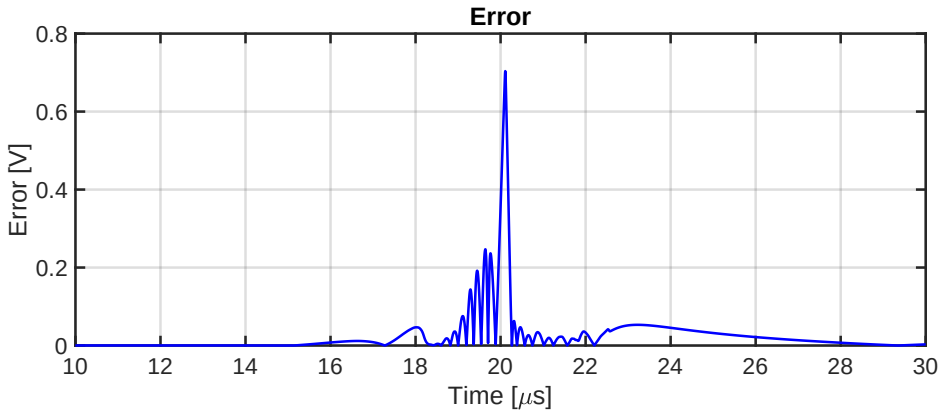



Figure 4.28: LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the error signal, which the the absolute difference between the $\alpha$-MOSFET $v_{ds}$ and the $\alpha$-MOSFET $v_{ds}$ reference profile. The half-bridge circuit is operating under load.

Figure 4.29 presents the harmonic spectral comparison of a trapezoidal waveform (black), LTSPICE simulation results (grey), and ideal logistic-shaped (red) switching transitions when the half-bridge circuit is operating under constant full load conditions. The PWM waveforms are synthesised with the shaped transitions considering a 10 kHz switching frequency, and all harmonic spectra plotted include the spectral bound (envelope) for comparison. The trapezoidal transition is modelled with the same transition time of 20 $\mu$s, which is a slow transition time and low-EMI compared to hard-switched MOSFETs. Although the LTSPICE spectral content does not demonstrate the steep harmonic roll-off expected of the ideal logistic-shaped transition, the harmonic content of the LTSPICE simulation results is considerably less than the slowed trapezoidal waveform.

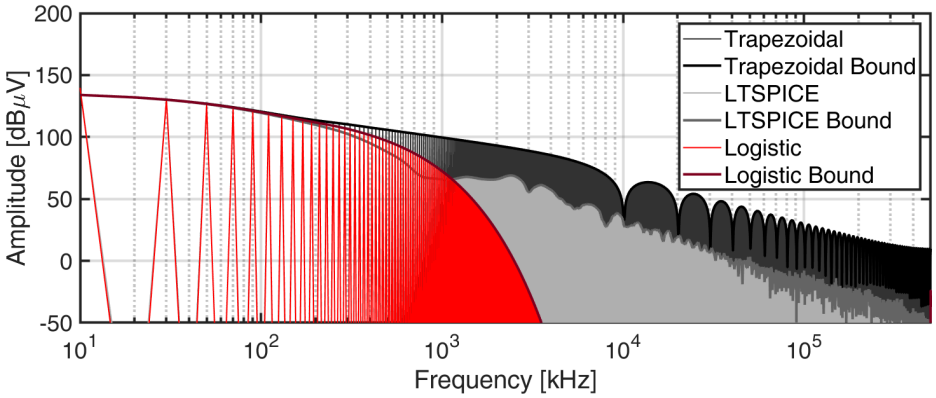



Figure 4.29: Harmonic spectral comparison of a trapezoidal waveform (black), LTSPICE simulation results (grey), logistic-shaped (red) shaped waveforms when the half-bridge circuit is operating under constant load. Pulse-width modulated waveforms are synthesised with the shaped transitions considering a 10 kHz switching frequency. All harmonic spectra plotted include the spectral bound (envelope) for comparison. The half-bridge circuit is operating under load.

Lastly, Figure 4.30 presents a comparison of the waveform derivatives during a shaped switching transitions between the LTSPICE simulation results and the reference logistic waveform. The results demonstrate that the derivative is not smooth and is preventing the steep spectral roll-off from being realised. The outcome is consistent with Section 3.5 of Chapter 3, which outlines the practical limitations of producing steep spectral roll-off where signal quantisation or discontinuities prevent the shaped switching transitions and the derivatives of the waveform from being smooth. The dominant contributing factors are the occurrences of rapid $dv_{ds}/dt$ observed between 19 $\mu$s and 20.5 $\mu$s.

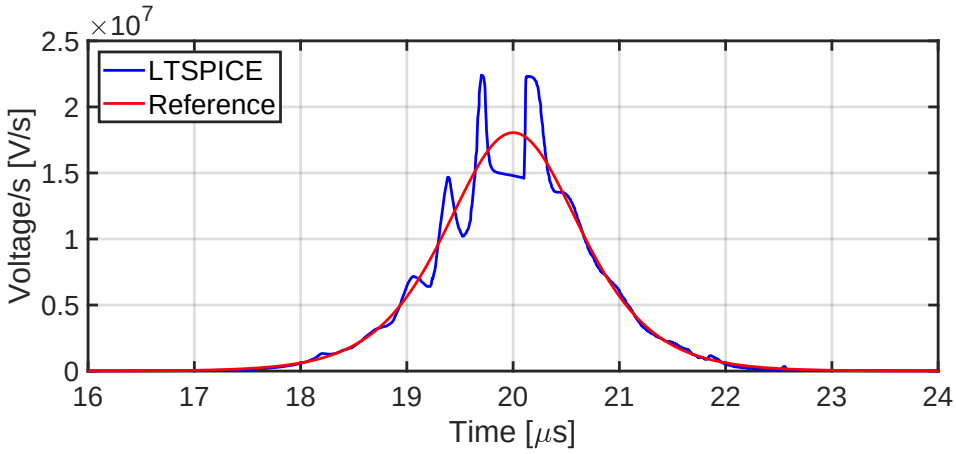



Figure 4.30: Comparison of LTSPICE (blue) and reference logistic function (red) shaped switching transition derivatives with the circuit operating under constant load.

### 4.5.2 Complete Half-Bridge Operations - No Load

This section presents the LTSPICE and MATLAB circuit simulations for the low-EMI half-bridge circuit operating under no-load conditions. The schematic is created with the IRFP150NpbF n-channel 100 V 36 mΩ power MOSFETs and the PSMN038-100YL n-channel 100 V 37.5 mΩ injection MOSFETs. SPICE models of each MOSFET are imported into LTSPICE to model the transient response of each MOSFET accurately. The AP9465GEM N-channel 40 V 25 mΩ MOSFETs is used for the auxiliary branch MOSFETs selected from the LTSPICE component library. The LTSPICE schematic for the low-EMI half-bridge circuit operating under no-load conditions is presented in Figure 4.31.

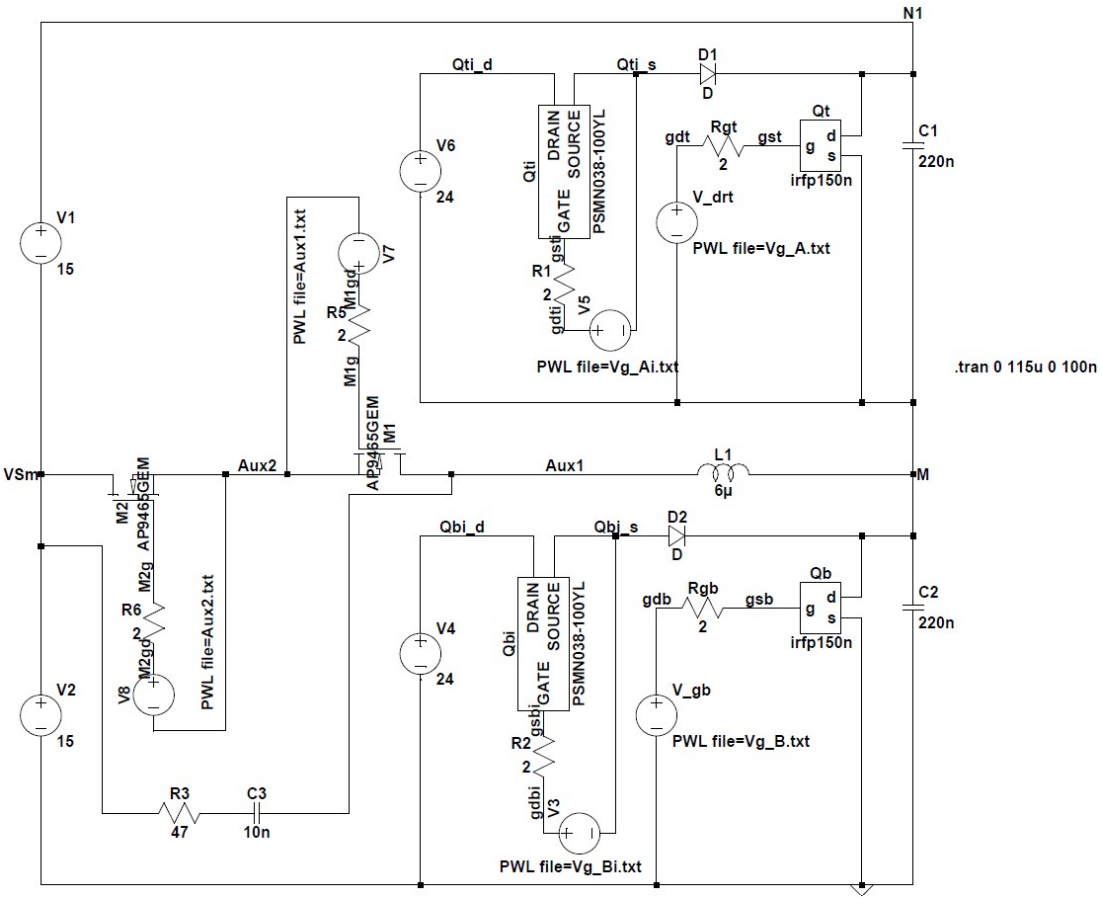



Figure 4.31: LTSPICE schematic for the low-EMI half-bridge circuit configured to operate under no-load.

The gate-drive voltages and currents that are presented in Figure 4.32 and Figure 4.33, respectively, show a similar response with the same timed sequence as the full load condition. Figure 4.34 presents the drain-source currents of each power and injection MOSFET, parallel capacitor currents, and the auxiliary branch current. Figure 4.35 shows a different control sequence of the auxiliary branch since the requirements to meet the $I_{load} + i_{aux} = 1$ pu criteria has changed, since $I_{load} = 0$ A. Therefore, when the top or the bottom power MOSFET is the $\alpha$-MOSFET current from the auxiliary branch is required since $I_{load} = 0$ pu. During the auxiliary branch turn-on, the $\alpha$-MOSFET $i_{ds}$ and $i_{aux}$ are equal in magnitude as shown in the first 3 $\mu$s of Figure 4.34. Similarly, the $\beta$-MOSFET $i_{ds}$ and $i_{aux}$ are equal during the final $\sim$2.5 $\mu$s when the auxiliary inductor is slowly ramping back towards 0 A after the controlled portion of the shaped transition is complete.

Figure 4.35 presents the LTSPICE and MATLAB simulation results of the half-bridge auxiliary branch control during a complete rising and falling logistic shaped switching transition. Auxiliary MOSFET 2 ($T_{auxb}$) is turned on when the $\alpha$-MOSFET is the bottom power MOSFET to allows the current in the auxiliary branch to reach 10 A once the $\alpha$-MOSFET $v_{ds}$ has reached 15 V. Similarly, auxiliary MOSFET 1 ($T_{auxt}$) is turned on when the $\alpha$-MOSFET is the top power MOSFET to allows the current in the auxiliary branch to reach 10 A once the $\alpha$-MOSFET $v_{ds}$ has reached 15 V.

Figure 4.36 shows the error signal, which is the absolute difference between the $\alpha$-MOSFET $v_{ds}$ and the $\alpha$-MOSFET $v_{ds}$ reference profile. Similar to the full-load profile, greater errors are present during the first half of the control transition when the transient response is slower. Notably, the error signal present when $v_{ds}$ is 15 V is less compared to the full-load conditions, when the control transitions from the $\alpha$-MOSFET gate-drive control to the $\beta$-injection MOSFET gate-drive control. Figure 4.37 presents the harmonic spectral comparison of a trapezoidal waveform (black), LTSPICE simulation results (grey), logistic-shaped (red) waveforms when the half-bridge circuit is operating under no-load conditions. Lastly, Figure 4.38 presents a comparison of the waveform derivatives between the LTSPICE simulation results and the reference logistic waveform, which demonstrates that the derivative is not smooth and is preventing the steep spectral roll-off from being realised.

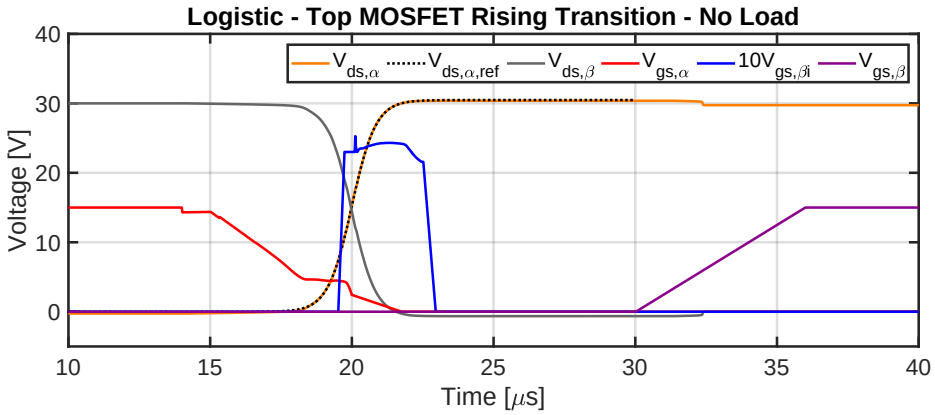



Figure 4.32: LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the $\alpha$-MOSFET $v_{ds}$ (orange), $\alpha$-MOSFET $v_{ds}$ reference profile (black-dashed), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ scaled by a factor for 10 (blue), and the $\beta$-MOSFET $v_{gs}$ (purple). The half-bridge circuit is operating under no load.

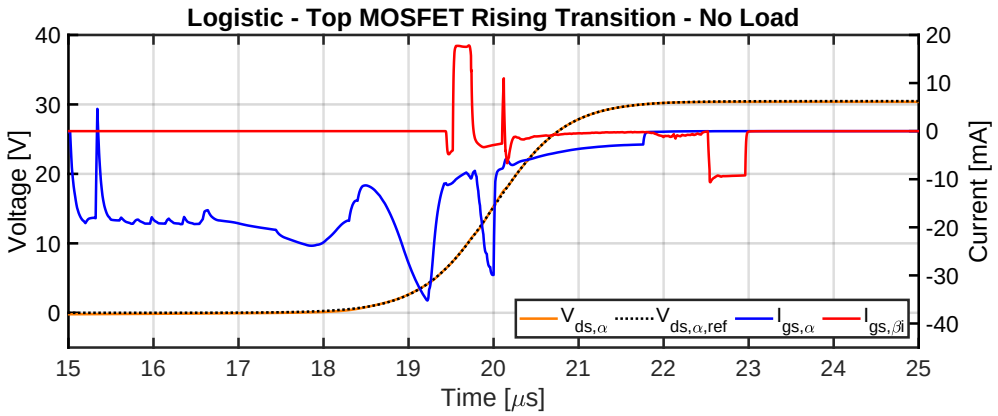



Figure 4.33: LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the $\alpha$-MOSFET $v_{ds}$ (orange), $\alpha$-MOSFET $v_{ds}$ reference profile (black-dashed), $\alpha$-MOSFET $i_{gs}$ (blue), and $\beta$-injection MOSFET $i_{gs}$ (red). The half-bridge circuit is operating under no load.

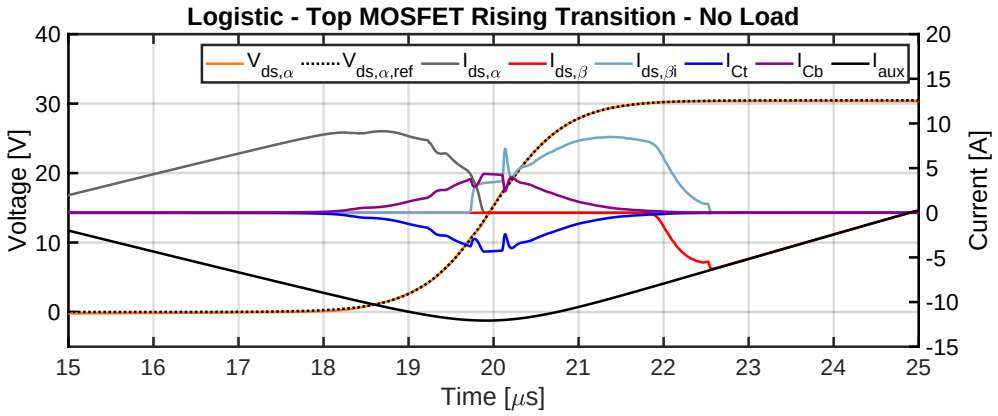



Figure 4.34: LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the $\alpha$-MOSFET $v_{ds}$ (orange), $\alpha$-MOSFET $v_{ds}$ reference profile (black-dashed), $\alpha$-MOSFET $i_{ds}$ (grey), $\beta$-MOSFET $i_{ds}$ (red), $\beta$-injection MOSFET $i_{ds}$ (light-blue), top capacitor current $i_{C_t}$ (blue), bottom capacitor current $i_{C_b}$ (purple), and the auxiliary branch current $i_aux$ (black). The half-bridge circuit is operating under no load.

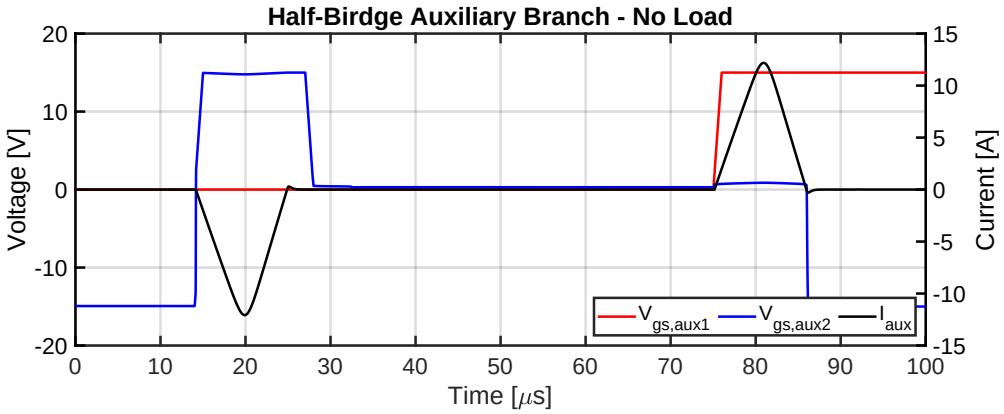



Figure 4.35: LTSPICE and MATLAB simulation results of the half-bridge auxiliary branch control during a complete rising and falling transition for a logistic reference waveform. The plot shows the auxiliary MOSFET 1 ($T_{auxt}$) $v_{gs}$, auxiliary MOSFET 2 ($T_{auxb}$) $v_{gs}$, and the auxiliary branch current $i_{aux}$ (black). The half-bridge circuit is operating under no load.

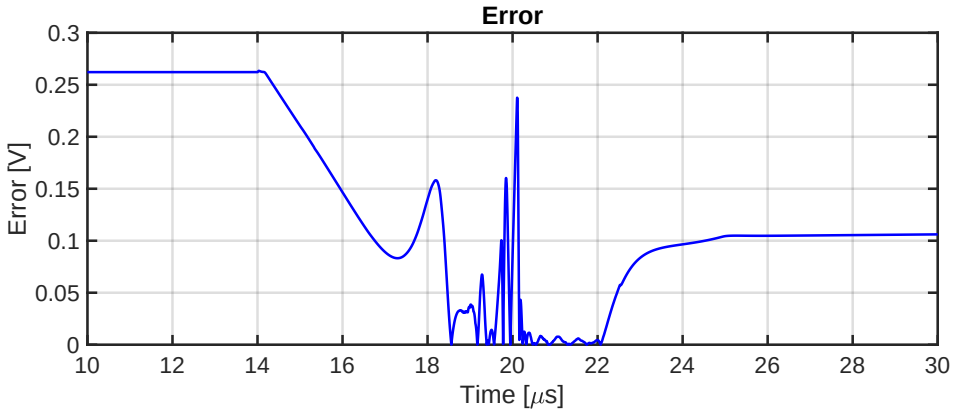



Figure 4.36: LTSPICE and MATLAB simulation results of a rising transition when the top power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile. The plot shows the error signal, which is the absolute difference between the $\alpha$-MOSFET $v_{ds}$ and the $\alpha$-MOSFET $v_{ds}$ reference profile. The half-bridge circuit is operating under no load.

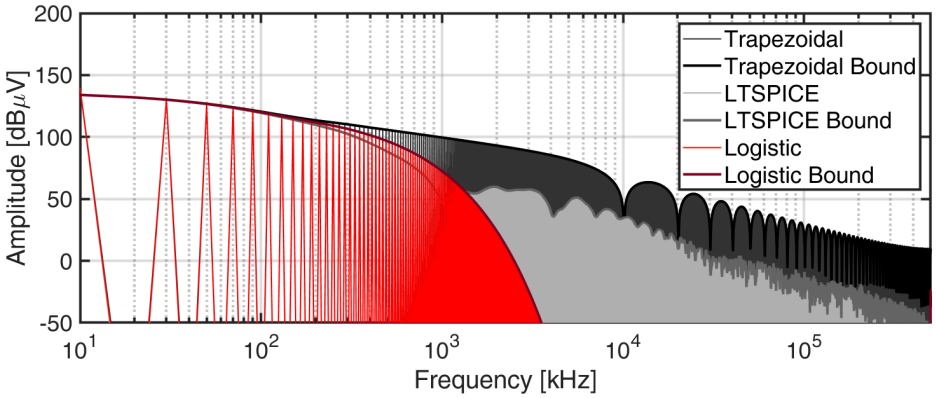



Figure 4.37: Harmonic spectral comparison of a trapezoidal waveform (black), LTSPICE simulation results (grey), logistic-shaped (red) shaped waveforms when the half-bridge circuit is operating under no load. Pulse-width modulated waveforms are synthesised with the shaped transitions considering a 10 kHz switching frequency. All harmonic spectra plotted include the spectral bound (envelope) for comparison. The half-bridge circuit is operating under no load.

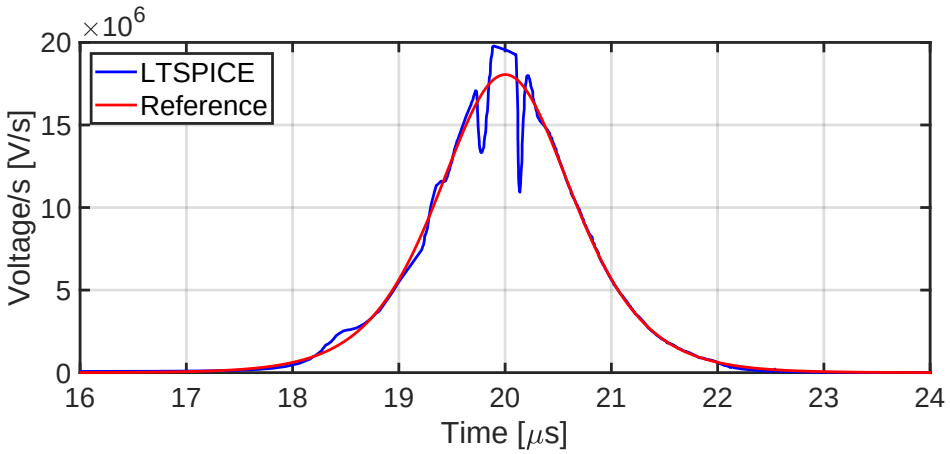



Figure 4.38: Comparison of LTSPICE (blue) and reference logistic function (red) shaped switching transition derivatives with the circuit operating under no load.

### 4.5.3 Summary

The LTSPICE and MATLAB modelling has demonstrated how shaped spectral transitions are realised within a half-bridge DC-DC converter. In doing so, the circuitry simulations have bridged the gap between a mathematical framework for identifying ideal shaped switching transitions and presenting a power converter topology that is capable of following a reference shaped switching transition. However, the LTSPICE and MATLAB simulations are not without practical limitations. The transient response of the MOSFET and the control algorithm create errors in the output switching waveform, causing the derivative of the waveform to not be smooth, which is undesirable for achieving high-frequency spectral roll-off. The circuit simulations are created with gate-drive resolutions representative of the prototype FPGA clock cycle, which is a contributing factor to the output waveform errors and derivative discontinuities observed in the simulations. However, the simulation outcomes are representative of the expected prototype performance, which is presented in the next Chapter.

## 4.6 References

[1] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics Converter, Applications and Design*. United States of America: John Wiley & Sons, Inc., 2003.

[2] S. S. Ang, *Power Switching Converters*. Madison Avenue, New York: Marcel Dekker, Inc., 1995.

[3] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Madison Avenue, New York: Oxford University Press, 2004.

[4] D. A. Grant and J. Gowar, *Power MOSFETS Theory and Application*. United States of America: Wiley-Interscience John Wiley & Sons, 1989.

[5] Y. Xiao, H. Shah, T. P. Chow, and R. J. Gutmann, "Analytical Modeling and Experimental Evaluation of Interconnect Parasitic Inductance on MOSFET Switching Characteristics," in *IEEE Appl. Power Electorn. Conf. Expo.*, vol. 1, 2004, pp. 516–521 Vol.1.

[6] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical Loss Model of Power MOSFET," *IEEE Trans. on Power Electron.*, vol. 21, no. 2, pp. 310–319, 2006.

[7] H. Raee, A. Rabiei, and T. Thiringer, "Analytical prediction of switching losses in mosfets for variable drain-source voltage and current applications," 06 2013, pp. 705–709.

[8] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Analysis of SiC MOSFETs under hard and soft-switching," in *IEEE Energy Conv. Cong. Expo.*, Sept 2015, pp. 2231–2238.

[9] I. Castro, D. G. Lamar, J. Roig, and F. Bauwens, "Modeling capacitive nonlinearities and displacement currents of high-voltage superjunction MOSFET in a novel analytical switching loss model," in *IEEE Work. Control and Model. for Power Electron.*, June 2014, pp. 1–9.

[10] I. Castro, J. Roig, R. Gelagaev, B. Vlachakis, F. Bauwens, D. G. Lamar, and J. Driesen, "Analytical switching loss model for superjunction MOSFETs with capacitive nonlinearities and displacement currents for DC-DC power converters," *IEEE Trans. Power Electron.*, vol. 31, pp. 2485–2495, March 2016.

[11] Z. Zhang, W. Eberle, Z. Yang, Y. Liu, and P. C. Sen, "Optimal Design of Current Source Gate Driver for a Buck Voltage Regulator Based on a New Analytical Loss Model," in *Power Electron. Specialists Conf.*, 2007, pp. 1556–1562.

[12] T. Meade, D. O'Sullivan, R. Foley, C. Achimescu, M. Egan, and P. McCloskey, "Parasitic inductance effect on switching losses for a high frequency DC-DC converter," in *IEEE Appl. Power Electorn. Conf. Expo.*, Feb 2008, pp. 3–9.

[13] M. Rodríguez, A. Rodríguez, P. F. Miaja, D. G. Lamar, and J. S. Zúniga, "An insight into the switching process of power MOSFETs: An improved analytical losses model," *IEEE Trans. Power Electron.*, vol. 25, pp. 1626–1640, June 2010.

[14] J. Fu, Z. Zhang, Y. Liu, and P. C. Sen, "MOSFET Switching Loss Model and Optimal Design of a Current Source Driver Considering the Current Diversion Problem," *IEEE Trans. on Power Electron.*, vol. 27, no. 2, pp. 998–1012, 2012.

[15] J. Wang, H. S. h. Chung, and R. T. h. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573–590, Jan 2013.

[16] D. Foty, *MOSFET Modelling with SPICE: Principles and Practice*. Upper Saddle River, New Jersey: Prentice Hall PTR, 1997.

[17] J. Yang, J. Shi, and T. Cui, "An active voltage controller of SiC MOSFET for reduced EMI generation," in *3rd IEEE Advanced Inf. Technol., Electron. Autom. Control Conf. (IAEAC)*, 2018, pp. 979–983.

[18] T. Cui, Q. Ma, P. Xu, and Y. Wang, "Analysis and optimization of power MOSFETs shaped switching transients for reduced EMI generation," *IEEE Access*, vol. 5, pp. 20 440–20 448, 2017.

# Chapter 5

## Low-EMI Prototype Design and Implementation

## 5.1 Introduction - Prototype Design Overview

The low-EMI half-bridge prototype design and implementation are presented in this Chapter. Firstly an overview of the shaped switching transition half-bridge is presented, including a summary of the major power and control circuitry. Following this, the half-bridge control system implementation to achieve shaped switching transitions is presented. The section provides a comprehensive summary of the control philosophy, control system sequencing, FPGA control implementation, control system initialisation, $\alpha$-MOSFET control, $\beta$-injection MOSFET control, auxiliary control, and hard-switching implementation. Additionally, the Chapter presents a laboratory assessment and performance verification of the shaped switching transition technology with the half-bridge prototype operating under no-load and constant load conditions. Lastly, the Chapter concludes with a theoretical analysis of the radiated emissions expected to be generated by the half-bridge prototype and the attenuation required to adhere to the SKA RFI/EMC standard threshold levels.

The half-bridge shaped switching transition process intends to control the mid-point voltage of the half-bridge circuit to follow a shaped reference profile. Capacitors are placed across the drain-source of the power MOSFETs to make the voltage controllable by implementing gate-drive control of the $\alpha$-MOSFET and $\beta$-injection MOSFET. As mentioned in the previous modelling sections, the additional circuitry required to deliver the low-EMI logistic-shaped switching transition includes the current injection circuits connected in parallel to each power MOSFETs and the auxiliary branch. The key characteristics of the low-EMI half-bridge prototype includes:

- The prototype is a working power converter, albeit at low voltages (30 V) and currents (3 A) when operating under load. However, the prototype can demonstrate that the shaped switching transition technology can be integrated with power converters controlled using PWM switching schemes.
- The control system works based on the gate-drive of the $\alpha$-MOSFET for the first half of the shaped transition, and by controlling the gate-drive of the $\beta$-injection MOSFET to inject the required amount of current for the second half of the shaped transition. The control mechanism intends to deliver smooth voltage and current waveforms.
- The control system is loaded with three reference profiles, which allows for the prototype to produce sinusoidal-shaped, S-shaped and logistic-shaped switching transitions. Multiple shaped transitions test the capability of the control and allow for multiple shaped transitions to be compared.

- The prototype also includes a half-bridge power circuit that operates under hard-switching conditions. In addition to comparing different shaped-transitions profiles, a baseline hard-switching waveform can also be compared.

The low-EMI power converter half-bridge DC-DC converter consists of two n-channel power MOSFETs connected in series between a voltage source. The injection circuits are connected in parallel to each power MOSFET. The injection circuits include a PSU capable of delivering up to 10 A and a MOSFET to provide the required current profile by controlling the injection MOSFET gate-drive. A smoothing inductor, $L_{aux}$, is connected at the midpoint of the half-bridge. An overview of the half-bridge circuit is presented in Figure 5.1. A table of all major circuitry components is presented in Table 5.1.

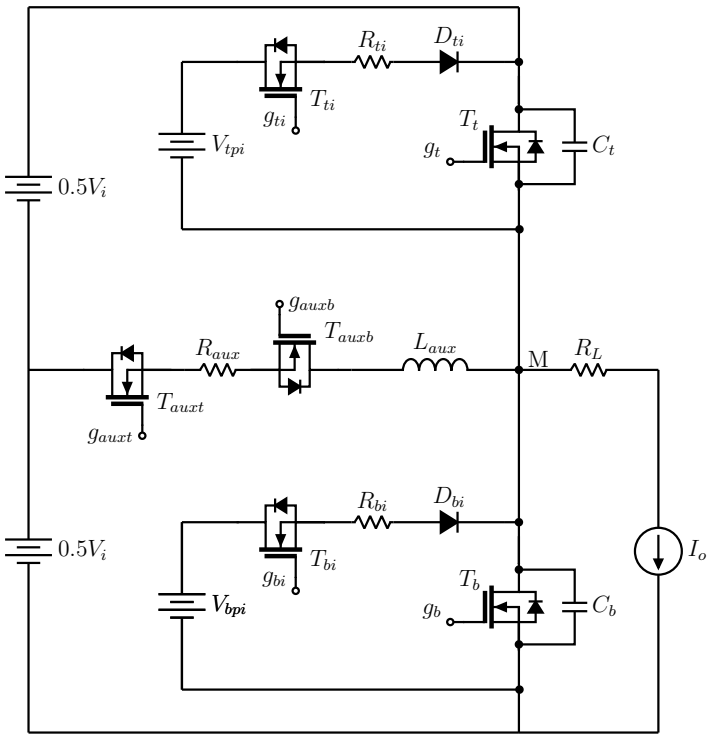



Figure 5.1: Prototype half-bridge DC-DC converter circuit capable of producing low-EMI shaped switching transitions.

Table 5.1: Major half-bridge DC-DC converter circuitry components

| **Label** | **Component Description** |
|---|---|
| $T_t$ | Top half-bridge power MOSFET |
| $T_b$ | Bottom half-bridge power MOSFET |
| $T_{ti}$ | Top injection circuit MOSFET |
| $T_{bi}$ | Bottom injection circuit MOSFET |
| $T_{auxt}$ | Auxiliary branch MOSFET 1 |
| $T_{auxb}$ | Auxiliary branch MOSFET 2 |
| $C_t$ | Top half-bridge power MOSFET capacitor |
| $C_b$ | Bottom half-bridge power MOSFET capacitor |
| $D_{ti}$ | Top injection circuit reverse current protection diode |
| $D_{bi}$ | Bottom injection circuit reverse current protection diode |
| $L_{aux}$ | Auxiliary branch inductor |
| $R_{ti}$ | Top injection circuit current sense resistor |
| $R_{bi}$ | Bottom injection circuit current sense resistor |
| $R_{aux}$ | Auxiliary branch current sense resistor |
| $R_L$ | Load current sense resistor |

The major hardware of the low-EMI half-bridge power converter prototype consists of a power circuit DC-link, half-bridge, and drain-source capacitors. Additionally, the prototype includes gate-drive circuitry for each power MOSFET and current injection circuitry for each injection MOSFET. Power supply circuitry is required for the gate drives and injection circuitry.

The major control circuits that that are required to provide shaped switching transitions of the half-bridge mid-point voltage include power control circuitry for the top power MOSFET and top injection circuit, power control circuitry for the bottom MOSFET and bottom injection circuit, a power supply circuit for the gate drives and injection circuits, and the auxiliary branch control circuit. The auxiliary control board also contains the gate signals for the hard-switched half-bridge used as a baseline comparison for the low-EMI half-bridge prototype.

A high-level overview of the power and control circuity interfacing is shown in Figure 5.2. The hardware to provide power and control for the current injection circuit and MOSFET control are presented in the remainder of this Chapter.

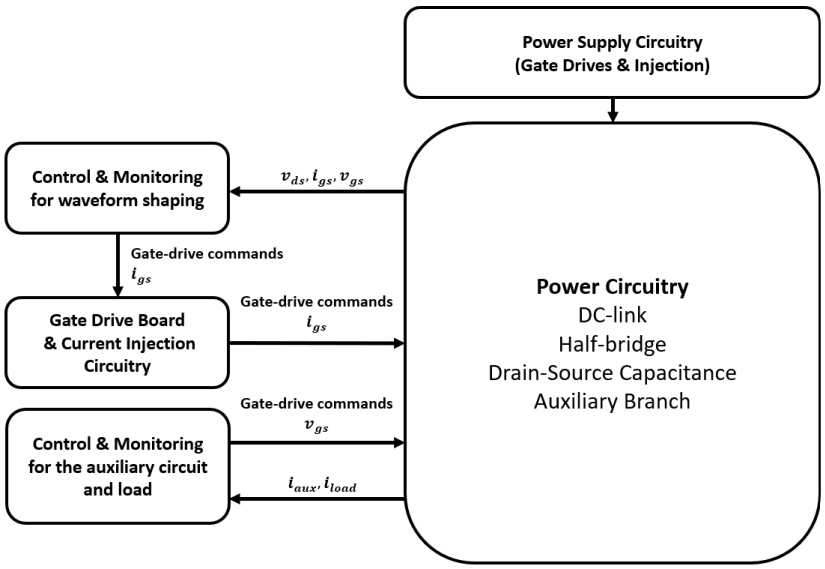



Figure 5.2: High-level overview of the power and control circuity interfacing.

## 5.2 Half-Bridge Power Converter Design

### 5.2.1 Half-Bridge Power Circuitry

The half-bridge power circuitry consists of two n-channel MOSFETs, a DC-link electrolytic capacitance, parallel capacitors on each power MOSFET, and connections to the control and monitoring circuitry. Additionally, a 5-m$\Omega$ current sensing resistor and current sense op-amp is used to measure the load current of the half-bridge. An overview of the half-bridge power circuitry is presented in Figure 5.3.

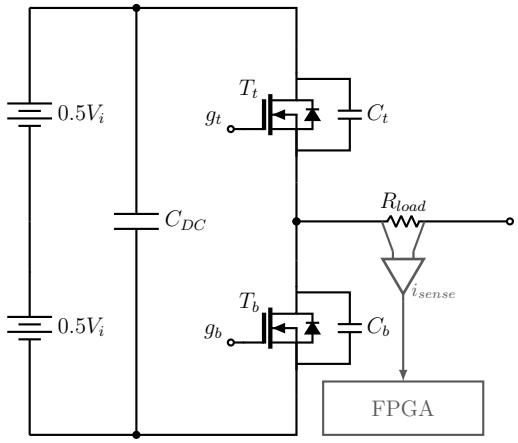



Figure 5.3: Half-bridge power circuitry.

### 5.2.2 Half-Bridge Gate-Drive and Injection Circuitry

The half-bridge gate-drive and injection circuitry for the low-EMI half-bridge power circuit is separated into two main sections, one for each power MOSFET and injection MOSFET pair, which are $T_t/T_{ti}$ and $T_b/T_{bi}$, respectively. Each section contains gate current sourcing for the power MOSFET gate-drive, gate current sourcing for the injection MOSFET gate-drive, a 2 m$\Omega$ current sense resistor and op-amp for the injection circuit current sensing, and voltage sensing of the $v_{ds}$ of the power MOSFET. An overview of the gate-drive and injection circuitry, considering $T_t$ and $T_{ti}$ is shown in Figure 5.4. Note that the parallel capacitors ($C_t$ and $C_b$) are not included, so the control and monitoring signals are clearly presented. The half-bridge gate-drive and injection circuitry performs the following control sequences:

- Commences the turn-off transition of the power MOSFET by controlling the gate-drive.
- Shapes the turn-off transition of the bottom-MOSFET by controlling the gate-drive of the top injection circuit.

The FPGA is programmed with the $v_{ds}$ reference profile and $i_{gs}$ profiles, which are iteratively updated to allow the half-bridge circuity to converge on the target reference profile. The switching transition timing is initiated by the reception of a command to commence switching. An op-amp is used to measure the voltages, whereas an op-amp and current sense resistor measure the currents. Each half-bridge gate-drive and injection circuit measures the injection circuit current profile, power MOSFET $v_{ds}$, power MOSFET $v_{gs}$, and injection circuit MOSFET $v_{gs}$. Additionally, the DACs are required to provide the $i_{gs}$ gate-drive control commands to the power and injection MOSFETs.

The injection current sensing is designed to handle up to 25 A, which gives a maximum signal of 50 mV. The current sensing resistor is placed at the source of the injection MOSFET to provide a low common-mode voltage to the input of the current sense op-amp. The differential voltage across the current sense resistor is amplified by a factor of ten to give a maximum of 0.50 V output signal, which is transferred to the control and monitoring circuit for the shaped switching transition control.

The controlled current source that drives current into the gate of each power MOSFET is created by an op-amp with voltage feedback across a 33 Ω gate resistor. The op-amp output will move to create the necessary voltage across the gate resistor, and the resistance determines the current source. The controlled current source driving current into the gate of each injection MOSFET is created by an op-amp with voltage feedback across a 68 Ω gate resistor. Within the top power MOSFET portion of the board, there is a current sense amplifier for the load current.

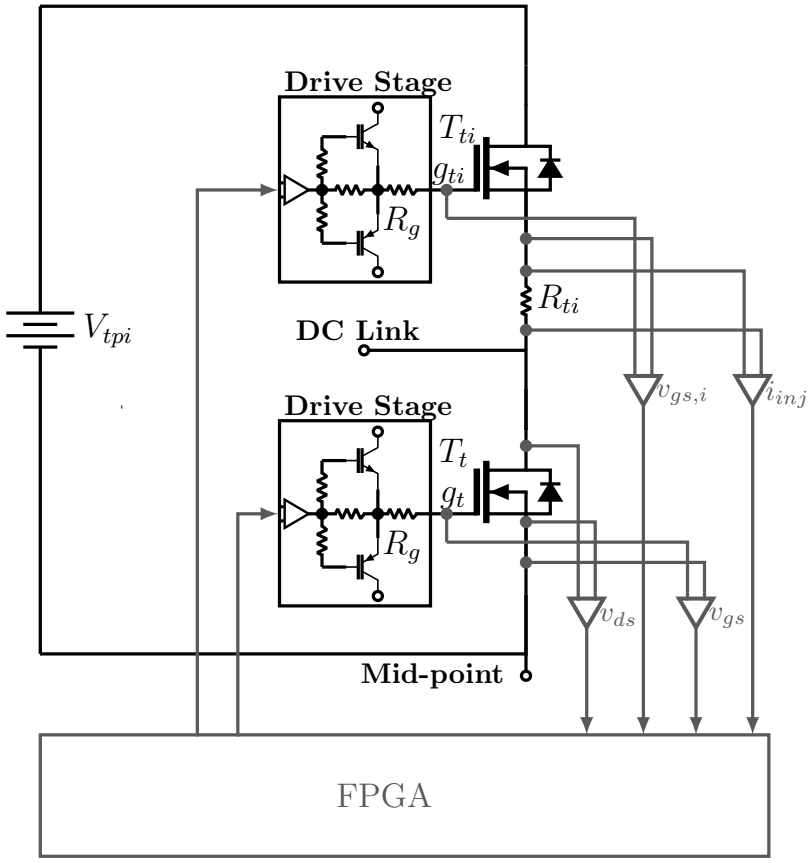



Figure 5.4: Half-bridge gate-drive and injection circuitry considering $T_t$ and $T_{ti}$.

Additionally, a power supply circuit consisting of six power supplies provides power to the half-bridge gate-drive and injection circuitry. Four power supplies are required to power the ±15 V gate-drives for each power MOSFET and each injection MOSFET. Additionally, 0V is connected to the source of each power MOSFET to facilitate the power MOSFET gate current sourcing. Two 24 V power supplies are required for the current injection supplies, including a 10 $\mu$F high-frequency capacitor to maintain the 24 V supply voltage throughout the injection period. Each section has +5 V and -5 V voltage regulators to provide the injection current sensing power. Lastly, eight 22 Ω resistors in parallel were added in series to the output of each of the two 24 V injection circuit power supplies to limit the total magnitude of the injection current.

### 5.2.3 Auxiliary Branch Circuitry

The auxiliary branch control circuit will turn on and turn off the auxiliary branch when required to control the auxiliary current used in the power converter, ensuring the same current is conducting in the power MOSFETs during every shaped switching transition. Therefore, the auxiliary current is used to add to the load current to ensure the $\alpha$-MOSFET undergoing a rising shaped switching transition always starts with the same $i_{ds}$ in the MOSFET. The current in the $\alpha$-MOSFET undergoing a rising shaped switching transition is intended to be a relatively fixed current, so $i_{aux}$ is ramped to satisfy $I_{load} + I_{aux} = 1$ pu as the shaped switching transition reaches $0.5V_i$ while the $\alpha$-MOSFET is being controlled.

The auxiliary power circuit contains a 5.5 $\mu$H auxiliary inductor, a 2 mΩ current sensing resistor placed between the sources of the two MOSFET switches, and two auxiliary MOSFETs, all in series. The top auxiliary MOSFET, $T_{auxt}$, is the MOSFET that is turned on to ramp up $i_{aux}$ to increase $i_{ds}$ in the top power MOSFET. The bottom auxiliary MOSFET, $T_{auxb}$, is the MOSFET that is turned on to ramp up $i_{aux}$ to increase $i_{ds}$ in the bottom power MOSFET. The sources of the two auxiliary MOSFETs are connected so that both switches can be controlled from a single ±15 V supply.

The auxiliary branch control circuit requires ADCs to measure $i_{aux}$ and $v_{ds}$ across both auxiliary MOSFETs. The DAC converters are required for the $T_{auxt}$ and $T_{auxb}$ gate-drives. A 2 mΩ current sense resistor and op-amp are used for the auxiliary current sensing. The controlled current source driving current into the gate of each auxiliary MOSFET is created by an op-amp with feedback of the voltage across a 22 Ω gate resistor. Changing the op-amp output creates the necessary voltage across the gate resistor, which determines the gate current. An overview of the auxiliary branch circuit with monitoring and control is presented in Figure 5.5.

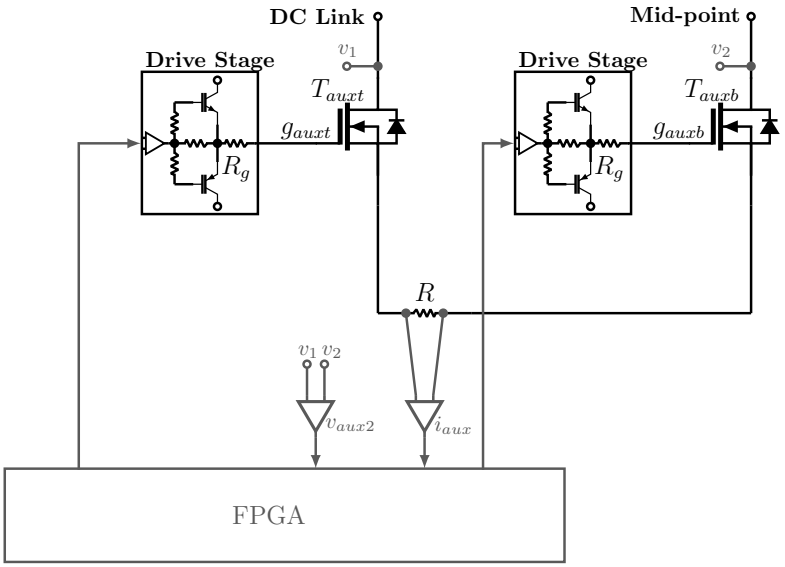



Figure 5.5: Auxiliary branch circuitry. $v_{aux2}$ denotes the combined $v_{ds}$ of both auxiliary MOSFETs.

### 5.2.4 Shaped Switching Transition and Auxiliary Branch Control Boards

The shaped switching transition control board is used for the main control of the power converter. It contains:

- Four ADCs with associated analogue signal processing.
- Two DACs with associated analogue signal processing.
- Two ± 5 V output DC-DC and two 3.3 V DC-DC converters to provide the +5 V and -5 V rails and +3.3 V rails, respectively.

This circuit has two 12-bit DACs, which provides the power MOSFET and injection MOSFET $i_{gs}$ commands. The 12 data lines from the FPGA daughter-board are fed through 47 Ω resistors to the DAC chip, which is set using 7680 Ω to give a 5.0 mA full-scale output. 5.0 mA through the 200 Ω load resistors gives a full load signal voltage of 1.0 V. The voltages are fed through a buffer amplifier with a gain of 2, providing a full load output voltage of 2.0 V. Three ICs are used as single-pole-single-throw (SPST) analogue switches. One IC is used to send the $i_{gs}$ command to either the top power MOSFET or the bottom power MOSFET when controlled. The other two ICs drive each power MOSFET completely on or off as required by the power converter control. As the power MOSFETs are switched, the signals from the SPST analogue switch outputs will be pulled upwards when the top power MOSFET is on or downwards when the bottom power MOSFET is on. Similarly, three ICs are used as SPST analogue

switches to either route the injection MOSFET gate current command to the top or bottom injection MOSFET when controlled or drive each power MOSFET fully on or fully off as required by the power converter control.

The shaped transition control board also has the four 12-bit ADC, for the power MOSFET $v_{ds}$, power MOSFET $v_{gs}$, injection MOSFET $v_{gs}$, and the injection current measurements. An analogue double-pole-single-throw (DPST) switch allows the FPGA to select which power MOSFET is sampled, $T_t/T_b$, and which injection MOSFET is sampled, $T_{ti}/T_{bi}$. The $v_{gs}$ voltage measurements have op-amps that are scaling 20 V down to 2.4 V, the $v_{ds}$ voltage measurements have op-amps scaling 60 V down to 2.4 V, and the current injection measurements have op-amps scaling 0.5 V up to 2.4 V for input to the analogue DPST switches. The differential pair op-amps connected to each ADC scales the 2.4V input signal down to 1.225 V signals, which are inverted from each other around a 0.6125 V common reference corresponding to 0 V in the power circuit. Hence, the digital output of the ADCs is read as an offset binary number.

Similarly, the auxiliary control circuit is used for the control of the auxiliary branch. The control board has similar functionality as the shaped switching transition control board, except the control board is used to control the gate-drives of the auxiliary MOSFETs. ADCs are required to measure the $v_{ds}$ across both auxiliary MOSFETs, $v_{gs}$ of each auxiliary MOSFET, and the auxiliary branch current.

### 5.2.5 Additional Hard Switching Half-Bridge Circuit

The additional hard-switching half-bridge circuit provides a baseline comparison for the prototype to assess EMI performance. The half-bridge consists of two-channel MOSFETs, DC-link electrolytic capacitance, DC-link HF capacitance, and connections to the control and monitoring boards. The DC-link HF capacitance is added in place of the parallel capacitances connected across the MOSFETs. Note that the PCB has not been optimised for hard-switching, so higher than normal ringing is anticipated. An overview of the hard-switching half-bridge circuit is presented in Figure 5.6.

Additionally, a gate-drive board is configured to operate as a hard-switching half-bridge using only the current sourcing section for the power MOSFET gate-drive. Additionally, the gate-drive board is configured with lower gate resistance and excludes the injection circuitry. The power supply circuitry provides two power supplies for the ±15 V gate-drives for each power MOSFET with 0 V connected to the power MOSFET source to facilitate the power MOSFET gate current sourcing. The controlled current source driving current into the gate of each power MOSFET is created by an op-amp with feedback of the voltage across a 15 Ω gate resistor. The op-amp will change the output

to create the necessary voltage across the gate resistor, and the current sourced is determined by the resistance.

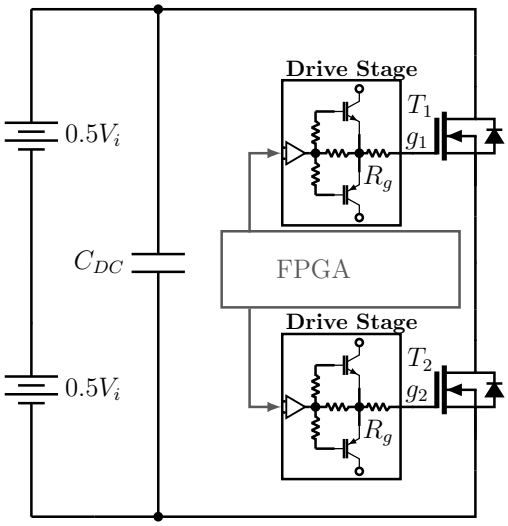



Figure 5.6: Hard-switching half-bridge circuit.

## 5.3 Half-Bridge Control Philosophy

### 5.3.1 Control Strategy Overview

Due to a large number of DAC and ADC conversions, two FPGA processors are used. Therefore, the control system must determine when switching transitions should be initiated and send out control signals to each FPGA to initiate the switching transitions. The control requires fast ADC but has the advantage of varying the gain of the control loop, depending on the gate-voltage and the MOSFET region of operation. The control will fine-tune the $v_{ds}$ with each successive switching transition, which accounts for differences in the MOSFET parasitic components. Additionally, the derivative of the transitions at $0.5V_i$ will reach a maximum and will set the steepness parameter of the reference logistic waveform. Since there can be as much as a 10% error in the capacitance rating, the reference waveform must ensure the maximum derivative does not exceed the linear response of the capacitor once it is fully charged. Otherwise, there will be inconsistencies in the output waveforms of the controlled MOSFETS, and the desired low-EMI outcome will not be achieved.

Lastly, a complete shaped switching transition requires the $\alpha$-MOSFET to undergo a controlled turn-off during the first half of the shaped-switching transition and the $\beta$-injection-MOSFET to undergo a controlled turn-on during the second half of the shaped

transition. Therefore, understanding the transient response of the MOSFET during turn-on and turn-off is required as the MOSFET moves between various operating regions as the gate drives are being controlled. The MOSFET control sequences for the $\alpha$-MOSFET and $\beta$-injection MOSFET are outlined in the following sections.

### 5.3.2 Power MOSFET Control Overview

During MOSFET turn-off, the $\alpha$-MOSFET $v_{ds}$ can be controlled to start at zero, and the shaped switching transition can follow the reference waveform that is stored in a look-up table. Additionally, the $\alpha$-MOSFET will be switched off once $0.5V_i$ is reached. The default $v_{ds}$ target waveform can be set based on the maximum $dv_{ds}/dt$ that could occur, which is constrained by the selection of the capacitor used and the minimum expected capacitance value based on manufacturing margins of error.

Since the power MOSFETs in the half-bridge are acting complementary to each other when the $\alpha$-MOSFET undergoes a controlled rising transition of $v_{ds}$, the $\beta$-MOSFET will undergo a falling transition. The control implementation outlined in the remainder of this Section is intended to achieve a controlled rising transition of the $\alpha$-MOSFET. Note that the control philosophy presented in the remainder of this Section is generalised, and the currents are represented on a normalised per-unit (pu) basis, where is 1 pu is the maximum design value.

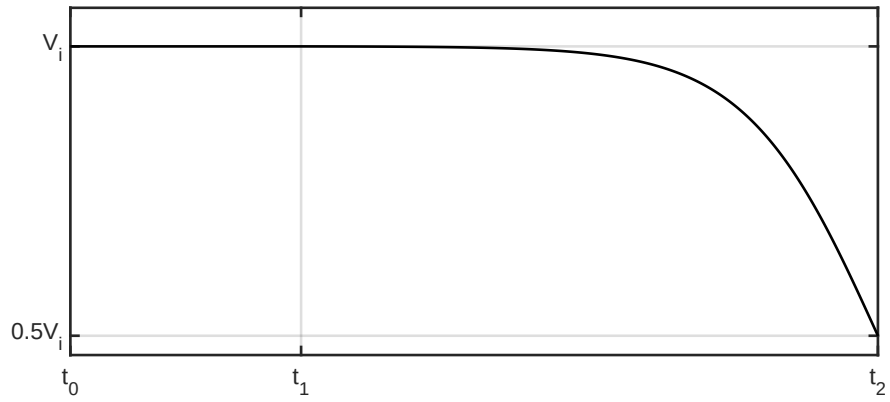
Initially, the MOSFET requires a 1 pu $i_{ds}$ at the start of the turn-off transition, ensuring a consistently shaped switching transition for all switching instances. Considering the load current may vary anywhere between -1 pu and 1 pu, the current in the auxiliary branch will vary between 2 pu and 0 pu, respectively. Bidirectional current is required in many power converters and is specifically required in inverters. The auxiliary branch circuit must be initiated before switching, where the total current in the load and auxiliary branch ($I_{load} + i_{aux}$) reaches 1 pu at the point where the MOSFET is entirely turned off and all current is now flowing through the parallel smoothing capacitors. For the auxiliary branch current to satisfy the $I_{load} + i_{aux} = 1$ pu criteria, the time required to ramp the auxiliary branch current to the target value is dependant on the load current. For example, if $I_{load}$ is close to -1 pu, then the auxiliary branch current needs to reach close to 2 pu, which the auxiliary branch must initialise a considerable amount of time before the MOSFET turn-off commences. Conversely, if the load current is 1 pu, then the auxiliary branch is not required.

When considering the prototype development, two modes of operation are implemented, which operates the half-bridge circuit under no-load and constant load conditions. For the circuit to operate under no-load conditions, the circuit relies on the auxiliary branch

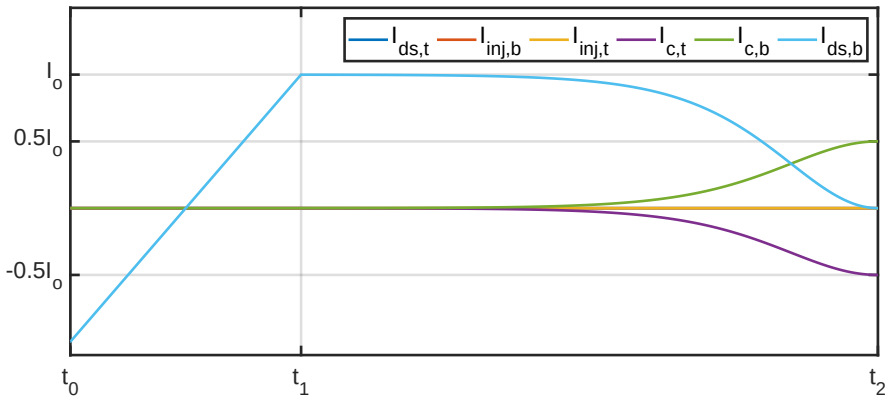
to ramp to 1 pu just before the turn-off is complete. When the circuit is operating when there is load such that $i_{ds} < 1$ pu, the auxiliary branch will still operate to ensure the MOSFET $i_{ds}$ of 1 pu is satisfied. Therefore, if the load current is 0.5 pu, the auxiliary branch will ramp to 0.5 pu when the top power MOSFET is the $\alpha$-MOSFET, and will ramp to 1.5 pu when the bottom power MOSFET is the $\alpha$-MOSFET.

The $\alpha$-MOSFET shaped rising transition commences with the $v_{ds}$ being controlled to follow the desired reference $v_{ds}$ shaped transition provided by a look-up table in the FPGA. The shaped transitions start from zero, or a small DC offset governed by the on-state $v_{ds}$ voltage drop of the $\alpha$-MOSFET. Initially, this is achieved with direct $i_{gs}$ control of the half-bridge $\alpha$-MOSFET. When $v_{ds}$ approaches $0.5V_i$, the $\beta$-injection MOSFET circuit will take over the control of the $v_{ds}$ waveform from the $\alpha$-MOSFET gate-drive control. The $v_{gs}$ undergoes a controlled ramp from $V_{th}$ to 0 V by injecting constant current into the gate of the $\beta$-injection MOSFET, to provide a smooth transfer. Note that the ramp-down will vary from MOSFET to MOSFET due to differences in $V_{th}$, and the time-scale is merely estimated for discussion purposes.

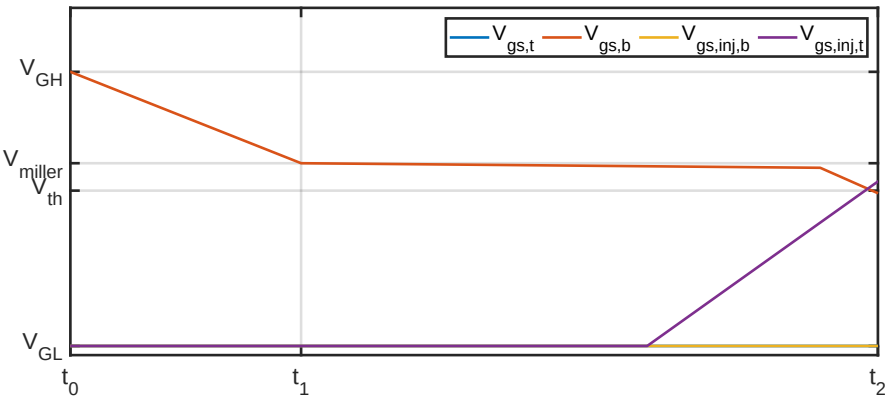
Figure 5.7 provides a waveform overview for $\alpha$-MOSFET control sequence. The illustrative example presents the expected behaviour of the half-bridge mid-point voltage, all power and injection MOSFET $i_{ds}$, all power and injection MOSFET $v_{gs}$, the parallel capacitor currents, and the auxiliary branch current. Furthermore, since the timing instances are generalised, the auxiliary current is not included. Instead, $i_{ds}$ of the the $\alpha$-MOSFET is ramped during the time interval $[t_0, t_1]$ to illustrate the effects of the auxiliary branch current on the $i_{ds}$ of the power MOSFET.




(a)




(b)




(c)

Figure 5.7: Illustrative example of the waveforms for the $\alpha$-MOSFET control sequence.

### 5.3.3 Injection MOSFET Control Overview

The $\beta$-injection MOSFET control mechanism is outlined in this Section. When the half-bridge is in the middle of a controlled switching transition, the half-bridge $\alpha$- and $\beta$-MOSFETs are both off, and the current ($I_{load}$+ $i_{aux}$) is flowing in the smoothing capacitors with a constant $dv_{ds}/dt$. Note that for ideal low-EMI shaped switching control, the constant $dv_{ds}/dt$ is momentary. These initial stages of this transition require the current to be ramped in the auxiliary branch, for instances where the load current is not 1 pu. Before the $\alpha$-MOSFET is turned off, the auxiliary branch is turned on to allow current to build up in the $\alpha$-MOSFET, which is transferred to the two capacitors as the controlled, shaped transition progresses. Once the current in the $\alpha$-MOSFET reaches 1 pu, the remainder of the controlled, shaped transition utilises the $\beta$-injection MOSFET.

Before $v_{ds}$ reaches $0.5V_i$, the $\beta$-MOSFET is prepared before injecting current, which requires $v_{gs}$ to almost reach $V_{th}$ of the MOSFET. Once $v_{gs}$ is near $V_{th}$, there is adequate charge build-up in the gate of the $\beta$-injection MOSFET to reduce the transient response time, which is desired for a smooth transition between the $\alpha$-MOSFET being turned off and the $\beta$-injection MOSFET being turned on to control the waveform shaping for the second half of the controlled switching transition.

Once the $\alpha$-MOSFET is turned off, and the $v_{ds}$ has reached $0.5V_i$, the $\beta$-injection MOSFET commences the gate-drive control to shape $v_{ds}$ during the second half of the transition. When the $v_{ds}$ approaches $0.5V_i$, the $\alpha$-MOSFET has reached a full-turn off, and all current should be in the smoothing capacitors. The injection circuit controls the $v_{ds}$ waveform by controlling the gate-drive of the $\beta$-injection MOSFET, which controls the injection current to achieve the desired $dv_{ds}/dt$ for the switching transition shaping.

After $v_{ds}$ has reached $V_i$, the $\beta$-injection MOSFET is turned off, and the $\beta$-MOSFET is turned on, which is the end of the controlled shaped switching transition. Since the $\beta$-MOSFET is turned on under zero-voltage conditions, no current transfer to the $\beta$-MOSFET occurs until the $\beta$-injection MOSFET is turned off.

Figure 5.7 provides a waveform overview for $\beta$-injection MOSFET control sequence. The illustrative example presented the expected behaviour of the half-bridge mid-point voltage, all power and injection MOSFET $i_{ds}$, all power and injection MOSFET $v_{gs}$, the parallel capacitor currents, and the auxiliary branch current. Furthermore, since the timing instances are generalised, the auxiliary current is not included. Instead, $i_{ds}$ of the the $\alpha$-MOSFET is ramped during the time interval $[t_3, t_4]$ to illustrate the effects of the auxiliary branch current on the $i_{ds}$ of the power MOSFET.

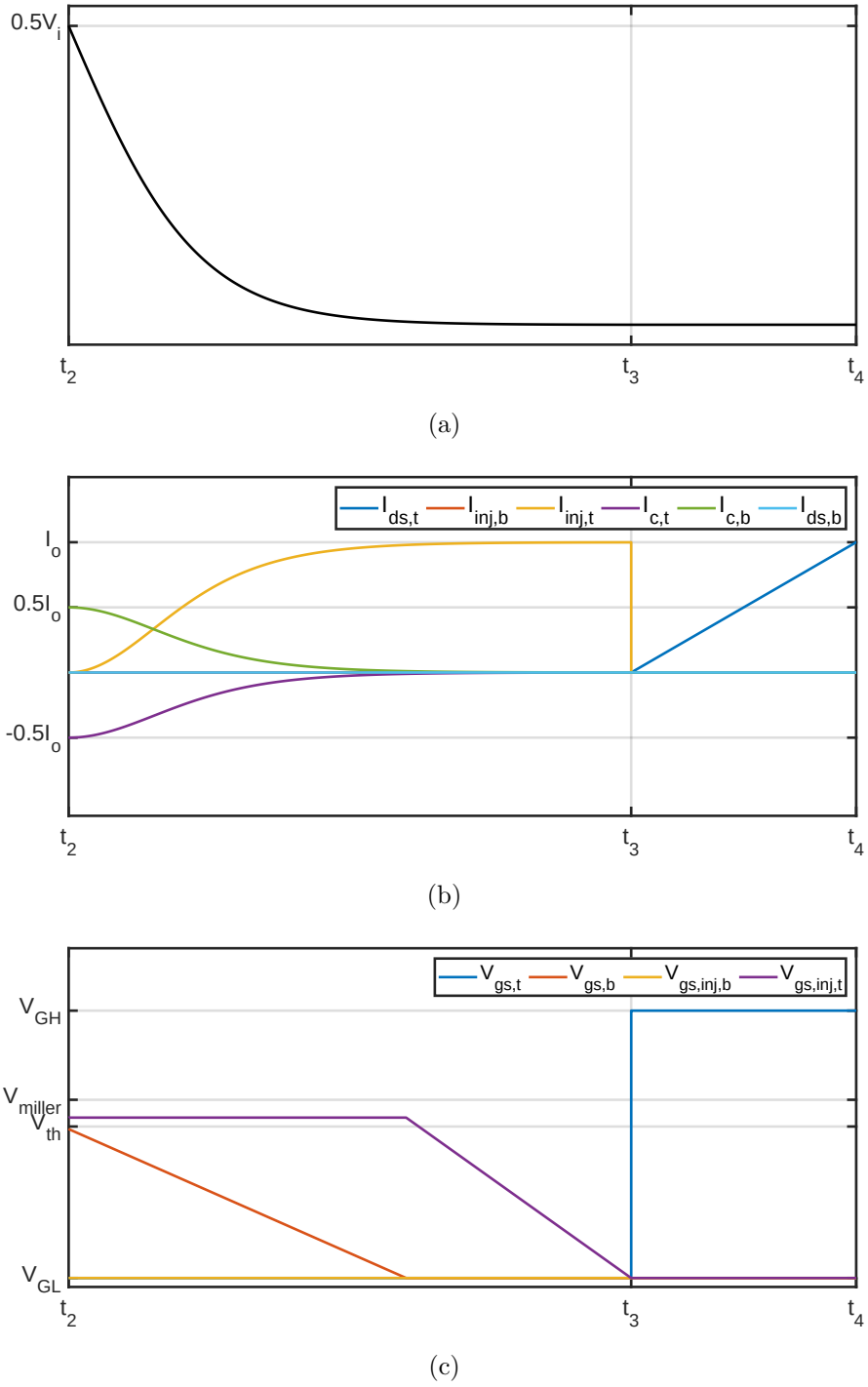



Figure 5.8: Illustrative example of the waveforms for the $\beta$-injection MOSFET control sequence.

## 5.4 FPGA Control Implementation

### 5.4.1 Overview

The FPGAs contain all the programmable logic to operate the prototype low-EMI power converter. All necessary voltage and current measurements are brought into the FPGA for processing to be used to control the half-bridge power converter. The measured $v_{ds}$ of the power MOSFETs are compared to a reference waveform, and the control is implemented, which causes the power circuit mid-point voltage to follow the reference waveform. The power converter operation is controlled with typical PWM using a 50% duty cycle. There are two FPGAs used in the control of the prototype low-EMI power converter. The first FPGA contains all the programmable logic for the control system initialisation, control signal timing, $\alpha$-MOSFET control and $\beta$-injection MOSFET control. The second FPGA contains all the programmable logic for the auxiliary branch control and the hard-switching control.

Measured values from the ADCs, and values sent to the DACs, appear in the FPGA as 12 bit offset binary words. These are converted into two's complement (2c) for ease of arithmetic in the control logic. Different measured signals have unique peak values, and hence resolution. The load and $v_{ds}$ signals have a peak measurement value of 60 V, $v_{gs}$ signals have a peak measurement value of 20 V, and current measurements have a peak measurement value of 25 A. A table of bits and resolutions is presented in Table 5.2.

### 5.4.2 Control System Initialisation

The FPGA is initially set up with timing logic to define the various control regions of the low-EMI half-bridge prototype and data inputs for voltage and current measurements. Clock signals are generated to define global timing and establish timing commands for the auxiliary circuit control, switching command control, switching transition, and inter-transition control. Part of the initialisation phase includes setting up various constants used as either time delays in the error calculation algorithm or as time constants used to initialise commands throughout the switching transition. For example, a delay is implemented in the error calculation algorithm to represent the transient response delay of the MOSFET and FPGA signal delays. Additionally, time constants are established, which define the time to start the auxiliary circuit control, switching command control and waveform shaping control.

Firstly, the control is established with the clock signal and global timing-related logic, push-button input, control initialisation settings, dip-switch inputs for various shaped references and definitions of various constants used throughout the control. The FPGA clock signal operates at a 50 MHz frequency, corresponding to 20 ns time-steps. Ad-

Table 5.2: Bit resolutions for various voltage and current signals

| **Maximum** | 60 V | 20 V | 25 A |
|---|---|---|---|
| **Unit** | V | V | A |
| 11 MSB | sign | sign | sign |
| 10 | 30.00 | 10.00 | 12.50 |
| 9 | 15.00 | 5.00 | 6.25 |
| 8 | 7.50 | 2.50 | 3.13 |
| 7 | 3.75 | 1.25 | 1.5625 |
| 6 | 1.875 | 0.625 | 0.78125 |
| 5 | 0.9375 | 0.3125 | 0.39063 |
| 4 | 0.46875 | 0.15625 | 0.19531 |
| 3 | 0.23438 | 0.07813 | 0.09766 |
| 2 | 0.11719 | 0.03906 | 0.04883 |
| 1 | 0.05859 | 0.01953 | 0.02441 |
| 0 (LSB) | 0.02930 | 0.00977 | 0.01221 |
| Resolution (mV) | 29.30 | 9.77 | 12.21 |

ditionally, a 10 MHz clock signal is generated and used throughout the control logic. The counting of the clock signals is used to define the timing instances throughout the control system implementation. Firstly, a global timing signal is created using a counter, which is used to initiate the control commands of the auxiliary circuit control, switching command control, and switching transition control. The global timing starts the switch command, which sets the switching frequency of the power converter. Additionally, the global timing toggles the auxiliary branch control commands, where each rising edge of the signal generates a signal to commence the auxiliary branch control.

Additionally, the initialisation includes input from the FPGA dip-switches used to select either a logistic-shaped, sinusoidal-shaped or S-shaped reference waveform stored in the FPGA. Therefore, the prototype can compare the performance of various shaped waveforms using the same power converter circuitry whilst also allowing the robustness of the control to be tested by assessing whether the prototype can accurately follow numerous reference profiles.

Four 12-bit parallel data inputs from the four ADCs on the control and monitoring board include interfacing logic to provide the power MOSFET $v_{gs}$, power MOSFET $v_{ds}$, injection MOSFET $v_{gs}$, and auxiliary current measurements data in offset binary

format. The offset binary is converted into 2c and negative 2c to compute data throughout the control logic.

An approximate 2.5 kHz square wave generator is created using an 11-bit counter, and when enabled by the global timer, forms the switch command for the low-EMI half-bridge. Since the charging of the auxiliary inductor and shaped transition control occurs at different times, the switch command edge initiates a separate time for each. A switch command edge occurs whenever the switch command is detected and initiates a controlled rising transition of the low-EMI half-bridge mid-point voltage. Conversely, a low switch command initiates a controlled falling transition of the half-bridge mid-point voltage, which creates a 50% duty cycle. When a rising or falling transition is required, a timer for the initiation of the switching commands and auxiliary command is activated. Note that the timing instances to start controlling the auxiliary branch depends whether the half-bridge mind-point voltage is undergoing a controlled rising or falling transition.

Lastly, the switching transition command is generated, which is the period when the waveform shaping for the half-bridge prototype is in effect. The switching transitions command is initiated by a timer when a switching start command is detected. The switching transition command is active when switching start commands are detected and remains high until a counter for the transition command reaches the transition period, set to 10 $\mu$s. After 10 $\mu$s, the switching transition command is reset and does not become active again until the waveform shaping is required for the subsequent switching instant. An illustrative overview of the FPGA initialisation sequence considering the switching initialisation command ($I_{CMD}$), auxiliary branch command ($A_{CMD}$), switching command ($S_{CMD}$), and transitions command ($T_{CMD}$) and the respective counter time delays $\Delta t_{init}$, $\Delta t_{aux}$, $\Delta t_{sw}$, and $\Delta t_{tran}$ is presented in Figure 5.9. Note the time delay between $\Delta t_{sw}$ and $\Delta t_{tran}$ is one clock cycle. The time delays between $\Delta t_{init}/\Delta t_{aux}$, and $\Delta t_{init}/\Delta t_{sw}$ include multiple clock cycles which represent the time delays.

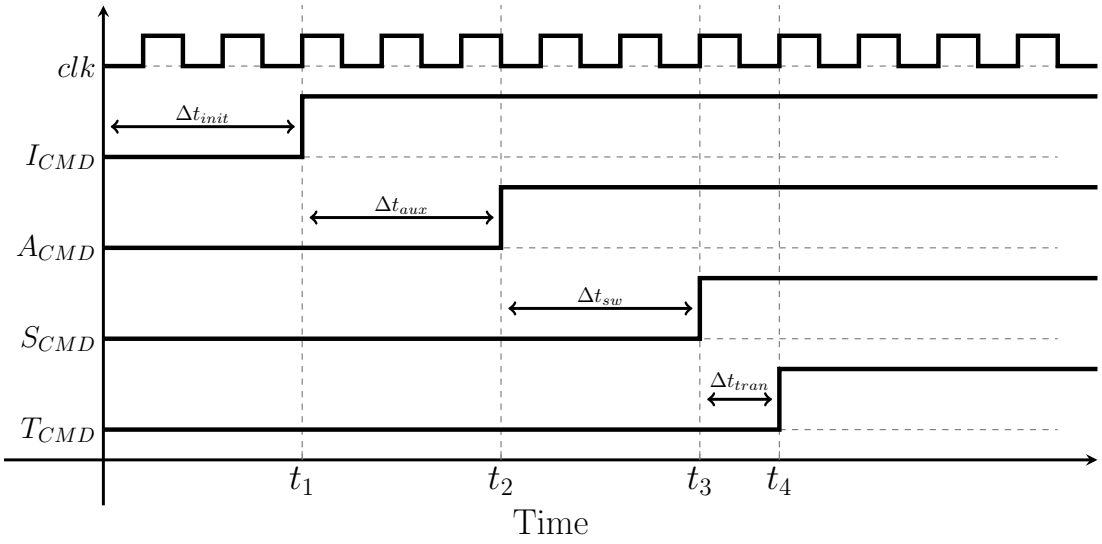



Figure 5.9: FPGA initialisation sequence considering the switching initialisation command ($I_{CMD}$), auxiliary branch command ($A_{CMD}$), switching command ($S_{CMD}$), transition command ($T_{CMD}$), and the respective counter time delays $\Delta t_{init}$, $\Delta t_{aux}$, $\Delta t_{sw}$, and $\Delta t_{tran}$.

Within the period of a shaped transition, timing instances are defined, which establish regions of set-up and control during the shaped transition. These timing instances are defined as follows:

- The period of the gate current command that is sent to the DAC of the $\alpha$-MOSFET gate-source during a rising transition.
- The period of the gate current command that is sent to the DAC of the $\alpha$-MOSFET gate-source during a falling transition.
- Timed instances within a transition period are defined as follows:
  - Region 1: 480 ns. Becomes active when the transition count exceeds 480 ns.
  - Region 2: 1,280 ns. Becomes active when the transition count exceeds 1,280 ns, which is the mid-point of the transition.
  - Near $0.5V_i$: Becomes active 200ns before the mid-point.

Logic is also established to determine periods within a shaped transition. These instances help determine the control actions to take during the transition, such as gate-drive preparation, gate-drive control, gate-drive to full-on, and gate-drive to full-off. The near-$0.5V_i$ is used to select which $v_{gs}$ and $v_{ds}$ voltage signals goes to each ADC that are required for their respective control within the transition sequence. In the first

half of the transition, the $\alpha$-MOSFET $v_{gs}$ and $v_{ds}$ signals are required. In the second half of the transition, the $\beta$-MOSFET $v_{ds}$ and $\beta$-injection MOSFET $v_{gs}$ signals are required. Lastly, the switch and auxiliary branch commands are also sent as timing commands to the second FPGA. The auxiliary branch control determines which MOSFET in the auxiliary branch to turn on, and hence, the direction of current will flow in the auxiliary branch.

### 5.4.3 $\alpha$-MOSFET Control

This section outlines the $\alpha$-MOSFET control, which uses stored reference waveforms for the $v_{ds}$ transition and performs error signal processing computation to determine the gate-drive commands and reduce the error between the reference $v_{ds}$ and the measured signal. An overview of the $\alpha$-MOSFET control strategy is presented in Figure 5.10. At a high level, the $\alpha$-MOSFET control performs the following functions:

- Reference waveforms are stored in memory and are converted into 2c format for error signal computation.
- $0.5V_i$ detection is implemented to ensure the $\alpha$-MOSFET control does not exceed $0.5V_i$ of the switching transition.
- The error signal is computed, which is an array of the 16 most recent error signals and is shifted up by 16-bits for improved resolution.
- Logic is created to determine when the $\beta$-MOSFET is turned on.
- The $v_{ds}$, $v_{gs}$, and $i_{gs}$ reference waveforms are read out from temporary storage. The error signal is added, and the $i_{gs}$ command of the $\alpha$-MOSFET is determined.
- Gate-drive commands are sent to the $\alpha$-MOSFET and $\beta$-MOSFET depending on timing within the transition. The $i_{gs}$ command is used to control the MOSFETs when $v_{ds}$ is in the first half-of of the transition ($v_{ds} < 15$ V $= 0.5V_i$).

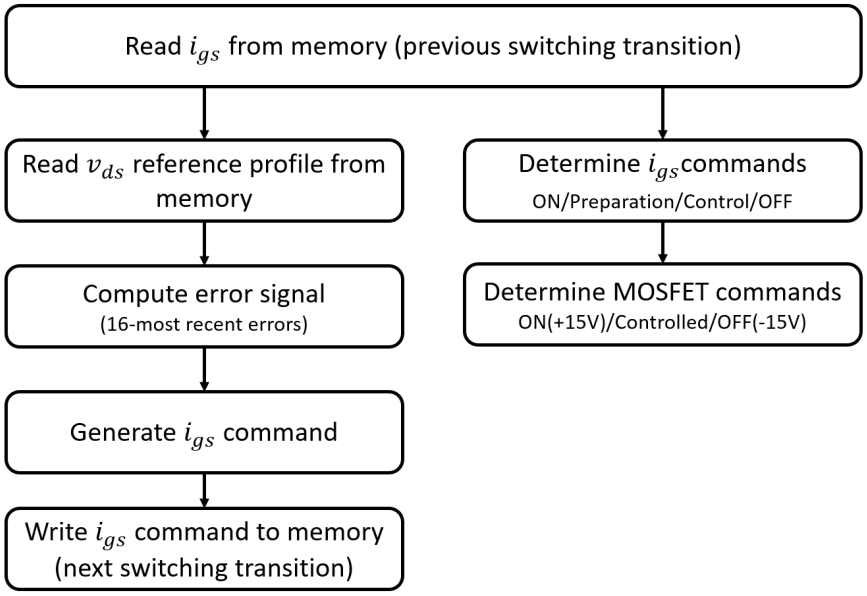



Figure 5.10: $\alpha$-MOSFET control strategy.

The $v_{ds}$ reference waveforms are stored in a 36-bit ROM memory block. The ROM block stores three reference waveforms, which utilise 12-bits of data each. The top-third of the ROM memory block store the logistic reference waveform, which is accessed by setting 11 on the dip-switches. The middle-third of the ROM memory block stores the sinusoidal reference waveform, which is accessed by setting 10 on the dip-switches. The bottom-third of the ROM memory block stores the S-shaped reference waveform, which is accessed by setting 01 on the dip-switches. The outputs generated by the stored reference waveforms include a binary output indicating when a reference profile is being generated and a binary output indicating the period when the $v_{ds}$ reference profile is the reference profile for the $\alpha$-MOSFET or the $\beta$-injection MOSFET.

When the switch start and transition start commands are enabled, an up-down counter will count up during the first half of the waveform, and count down for the second half of the transition. The counter designates the stored $v_{ds}$ reference waveform for the $\alpha$-MOSFET and $\beta$-injection MOSFET portions of the transition, respectively. A load enable command is generated when the timing in the transition reaches 1.68 $\mu$s, which allows the waveform to be delivered in sequential order, then reverse order for the $\alpha$-MOSFET and $\beta$-MOSFET injection portions of the transition, respectively. An example of how the $v_{ds}$ reference waveform is delivered is presented in Figure 5.11. The example shows the first half of the rising transitions being used for the $\alpha$-MOSFET and the second half of the falling transitions for the $\beta$-injection MOSFET.

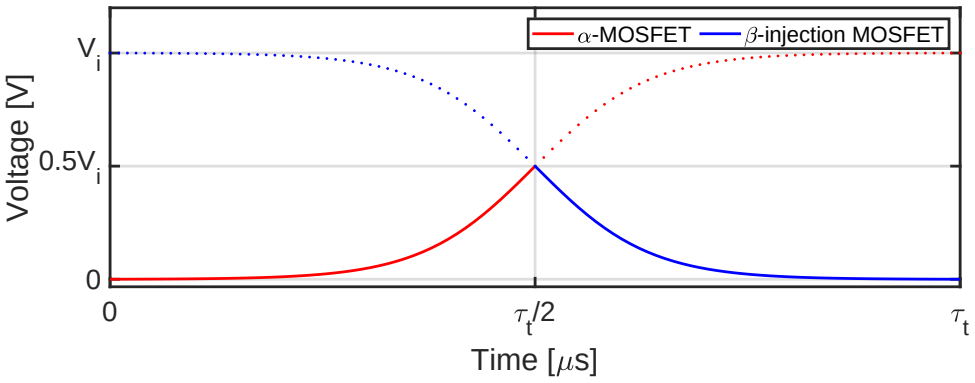



Figure 5.11: $v_{ds}$ portions of the reference profile for the $\alpha$-MOSFET (red trace) and $\beta$-injection MOSFET (blue trace).

The reference waveform is converted to negative 2c and then subtracted from the measured $\alpha$-MOSFET $v_{ds}$ to compute the error signal. Following this, the signal is passed through the $0.5V_i$ detection. If $v_{ds} < 0.5V_i$, the error signal is permitted. Otherwise, the error signal is set to zero, preventing conflicting control between the $\alpha$-MOSFET and $\beta$-injection MOSFET gate-drives.

Next, the error signal algorithm is applied to sum the 16 most recent error signals, which uses an 8-signal error summing function twice. The error signal function outputs the sum of the eight most recent signals and an 8-clock cycle delayed error signal. The 8-clock cycle delayed signal is then passed through the error signal function, which outputs the sum of another eight error signals and a 16-clock cycle delayed error signal. The two summed 8-clock cycle error signals are added together to produce the sum of the 16 most recent error signals. A gain is applied to the error signal and is then added to the gate current command signal from the previous transition. The resultant is the $i_{gs}$ command for the subsequent switching transition.

Next, the $\alpha$-MOSFET $i_{gs}$ command signal is generated and stored, and then the output binary signals and commands to control the $\alpha$-MOSFET are created. The $\alpha$-MOSFET $i_{gs}$ command created in the previous switching transition is read out of temporary storage, and the summed error signal is added to the $i_{gs}$ command, which is then stored in temporary storage for the next transition and applied at the same instant of each transition. The $i_{gs}$ commands are read out of separate memory blocks for the rising and falling transitions, and the writing of the $i_{gs}$ commands are enabled only when the respective rising or falling transition is enabled. The $i_{gs}$ command read from stored memory is then added with the accumulated error signal during the current switching

transition before it is stored in memory for the next transition. Positive and negative limits are included in the summing function to ensure the $i_{gs}$ command does not reach unexpected or out of range values, which can be caused by significant errors when the circuit is first energised or if there are timing issues during initial implementation and troubleshooting.

The timing of the reading and writing of the $i_{gs}$ command is critical since it considers the signal delays within the FPGA and the transient response of the MOSFET. Firstly, the $\alpha$-MOSFET $i_{gs}$ command is read from temporary storage 640 ns before the transition count is enabled, which ensures the error signal can be added to the $i_{gs}$ command before being stored for the next transition.

In addition to the $i_{gs}$ commands, the $v_{gs}$ is prepared to reach a target voltage at the start of the controlled operation. The target voltage ensures a fast response of the MOSFET, which limits the transient response time. The measured $v_{gs}$ and target $v_{gs}$ are compared to generate an error signal, which is used in a proportional control to ensure the $\alpha$-MOSFET $v_{gs}$ reaches the target voltage. The output of the proportional control is an $i_{gs}$ preparation command, which is fed to the $\alpha$ MOSFET $i_{gs}$ command before the $\alpha$-MOSFET gate drive control commences.

Once the $\alpha$-MOSFET $i_{gs}$ signal is calculated, the $\alpha$-MOSFET $i_{gs}$ command is then determined. Logic to determine the output $\alpha$-MOSFET $i_{gs}$ is dependant on whether the $i_{gs}$ control, $v_{gs}$ preparation, or if commands to drive the MOSFET on or off is required. Before the transition control is enabled, the $i_{gs}$ signal is held constant, and the MOSFET is on. Before the high or low transition becoming active, and after a pre-defined amount of time (480 ns), the $i_{gs}$ command is the proportional control that is required to prepare the $\alpha$-MOSFET $v_{gs}$.

Once the rising or falling transition is active, the $i_{gs}$ command is the $i_{gs}$ control signal, including the summed error signals. Once the transition reaches the mid-point, the $i_{gs}$ command is zero for the rest of the transition. Additionally, the $\beta$-MOSFET turns on at the end of the shaped transition when the $\beta$-injection is complete. The $\beta$-MOSFET is turned on and will stay on until the transition-start command is issued to commence the next switching transition. An example of the $\alpha$-MOSFET $i_{gs}$ commands is presented in Figure 5.12. The plot demonstrates the four $i_{gs}$ commands required throughout a shaped switching transition. From $t_0$ to $t_1$ the MOSFET is off. From $t_1$ to $t_2$ proportional control is implemented. Form $t_2$ to $t_3$ control is required during a rising or falling transition. Lastly from $t_3$ to $t_4$ the MOSFET is off.

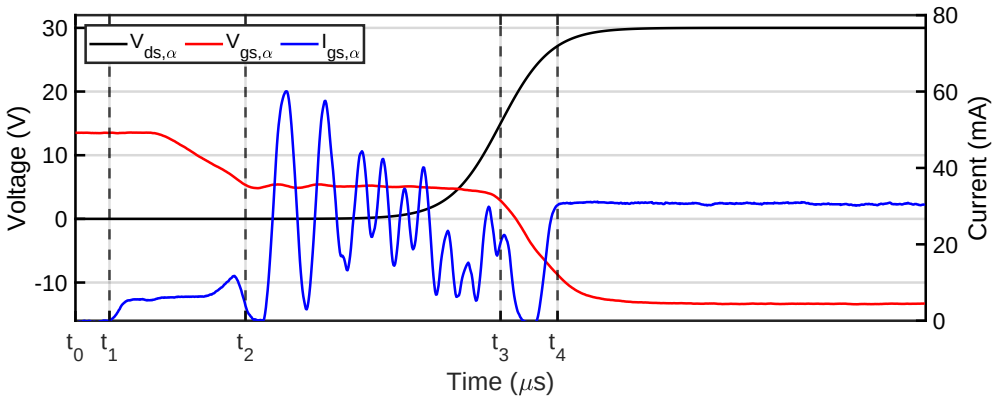



Figure 5.12: Example of $\alpha$-MOSFET $i_{gs}$ commands.

Once the conditions of the $\alpha$-MOSFET $i_{gs}$ command signal are determined, the MOSFET output commands are set, which are logic conditions to either turn the MOSFET on, turn the MOSFET off, or control the gate-drive of the MOSFET. The output commands are determined for both the bottom and top MOSFET, governed by the rising or falling transition of the half-bridge mid-point, respectively. The top MOSFET $v_{gs}$ is driven down to -15 V and is off when the top MOSFET is the $\alpha$-MOSFET, and the $v_{ds}$ has reached $0.5V_i$ of the shaped transition, or the top MOSFET is the $\beta$-MOSFET and is required to be off when the switch command is enabled since it is not required for waveform shaping. The top MOSFET is controlled when the transition command is active, the transition period between Region 1 and 2 is active, and the switch command is low. The MOSFET being controlled includes both the proportional control preparation and the $i_{gs}$ command. The top MOSFET $v_{gs}$ is driven up to 15 V and is on when the top MOSFET is the $\alpha$-MOSFET during the shaped transition before the control is initiated, or it is the $\beta$-MOSFET whilst the switch command is high, and the $\beta$-MOSFET on command is active.

### 5.4.4 $\beta$-Injection MOSFET Control

This section outlines the $\beta$-injection MOSFET control, which uses stored reference waveforms for the $v_{ds}$ transition and performs error signal computation and processing to update the gate-drive commands for the $\beta$-injection MOSFET and reduce the error between the reference $v_{ds}$ and the measured signal. An overview of the $\beta$-injection MOSFET control strategy is presented in Figure 5.15. At a high level, the $\beta$-injection MOSFET control performs the following functions:

- Defining $v_{gs}$ regions, near mid-point detection, $v_{gs}$ preparation, and $i_{gs}$ limits for the $\beta$-injection MOSFET.

- Establishing $\beta$-injection MOSFET control regions.
- Calculating the $v_{ds}$ error signal and generating the $\beta$-injection MOSFET gate-drive commands.
- Commands are sent to the injection MOSFETs depending on a rising or falling transition during the the second half-of the shaped transition ($v_{ds} > 15$ V).

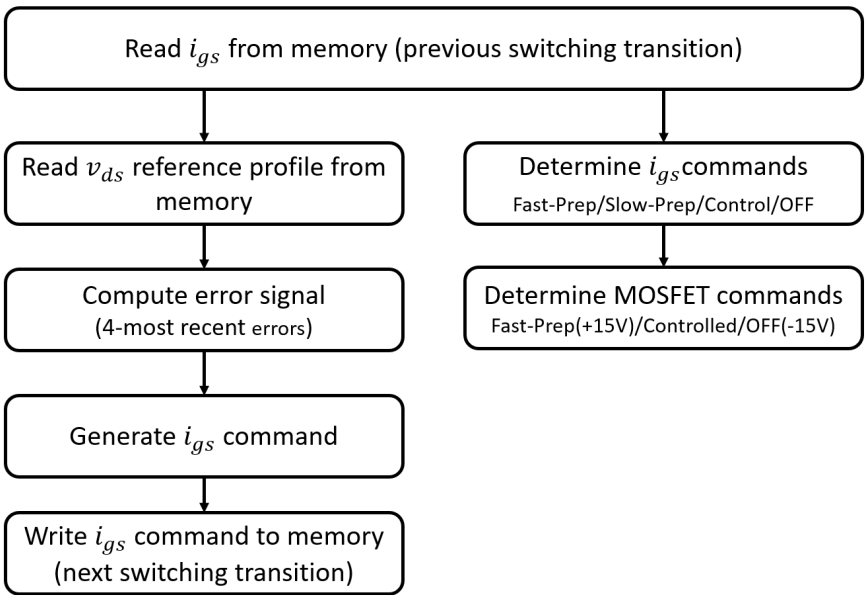



Figure 5.13: $\beta$-injection MOSFET control strategy.

Firstly, $v_{gs}$ regions are defined, which are 5 V, 2.656 V, 1.406 V and -5 V. Comparators are used to detect whether the $\beta$-injection MOSFET exceeds the voltage of a defined region. Additionally, the target starting $v_{gs}$ of the injection-MOSFETs are defined, which are 1.53 V and 1.72 V for the rising and falling transitions, respectively. The $\beta$-injection MOSFET $v_{gs}$ is prepared to reach a target voltage at the start of the controlled operation, which ensures a fast response of the MOSFET to limit the transient response time. The target $v_{gs}$ is around the $V_{th}$, which is the boundary between the cut-off region and Ohmic region of the MOSFET.

The measured $v_{gs}$ and target $v_{gs}$ are compared to generate an error signal, which is used in a proportional control to ensure the $\beta$-injection MOSFET $v_{gs}$ reaches the target voltage. The output of the operation is the $i_{gs}$ preparation command, which is fed to the $\beta$-injection MOSFET gate current command before the $\beta$-injection MOSFET gate drive commences. The period where the current injection preparation is active is set when the shaped transition control of the $\alpha$-MOSFET is active and $v_{ds}$ is less than the near-$0.5V_i$ voltage. The near-$0.5V_i$ value is set to 14.06 V, which will enable the

$\beta$-injection control once a counter reaches near-$0.5V_i$. Limits are placed the $i_{gs}$ values, which are defined by the $v_{gs}$ region values shown in Table 5.3. The current limits are used to keep the $\beta$-injection MOSFET $v_{gs}$ from moving rapidly beyond the controllable regions.

Table 5.3: Current limit regions based on gate-source voltage

| **Injection Gate Current Limit** | **Positive Gate Current** | **Negative Gate Current** |
|---|---|---|
| Upper | $v_{gs} < 1.406$ V | $v_{gs} > 1.805$ V |
| Lower | $1.406 \text{ V} \leq v_{gs} < 2.656$ V | $1.406 \text{ V} < v_{gs} \leq 1.805$ V |
| Zero | $v_{gs} \geq 2.656$ V | $v_{gs} \leq 1.406$ V |

Lastly, the various regions of the $\beta$-injection MOSFET control is defined. The first controlled region is the period when the $\beta$-injection MOSFET $v_{gs}$ is rapidly increased with the maximum gate current before controlled current injection for wavefrom shaping commences. This control region is active when the $\alpha$-MOSFET control is active before the $0.5V_i$ is reached, and the $v_{gs}$ is less than -5 V.

The second control region is when the $\beta$-injection MOSFET $v_{gs}$ is slowly being increased towards the target starting injection $v_{gs}$. This control region uses the aforementioned proportional control to increase the $v_{gs}$, which is active when the $\alpha$-MOSFET control is active before the near-$0.5V_i$ is reached, and the $v_{gs}$ is greater than 0 V. The third control region is the period when the $\beta$-injection MOSFET $i_{gs}$ command is controlled to shape the half-bridge mid-point voltage for the second half of the transition. The $\beta$-injection MOSFET injection control is active when the $v_{ds}$ is near-$0.5V_i$ ($\geq 14.06$ V).

The controlled regions are then used to determine whether data is to be sent to the $\beta$-injection MOSFET $i_{gs}$ DAC to control $i_{gs}$ or not. The control injection is enabled when the $v_{gs}$ preparation is required, and the injection current is required to shape the half-bridge mid-point voltage. The controlled injection is not required when the transition command is not active and the $\beta$-injection MOSFET $v_{gs}$ is being rapidly increased towards -5 V.

The following stages in the $\beta$-injection MOSFET control is the generation and processing of the error signal, which will be used to create the $i_{gs}$ command for the subsequent switching transition. The $0.5V_i$ detection enables the error signals to be calculated. Otherwise, the error is set to zero to prevent untimely error signals early in the transi-

tions used in the $\beta$-injection current control. Setting the $\alpha$-MOSFET to stop controlling at $0.5V_i$ and the $\beta$-injection MOSFET to start controlling ensures no undesired overlap between the two control strategies.

Instead of the 16-most recent errors signals required for the $\alpha$-MOSFET $i_{gs}$ command, the $\beta$-injection only requires the four most recent error signals. Since the $v_{ds}$ is at $0.5V_i$ when the current injection is applied, the response of the $\beta$-injection MOSFET needs to be rapid. Therefore the $v_{gs}$ is prepared to be near $V_{th}$ before the current injection commences. Conversely, although the $\alpha$-MOSFET is also prepared, the initial control of the $\alpha$-MOSFET during the initial turn off requires $v_{ds}$ to be controlled slowly, which requires careful control of $i_{gs}$ when $v_{gs}$ is near the Miller plateau region. The four most recent error signals are created using three D-flip-flops, which are summed to give the error signal for the $\beta$-injection MOSFET. The magnitude of the error signal is shifted by 18-bits to provide a gain to the error signal.

Next, the $\beta$-injection MOSFET $i_{gs}$ command signal is generated and stored. Additionally, the output binary signals and command data values are created to control the $\beta$-injection MOSFET. The $\beta$-injection MOSFET $i_{gs}$ is read out of temporary storage, which was generated in the previous switching transition, so the summed error signal and applied gain can be added to the $i_{gs}$ command before the command is stored for the next transition. The timing of the reading and writing of the $i_{gs}$ command is essential since it considers the signal delays within the FPGA and the transient response of the MOSFET. Firstly, the $\beta$-injection MOSFET $i_{gs}$ command is read from temporary storage 720 ns before the transition count being enabled, which ensure the error signal can be added to $i_{gs}$ command before being stored for the next transition.

The $i_{gs}$ command values are only read from memory when enabled by the $0.5V_i$ detection, which ensures the $i_{gs}$ command values are read out only when $i_{gs}$ control is required. Note, the $i_{gs}$ commands are read out of separate memory blocks for the rising and falling transitions and are only enabled when the respective rising or falling transition is enabled. The $i_{gs}$ command that has just been read out of stored memory is then stored in memory to be used in the same transition when adding the accumulated error signal before it is stored in memory before the next transition.

Once the $\beta$-injection MOSFET $i_{gs}$ signal is calculated, the $\beta$-injection-MOSFET $i_{gs}$ command is then determined. Before the high or low transition becoming active, before the midpoint is reached, and the $v_{gs}$ is greater than 0 V, the $i_{gs}$ command is the proportional control to increases the $\beta$-injection MOSFET $v_{gs}$ towards the target $v_{gs}$. Once the rising or falling transition is active, the $i_{gs}$ command is controlled, which

includes the summation of the error signals. Beyond the controlled region of the $\beta$-injection MOSFET, the injection current is set to 0 A. Once the conditions of the $\beta$-injection MOSFET $i_{gs}$ command signal is determined, the MOSFET output commands are determined. The output commands are determined for both the top and bottom MOSFET, governed by a rising or falling transition.

An example of the $\beta$-injection MOSFET $i_{gs}$ commands is presented in Figure 5.14. The plot demonstrates the four $i_{gs}$ commands required throughout a shaped switching transition. From $t_0$ to $t_1$ the injection MOSFET is off and not required. From $t_1$ to $t_2$ the MOSFET is quickly increased. Form $t_2$ to $t_3$ proportional control is implemented to reach the target $v_{gs}$. Form $t_3$ to $t_4$ control is required during a rising or falling transition. Lastly from $t_4$ onwards the $\beta$-injection MOSFET is turned off.

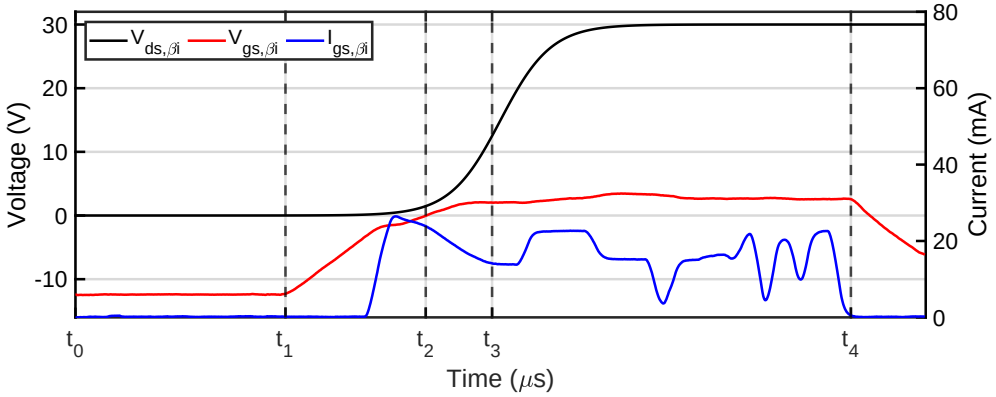



Figure 5.14: Example of the $\beta$-injection MOSFET $i_{gs}$ commands.

### 5.4.5 Auxiliary Control and Hard Switching Implementation

The second FPGA contains all the logic and control for the auxiliary branch and the hard switching implementation. Like the set-up of the first FPGA, the second FPGA is programmed to initialise the control, which includes clock signal generation, global timing, the logic for enabling the hard-switching mode, establishing data inputs for the load current, the $v_{ds}$ of each auxiliary MOSFET, the $v_{gs}$ of the auxiliary MOSFETs, and the auxiliary branch current measurement. As with the first FPGA, the logic for establishing the clock signals and global timing is the same as Section 5.4.2. The load signal for the second FPGA determines whether the hard-switching is required or not, which is toggled with each push-button press.

Parallel data inputs from the ADC on the control and monitoring board, include interfacing logic to provide the load current, the power MOSFET $v_{gs}$, power MOSFET $v_{ds}$, and the auxiliary branch current measurement data in offset binary format. The data format for all the data inputs is in offset binary, which is converted into 2c and negative 2c for ease of computation. Additionally, the auxiliary on command and switch command is received from the other FPGA. After the auxiliary and hard-switching branches of the FPGA is initialised, the control logic is implemented. If hard-switching mode is enabled, control of the top and bottom power MOSFETs are enabled. If hard-switching is disabled, the control of the top and bottom auxiliary MOSFETs is enabled.

Once the conditions for hard-switching are determined, the top and bottom MOSFET output commands are determined. The top MOSFET $v_{gs}$ is driven down to -15 V and is off when the switching command is low, and the hard-switching is active, or hard switching is not active. The top MOSFET $v_{gs}$ is driven up to 15 V and is on when both the switching command and hard switching mode is active. The bottom MOSFET $v_{gs}$ is driven down to -15 V and is off when both the switch command and hard switching mode are active or when the hard switching mode is not active. The bottom MOSFET $v_{gs}$ is driven up to 15 V and is on when the switch command is low, and the hard switching mode is active.

Once the conditions for the auxiliary branch control are determined, the auxiliary MOSFET output commands are determined. The top auxiliary MOSFET $v_{gs}$ is driven up to 15 V to turn on the MOSFET when the auxiliary command is active, the switch command is active, and the hard switching command is disabled. If either of these conditions is not met, the top auxiliary MOSFET $v_{gs}$ is driven down to -15 V and is turned off. The bottom auxiliary MOSFET $v_{gs}$ is driven up to 15 V to turn on the MOSFET when the auxiliary command is active, the switch command is low, and the hard switching command is disabled. If either of these conditions is not met, the bottom auxiliary MOSFET $v_{gs}$ is driven down to -15 V and is turned off. An overview of the auxiliary branch control and hard-switching control is presented in Figure 5.15.

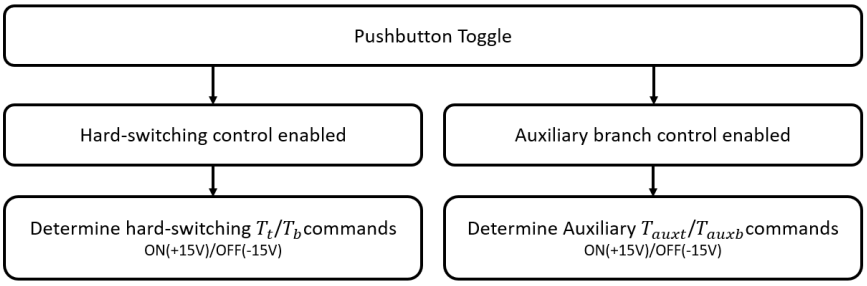



Figure 5.15: Auxiliary branch control and hard-switching control overview.

## 5.5 Laboratory Assessment and Performance Verification

### 5.5.1 Measurement Set-up and Methodology

Experimental tests were performed on the low-EMI half-bridge prototype to verify the performance of the prototype. The circuit was operated under no-load and constant load conditions, with the S-shaped, sinusoidal-shaped, and logistic-shaped reference waveforms being implemented in the FPGA. Additionally, the prototype was configured to operate under hard-switching conditions to provide a baseline for comparison. The load connected to the circuit for experimental evaluation of the half-bridge prototype was a resistive-inductive load. For both the top and bottom power MOSFET, measurements were performed to capture the rising and falling transitions, showing how the MOSFET is responding when acting as both the $\alpha$-MOSFET and $\beta$-MOSFET, respectively. All measurements of the bottom power MOSFET undergoing a controlled shaped switching transitions is presented in this Section. All measurements of the top power MOSFET undergoing a controlled shaped switching transitions is presented in Appendix A.

All measurements were performed using the MSO7054A 500 MHz, four analogue channel Mixed Signal Oscilloscope. The selected probes were Agilent 10073D 10:1, 500MHz, passive probes. For each shaped switching transition synthesised, measurements were performed on each power and injection MOSFET during a rising and falling transition of the half-bridge operating under no-load and load conditions. Additionally, measurements were taken for each MOSFET during turn-on and turn-off under no-load and load conditions for the prototype operating with hard switching. For each transition synthesised, the key metrics to verify the control and operation of the circuit were measured. For every transition, the key time-domain metrics that were measured include the following:

- $\alpha$-MOSFET: $v_{ds}$, $v_{gs}$, $i_{gs}$ command

- $\beta$-injection MOSFET: $v_{gs}$, $i_{gs}$ command, $i_{ds}$
- $\beta$-MOSFET: $v_{ds}$, $v_{gs}$
- Auxiliary branch: Auxiliary MOSFET commands, $v_{ds}$, $i_{aux}$

Since the research project is also concerned with the EMI performance of the prototype, the frequency-domain of the $v_{ds}$ shaped waveforms were analysed. The prototype laboratory measurement set-up is presented in Figure 5.16.

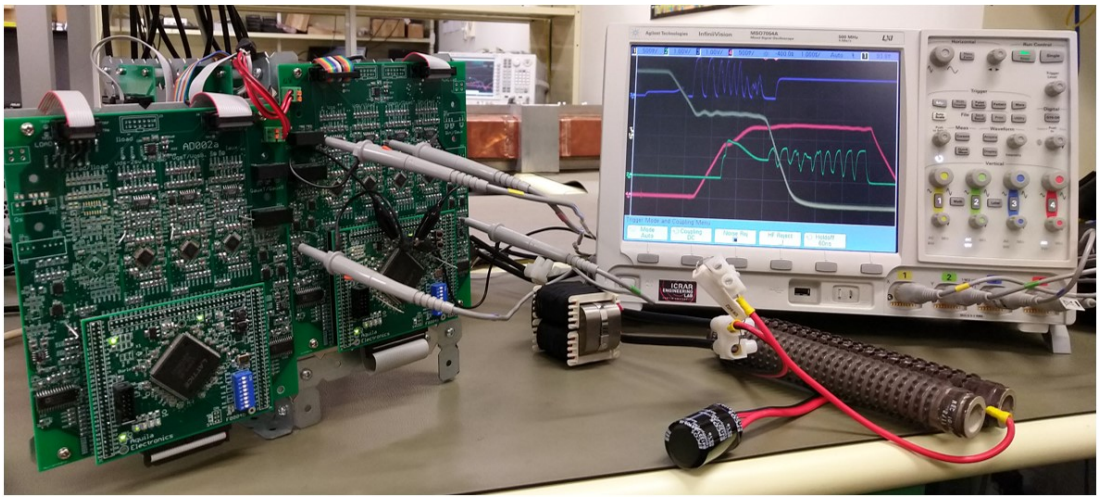


Figure 5.16: Laboratory measurement set-up.

### 5.5.2 Laboratory Measurements

#### 5.5.2.1 Logistic-Shaped Transition - No Load

Figure 5.17 presents the laboratory measurements of a rising transition when the bottom power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile with the half-bridge circuit operating under no load. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. Firstly, the plot shows that the $\alpha$-MOSFET $v_{ds}$ accurately follows the reference logistic-shaped waveform. Concurrently, the $\beta$-MOSFET $v_{ds}$ also produces a logistic shaped switching transition since it acts complimentary to the $\alpha$-MOSFET. Lastly, the $v_{gs}$ waveforms of the $\alpha$-MOSFET, $\beta$-injection MOSFET, and $\beta$-MOSFET are presented, which indicates the control sequence of the low-EMI half-bridge. Initially, the $\alpha$-MOSFET is controlled up to $0.5V_i$ to provide the shaping of the $\alpha$-MOSFET $v_{ds}$, which occurs at 5 $\mu$s. Above $0.5V_i$ the $\alpha$-MOSFET $v_{gs}$ is controlled towards -15 $V$ and is completely off.

Considering the $\beta$-injection MOSFET, the MOSFET $v_{gs}$ is ramped from -15 V to a voltage set-point just below $V_{th}$. This is required to ensure there is sufficient charge in the MOSFET to reduce the transient response time when the MOSFET is expected to start conducting to allow injection current to flow into the circuit to shape the $\alpha$-MOSFET $v_{ds}$. From $0.5V_i$ at 5 $\mu$s to ~9.2 $\mu$s, the $\beta$-injection MOSFET gate-drive is controlled to inject the required amount of current. Note that the injection control lasts longer than the simulations since the injection is also implemented to reduce the current ripple during the rising transition. Lastly, at ~9.2 $\mu$s, the $\beta$-injection MOSFET $v_{gs}$ is ramped downwards to -15 V to turn off the current injection. At ~9.2 $\mu$s, the $\beta$-MOSFET $v_{gs}$ is slowly ramped from 0 V to 15 V over 1.5 $\mu$s, which turns on the MOSFET.

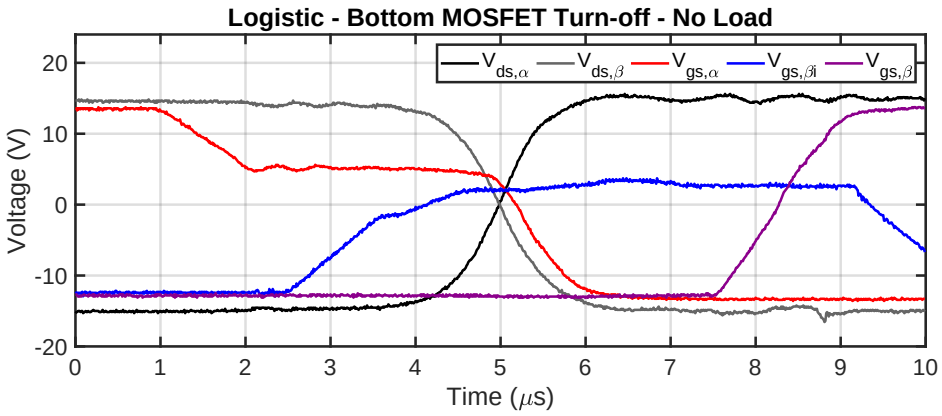



Figure 5.17: Turn-off sequence for a logistic-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under no load.

Figure 5.18 presents the laboratory measurements of the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The plot shows the current that is injected into the gate of the $\alpha$-MOSFET and $\beta$-injection MOSFET to get the desired $v_{gs}$ that is required to produce the logistic shaped transition.

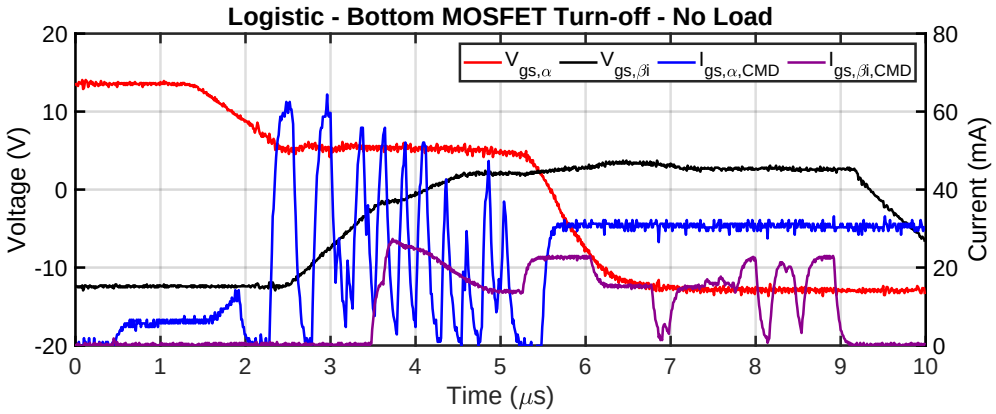



Figure 5.18: Turn-off sequence for a logistic-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under no load.

Figure 5.19 presents the laboratory of the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black). The plot shows the $\alpha$-MOSFET $v_{gs}$ and the $\beta$-injection MOSFET $i_{ds}$ that produces the desired logistic-shaped $\alpha$-MOSFET $v_{ds}$ rising transition.

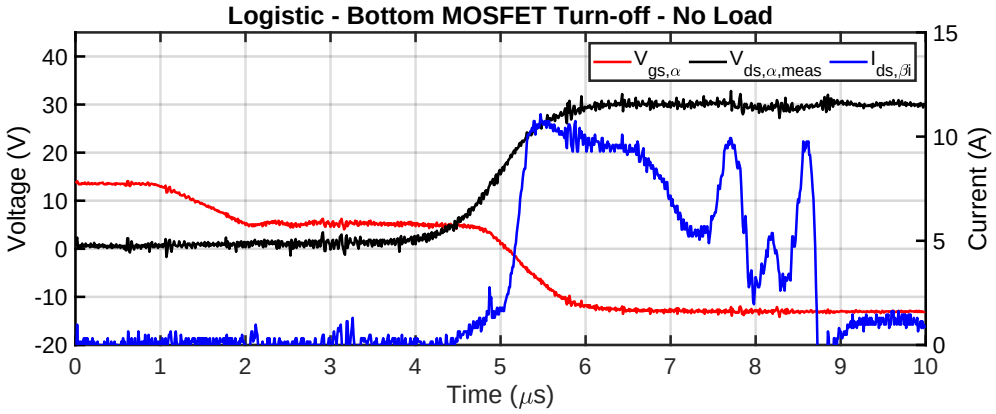



Figure 5.19: Turn-off sequence for a logistic-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under no load.

#### 5.5.2.2 Logistic-Shaped Transition - Load

This section presents the laboratory measurements of a rising transition when the bottom power MOSFET is the $\alpha$-MOSFET following a logistic-shaped reference profile with the half-bridge circuit operating under constant load. Figure 5.20 presents the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. Figure 5.21 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. Figure 5.22 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements.

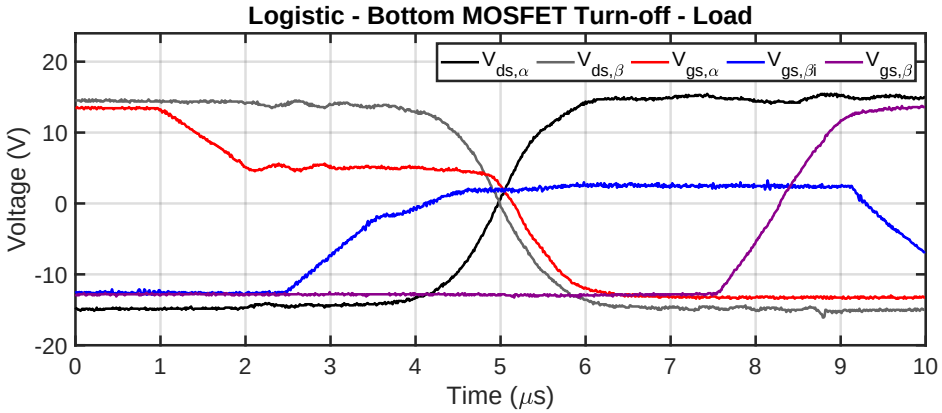



Figure 5.20: Turn-off sequence for a logistic-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under load.

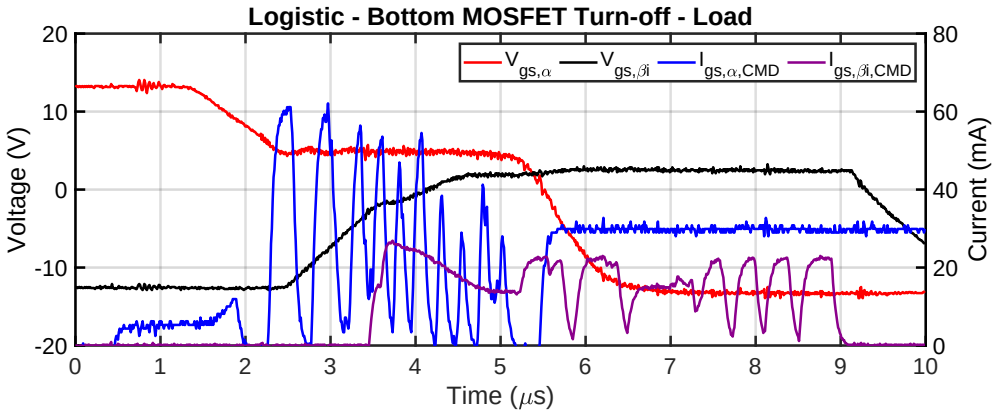



Figure 5.21: Turn-off sequence for a logistic-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under load.

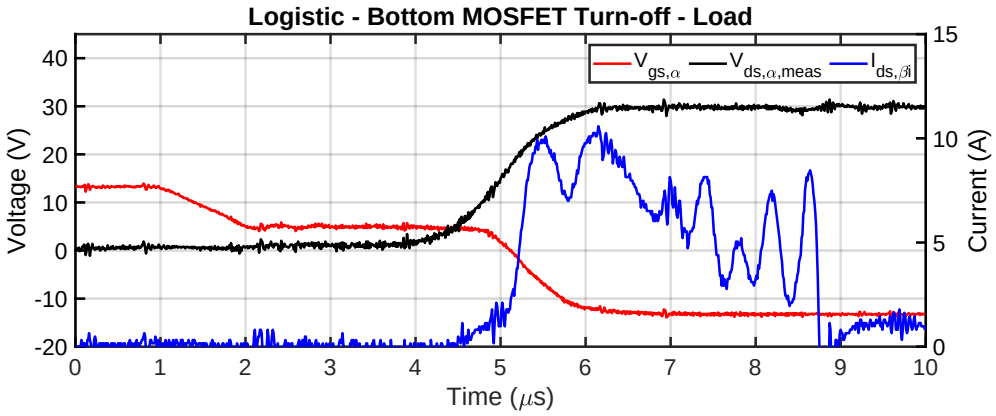



Figure 5.22: Turn-off sequence for a logistic-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under load.

#### 5.5.2.3 Sinusoidal-Shaped Transition - No Load

This section presents the laboratory measurements of a rising transition when the bottom power MOSFET is the $\alpha$-MOSFET following a sinusoidal-shaped reference profile with the half-bridge circuit operating under no load. Figure 5.23 presents the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection

MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. Figure 5.24 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. Figure 5.25 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements.

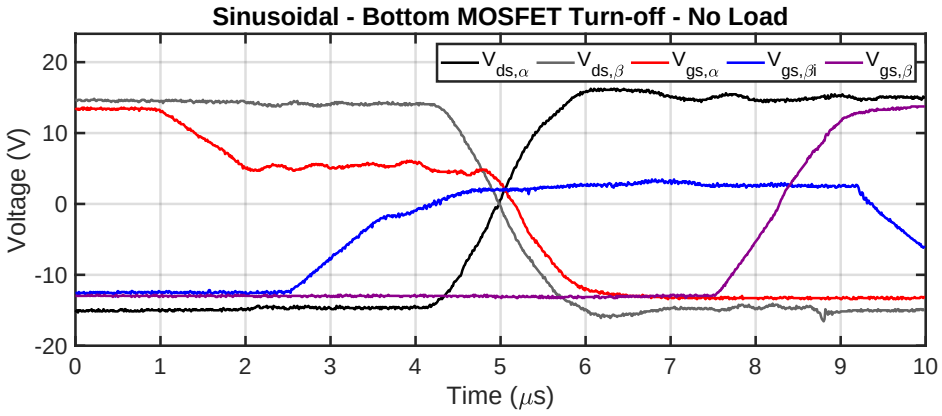



Figure 5.23: Turn-off sequence for a sinusoidal-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under no load.

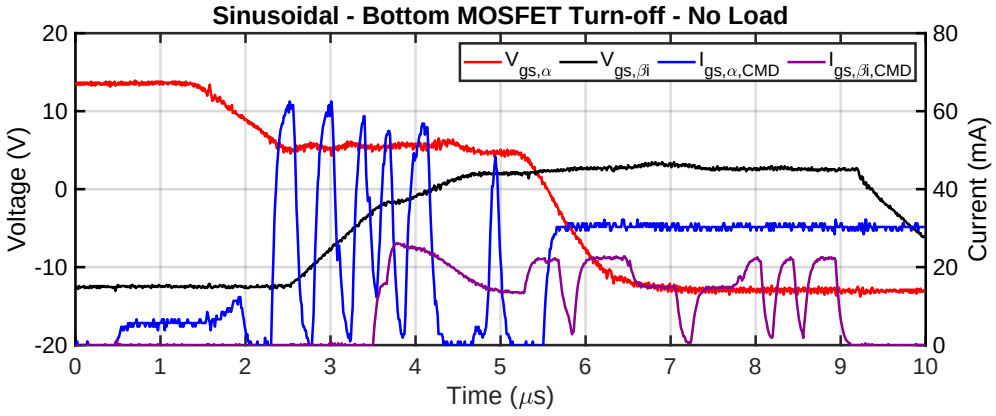



Figure 5.24: Turn-off sequence for a sinusoidal-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under no load.

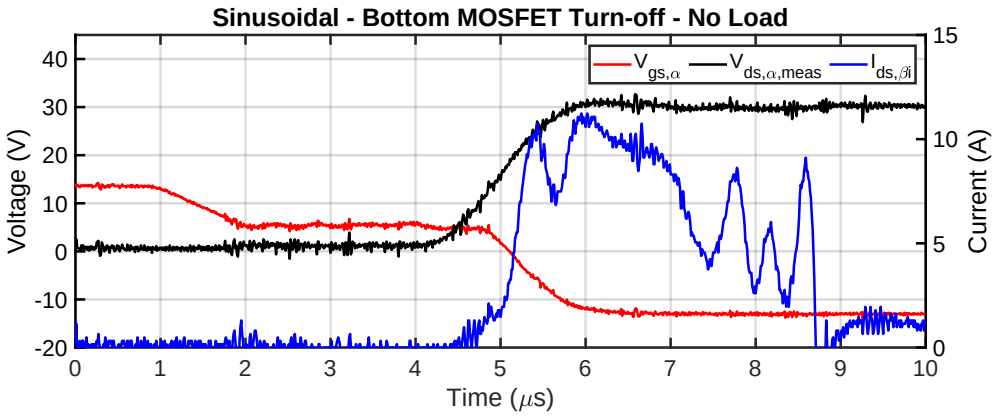



Figure 5.25: Turn-off sequence for a sinusoidal-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under no load.

#### 5.5.2.4 Sinusoidal-Shaped Transition - Load

This section presents the laboratory measurements of a rising transition when the bottom power MOSFET is the $\alpha$-MOSFET following a sinusoidal-shaped reference profile with the half-bridge circuit operating under constant load. Figure 5.26 presents the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. Figure 5.27 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. Figure 5.28 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements.

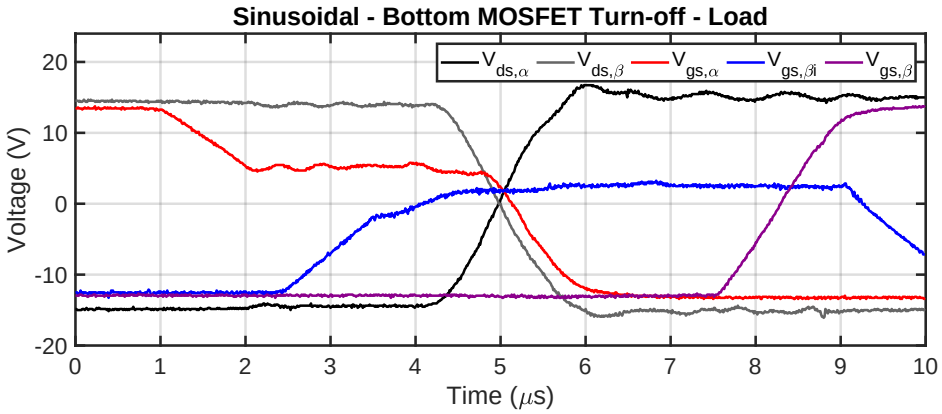



Figure 5.26: Turn-off sequence for a sinusoidal-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under load.

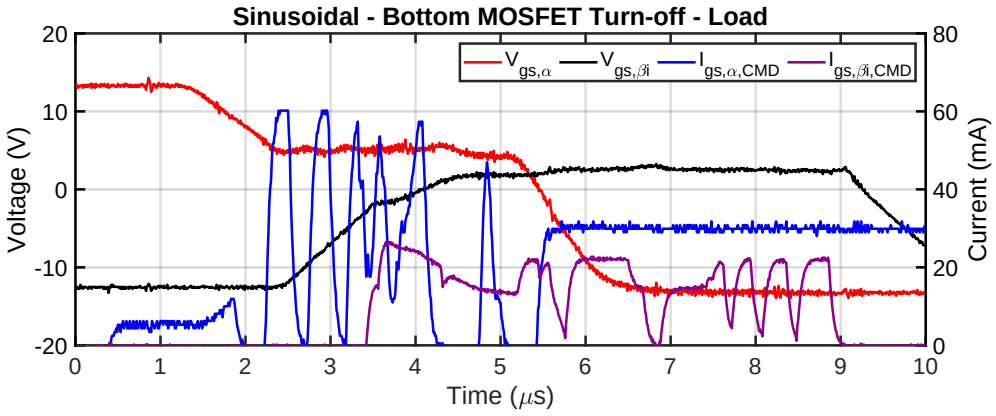



Figure 5.27: Turn-off sequence for a sinusoidal-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under load.

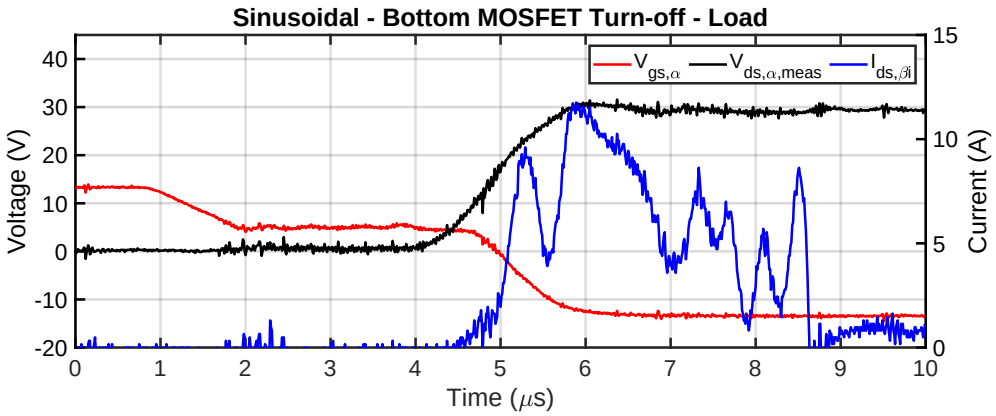



Figure 5.28: Turn-off sequence for a sinusoidal-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under load.

#### 5.5.2.5 S-Shaped Transition - No Load

This section presents the laboratory measurements of a rising transition when the bottom power MOSFET is the $\alpha$-MOSFET following a S-shaped reference profile with the half-bridge circuit operating under no load. Figure 5.29 presents the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. Figure 5.30 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. Figure 5.31 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements.

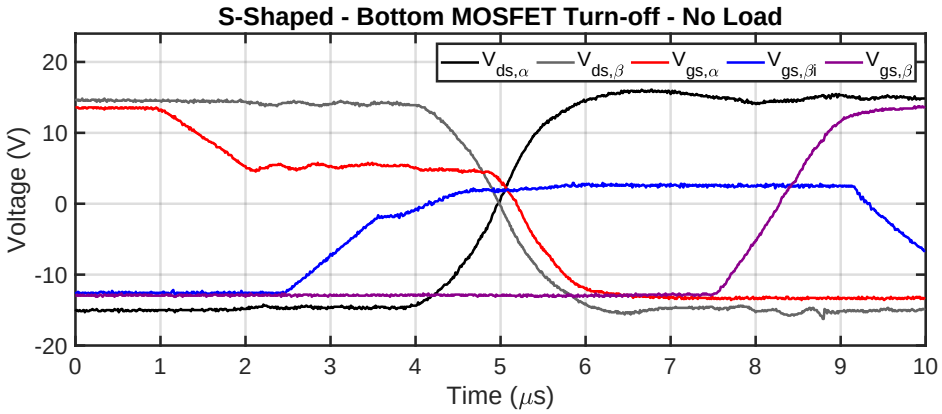



Figure 5.29: Turn-off sequence for a S-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under no load.

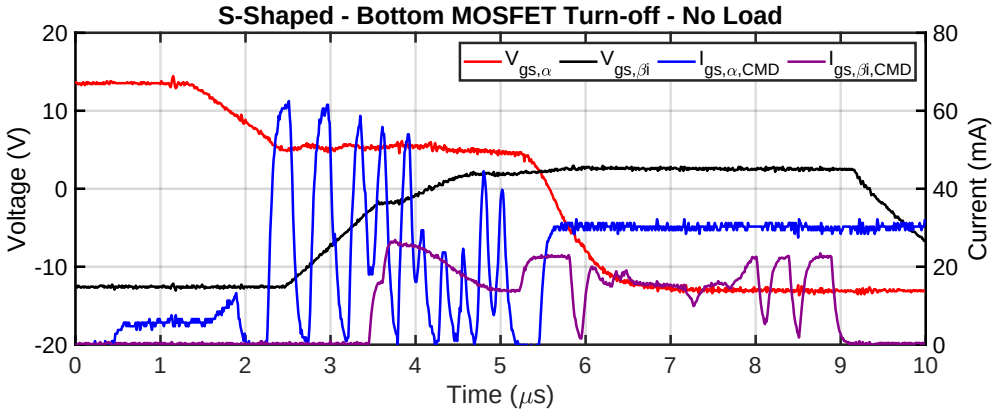



Figure 5.30: Turn-off sequence for a S-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under no load.

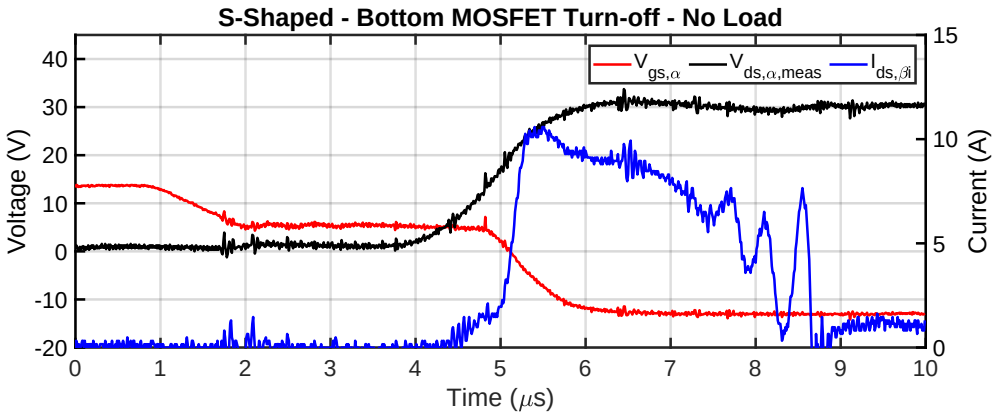



Figure 5.31: Turn-off sequence for a S-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under no load.

#### 5.5.2.6 S-Shaped Transition - Load

This section presents the laboratory measurements of a rising transition when the bottom power MOSFET is the $\alpha$-MOSFET following a S-shaped reference profile with the half-bridge circuit operating under constant load. Figure 5.32 presents the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. Figure 5.33 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. Figure 5.34 presents the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements.

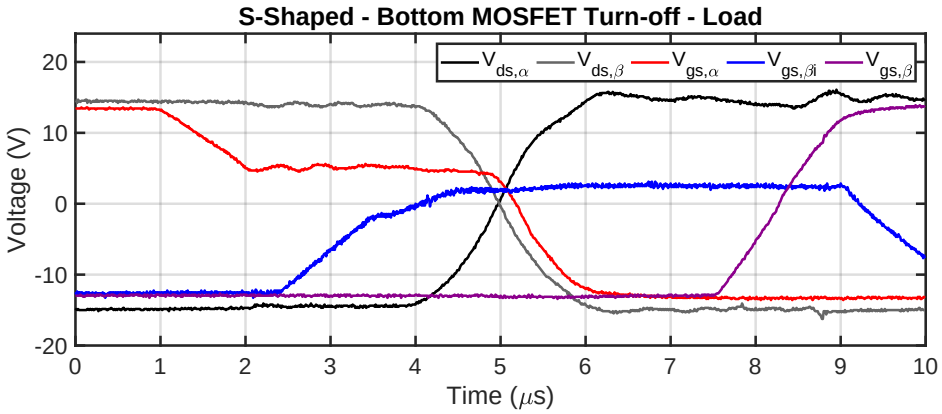



Figure 5.32: Turn-off sequence for a S-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under load.

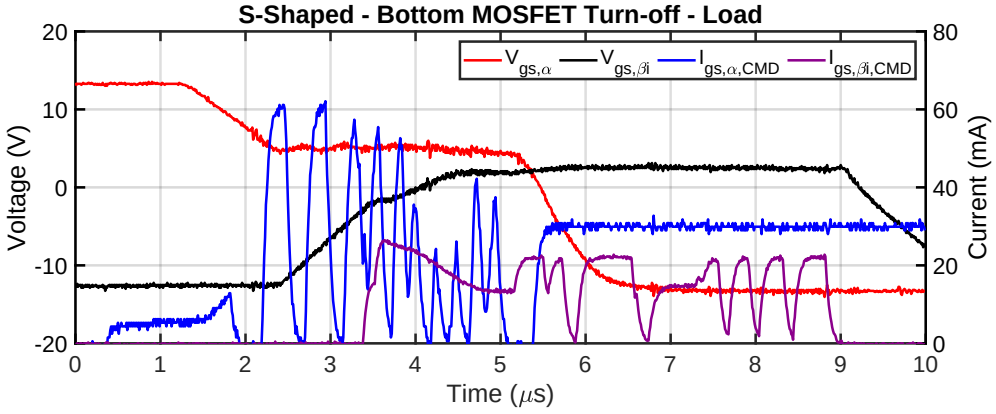



Figure 5.33: Turn-off sequence for a S-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under load.

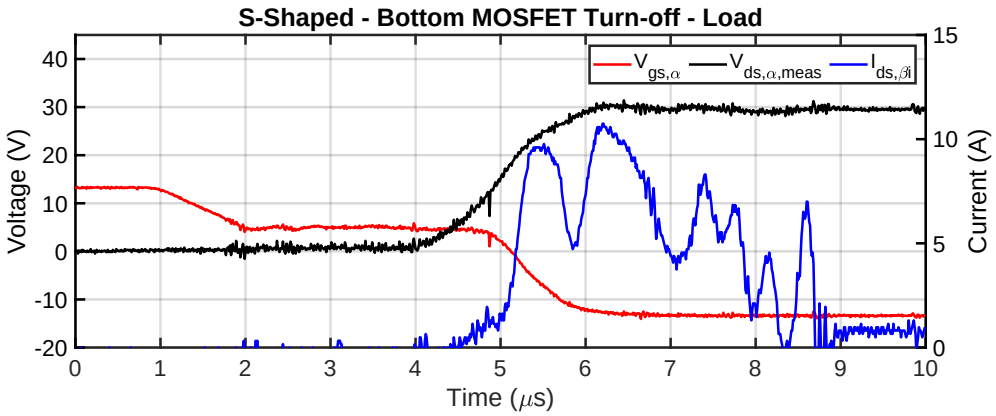



Figure 5.34: Turn-off sequence for a S-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under load.

#### 5.5.2.7 Auxiliary Branch Measurements

This section presents the auxiliary branch measurements during a shaped switching transition for the bottom and top power MOSFETs when the half-bridge circuit operates under no-load and constant load. The auxiliary branch operation when the top power MOSFET is $\alpha$-MOSFET for the half-bridge operating under no-load and constant load is presented in Figure 5.35 and Figure 5.36, respectively. The auxiliary branch operation when the bottom power MOSFET is $\alpha$-MOSFET for the half-bridge operating under no-load and constant load is presented in Figure 5.37 and Figure 5.38, respectively.

The no-load and load auxiliary branch measurements demonstrate the differences in timing and control of the auxiliary branch to satisfy the auxiliary branch operating condition of $I_{load} + i_{aux} = 10$ A. For the no-load conditions, the auxiliary branch is operated to ensure the auxiliary branch is ramped to 10 A when the switching transition voltage reaches $0.5V_i$. For the power converter operating under load, the auxiliary branch current is ramped to $|i_{aux}| = 10\ A - I_{load}$ for the top power MOSFET when the switching transition voltage reaches $0.5V_i$. Additionally the auxiliary branch current is ramped to $|i_{aux}| = 10\ A + I_{load}$ for the bottom power MOSFET.

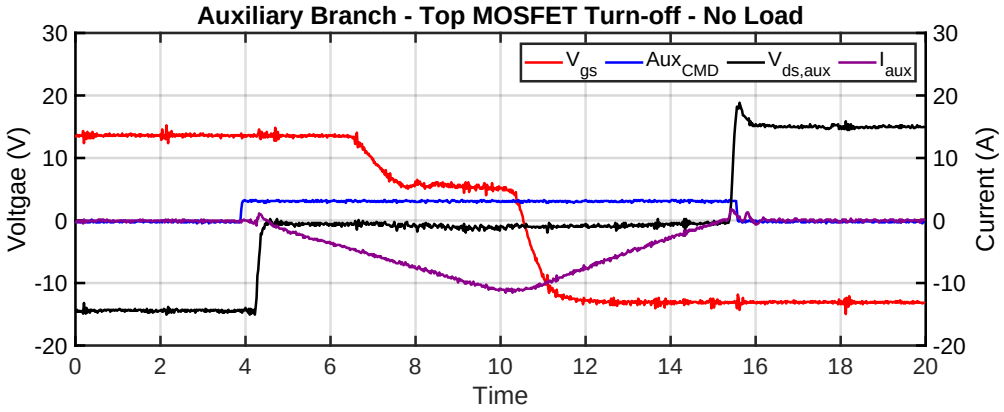



Figure 5.35: Auxiliary branch measurements of a turn-off sequence when the top MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), auxiliary-MOSFET command signal (blue), auxiliary-MOSFET $v_{ds}$ (black), and auxiliary branch current $i_{aux}$ (purple) measurements. The half-bridge circuit is operating under no load.

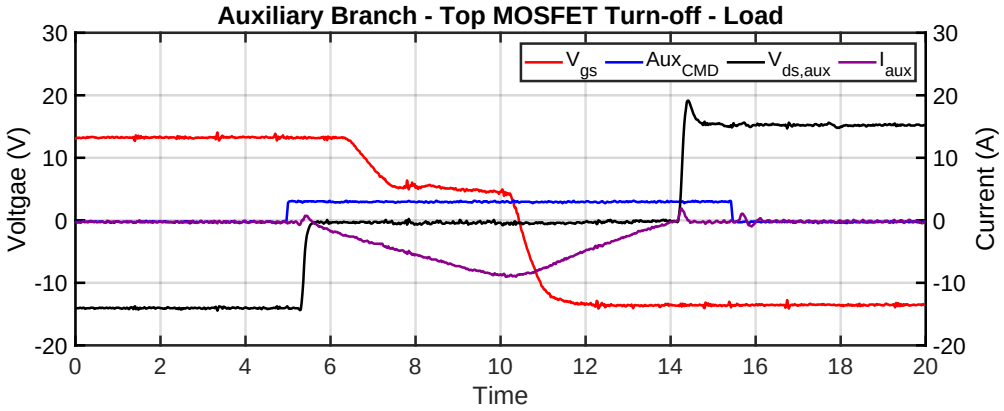



Figure 5.36: Auxiliary branch measurements of a turn-off sequence when the top MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), auxiliary-MOSFET command signal (blue), auxiliary-MOSFET $v_{ds}$ (black), and auxiliary branch current $i_{aux}$ (purple) measurements. The half-bridge circuit is operating under load.

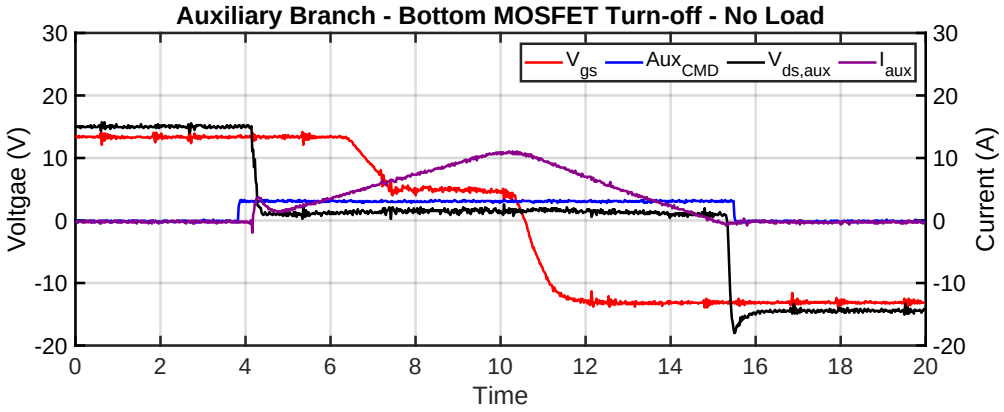



Figure 5.37: Auxiliary branch measurements of a turn-off sequence when the bottom MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), auxiliary-MOSFET command signal (blue), auxiliary-MOSFET $v_{ds}$ (black), and auxiliary branch current $i_{aux}$ (purple) measurements. The half-bridge circuit is operating under no load.

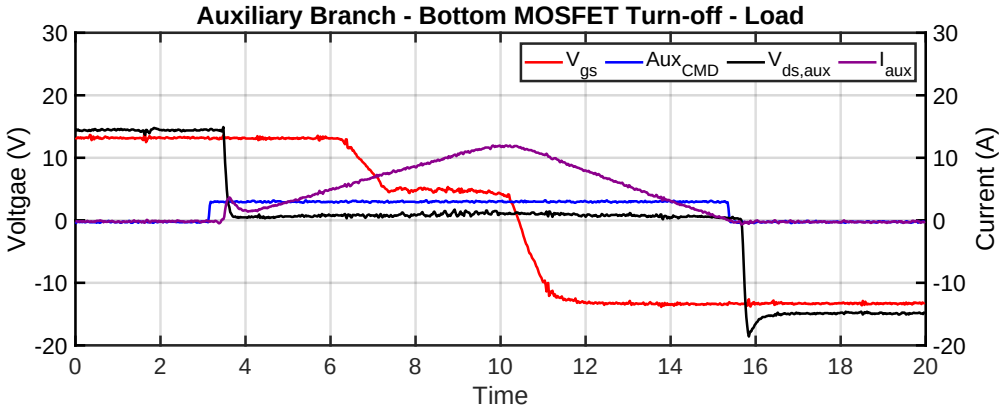



Figure 5.38: Auxiliary branch measurements of a turn-off sequence when the bottom MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), auxiliary-MOSFET command signal (blue), auxiliary-MOSFET $v_{ds}$ (black), and auxiliary branch current $i_{aux}$ (purple) measurements. The half-bridge circuit is operating under load

#### 5.5.2.8 Hard Switching

The hard switching measurements are presented for the bottom and top power MOSFETs when the half-bridge circuit operates under no-load and constant load. The hard switching measurements of the top power MOSFET operating under no-load and constant load is presented in Figure 5.39 and Figure 5.40, respectively. The hard switching measurements of the bottom power MOSFET operating under no-load and constant

load is presented in Figure 5.41 and Figure 5.42, respectively. Each plots presents the power MOSFET $v_{ds}$ (red) and $v_{gs}$ (blue).

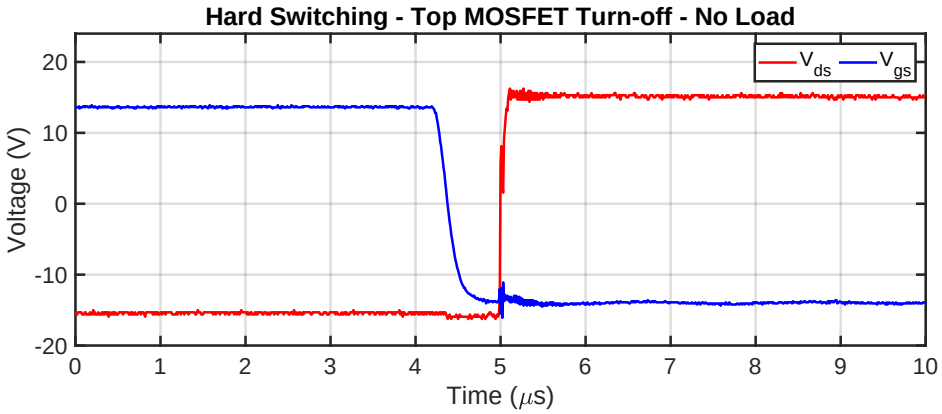



Figure 5.39: Hard switching waveforms of the top MOSFET $v_{ds}$ (red) and $v_{gs}$ (blue) during turn-off. The half-bridge circuit is operating under no load.

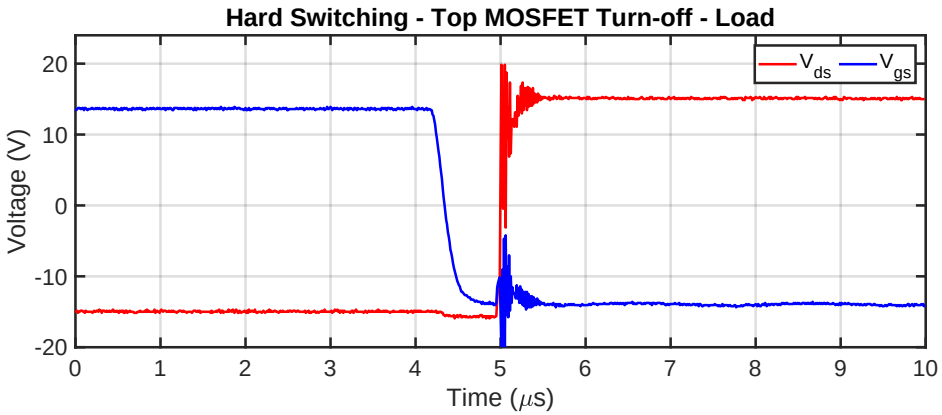



Figure 5.40: Hard switching waveforms of the top MOSFET $v_{ds}$ (red) and $v_{gs}$ (blue) during turn-off. The half-bridge circuit is operating under load.

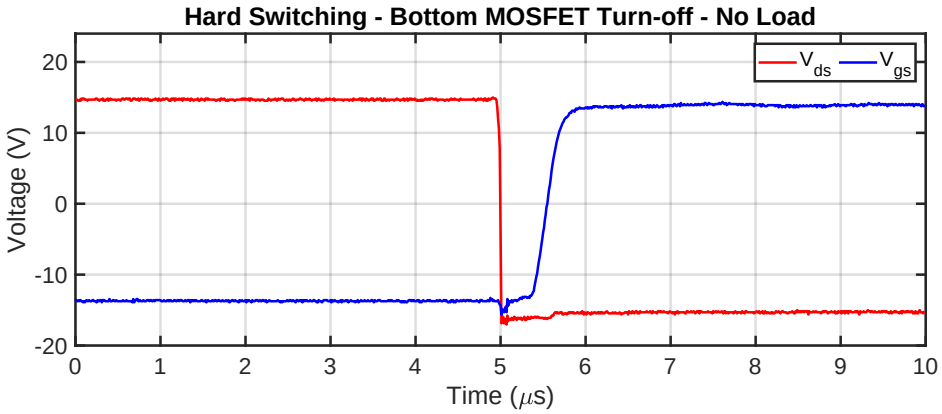



Figure 5.41: Hard switching waveforms of the bottom MOSFET $v_{ds}$ (red) and $v_{gs}$ (blue) during turn-off. The half-bridge circuit is operating under no load.

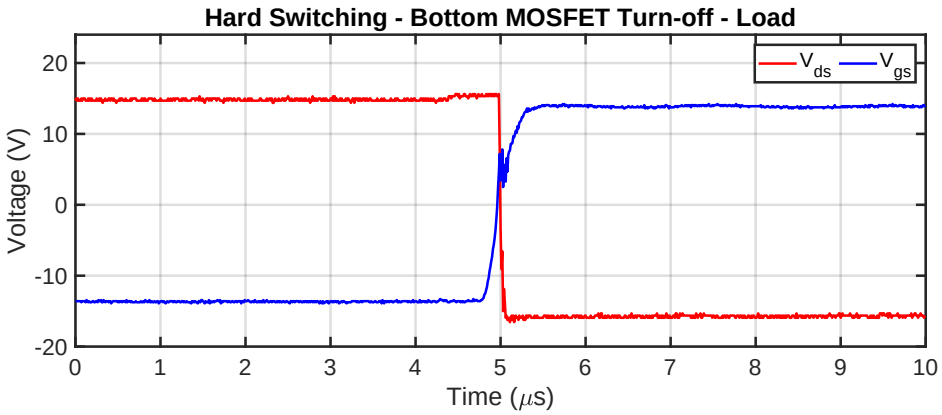



Figure 5.42: Hard switching waveforms of the bottom MOSFET $v_{ds}$ (red) and $v_{gs}$ (blue) during turn-off. The half-bridge circuit is operating under load.

### 5.5.3 Spectral Comparison

#### 5.5.3.1 Waveform Averaging

Since assessing the EMI performance of the prototype is required, the frequency-domain of the $v_{ds}$ shaped waveforms were analysed. One major challenge presented in the measurement approach is the low switching frequencies relative to the time-steps required to sample the waveform to achieve the highest frequency measurement required, which may be restricted by the resolution of the measuring device and accuracy of the measurement probes. Additionally, the switching waveform includes the low-frequency switching harmonics, which are orders of magnitude lower than the high-frequency content, which is being assessed. Finally, the high-frequency spectral content can get lost in the noise of the measurement equipment.

Since time-domain and frequency-domain measurements are required, an oscilloscope is used. Although characterising the steep-roll of shaped switching waveforms, the oscilloscope bandwidth is limited by the measurement signal to noise ratio created by the analogue to digital circuitry quantising the signal. Since MOSFET switching is periodic and random noise is present in the measurement, time-domain averaging is suitable for increasing the measurement bandwidth. The time-domain average of the logistic-shaped, sinusoidal-shaped, and S-shaped reference profile for a shaped switching transition is presented in this Section.

The logistic shaped switching transitions considering the bottom power MOSFET as the $\alpha$-MOSFET for the half-bridge operating under no-load and load conditions is presented in Figure 5.43 and Figure 5.44, respectively. The sinusoidal shaped switching transitions considering the bottom power MOSFET as the $\alpha$-MOSFET for the half-bridge operating under no-load and load conditions is presented in Figure 5.45 and Figure 5.46, respectively. The S-shaped switching transitions considering the bottom power MOSFET as the $\alpha$-MOSFET for the half-bridge operating under no-load and load conditions is presented in Figure 5.47 and Figure 5.48, respectively.

The plot of each shaped transition includes the $v_{ds}$ waveform of the $\alpha$- and $\beta$-MOSFET as shown by the red and blue traces, respectively. Additionally, the $v_{ds}$ reference profiles of the $\alpha$- and $\beta$-MOSFET is shown by the solid black and dashed black traces, respectively. Lastly, the hard-switching waveforms considering the bottom power MOSFET for the half-bridge operating under no-load and load conditions is presented in Figure 5.49 and Figure 5.50.

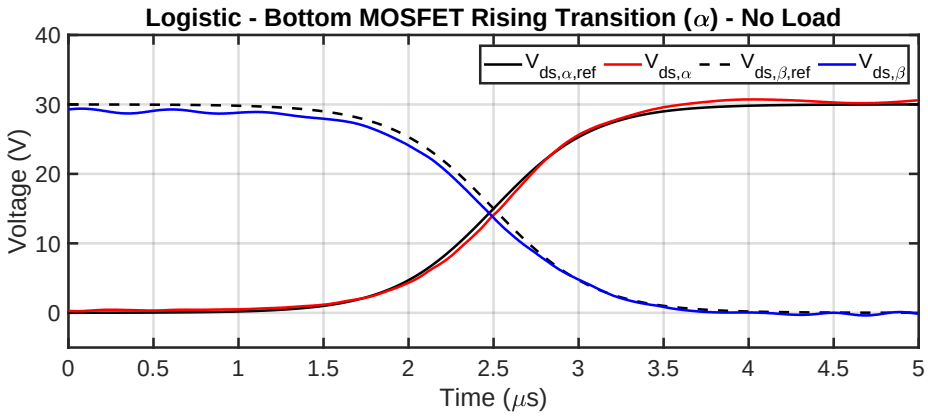



Figure 5.43: Waveform averaging for a logistic-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines, respectively. The half-bridge circuit is operating under no load.

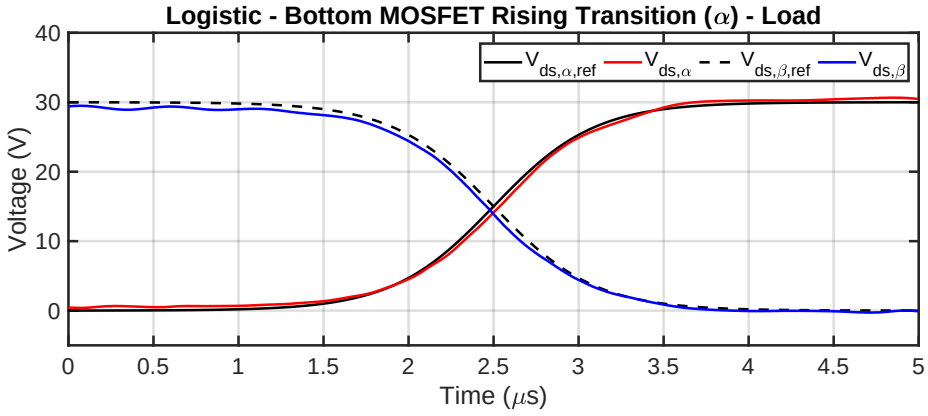



Figure 5.44: Waveform averaging for a logistic-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines, respectively. The half-bridge circuit is operating load.

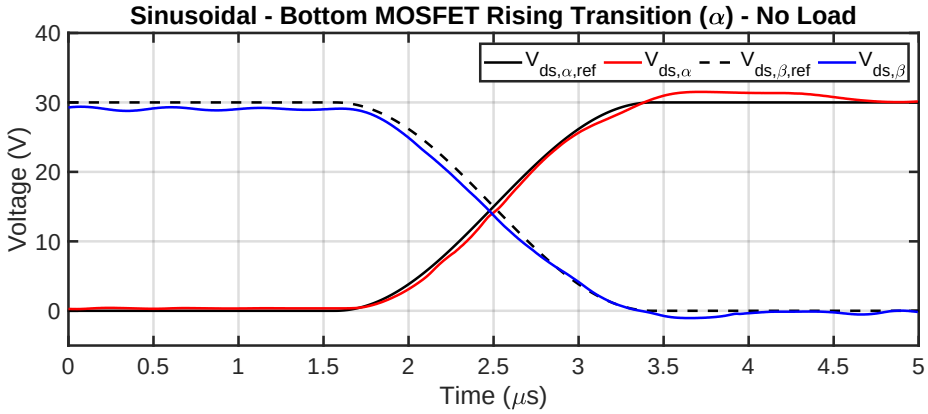



Figure 5.45: Waveform averaging for a sinusoidal-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines, respectively. The half-bridge circuit is operating under no load.

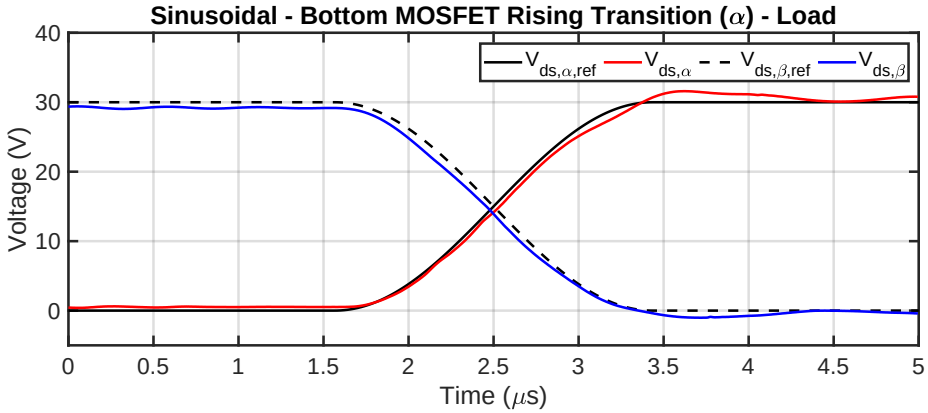



Figure 5.46: Waveform averaging for a sinusoidal-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines, respectively. The half-bridge circuit is operating load.

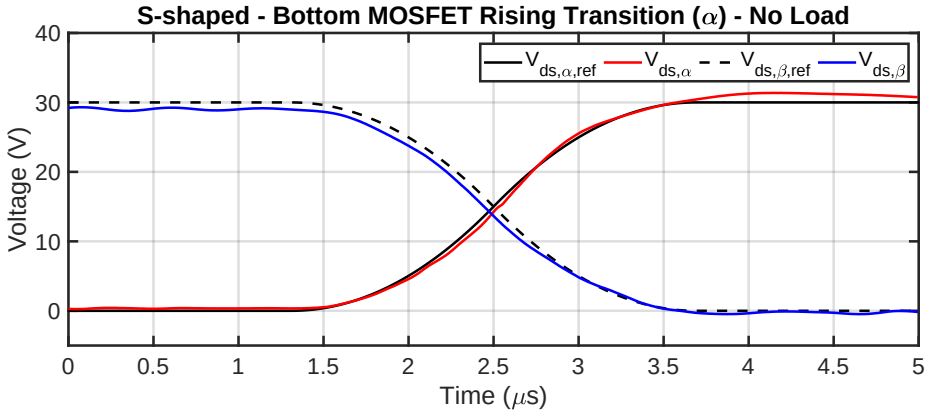



Figure 5.47: Waveform averaging for a S-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines, respectively. The half-bridge circuit is operating under no load.

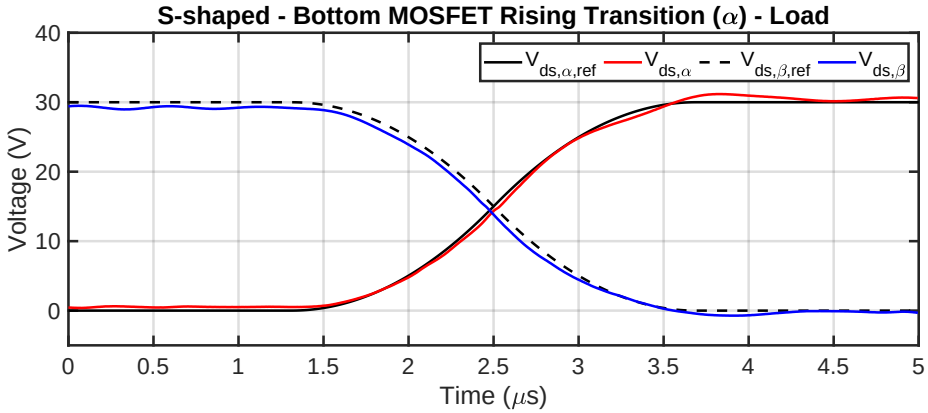



Figure 5.48: Waveform averaging for a S-shaped reference waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines, respectively. The half-bridge circuit is operating load.

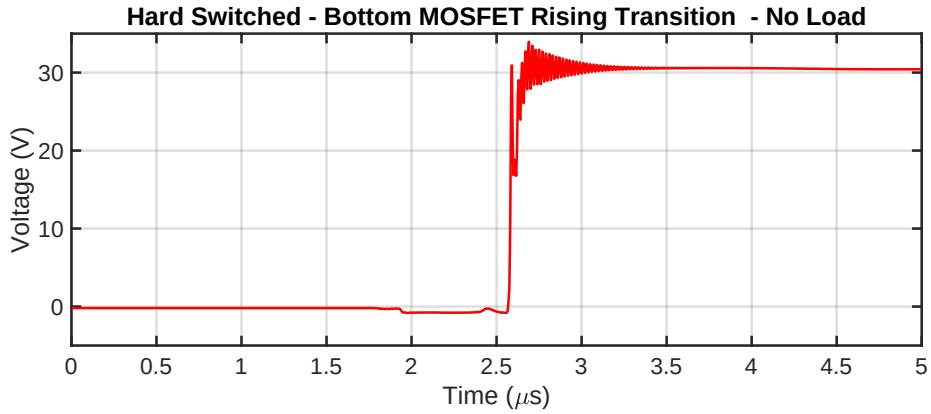



Figure 5.49: Waveform averaging for a hard switching waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The half-bridge circuit is operating under no load.

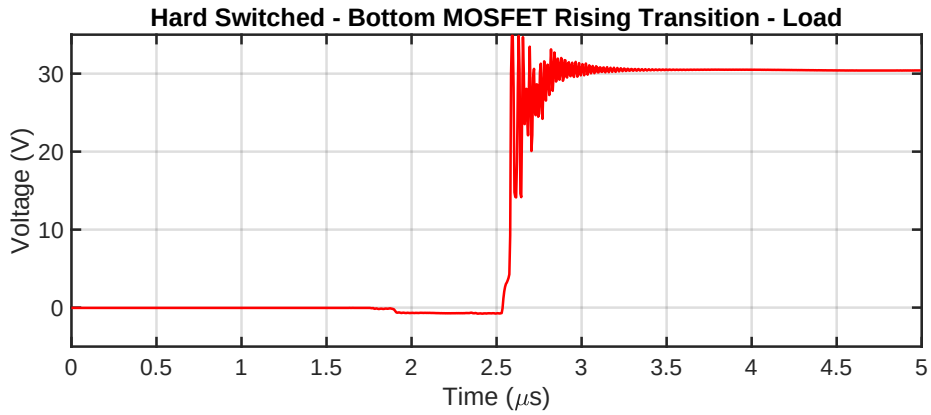



Figure 5.50: Waveform averaging for a hard switching waveform when the bottom power MOSFET is the $\alpha$-MOSFET. The half-bridge circuit is operating under load.

#### 5.5.3.2 Harmonic Spectra

Lastly, a harmonic spectral comparison is presented between the hard-switching, logistic, sinusoidal, and S-shaped switching transitions. Figure 5.51 presents the harmonic spectra and spectral bound (envelope) of a hard-switching (black), logistic-shaped (purple), sinusoidal-shaped (red) and S-shaped (blue) switching transition when the half-bridge circuit is operating under no-load. The PWM waveforms are synthesised by combining the time-averaged rising and falling transitions considering a 1 kHz switching frequency. Figure 5.52 presents the spectral comparison from 1 MHz to 10 MHz to compare better the performance between the logistic-shaped, sinusoidal-shaped, and S-shaped switching transitions.

Similarly, Figure 5.53 presents the harmonic spectral comparison of a hard-switching (black), logistic-shaped (purple), sinusoidal-shaped (red) and S-shaped (blue) switching transition when the half-bridge circuit is operating under constant load. The spectral comparison from 1 MHz to 10 MHz is shown in Figure 5.54. Although the spectral comparison of the logistic-shaped waveform does not demonstrate the steep harmonic roll-off of the ideal logistic-shaped transition, the harmonic content of the shaped transitions is considerably less than the hard-switching waveform.

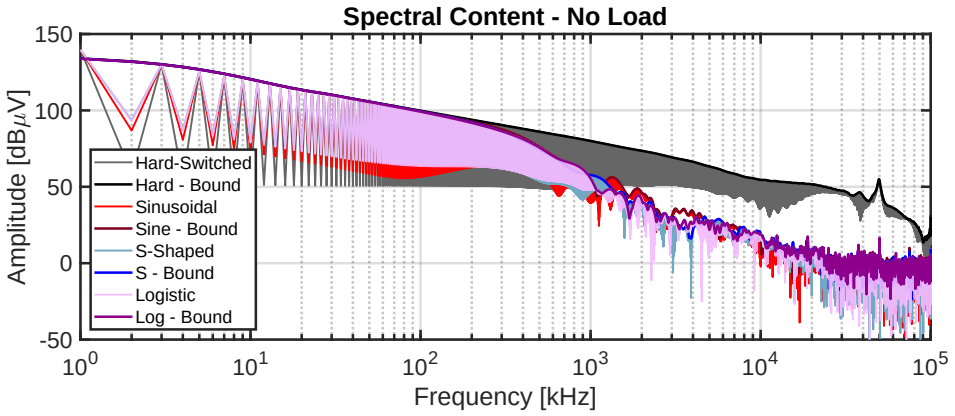



Figure 5.51: Harmonic spectral comparison of the hard-switching (black), sinusoidal-shaped (red), S-shaped (blue) and logistic-shaped (purple) when the half-bridge circuit is operating under no load. All harmonic spectra plotted include the spectral bound (envelope) for comparison. The spectra is plotted from 1 kHz (fundamental frequency) to 100 MHz.

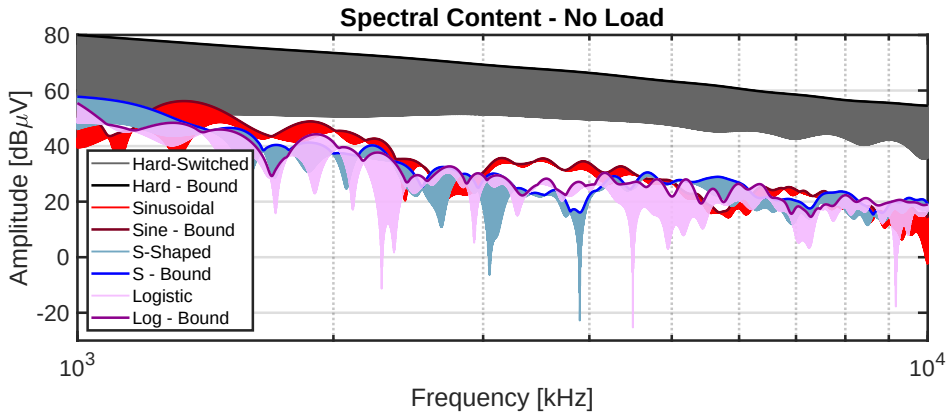



Figure 5.52: Harmonic spectral comparison of the hard-switching (black), sinusoidal-shaped (red), S-shaped (blue) and logistic-shaped (purple) when the half-bridge circuit is operating under no load. All harmonic spectra plotted include the spectral bound (envelope) for comparison. The spectra is plotted from 1 MHz to 10 MHz to better compare the harmonic content within that frequency range.

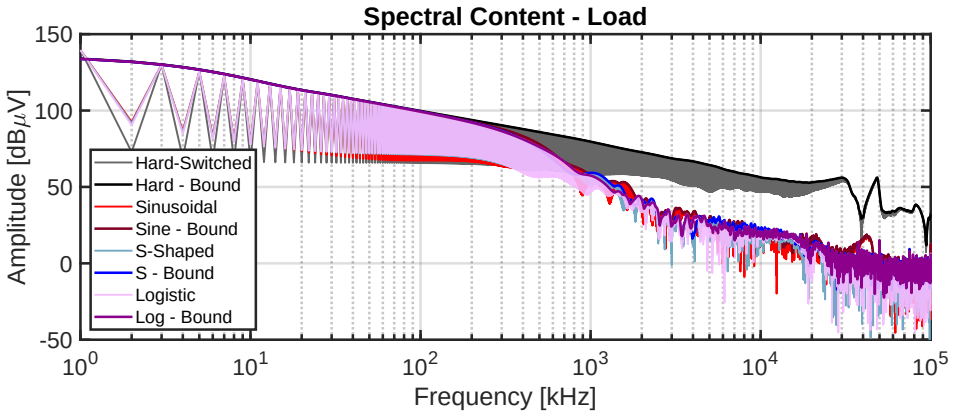



Figure 5.53: Harmonic spectral comparison of the hard-switching (black), sinusoidal-shaped (red), S-shaped (blue) and logistic-shaped (purple) when the half-bridge circuit is operating under load. All harmonic spectra plotted include the spectral bound (envelope) for comparison. The spectra is plotted from 1 kHz (fundamental frequency) to 100 MHz.

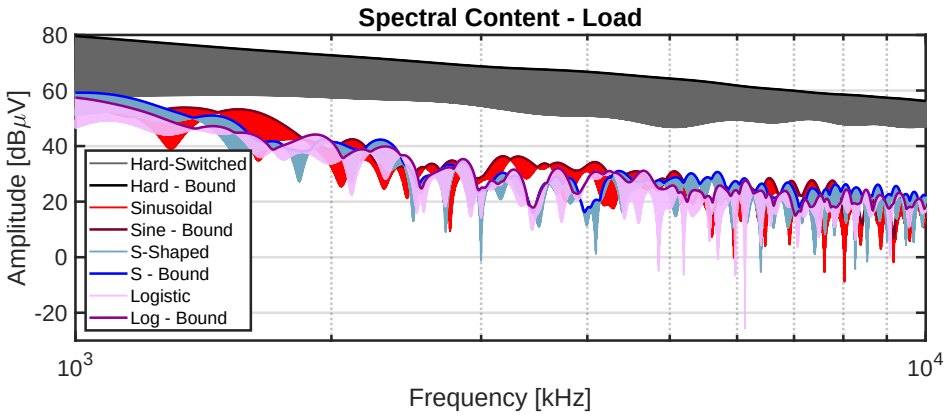



Figure 5.54: Harmonic spectral comparison of the hard-switching (black), sinusoidal-shaped (red), S-shaped (blue) and logistic-shaped (purple) when the half-bridge circuit is operating under load. All harmonic spectra plotted include the spectral bound (envelope) for comparison. The spectra is plotted from 1 MHz to 10 MHz to better compare the harmonic content within that frequency range.

## 5.6 Radiated Emissions Prediction

This section presents a theoretical prediction of the expected radiated emissions levels and the attenuation of logistic-shaped switching transitions by analysing ideal shaped transitions and the prototype half-bridge spectral results. Additionally, the estimated emission levels are compared to the SKA RFI/EMC emission limits to identify the reduction in shielding and filtering requirements by implementing the logistic-shaped switching transition presented in this dissertation. Firstly, a theoretical prediction is presented, considering the ideal waveforms presented in Chapter 3. The analysis presents an expectation of what can be theoretically achieved by a power converter capable of undergoing ideal logistic shaped switching transitions.

Additionally, this section concludes with a presentation of attenuation estimates using the prototype half-bridge waveforms presented in Section 5.5.3.2 of this Chapter. The analysis of the prototype operating under no-load and constant load conditions quantifies what is currently achievable with the developed technology. The theoretical prediction presented in this section estimates the expected radiated emissions generated by a power converter capable of undergoing logistic-shaped transitions, contrasted to hard-switching PWM. The attenuation requirements of logistic-shaped transitions and hard-switching PWM required to satisfy the SKA RFI/EMC emission limits is presented. The reduction in emissions attenuation will have advantageous cost implications considering the stringency of the SKA RFI/EMC Standard [1].

Typically, the outcomes presented in the literature demonstrate EMI mitigation compared to a worst-case scenario for switching noise such as hard-switching. Therefore, mitigation strategies, whether applied to the power circuitry or control strategy, will seek to demonstrate compliance with CISPR22 Class A or Class B limits and compare emissions to the hard switching case. Since the SKA-low emission limits are approximately 100 dB less than MIL-STD-461F RE102 and 120 dB for CISPR22 Class B, compliance is expected to be achieved with multiple levels of shielding and filtering with a device that is CISPR22 compliant.

An overview of the CISPR22 Class B emission limits compared to the SKA-Low emission limit is presented in Figure 5.55, which adopts the methodology presented SKA-Low EMC requirements [1] and summarised in Section 1.6.3. CISPR22 Class B compliant power converters are preferred over CISPR22 Class A power supplies for the SKA-low since they generate lower radiated emissions. Additionally, CISPR22 Class B power supplies are cost-effective compared to MIL-STD-461F compliant COTS or modified-COTS power supplies. A mitigation strategy combining novel and conventional mitigation techniques must be adopted to comply with the SKA-low EMC standard, which seeks to achieve the greatest attenuation beyond 30 MHz.

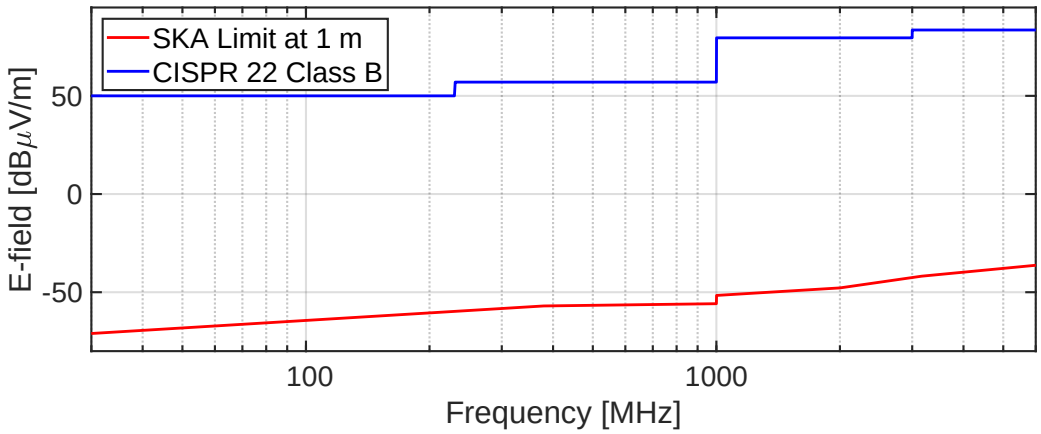



Figure 5.55: SKA-Low EMC emissions limit considering a 1 m distance to the nearest antenna. The CISPR22 Class B limit value is included for comparison, establishing a worst-case scenario for an emission culprit.

A computational study was performed to outline the expected attenuation from ideal logistic-shaped switching transitions and from laboratory measurements. Considering the SKA-low EMC standard, this modelling identifies the reduction in attenuation requirements from shielding and filtering techniques compared to hard-switching PWM.

The following assumptions are made to estimate the attenuation requirements against the SKA-low EMC standards:

1. It is assumed that a power converter generates radiated emissions at the CISPR-B limit line to establish a worst-case scenario. Therefore, only emissions up to 500 MHz are considered for this study, including the SKA-low frequency range.

2. A conservative assumption is made, where the switching waveform of a hard-switching power converter is a slowed trapezoidal waveform which is inherently low noise compared to a hard-switching square wave.

3. This computational study only considers the emissions generated by switching noise since this was the focus of the research presented in this thesis.

4. Radiated emissions generated by the digital control circuitry, and PCB layout are not considered.

5. A switching frequency of 10 kHz is considered to better represent the switching frequencies of power converters. Note that a 1 kHz switching frequency was implemented for the prototype to allow for increased transition times required to demonstrate the feasibility of shaped transitions during prototype development.

The difference in dB between the trapezoidal waveform and logistic-shaped waveform provides an estimate for the theoretical attenuation that can be achieved from an ideal logistic-shaped switching transition. The radiated emissions estimated for a logistic shaped transition is presented in Figure 5.56, which is compared to a power converter generating radiated emissions at the CISPR-B limit line. The emissions estimate of the logistic shaped switching transitions is calculated by subtracting the difference in dB between the spectral bound of a trapezoidal waveform and a logistic shaped waveform, as shown in Figure 3.16, from the CISPR 22 Class B limit line. Figure 5.56 shows that the attenuation achieved by a logistic-shaped switching transition (black trace) exceeds 200 dB when comparing the harmonic spectra with a slow-transitioning trapezoidal waveform (red trace). The SKA-low limit is shown in blue.

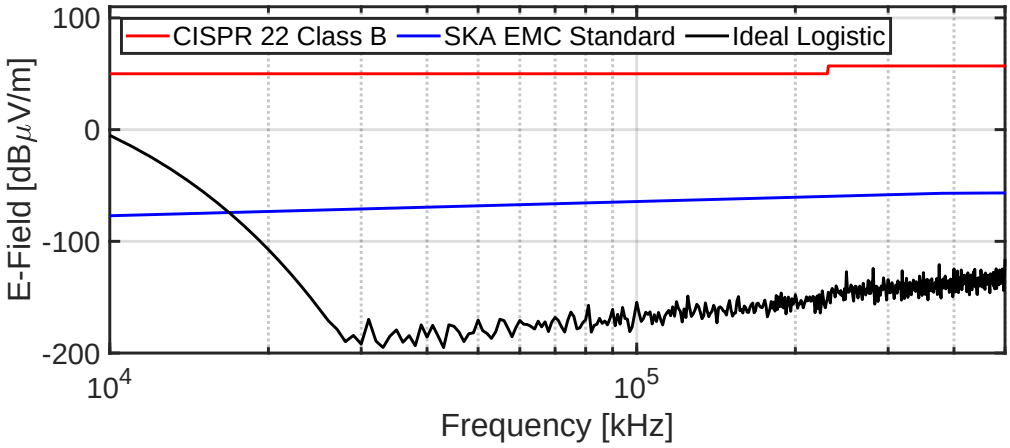
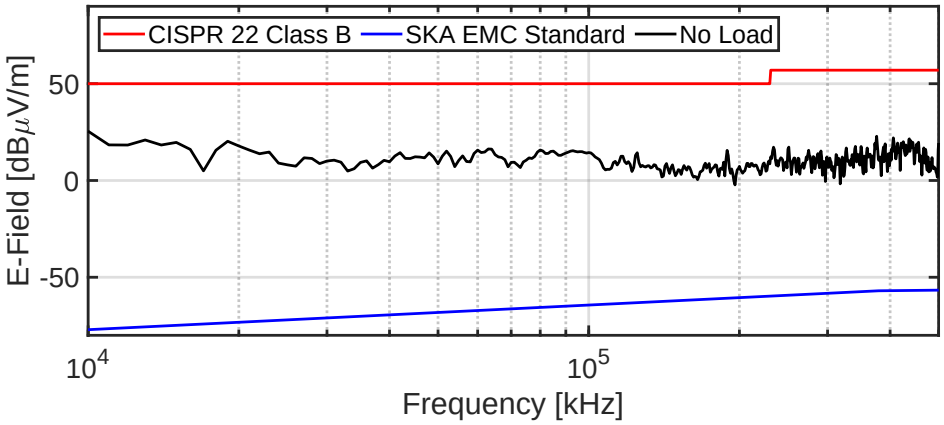
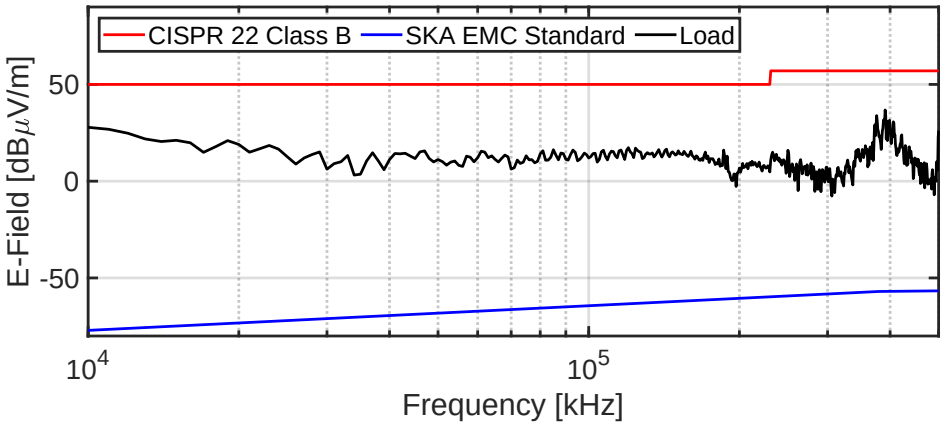



Figure 5.56: Estimated theoretical radiated emissions generated by logistic-shaped switching transitions. In this computational study, a trapezoidal waveform is assumed to be emitting at the CISPR-B limit line.

Based on the prototyping outcomes, practical limitations hinder the ideal spectral roll-off from being achieved. The drawbacks include digital control circuity introducing signal quantisation, discontinuities and errors in the waveform shaping, and the oscilloscope introducing noise to the measurements. The radiated emissions estimate for the prototype half-bridge producing a logistic shaped transition compared to a power converter generating radiated emissions at the CISPR-B limit line is presented in Figure 5.57(a) and Figure 5.57(b), for the prototype operating under no-load and constant load, respectively. The no-load and constant load curves are calculated by subtracting the difference in dB between the spectral bound of the hard-switching waveform and a logistic shaped waveform as shown in Figure 5.51 and Figure 5.53, respectively, from the CISPR 22 Class B limit line.




(a)




(b)

Figure 5.57: Estimated theoretical radiated emissions generated by the half-bridge prototype operating under (a) no-load and (b) constant load undergoing logistic-shaped switching transitions. In this study, the hard-switching measurements are assumed to be emitting at the CISPR-B limit line.

Although there will be other factors such as parasitic components and propagation paths that will limit the amount of attenuation that is practically achieved, the spectral content analysis provides a basis for estimating the expected emission levels of a power converter undergoing logistic-shaped switching transitions considering the SKA EMI/RFI threshold limits. For instance, as demonstrated in Figure 5.58, a power converter producing logistic-shaped switching transitions reduces the attenuation from shielding and filtering compared to the hard-switching measurements.

Based on the prototype measurements and attenuation estimates, the logistic shaped switching transitions for no-load (black trace) and constant load conditions (purple trace) provides 40 dB more attenuation on average compared to hard switching (red trace). The ideal logistic shaped transition is also presented (blue trace) to show the theoretical limit. Note that if the estimated emissions for the ideal logistic shaped transition in Figure 5.56 are less than the SKA EMI/RFI threshold limit, the attenuation is 0 dB.

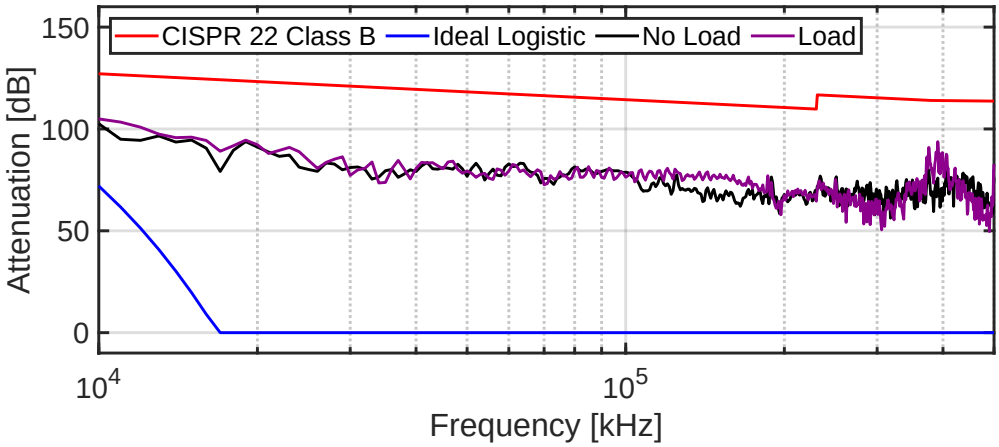



Figure 5.58: Estimated theoretical shielding and filtering attenuation requirements considering the SKA EMI/RFI threshold limits of the ideal logistic waveform (blue), prototype operating under no-load (black), and prototype operating under constant load (purple).

The analysis demonstrates that the prototype will require, on average, 70 dB of attenuation between 30 MHz and 500 MHz to reduce the switching noise to the SKA EMI/RFI limit value. Whereas, a power converter emitting at the CISPR 22 Class B limit line, requires on average 114 dB of attenuation. Lastly, a power converter capable of producing ideal logistic transitions, in theory, requires no attenuation beyond 30 MHz. The results of the predictive attenuation modelling identify the benefits expected to be achieved by power converters undergoing shaped switching transitions.

## 5.7 Summary

Lastly, a comparison of the waveform derivatives of a shaped switching transitions between the prototype laboratory measurements and the reference logistic, sinusoidal and S-shaped switching transitions is presented in Figure 5.59, Figure 5.60, and Figure 5.61, respectively. The results demonstrate that the derivative is not smooth for all shaped switching transitions and prevents the steep spectral roll-off in the logistic shaped switching transition being observed. The outcome is consistent with Section 3.5 of Chapter 3, which outlines the practical limitations of producing steep spectral roll-off where signal quantisation or discontinuities prevent the shaped switching transitions and the derivatives of the waveform from being smooth.

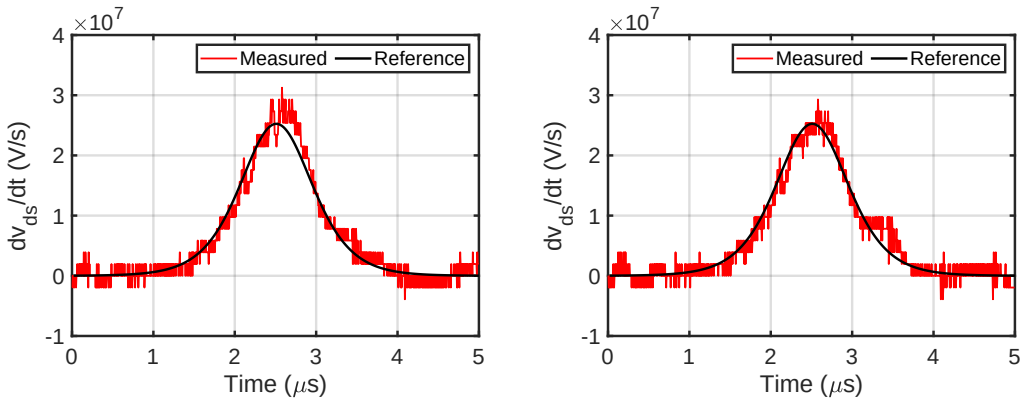



Figure 5.59: Derivative of the measured (red) and reference (black) logistic shaped transition when the bottom-MOSET is the $\alpha$-MOSFET. The half-bridge circuit is operating under (a) no load and (b) constant load.

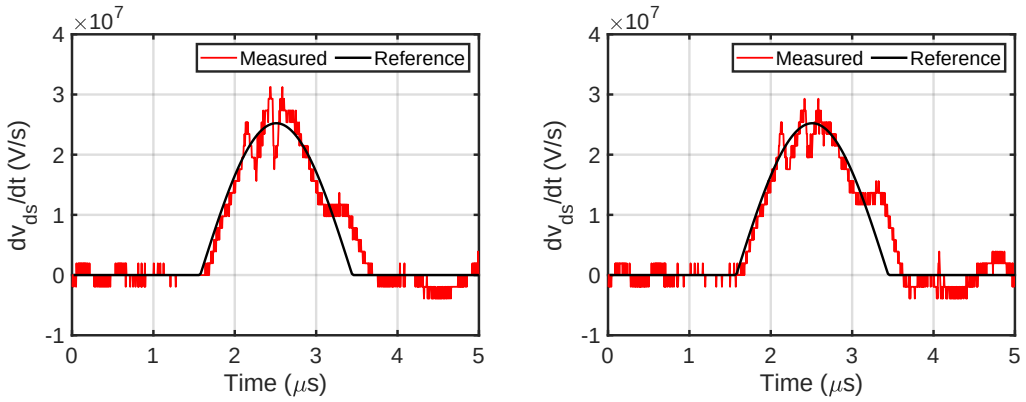



Figure 5.60: Derivative of the measured (red) and reference (black) sinusoidal shaped transition when the bottom-MOSET is the $\alpha$-MOSFET. The half-bridge circuit is operating under (a) no load and (b) constant load.

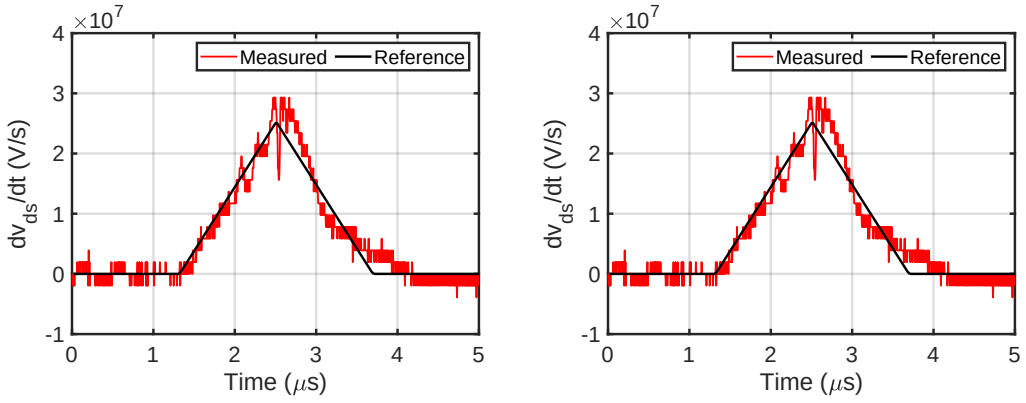



Figure 5.61: Derivative of the measured (red) and reference (black) S-shaped transition when the bottom-MOSET is the $\alpha$-MOSFET. The half-bridge circuit is operating under (a) no load and (b) constant load.

The laboratory measurements have demonstrated how shaped spectral transitions are produced within a half-bridge DC-DC converter. The operational prototype has demonstrated a power converter topology capable of following a shaped switching transition reference function. The prototype extends the capability beyond the ideal mathematical framework and a single MOSFET or IGBT to a power converter operating with a PWM switching scheme. Although, practical limitations are hindering the performance of the prototype considering high-frequency EMI mitigation. The digital control circuity introduced signal quantisation, discontinuities and errors to the waveform shaping technology. Additionally, the oscilloscope introduces noise to the measurements. Best

efforts to reduce these limitations have been demonstrated throughout the prototype development, including adding a parallel capacitor to the MOSFET drain-source, and applying a quantised control signal to the gate-drive only, and not to the output drain-source of the MOSFET. Additionally, the time-domain measurements of the prototype applied measurement averaging to reduce the inherent measurement noise of the oscilloscope.

However, even with the attempts made to reduce the high-frequency noise contributions to achieve spectral content roll-off, the derivatives of the shaped waveforms presented in Figure 5.59, Figure 5.60, and Figure 5.61, are not smooth. Even though the prototype performance provides significant EMI mitigation compared to the hard-switching half-bridge DC-DC converter and improves the waveform shaping performance compared to the studies presented in the literature, further improvements and refinements are still required to achieve spectral roll-off. The level of precision required to reduce errors in the half-bridge switching waveform and produce a smooth waveform derivative requires further research to identify the areas where the greatest amount of improvement can be achieved. The next chapter addresses the prototype improvements and future work of this research.

## 5.8 References

[1] *SKA RFI/EMC Standard*, Square Kilometre Array Organisation Std. SKA-TEL-SKO-0 000 202, 2021.

# Chapter 6

## Prototyping Improvements, Discussion and Conclusion

## 6.1 Low-EMI Half-Bridge Prototype Improvements

### 6.1.1 Identified Prototype Improvements

Presently in this dissertation, the computational modelling and prototype development have demonstrated the feasibility of the shaped switching transition technology in a half-bridge power converter. The prototype serves as a proof of concept for the low-EMI technology, and improvements will allow the technology to reach the maturity level ready for market production. A staged approach for the prototype improvements is presented in Figure 6.1 and discussed throughout the remainder of this section.

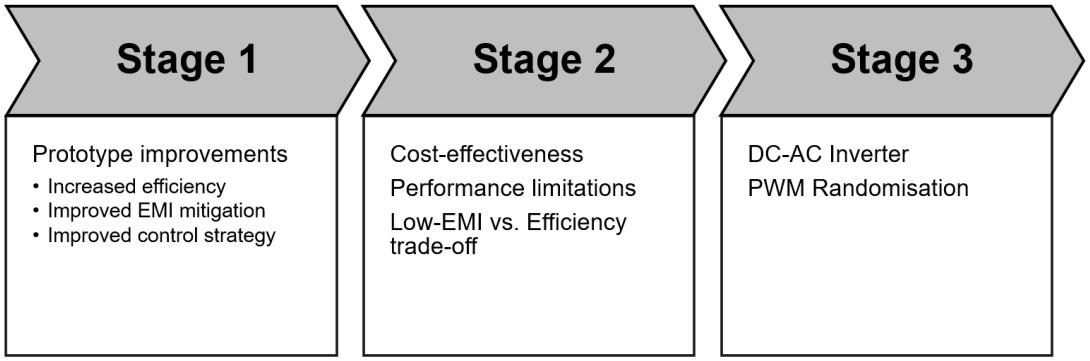



Figure 6.1: Staged approach for prototype improvements.

Firstly, design enhancements can be made to the power circuitry and control circuitry to improve the overall performance of the half-bridge. The next iteration of the half-bridge prototype will improve the power converter efficiency and the accuracy of the control strategy. By improving the control strategy, the EMI mitigation of the shaped switching transition control will be refined. Identified improvements to the low-EMI half-bridge prototype include the following:

- Reduce conduction losses associated with the current injection circuitry.
- Improve and automate the control of the auxiliary branch.
- Modify the control architecture to be a combination of an FPGA and micro-processor ($\mu$-processor).
- Increase switching frequency and reduce transition times.

With the current prototype design, the injection circuity relies on a DC power supply to provide the injected current, controlled by the $\beta$-injection MOSFET and generates undesired conduction losses. The next iteration of the prototype design will replace the power supply with a capacitor, which will be sized to store the amount of energy required for the current injection portion of the controlled, shaped transition. The capacitor sizing allows for the exact amount of energy to be stored, with allowable

tolerances, which will reduce the conduction losses of the DC power supply currently being used.

The auxiliary branch circuit is currently controlled with fixed timing instances under both constant load and no-load conditions. Future prototyping efforts intend to control the auxiliary branch turn-on timing using load current sense resistors to measure the actual current and determine when to control the auxiliary branch MOSFETs. The actual timing of the auxiliary branch will be determined by the load current, when the switching waveform will reach $0.5V_i$, and the auxiliary branch inductance value. The improvements will ensure that when the auxiliary branch is operated, the control and timing of the auxiliary branch will ramp the auxiliary branch inductor current to satisfy the $I_{load} + I_{aux} = 1$ pu criteria for any load current and change in load. Furthermore, once the power converter capability of the prototype can be demonstrated to function and provide low-EMI shaped transitions under changing load, additional power converter topologies such as a DC-AC inverter can be prototyped.

The control architecture of the half-bridge prototype can be modified to improve the accuracy of the control system, which is intended to improve the EMI mitigation of the shaped switching transitions. The current control system uses two FPGAs to perform all control and monitoring tasks. There are limitations in this approach since the FPGAs must perform all the required control and computation during a switching transition. In the case of the prototyping, the transition time is 20 $\mu$s. However, the expectation is that the shaped switching transition technology can be applied to shorter transition times. Therefore, there is a desire to combine an FPGA with a $\mu$-processor to improve the low-EMI half-bridge control. The intent is to use the FPGA for all real-time monitoring and sending the output control signals to the required power, injection and auxiliary MOSFETs. The $\mu$-processor will receive all recorded data from the FPGA or have a suitably selected ADC and perform the feedback control loop as required. The $\mu$-processor will have nearly the entire switching period to perform any necessary computation. The control system can be improved to decide the duration of the error-signal window, the error signal gain, and the timing of the control initialisation of each MOSFET.

The capability of the control system will be tested to determine the fastest transition time and switching period that the improved low-EMI half-bridge power converter can achieve. A faster transition time will reduce the switching losses since the $\alpha$-MOSFET $v_{ds}$ and $i_{ds}$ signal overlap is reduced, and less injection current will also be required. Additionally, extending the capability of the power converter to higher frequencies allows for the power converter to be miniaturised and become more cost-effective.

Based on the prototype improvements outlined, the following research topics can be studied:

- Improved control system capability to reduce output signal errors and improve EMI mitigation.
- Identification of various low-EMI applications based on performance trade-off assessments including maximum operating switching frequency, shortest transition time, and switching losses.
- Extend the prototype capability to operate for any load and change in load to verify the low-EMI capability of the technology.
- Inverter prototype and demonstration of the waveform shaping technology with inverter PWM techniques.

### 6.1.2 Cost-Effectiveness and Performance Trade-Offs

Once the subsequent prototype iterations have been developed, the prototype can be studied for various performance trade-off assessments, and the prototype can be re-designed as a cost-effective solution. Various trade-off assessments can be performed to understand the capability and limitations of the power converter. For the prototype low-EMI half-bridge power converter to operate effectively, the converter must be cost-effective, operate with high efficiency, and achieve circuitry miniaturisation. In no particular order or prioritisation, the cost-effectiveness and performance trade-off assessments are identified as follows:

- Cost and capability of FPGAs and $\mu$-processors
- Reduced power consumption of all auxiliary and control components
- Cost-effectiveness assessment
- Lowest power level that can cost-effectively be achieved
- Highest operating switching frequency and miniaturisation
- EMI performance and power converter efficiency trade-off assessment

Firstly, identifying better-suited FPGAs, $\mu$-processors, DACs, and ADCs for the shaped switching transitions is desired. Determining the best processor clock speed, which translates to the smallest time-step achieved in the control implementation, and the best n-bit DACs/ADCs for suitable data resolution is required. Determining the minimum time-step and highest data resolution required for the control system will stipulate the performance requirements for the FPGA, $\mu$-processors, DACs, and ADCs. Once the control system is improved and refined, the computational capacity and memory allocation should be determined to specify the FPGAs, and $\mu$-processors required. Additionally, the FPGA, $\mu$-processors, DACs, and ADCs should be selected based on

reduced power consumption where possible. Improved efficiency of the shaped transition control will allow the technology to be suitable at lower power levels.

The design should be carefully assessed to identify more cost-effective solutions once the improved prototype is operational. Although the exact aspects of the design are not identified at this stage, once the design and control are converging on a final solution, major components should be carefully assessed to identify cost savings where applicable. Such major components will include, but will not be limited to, the selection of MOSFETs, FPGAs, $\mu$-processors, DACs, ADCs, current and voltage sense circuity, current injection design and circuitry, power MOSFET capacitance, and auxiliary branch inductance.

The shortest transition that can accurately provide low-EMI-shaped switching transitions and the maximum operating frequency should be identified during continued prototype development and improvement. Higher switching frequencies are desirable as the size of the inductive and capacitive components are reduced. Additionally, the faster transition time will reduce switching losses and will require less injection current. Additionally, faster transitions times can reduce switching losses without compromising the EMI mitigation performance of the shaped waveform control. Although faster transition times increase the high-frequency emissions, it is outweighed by the high-frequency spectral roll-off achieved by a logistic-shaped switching transition. The inherent advantages may place less dependency on the piecewise switching transitions, which are outlined in the remainder of this Section, and modelled in subsequent sections of this Chapter.

Piecewise shaped transitions offer a trade-off between EMI performance and switching losses. The implementation of the low-EMI half-bridge prototype controls the gate drive of the power $\alpha$-MOSFET and $\beta$-injection MOSFET to allow the drain-source voltage of the MOSFET to track a logistic shaped reference waveform. A capacitor is connected in parallel to a power MOSFET, which is sized based on the load demand of the system and the $dv_{ds}/dt$ at $0.5V_i$ of the shaped transition, set by the logistic reference profile growth rate. At $0.5V_i$, the current is completely transferred to the capacitive branches of the half-bridge. Alternatively, a particular target voltage and corresponding derivative is defined, which is reached before $0.5V_i$ of the transition. The capacitor can then be sized to ensure that all current is transferred at the target voltage before $0.5V_i$. At the point where all current is transferred to the capacitor, the voltage profile is linear. The modelling allows for various voltage profiles and slopes to be studied, considering the spectral content of each transition. The investigation lends itself to a low-EMI and efficiency trade-off, with the piecewise transition characteristics

playing an essential role in the switching performance of the prototype. A preliminary computational study, which assess the impacts of the piecewise transitions is presented in Section 6.2.

### 6.1.3 DC-AC Inverter Design

Currently, the low-EMI switching power converter prototype has demonstrated that the technology is suitable for DC-DC converters since the prototype was operated under constant load for a 50% duty cycle. The next progression in the low-EMI power converter development is prototyping a DC-AC inverter that can undergo shaped switching transitions. The control sequencing is similar to the DC-DC converter, where a shaped switching transition command will be sent whenever the $\alpha$-MOSFET is required to undergo a shaped switching transition. The prototype developed in this research confirmed that the shaped switching transition control was suitable for PWM switching strategies. However, the added complexity of DC-AC inverter PWM switching strategies requires additional consideration to the switching transition control. For any inverter PWM waveform, the rise time $\tau_r$, the fall-time $\tau_f$, and the on-time $\tau$ must be carefully considered to avoid signal overlap. The following conditions must be satisfied to avoid overlapping:

$$\begin{aligned} d + \frac{\tau_r}{T} + \frac{\tau_f}{T} &\leq 1 \\ \frac{\tau_r}{T} + \frac{\tau_f}{T} &\leq \frac{d}{2} \end{aligned} \tag{6.1}$$

Where $T$ is the period of a pulse in the PWM waveform. In addition to signal overlap considerations, the transition times of shaped transitions are slower than the conventional transition times of hard-switched PWM waveforms. Therefore, the transition time set by the reference profile and what is practically achievable by the control system hardware will set the minimum pulse duration that can be achieved during PWM switching, which must be considered when establishing the PWM strategy for the inverter circuit.

### 6.1.4 PWM Randomisation

Although all applications seek to reduce EMI in power converters, novel mitigation strategies for the SKA-low should be considered in conjunction with conventional EMC design techniques. The additional mitigation strategies should be selected based on the amount of attenuation required to meet the SKA-low EMC limits.

Logistic functions must be considered as they allow for steep roll-off to be achieved. Additionally, the logistic function is defined by its growth rate, a temporal charac-

teristic selected for significant EMI mitigation. Shaped switching transitions should be combined with randomised-PWM (R-PWM) strategies to reduce further the spectral contribution of the switching waveform. A computational study was performed to outline the attenuation expected from applying multiple mitigation approaches when designing a power converter. A logistic-shaped waveform is synthesised, and conventional PWM and R-PWM strategies are compared, which is presented in Section 6.4. In the computational study, the R-PWM is synthesised by randomising the pulse position (delay) and the switching frequency. Although there will be other factors such as parasitic components and propagation paths that will limit the amount of attenuation that is practically achieved, the spectral content analysis provides a basis for making informed estimates considering the expected amount of attenuation that can be achieved.

## 6.2 EMI and Efficiency Trade-off

This section outlines the modelling methodology developed to compare the spectral content of numerous shaped transitions, which considers shaped-linear-shaped piecewise switching transitions. The parallel power MOSFET capacitance governs the duration and commencement of the linear region. The piecewise transitions are evaluated and compared to the ideal logistic-shaped switching transition to assess low-EMI performance. The two types of transitions compared are hereafter referred to as piecewise and ideal transitions. The modelling seeks to bridge the gap between theoretical modelling and continued circuitry prototype development, providing an ideal transition if low-EMI performance is the primary design consideration or providing piecewise transitions if switching losses and low-EMI performance must be considered.

Furthermore, piecewise analysis is included if the control strategy cannot achieve the ideal shaped transition and a delay during the switch transition near $0.5V_i$ of the reference voltage waveform is required. The delay would be required if the desired rate of change of drain-source voltage could not be achieved at $0.5V_i$. Therefore, the gate-drive could be adjusted to allow current to be diverted to the capacitors before $v_{ds}$ reaches $0.5V_i$. Furthermore, this functionality may be required if the switching losses are too significant, and a trade-off between EMI and efficiency is required. Alternatively, if less stringent EMI requirements are specified, then piecewise transitions may be better suited.

The effects of the target voltage on EMI is studied. The more time spent in the controlled region of the transition, the greater the losses. However, the most significant theoretical EMI spectral roll-off is achieved for a capacitor sized so that all current is

diverted to the capacitors at $0.5V_i$. Setting a target voltage and consequently a linear region of the shaped switching transition is detrimental to EMI mitigation. The linear region can be considered a trapezoidal signal, with a reduced amplitude compared to the complete switching transition. Two things need to be considered when assessing the impacts the linear region will have on EMI. Although smaller in amplitude, a shorter linear region will be steeper since the derivative is greater near $0.5V_i$, which will generate more EMI. More extended linear regions will be more significant in amplitude but will be less steep. The former may be least desired since the short linear regions may generate unwanted EMI and will not provide any considerable improvements to the switching losses. Conversely, more extended linear transition regions will be detrimental to EMI mitigation, but switching losses are considerably improved.

### 6.2.1 EMI Considerations of Piecewise Shaped Transitions

The effects of the target voltage on EMI attenuation is studied. The switching transition is shaped until the target voltage is reached and is linear until the next target voltage is reached. Note that both target voltages points are equidistant from $0.5V_i$ to ensure the transition is symmetrical. Afterwards, the transitions become shaped again until the transition is complete. The transitions need to be continuous to avoid discontinuities that generate unwanted EMI. Therefore the gradients of each part of the piecewise transition need to be equal at the logistic-linear and linear-logistic boundaries. For example, for a 1 V waveform, 25% target voltages are 0.25 V and 0.75 V on the waveform. From 0 V to 0.25 V, the waveform is shaped by the $\alpha$-MOSFET. From 0.25 V to 0.75 V, the current is diverted to the capacitors, and the output voltage is linear. From 0.75 V to 1 V, the waveform is shaped by the $\beta$-injection MOSFET. An example of a piecewise transitions compares to an ideal transitions is shown in Fig 6.2. When the output voltage is linear, there are no switching losses. Although the linear portion limits EMI mitigation, it improves switching losses.

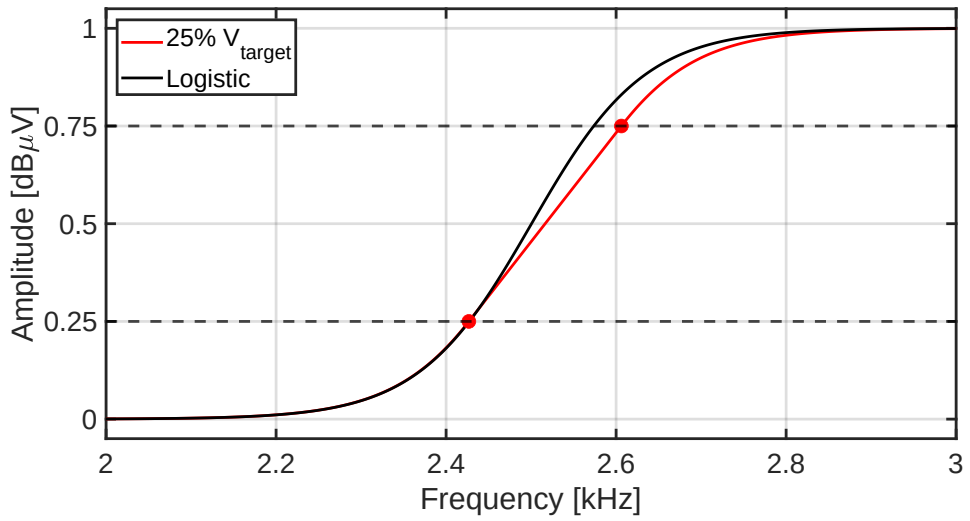



Figure 6.2: Example piecewise shaped transition considering a 25% target voltage.

Figure 6.3 presents a spectral comparison of an ideal logistic shaped switching waveform compared to waveforms that are only shaped for a portion of the transition, which create piecewise transitions that are shaped-linear-shaped. The target voltage is set to 30%, 35% and 40% of the shaped waveform for the spectral comparison performed. All waveforms are modelled with a 10 kHz switching frequency, a signal amplitude of 1 V, a transition time of 5 $\mu$s, and a growth rate of $15 \times 10^6$.

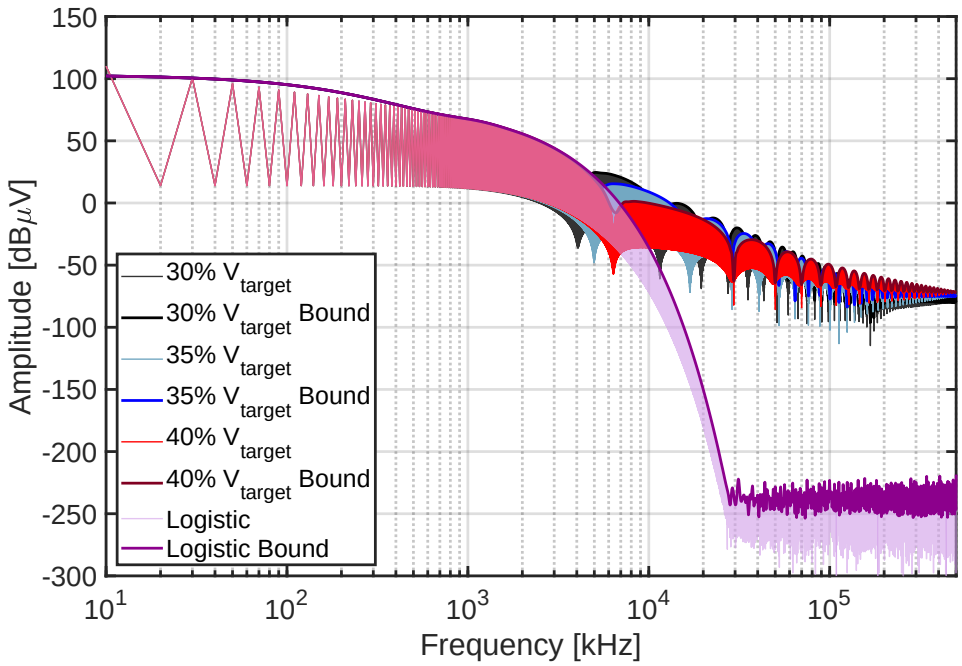



Figure 6.3: Harmonic spectra of a logistic shaped PWM waveform compared to piecewise shaped transitions synthesised with a 30%, 35% and 40% target voltage.

## 6.3 Considerations for Low-EMI Inverters

### 6.3.1 Overview

The theory and analytical Fourier series to predict the harmonic spectrum of regularly sampled hard-switching PWM are presented in [1]. Additionally, the analytical Fourier series for an S-shaped transition is presented in [2]. The two techniques are combined to determine a regularly sampled PWM technique with S-shaped switching transitions. The approach outlines how to derive the regularly sampled PWM technique with logistic-shaped switching transitions.

### 6.3.2 Numerical Assessment of Inverter PWM Shaped Transitions

#### 6.3.2.1 Hard-Switching Regularly Sampled PWM

Provided the ratio of the carrier frequency ($f_c$), and modulation ($f_m$) frequency is an integer, the spectral content of a regularly sampled PWM waveform spectrum is given by [1]:

$$S(k) = \frac{2A}{\pi k}\left|\sum_{v=1}^{N}\sin\left(\frac{\pi k}{2N}\left(1+m\sin\left(2\pi\frac{v}{N}\right)\right)\right)e^{-j2\pi k\frac{v}{N}}\right| \tag{6.2}$$

Where $k$ is the integer harmonic number of the modulation frequency, and $m$ is the modulation index. $N$ is defined as the ratio of the carrier frequency to the modulation frequency. Additionally, the duty cycle of each pulse in the regularly sampled waveform is defined by $d = \frac{1}{2N}\left(1 + m\sin\left(2\pi\frac{v}{N}\right)\right)$. Where $m$ is the modulation factor of the inverter. With the inclusion of slew rates, the harmonic spectrum is given by [1]:

$$S(k) = \frac{A}{\pi k}\left|\sum_{v=1}^{N}\left[\operatorname{sinc}(\pi k\frac{\tau_r}{T})e^{i\frac{\pi k}{2N}\left(1+m\sin\left(2\pi\frac{v}{N}\right)\right)}\right.\right. \\ \left.\left. - \operatorname{sinc}(\pi k\frac{\tau_f}{T})e^{-i\frac{\pi k}{2N}\left(1+m\sin\left(2\pi\frac{v}{N}\right)\right)}\right]e^{-i2\pi\frac{v}{N}}\right| \tag{6.3}$$

Where $\tau_r$ and $\tau_f$ are the rise time and fall time of the switching waveform, respectively. The following in-equation must be satisfied to avoid signal overlap:

$$\frac{1}{2}m + \frac{\tau_r}{T} + \frac{\tau_f}{T} \leq \frac{1}{2} \tag{6.4}$$

#### 6.3.2.2 Regularly Sampled PWM with S-Shaped Transitions

To combine the regularly sampled PWM Fourier series, with the S-shaped transition Fourier series, some notation must be noted, where $d = \frac{\tau}{T}$ and $\pi d = \frac{\omega_0\tau}{2}$. When considering PWM, the duty cycle and, therefore $\tau$, of each subsequent pulse varies according to:

$$d = \frac{1}{2N}\left(1 + m\sin\left(2\pi\frac{v}{N}\right)\right) \tag{6.5}$$

Where $v$ is a particular pulse, and $N$ is the total number of pulses. Since $\pi d = \frac{\omega_0\tau}{2}$ for a sinusoidal PWM switching scheme:

$$\pi\left(\frac{1}{2N}\left(1 + m\sin\left(2\pi\frac{v}{N}\right)\right)\right) = \frac{\omega_0\tau}{2} \tag{6.6}$$

The regularly sampled PWM amplitude spectrum combined with the S-shaped switching transition amplitude spectrum is, therefore:

$$C_n = \frac{A\pi}{2N}\left|\sum_{v=1}^{N}\left[\left(1 + m\sin\left(2\pi\frac{v}{N}\right)\right)\operatorname{sinc}\left(n\frac{\pi}{2N}\left(1 + m\sin\left(2\pi\frac{v}{N}\right)\right)\right)\times\right.\right. \\ \operatorname{sinc}\left(n\omega_0\frac{\tau_r - \tau_{r(dv/dt)}}{2}\right)\operatorname{sinc}\left(n\omega_0\frac{\tau_{r(dv/dt)}}{2}\right)\times \\ \left.\left.\left(e^{jn\frac{\pi}{2N}\left(1+m\sin\left(2\pi\frac{v}{N}\right)\right)}\right)\left(e^{jn\omega_0\frac{\tau_{r(dv/dt)}}{2}}\right)\right]e^{-j2\pi n\frac{v}{N}}\right| \tag{6.7}$$

#### 6.3.2.3 Regularly Sampled PWM with Logistic Shaped Transitions

The hard-switching regularly sampled PWM analytical Fourier series expressions provided in Equation 6.2 and Equation 6.3 use the time-shifting property of the Fourier series since the periodic PWM waveform consists of $N$ pulses, with unique pulse widths. Similarly, the approach can be utilised to define a regularly sampled PWM analytical Fourier series with logistic shaped switching transitions. Recalling the Fourier series representation of a logistic shaped switching transition:

$$C_n = \left(1 - \mathrm{e}^{-i2\pi n\tau/T}\right) A(t) + \mathrm{e}^{-i2\pi n\tau_t/T} E(t) \tag{6.8}$$

Where:

$$\begin{aligned} A(t) = -\frac{iA\alpha}{2\pi n(\beta-\alpha)} \Bigg( & \beta \mathrm{e}^{-i2\pi nt/T} \left[ -1 + {}_2F_1\left( \left[ 1, \frac{i2\pi n/T}{k} \right]; 1 - \frac{i2\pi n/T}{k}; -\mathrm{e}^{k(t-\tau_t/2)} \right) \right] \Bigg|_0^{\tau_t} \\ & - \mathrm{e}^{-i2\pi nt/T} \Bigg|_0^{\tau_t} \Bigg) \\ E(t) = \frac{iA}{2\pi n} & \mathrm{e}^{-i2\pi nt/T} \Bigg|_0^{\tau} \end{aligned} \tag{6.9}$$

Considering the Fourier series of the DC-AC inverter hard-switching regularly sampled PWM, the expression can be modified to include logistic shaped transitions. The analytical Fourier series for a regularly sampled PWM with logistic shaped transitions becomes:

$$C_n = \sum_{v=1}^{N} \left[ \left[ \left(1 - \mathrm{e}^{-i2\pi n\left[\frac{1}{2N}\left[1 + m\sin\left(2\pi\frac{v}{N}\right)\right]\right]}\right) A(t) + \mathrm{e}^{-i2\pi\tau_t n/T} E(t) \right] \right] \tag{6.10}$$

Where:

$$\begin{aligned} A(t) = -\frac{iA\alpha}{2\pi n(\beta-\alpha)} \Bigg( & \beta \mathrm{e}^{-i2\pi nt/T} \left[ -1 + {}_2F_1\left( \left[ 1, \frac{i2\pi n/T}{k} \right]; 1 - \frac{i2\pi n/T}{k}; -\mathrm{e}^{k(t-\tau_t/2)} \right) \right] \Bigg|_0^{\tau_t} \\ & - \mathrm{e}^{-i2\pi nt/T} \Bigg|_0^{\tau_t} \Bigg) \\ E(t) = \frac{iA}{2\pi n} & \mathrm{e}^{-i2\pi nt/T} \Bigg|_0^{\frac{T}{2N}\left[1 + m\sin\left(2\pi\frac{v}{N}\right)\right]} \end{aligned} \tag{6.11}$$

### 6.3.3 Spectral Modelling of Inverter PWM

The harmonic content and spectral bound up to 50 MHz of an inverter PWM undergoing S-shaped and logistic-shaped switching transitions are presented in Figure 6.4. Both PWM waveforms are modelled with a 10 kHz switching frequency, 50 Hz modulation frequency, the signal amplitude of 1 V, and transition time of 5 $\mu$s. Additionally, the logistic shaped transition is modelled with a growth rate of $15 \times 10^6$.

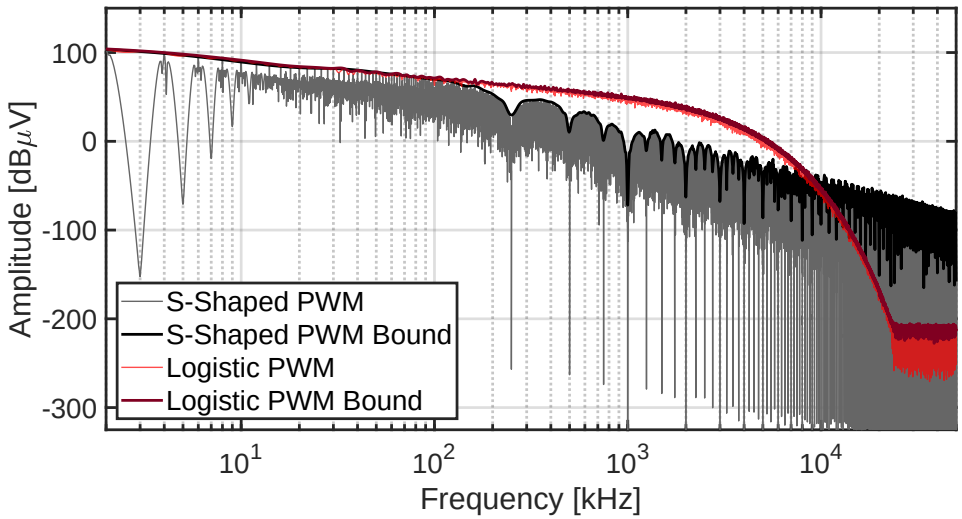



Figure 6.4: Spectral modelling of a DC-AC inverter using regularly sampled PWM undergoing S-shaped (black) and logistic-shaped (red) switching transitions.

## 6.4 Randomised Shaped Transitions

### 6.4.1 Randomised PWM Waveform Synthesis

Recalling, the piecewise representation of a switching waveform with a shaped switching transition function, $r(t)$, is given by:

$$\begin{aligned} f(t) &= r(t), & 0 \leq t < \tau_t \\ f(t) &= A, & \tau_t \leq t < \tau \\ f(t) &= A - r(t-\tau), & \tau \leq t < \tau + \tau_t \\ f(t) &= 0, & \tau + \tau_t \leq t < T \end{aligned} \tag{6.12}$$

Eq. 6.12 is the fixed frequency case. For any logistic-shaped switching transitions, the piecewise function can be modified to define the $i$-th pulse in the randomised waveform where the pulse delay $t_{di}$ and switching frequency $f_i$ (or switching period $T_i$) can be randomly varied. Note $t_{si}$ is the starting time of the $i$-th pulse. The piecewise function

for a shaped-pulse, $r(t)$, with a waveform amplitude $A$, a randomised switching period and randomised shaped-pulse delay is given as:

$$\begin{aligned}
f(t) &= 0, && t_{si} \leq t < t_{di} + t_{si} \\
f(t) &= r(t), && t_{di} + t_{si} \leq t < t_{di} + t_{si} + \tau_t \\
f(t) &= A, && t_{di} + t_{si} + \tau_t \leq t < t_{di} + t_{si} + \tau \\
f(t) &= A - r(t - \tau), && t_{di} + t_{si} + \tau \leq t < t_{di} + t_{si} + \tau + \tau_t \\
f(t) &= 0, && t_{di} + t_{si} + \tau + \tau_t \leq t < t_{si} + T_i
\end{aligned} \tag{6.13}$$

### 6.4.2 Randomised PWM Fourier Series

Considering the piecewise representation provided in Eq. 6.13, the integrals for each respective piecewise component considering that the pulse is described by a random switching frequency $f_i$ becomes:

$$\begin{aligned}
S(t) &= \frac{1}{T} \int_0^{\tau_t} r(t) \mathrm{e}^{-i2\pi nt/T} dt \\
S(t) &= \frac{1}{T} \int_{\tau_t}^{\tau_i} A \mathrm{e}^{-i2\pi nt/T} dt \\
S(t) &= \frac{1}{T} \int_{\tau_i}^{\tau_i + \tau_t} (A - r(t - \tau_i)) \mathrm{e}^{-i2\pi nt/T} dt \\
S(t) &= \frac{1}{T} \int_{\tau_i + \tau_t}^{T_i} 0 \mathrm{e}^{-i2\pi nt/T} dt
\end{aligned} \tag{6.14}$$

Combining each piecewise term and ignoring the integrals equating to zero, the total expression is given by:

$$\begin{aligned}
S(t) = & \frac{1}{T} \int_0^{\tau_t} r(t) \mathrm{e}^{-i2\pi nt/T} dt + \frac{1}{T} \int_{\tau_t}^{\tau_i} A \mathrm{e}^{-i2\pi nt/T} dt \\
& + \frac{1}{T} \int_{\tau_i}^{\tau_i + \tau_t} A \mathrm{e}^{-i2\pi nt/T} dt - \frac{1}{T} \int_{\tau_i}^{\tau_i + \tau_t} r(t - \tau_i) \mathrm{e}^{-i2\pi nt/T} dt
\end{aligned} \tag{6.15}$$

The derivation method is the same as shaped switching transition analytical Fourier series derivation presented in Section 3.2.1, with the exception that the shaped transitions have a randomised delay and switching frequency to synthesise a random pulse train. Therefore, the analytical Fourier series, $A(t)$ and $E(t)$ are very similar except $t_{di}$ and $\tau_i$ are considered in the expressions for each random pulse. Therefore, $C_n$ becomes:

$$C_n = \left(1 - \mathrm{e}^{-i2\pi\tau_i/T}\right) A(t) + \mathrm{e}^{-i2\pi\tau_t/T} E(t) \tag{6.16}$$

Where:

$$\begin{aligned} A(t) &= \frac{1}{T}\int_0^{\tau_t} r(t)\mathrm{e}^{-i2\pi nt/T}dt \\ E(t) &= \frac{1}{T}\int_0^{\tau_i} A\mathrm{e}^{-i2\pi nt/T}dt \end{aligned} \tag{6.17}$$

Considering $r(t)$ as a logistic equation, $A(t)$ can be redefined and simplified considering logistic-shaped switching transitions:

$$r(t) = \frac{\alpha A}{\beta-\alpha}\left[\frac{\beta}{1+\mathrm{e}^{-k(t-\tau_t/2)}} - 1\right] \tag{6.18}$$

Therefore, expressions for $A(t)$ and $E(t)$ are given as:

$$\begin{aligned} A(t) = -\frac{iA\alpha}{2\pi n(\beta-\alpha)}\Bigg(&\beta\mathrm{e}^{-i2\pi nt/T}\left[-1+{}_2F_1\left(\left[1,\frac{i2\pi n/T}{k}\right];1-\frac{i2\pi n/T}{k};-\mathrm{e}^{k(t-\tau_t/2)}\right)\right]\Bigg|_0^{\tau_t} \\ &-\mathrm{e}^{-i2\pi nt/T}\Bigg|_0^{\tau_t}\Bigg) \\ E(t) = \frac{iA}{2\pi n}&\mathrm{e}^{-i2\pi nt/T}\Bigg|_0^{\tau_i} \end{aligned} \tag{6.19}$$

Therefore, the Fourier series representation of any randomised pulse in the train can be represented as a time-shifted equivalent of $A(t)$ and $E(t)$, where $t_{di}$ and $T_i$ are the randomised delays and randomised switching period, respectively. Therefore, the Fourier series of a switching waveform with logistic shaped switching transitions consisting of $p$ random pulses is given by:

$$C_n = \sum_{i=1}^{p}\left(\mathrm{e}^{-i2\pi n(t_{di}+\sum_{a=1}^{i-1}T_a)/T}\left[\left(1-\mathrm{e}^{-i2\pi\tau_i n/T}\right)A(t)+\mathrm{e}^{-i2\pi\tau_t n/T}E(t)\right]\right) \tag{6.20}$$

### 6.4.3 Spectral Modelling of Randomised PWM for DC-DC Converters

Computational studies have been performed on the spectral content of randomised PWM waveforms with logistic shaped transitions. The modelling considers the randomisation of the pulse delay, $t_{di}$, and the switching frequency, $f_i$. The spectral analysis is performed on a random PWM waveform where both the time delay and switching frequency were simultaneously varied by ±5%, ±10%, and ±15%, as shown in Figure 6.5. Each scenario is modelled with a signal amplitude of 1 V, a transition time of 5 $\mu$s, a growth rate of $15\times10^6$, and a nominal switching frequency is 10 kHz. Each waveform is randomised with 1000 random pulses. Each scenario shows negligible improvement between the ±5%, ±10%, and ±15% cases. The critical consideration is that randomising the pulse delay and switching frequency is desirable for EMI mitigation.

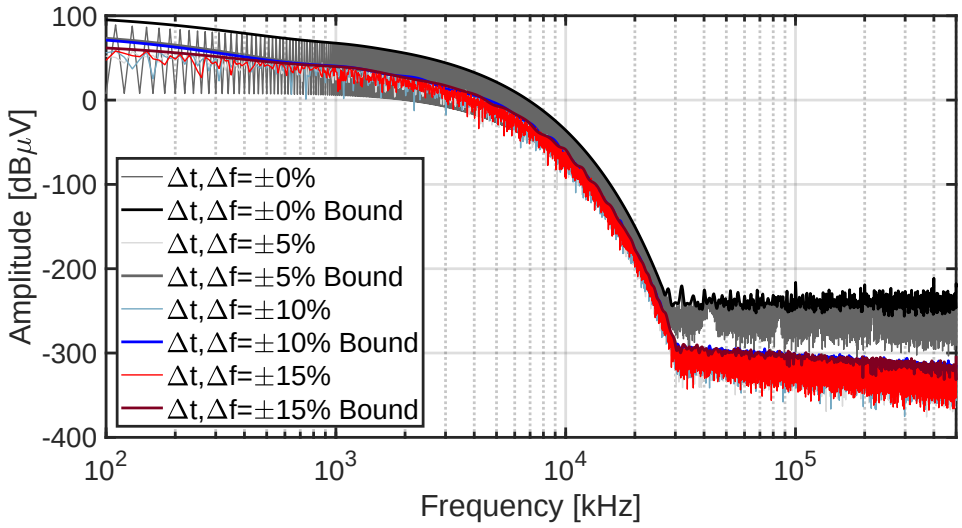



Figure 6.5: Spectral modelling of randomised PWM with logistic shaped transitions. The plot shows the spectral content of fixed-frequency logistic-shaped transitions (black), and the waveform generated with the switching frequency and pulse position both randomised. Each waveform is randomised with 1000 random pulses.

Lastly, the spectral content of the shaped transitions was modelled considering a different number of random pulses. Figure 6.6 presents the harmonic spectra of a fixed-frequency logistic-shaped transition compared to randomised PWM with logistic shaped transitions synthesised with 100, 1,000 and 10,000 pulses. Each scenario is modelled with a signal amplitude of 1 V, a transition time of 5 $\mu$s, a growth rate of $15 \times 10^6$, and a 10 kHz nominal switching frequency.

The spectral content shows improved attenuation is achieved with an increased number of random pulses. The outcome is expected since the number of random pulses sets the waveform period, $T$, creating a low-frequency response that is an artefact of the analytical Fourier series. The number of pulses provides a trade-off between theoretical attenuation and computational time. The ideal scenario would be to determine the spectral content for an infinite number of random pulses. However, it is computationally impractical. A finite number of random pulses also depicts the limitations present in actual implementation, where random switching may be configured with a predetermined number of random pulse delays and switching frequencies.

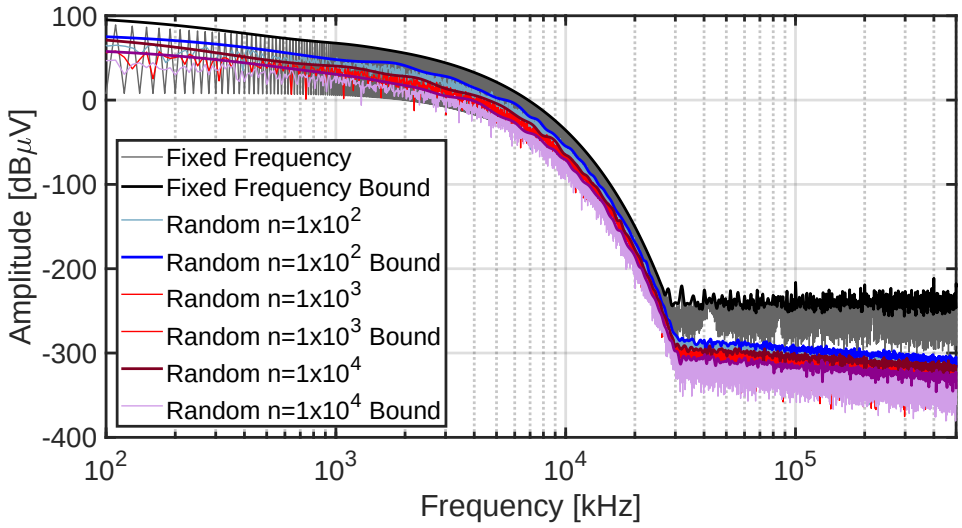



Figure 6.6: Spectral modelling of randomised PWM with logistic shaped transitions. The plot presents the harmonic spectra of fixed-frequency logistic-shaped transitions (black), and the waveform generated with the switching frequency and pulse position both randomised. Each randomised waveform is modelled with a different number of random pulses including, 100, 1,000 and 10,000.

### 6.4.4 Randomised Regularly Sampled PWM Inverter with Logistic Shaped Transitions

Furthermore, the randomised PWM techniques can be extended to consider DC-AC inverters. Considering regularly sampled PWM, the Fourier series is considered the sum of each pulse in the train. Each pulse is defined by a duty cycle and a delay term calculated from the pulse number, $v$. Therefore, the Fourier series of a regularly sampled PWM waveform with logistic shaped transitions consisting of $p$ random pulses is given by:

$$C_n = \sum_{i=1}^{p} \left( \mathrm{e}^{-i2\pi n(t_{di} + \sum_{a=1}^{i-1} T_a + \frac{v}{N} T_i)/T} \right. \\ \left. \sum_{v=1}^{N} \left[ \left( 1 - \mathrm{e}^{-i2\pi n \left[ \frac{T_i}{2N} \left[ 1 + m\sin\left(2\pi \frac{v}{N}\right) \right] \right]/T} \right) A(t) + \mathrm{e}^{-i2\pi\tau_t n/T} E(t) \right] \right) \tag{6.21}$$

Where:

$$A(t) = -\frac{iA\alpha}{2\pi n(\beta-\alpha)}\left(\beta \mathrm{e}^{-i2\pi nt/T}\left[-1+{}_2F_1\left(\left[1,\frac{i2\pi n/T}{k}\right];1-\frac{i2\pi n/T}{k};-\mathrm{e}^{k(t-\tau_t/2)}\right)\right]\Bigg|_0^{\tau_t} - \mathrm{e}^{-i2\pi nt/T}\Bigg|_0^{\tau_t}\right)$$
$$E(t) = \frac{iA}{2\pi n}\mathrm{e}^{-i2\pi nt/T}\Bigg|_0^{\frac{T_i}{2N}\left[1+m\sin\left(2\pi\frac{v}{N}\right)\right]} \tag{6.22}$$

### 6.4.5 Spectral Modelling of Randomised PWM for DC-AC Inverters

The spectral content of the shaped transitions was modelled considering 1000 random pulses as shown in Figure 6.6. The analysis compares the spectral content of fixed-frequency and randomised switching frequency regularly sampled PWM with logistic-shaped switching transitions. Each scenario is modelled with a signal amplitude of 1 V, a transition time of 5 $\mu$s, a growth rate of $15 \times 10^6$, a 10 kHz nominal carrier frequency, a 50 Hz nominal modulation frequency, and a modulation factor of 0.8.

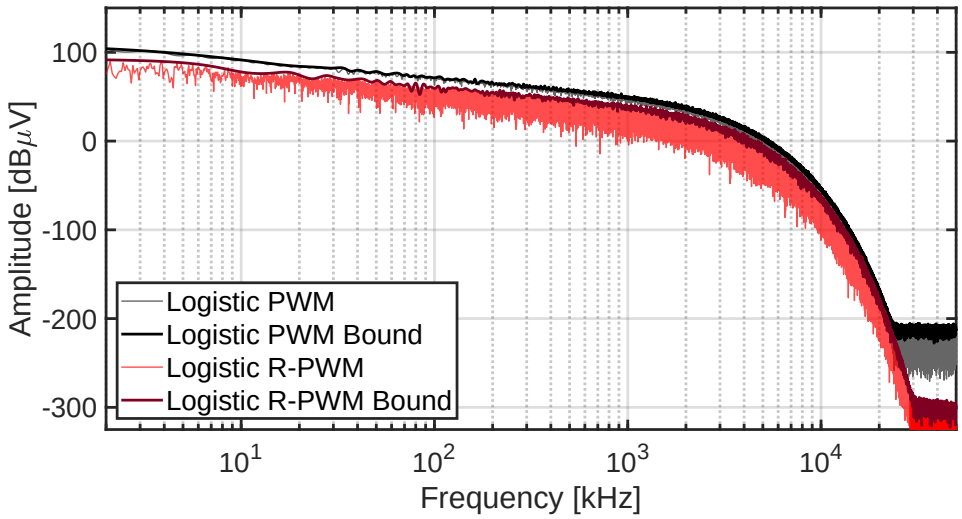



Figure 6.7: Spectral modelling of a DC-AC inverter using randomised regularly sampled PWM undergoing logistic-shaped switching transitions. The plot shows the spectral content of a fixed-frequency logistic-shaped transition (black), and the waveform generated with a randomised switching frequency (red), which is randomised with 1000 random pulses.

## 6.5 Discussion and Conclusion

### 6.5.1 Summary of Work

The primary motivation for this research work is the EMC and EMI/RFI mitigation requirements for power supplies intended for radio astronomy applications. Therefore, the need to develop low-noise power converters that undergo shaped switching transitions that produce steep spectral roll-off, in theory, was the primary driver for this research project. The work and intellectual contributions of this dissertation are summarised in this section.

Chapter 1 and Chapter 2 presented the background project information and a comprehensive literature review. Initially, an overview of the project objectives and the SKA-low project requirements, particularly EMC, was presented to outline the need for low noise power supplies beyond 30 MHz. Following this, a literature review on power converter EMI mitigation techniques and suitable approaches for radio astronomy was presented, which informed the engineering design methodology for achieving low-EMI shaped switching transitions for radio astronomy applications presented at the end of Chapter 2.

Chapter 3 presented the theoretical background and spectral content analysis of shaped switching transitions. Firstly, the analytical Fourier series of PWM switching waveforms with shaped switching transitions were presented. MATLAB codes were developed to understand the spectral content of shaped switching transitions and gain insight into the practical limitations expected in hardware implementation. The primary outcomes of Chapter 3 were:

- Development of an analytical Fourier series applied to shaped switching waveforms with an infinitely differentiable switching function.
- Modified logistic function with suitable asymptotes to ensure smooth switching transitions to avoid discontinuities that are undesirable for low-EMI outcomes.
- Identification and utilisation of logistic shaped switching transitions and suitable selection of the growth rate to identify steep spectral roll-off.
- Spectral content analysis of shaped switching transitions using available comparative metrics, including spectral roll-off, EMI metric, and spectral bounds.
- Signal discontinuities and quantisation impacts on high frequency EMI mitigation to specify the level of accuracy required to achieve spectral roll-off.

The combined content of Chapter 4 and Chapter 5 presented the modelling and design of the half-bridge prototype capable of generating shaped switching transitions. Chapter 4 began with an overview of a hard-switching half-bridge DC-DC converter to understand

the typical switching control sequence and MOSFET transient response. Following this, the half-bridge circuit topology and control strategy was presented. Circuit simulations to realise the shaped switching transitions in the half-bridge circuit was presented in Chapter 4. Chapter 5 presented the half-bridge circuit design, FPGA control strategy, and laboratory verification measurements. The primary outcomes were:

- Developing a half-bridge power converter with PWM switching control and demonstrating that shaped transitions can be integrated in power converters.
- Including current injection and parallel capacitors in the half-bridge prototype to produce shaped switching transitions that reduces signal quantisation and waveform discontinuities.
- Combining $\alpha$-MOSFET and $\beta$-injection MOSFET gate-drive control to shape the voltage across the $\alpha$-MOSFET parallel capacitors.
- LTSICE and MATLAB simulations of the prototype half-bridge demonstrating the feasibility of the approach and developing the control strategy algorithm.
- Prototype development with the ability to configure the reference profile to produce logistic, sinusoidal, and S-shaped switching transitions.
- Estimated emission levels considering ideal and the prototype logistic-shaped switching transitions compared to the SKA RFI/EMC emission limits to identify the reduction in shielding and filtering requirements.

Chapter 6 commenced with an overview of future improvements with preliminary modelling considering continued research efforts. The new modelling provided insights into:

- Commencing a low-EMI and efficiency trade-off by assessing the spectral content of piecewise transitions intended to reduce switching losses.
- Analytical Fourier series and spectral content analysis of regularly sampled inverter PWM switching with logistic shaped switching transitions.
- Analytical Fourier series and spectral content analysis of randomised PWM waveforms with logistic shaped switching transitions for a DC-DC converter and DC-AC inverter.

Numerous intellectual contributions have emanated from the research conducted on low-EMI power converters. Of particular importance is the invention of a novel approach to shaped switching transitions. Additionally, the modelling performed has provided insight into what is required to achieve high-frequency spectral content roll-off and how hardware limitations can hinder that.

### 6.5.2 Conclusion

The work presented in this dissertation concerns the prototype development, simulation, and laboratory testing of a half-bridge DC-DC converter undergoing shaped switching transitions. Using the SKA-low as the intended application, the primary objective was to mitigate power converter switching noise beyond 30 MHz.

The key concepts were all focused on making intellectual contributions in power converter EMI mitigation, namely, shaped switching transitions. Firstly, logistic shaped switching transitions were utilised, and appropriate growth rates were selected to achieve steep spectral roll-off. The half-bridge power converter, which not only extends the knowledge base on achieving shaped switching transitions using MOSFETs, also extends the capability of the shaped transitions to a power converter operating under constant load. Analytical Fourier series derivation of DC-DC converter and DC-AC inverter shaped switching transitions were adopted from literature and derived in the case of infinitely shaped switching transitions to study the frequency-domain behaviour of switching waveforms. Furthermore, the analytical Fourier series expressions were extended to randomised PWM for similar spectral content analysis. The analytical Fourier series representation of shaped switching transition waveforms and the spectral content modelling and analysis allows for key temporal characteristics to be identified that are suitable for EMI mitigation and high-frequency spectral content roll-off.

The prototype half-bridge development primarily allowed shaped switching transitions to be realised in an actual power converter operating under constant load. The novel approach controlled the gate-drive of the $\alpha$-MOSFET and $\beta$-injection MOSFET gate-drive control, which demonstrates the prototype can follow a reference logistic shaped switching transition to shape the voltage across the $\alpha$-MOSFET parallel capacitors.

## 6.6 References

[1] A. Nagel and R. W. De Doncker, "Analytical approximations of interference spectra generated by power converters," in *IEEE Ind. Appl. Conf.*, vol. 2, 1997, pp. 1564–1570.

[2] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 47, pp. 2154–2165, 2011.

# Appendix A

## Laboratory Measurements - Top MOSFET Switching

## A.1 Overview

The Appendix presented all the laboratory measurements performed when the top power MOSFET is the $\alpha$-MOSFET.

## A.2 Laboratory Measurements

### A.2.1 Logistic-Shaped Transition - No Load

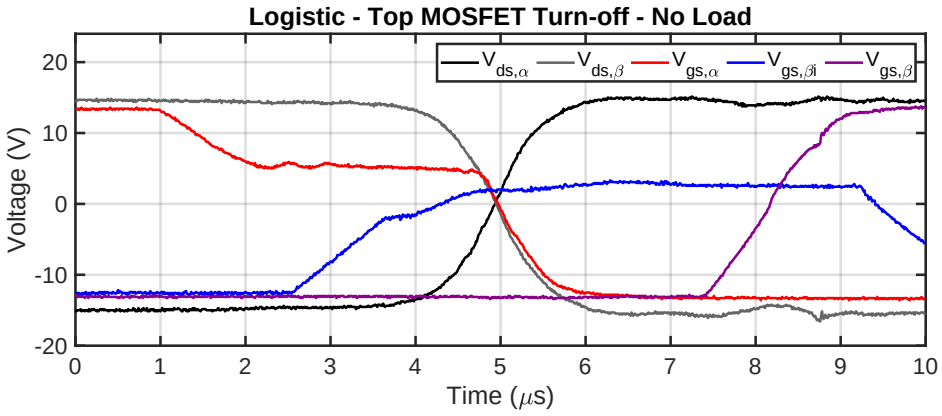



Figure A.1: Turn-off sequence for a logistic-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under no load.

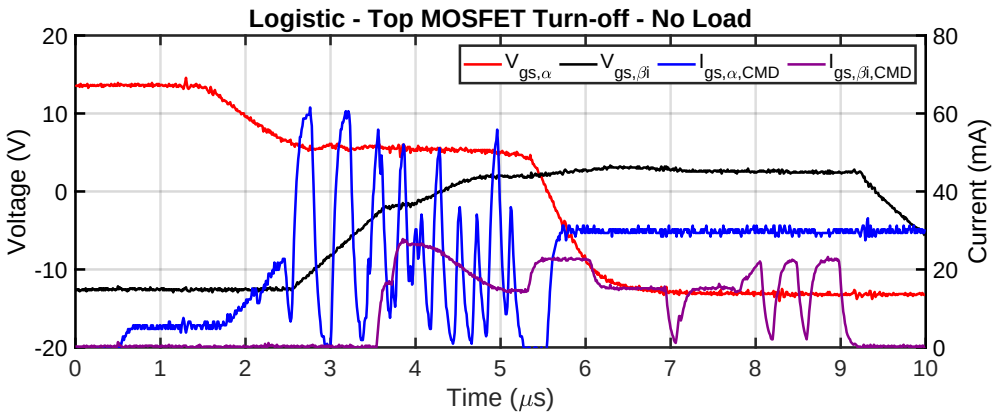



Figure A.2: Turn-off sequence for a logistic-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under no load.

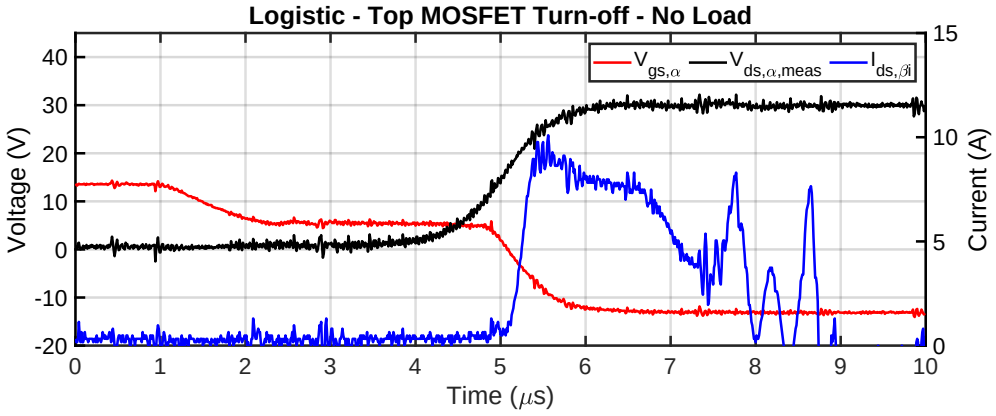



Figure A.3: Turn-off sequence for a logistic-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under no load.

### A.2.2 Logistic-Shaped Transition - Load

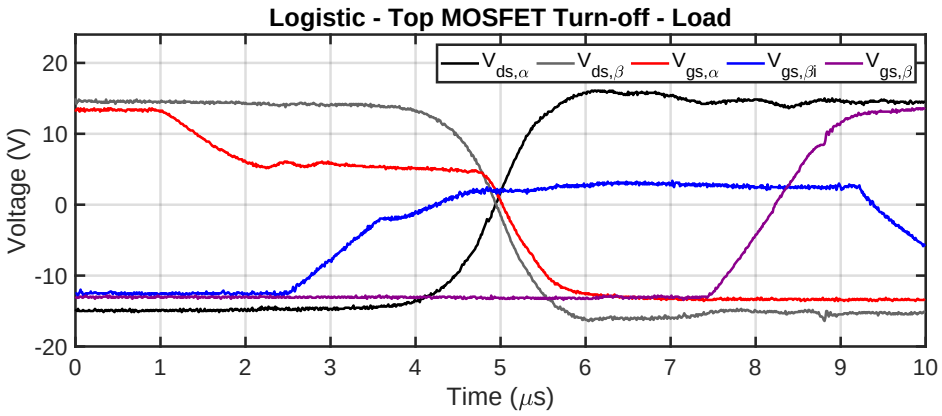



Figure A.4: Turn-off sequence for a logistic-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under load.

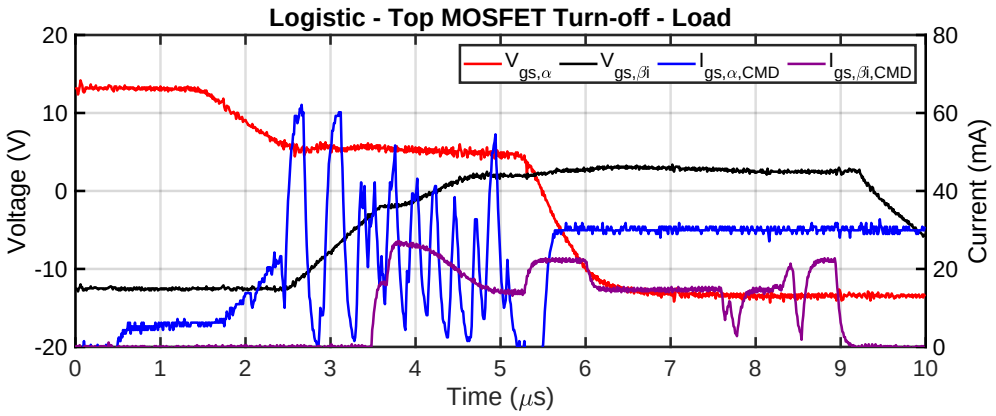



Figure A.5: Turn-off sequence for a logistic-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under load.

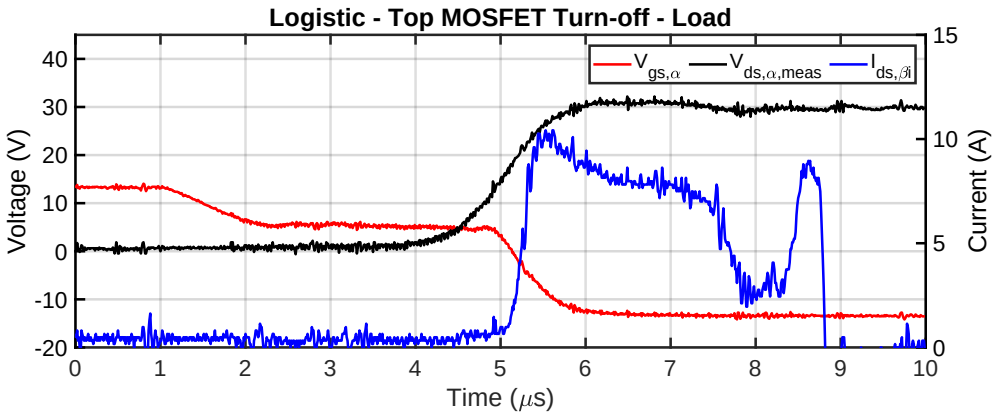



Figure A.6: Turn-off sequence for a logistic-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under load.

### A.2.3 Sinusoidal-Shaped Transition - No Load

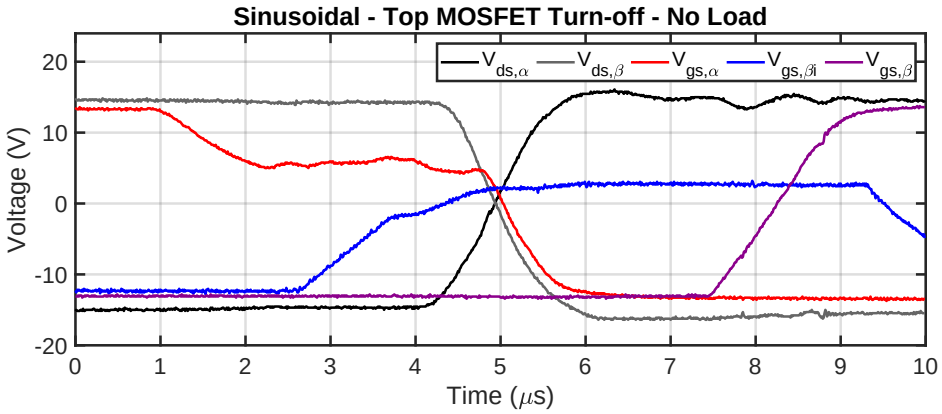



Figure A.7: Turn-off sequence for a sinusoidal-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under no load.

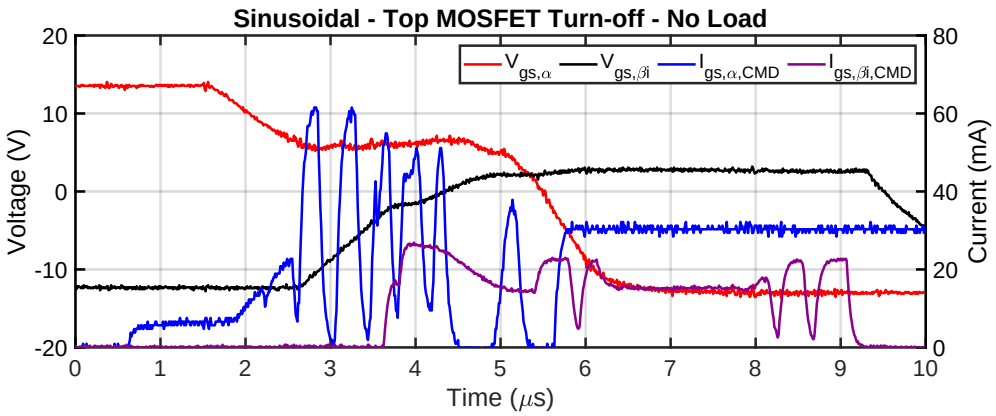



Figure A.8: Turn-off sequence for a sinusoidal-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under no load.

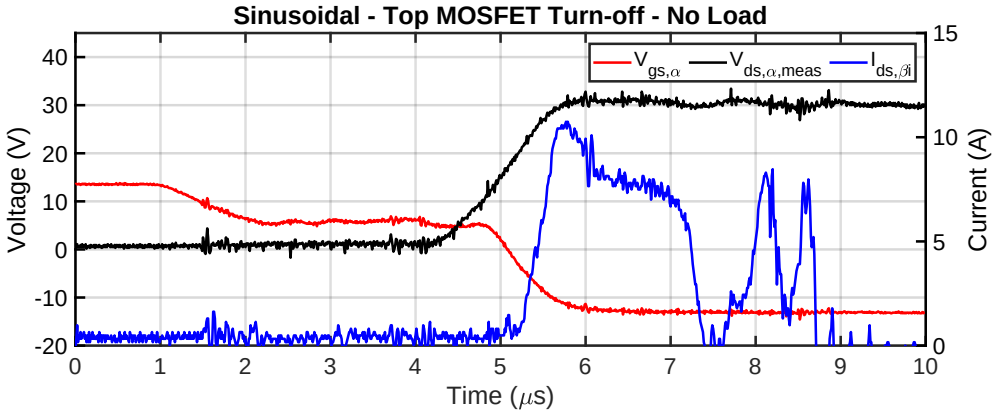



Figure A.9: Turn-off sequence for a sinusoidal-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under no load.

### A.2.4 Sinusoidal-Shaped Transition - Load

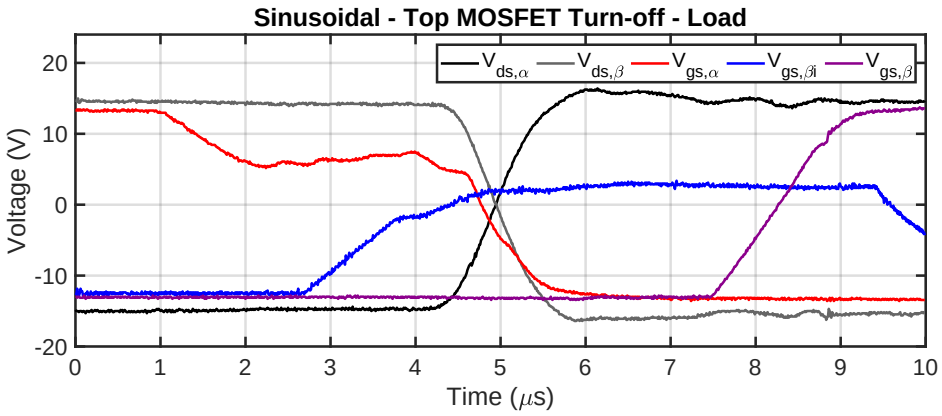



Figure A.10: Turn-off sequence for a sinusoidal-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under load.

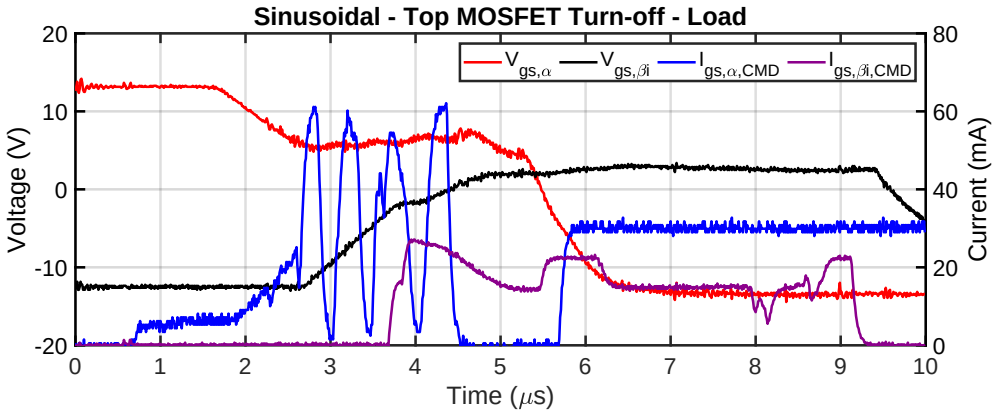



Figure A.11: Turn-off sequence for a sinusoidal-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under load.

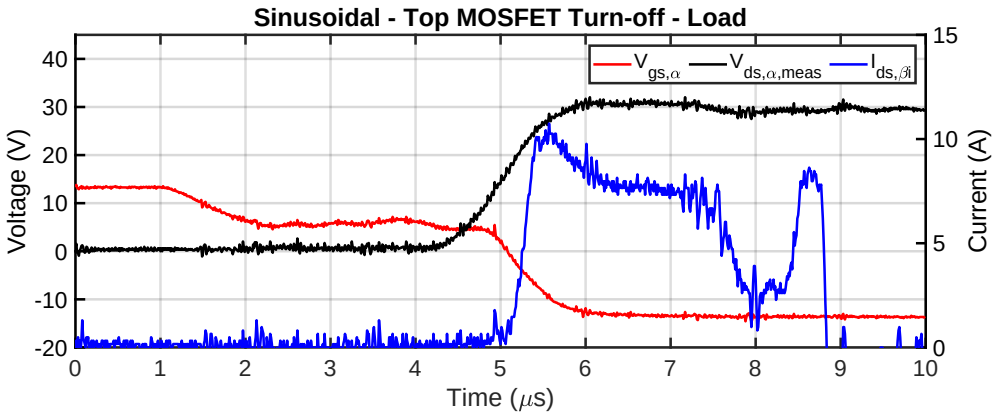



Figure A.12: Turn-off sequence for a sinusoidal-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under load.

### A.2.5 S-Shaped Transition - No Load

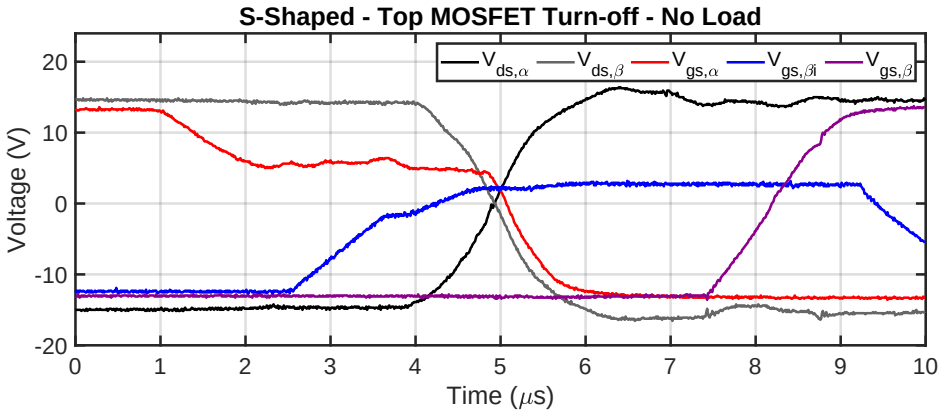



Figure A.13: Turn-off sequence for a S-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under no load.

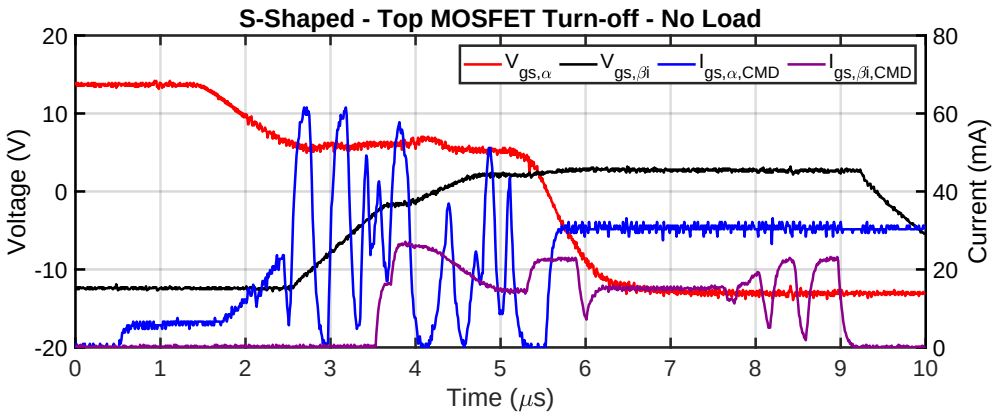



Figure A.14: Turn-off sequence for a S-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under no load.

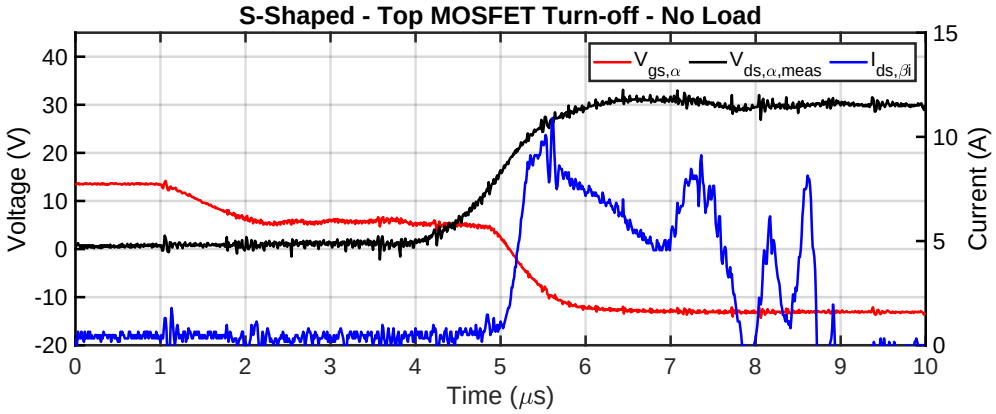



Figure A.15: Turn-off sequence for a S-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under no load.

### A.2.6 S-Shaped Transition - Load

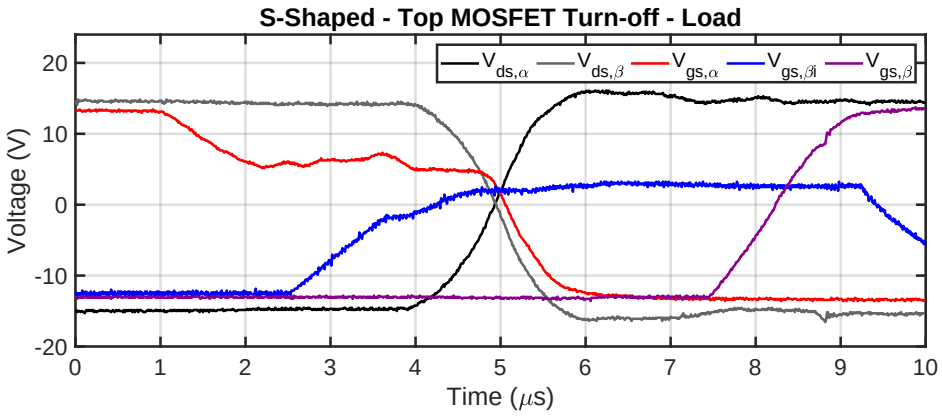



Figure A.16: Turn-off sequence for a S-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{ds}$ (black), $\beta$-MOSFET $v_{ds}$ (grey), $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (blue), and $\beta$-MOSFET $v_{gs}$ (purple) measurements. The half-bridge circuit is operating under load.

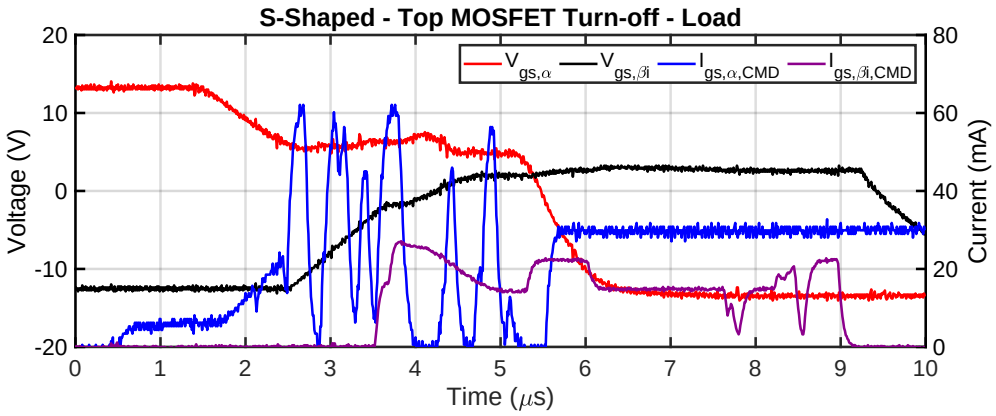



Figure A.17: Turn-off sequence for a S-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $v_{gs}$ (black), $\alpha$-MOSFET $i_{gs}$ command (blue), and $\beta$-injection MOSFET $i_{gs}$ command (purple) measurements. The half-bridge circuit is operating under load.

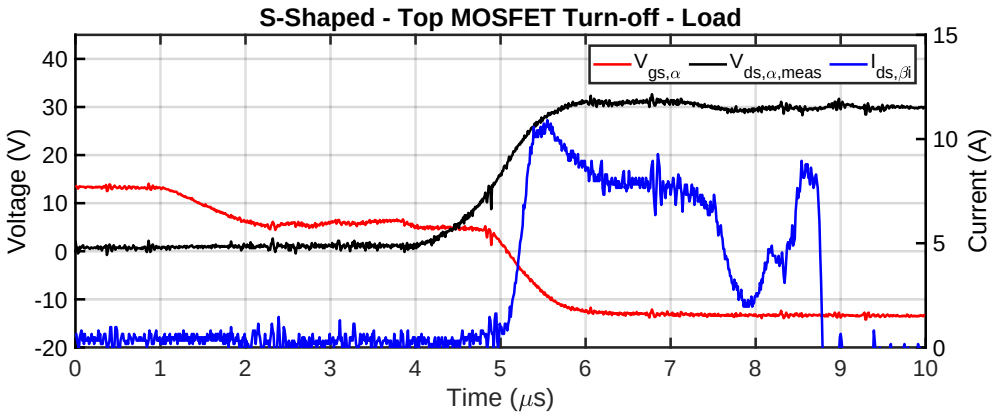



Figure A.18: Turn-off sequence for a S-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the $\alpha$-MOSFET $v_{gs}$ (red), $\beta$-injection MOSFET $i_{ds}$ (blue), and $\alpha$-MOSFET $v_{ds}$ (black) measurements. The half-bridge circuit is operating under load.

### A.2.7 Hard Switching

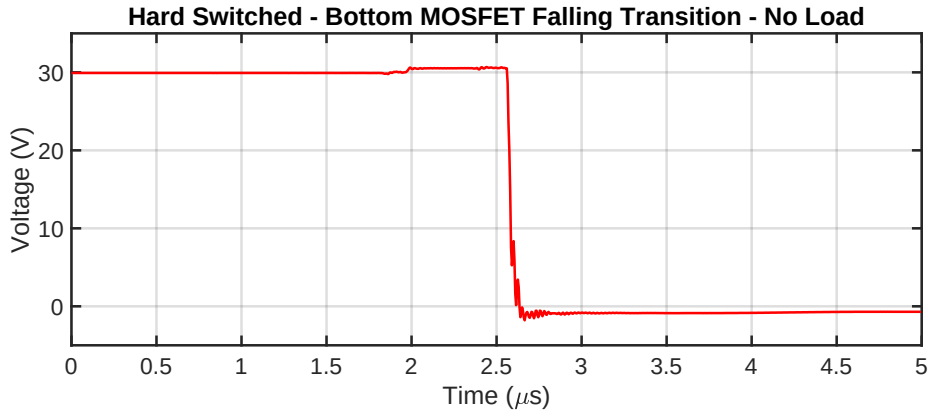



Figure A.19: Waveform averaging for a hard switching waveform when the top power MOSFET is the $\alpha$-MOSFET. The half-bridge circuit is operating under no load.

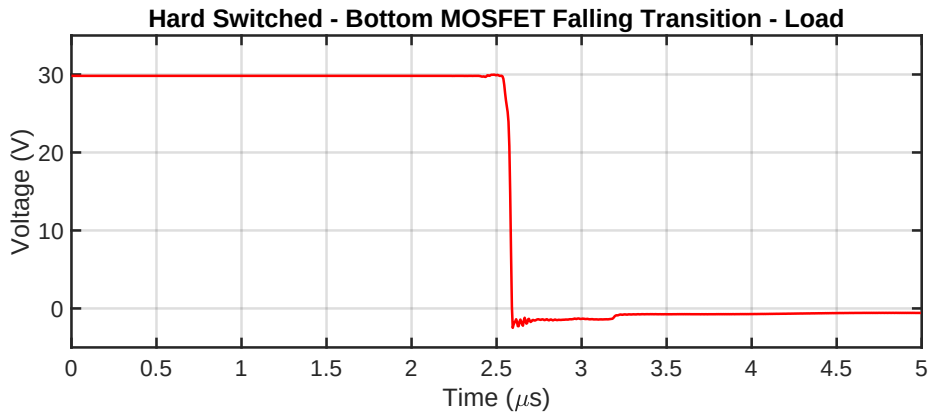



Figure A.20: Waveform averaging for a hard switching waveform when the top power MOSFET is the $\alpha$-MOSFET. The half-bridge circuit is operating under load.

## A.3 Waveform Averaging

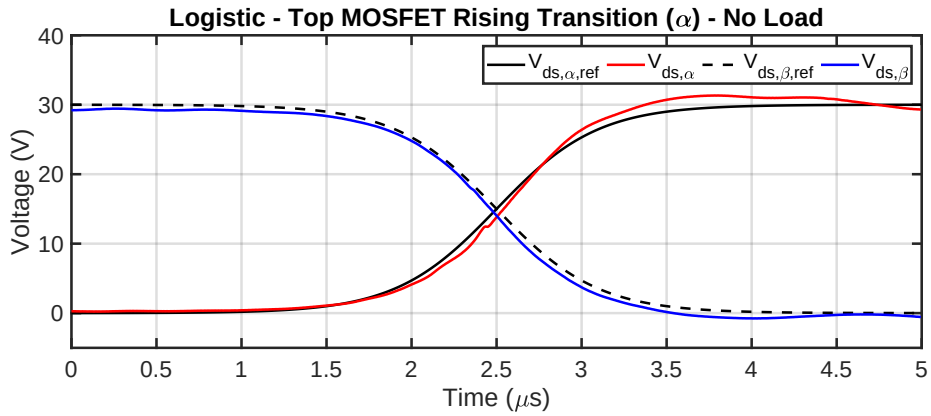



Figure A.21: Waveform averaging for a logistic-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines, respectively. The half-bridge circuit is operating under no load.

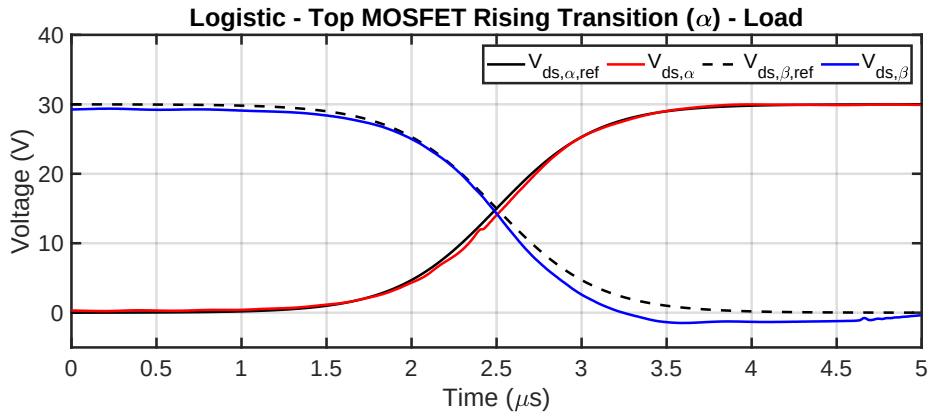



Figure A.22: Waveform averaging for a logistic-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines, respectively. The half-bridge circuit is operating under load.

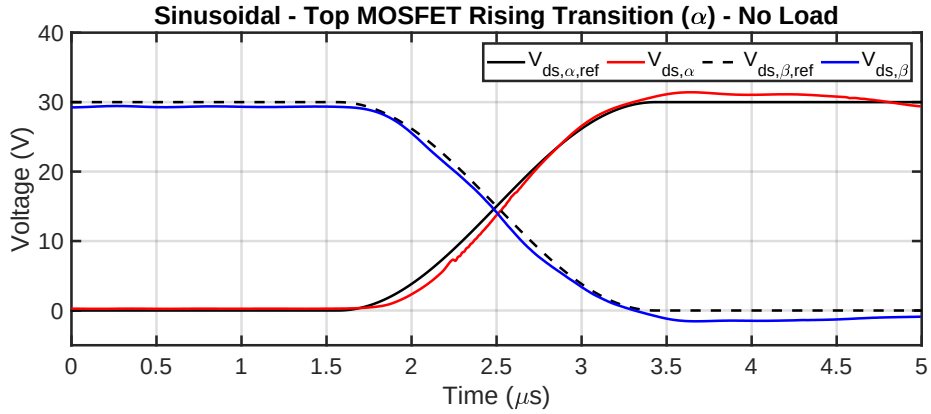



Figure A.23: Waveform averaging for a sinusoidal-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black-dashed lines respectively. The half-bridge circuit is operating under no load.

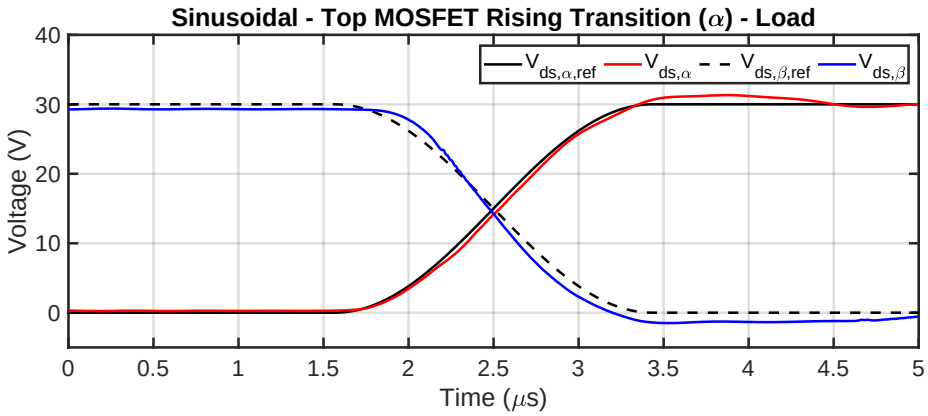



Figure A.24: Waveform averaging for a sinusoidal-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black- dashed lines respectively. The half-bridge circuit is operating under load.

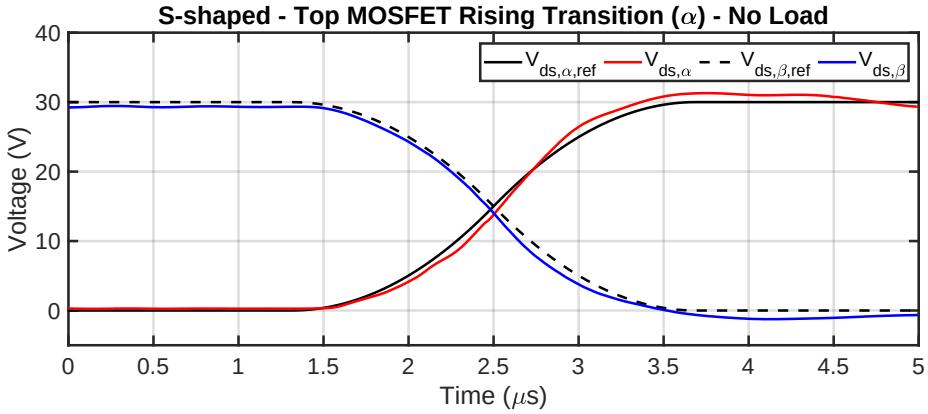



Figure A.25: Waveform averaging for a S-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black- dashed lines respectively. The half-bridge circuit is operating under no load.

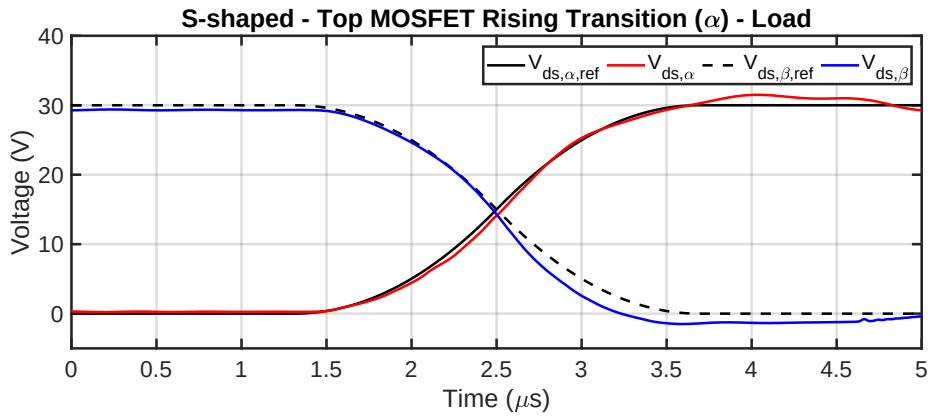



Figure A.26: Waveform averaging for a S-shaped reference waveform when the top power MOSFET is the $\alpha$-MOSFET. The plot shows the shows the $\alpha$-MOSFET $v_{ds}$ (red), $\beta$-MOSFET $v_{ds}$ (blue) with their reference waveforms shown by the black and black- dashed lines, respectively. The half-bridge circuit is operating under load.