Faculty of Engineering and Science

A New Topology of Cross-Switched Multilevel Inverter

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Doctor of Philosophy
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Declaration

To the best of my knowledge and belief, this thesis contains no material previously published by any other person except where due acknowledgment has been made.

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university.

Signature :

Date: 21st May 2022

List of Publications

1. “The new Topology of MLI with Reduced Number of Switches” in 2020 11th IEEE Control and System Graduate Research Colloquium
2. “The New Hybrid Multilevel Inverter with Reduced Number of Switches” in 2021 IEEE 11th International Conference on System Engineering and Technology

Abstract

Due to its importance in the power industry, multilevel inverter (MLI) is constantly researched for improvements. MLI that could produce a high level of output voltage with a reduced number of components is highly sought. The higher level of output will improve the THD percentage which eliminates the need for an output filter. The proposed topology was designed based on Cascaded H-Bridge (CHB)-MLI, Diode Clamped (DC)-MLI, and Cross Connected Source (CCS) – MLI. It consisted of 4 isolated DC sources, 4 diodes, and 10 switches. It can be configured with identical (symmetrical) and non-identical (asymmetrical) DC sources that resulted in 9-level, 13-level, and 17-level of voltage output. The proposed topology is also hybridized with H-MLI to produce 51-level of output. The proposed topology was verified with Matlab/Simulink simulation and supported by experimental testing. The testing was conducted in no-load and loading conditions with the modulation index, *m* equal to 1.0, 0.8, 0.5, and 0.3. The THD percentage (from simulation in loading conditions) produced by 9-level, 13-level, 17-level, and 51-level configurations is 10.21%, 7.83%, 6.42%, and 1.78%, respectively. The 51-level configuration was also implemented into a STATCOM as an example of an industrial application, and the operation was verified with simulation. Finally, the proposed topology was compared with the conventional MLIs and recently published MLI topologies. The outcomes concluded that the proposed topology uses a smaller number of components to generate a high level of output voltage, has a low THD percentage, and has a simpler structure. This study demonstrates that the proposed topology still has room for further improvements. Perhaps, in the future, the proposed topology can be cascaded to achieve a higher level of output voltage, or the dc-link capacitor can be introduced to reduce the dependency on the isolated DC sources.

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Table of Contents

Declaration……...i
List of Publication……...ii
Abstract……..iii
Acknowledgment……iv
Table of Contents…….....v
List of Figures……..viii
List of Tables…….xii
Abbreviation List……..xiv

Chapter 1: Introduction

1.1 Building Justification
1.1.1 The Research Field…….2
1.1.2 The Research Gaps…….3
1.1.3 Research Questions…….4
1.2 Objectives……..4
1.3 Outcome and Significance……..……..4
1.4 Ethical Issues…….5
1.5 Facilities and Resources……5
1.6 Data Storage……..5
1.7 Thesis Outline……6

Chapter 2: Literature Review on MLI, Modulation Techniques & STATCOM

2.1 Chapter Introduction….…….7
2.2 The Overview of Inverter……..7
2.2.1 The Two-level Inverter……...7
2.2.2 CHB-MLI……...8
2.2.3 FC-MLI……10
2.2.4 DC-MLI…….....14
2.2.5 CCS-MLI……..16
2.3 Modulation Techniques……...18
2.3.1 CB-PWM……..19
2.3.2 SV-PWM……..20

2.3.3 SHE……...22
2.3.4 Nearest Control Method……...23
2.4 STATCOM……..24
2.4.1 STATCOM Overview…...……...24
2.4.2 The Control Scheme…….25
2.5 Conclusion……26

Chapter 3: Research Methodology

3.1 Chapter Introduction ..…….28
3.2 Research Methodology…….....28
3.3 TI Control Suite and Code Composer Studio …….....31
3.4 Measuring Instruments……35
3.5 Conclusion..……..36

Chapter 4: The Proposed Topology & Hardware Implementation

4.1 Chapter Introduction…….....37
4.2 The Proposed Topology……...37
4.3 Hybrid Configuration …….40
4.4 The Proposed Topology Prototype……..42
4.5 Conclusion……...46

Chapter 5: Simulation and Experimental Results Analysis

5.1 Chapter Introduction……47
5.2 Simulation Analysis…….47
5.2.1 9-level Configuration ……...47
5.2.2 13-level Configuration…….....52
5.2.3 17-level Configuration.…….58
5.2.4 51-level Configuration…….....62
5.3 Experimental Testing Analysis…….....69
5.3.1 9-level Configuration…..……...70
5.3.2 13-level Configuration……..76
5.3.3 17-level Configuration...…….....83
5.3.4 51-level Configuration…….....90
5.4 Conclusion..……..98

Chapter 6: Comparative Analysis & STATCOM

6.1 Chapter Introduction..…….....100
6.2 Comparative Analysis ……100
6.2.1 Comparison with Conventional MLI……...100
6.2.2 Comparison with Recently Presented MLI…….104
6.3 STATCOM as an Example of Industrial Application …….....108
6.3.1 The Simulation Result ……....109
6.4 Conclusion……..112

Chapter 7: Conclusion & The Recommendation

7.1 Chapter Introduction……..113
7.2 Conclusion…….113
7.3 Recommendation & Improvement…….114

Reference

Appendix A
Appendix B
Appendix C
Appendix D

List of Figures

Chapter 2

Figure 2.1: The three phase two-level inverter……..... 8
Figure 2.2: H-MLI configuration…….……..... 9
Figure 2.3: The basic suggested MLI unit for topology presented in (Samsami, Taheru, & Samanbakhsh, 2017)……..... 10
Figure 2.4: Five-level capacitor clamped converter (Fujita, 2012)……..... 11
Figure 2.5: Circuit configuration per phase for n-level FC-MLI (Mochidate, Matsuo, Obara, & Sato, 2016)…….. 12
Figure 2.6: The presented topology in (Franquello, et al., 2008)…… 14
Figure 2.7: (Left) The type 1 and (Right) type 2…….. 15
Figure 2.8 : Topology presented in (Zolfaghar, Najafi, & Hasanzadeh, 2018)…… 16
Figure 2.8: A five-level CCS-MLI as being presented in (Gupta & Jain, 2014)……..... 17
Figure 2.9: The proposed CCS-MLI in (Dewangan, Gurjar, Ullah, & Zafar, 2014)……... 18
Figure 2.11: (a) Phase/in-phase disposition, (b) Alternative phase opposite disposition, and (c) Phase opposite disposition…… 20
Figure 2.12: The switching diagram for two-level inverter (Space Vector Modulation, 2017)……. 21
Figure 2.13: Multiple switching angle of PWM (Ahmadi, Zou, Li, Huang, & Wang, 2011)……. 22
Figure 2.14: The single-phase equivalent circuit of the STATCOM system (Subramaniam, Ramkumar, A.Amudha, & Kuppusamy, 2017)…… 25

Chapter 3

Figure 3.1: The NLC modulator setup…….. 29
Figure 3.2: The “xmakefilesetup” configuration…….. 31
Figure 3.3 (a-e): The parameter configuration……..... 32-34
Figure 3.4: The flow of switching signals…… 34
Figure 3.5: A photo of Fluke 43B (Fluke, 2001) ……. 35

Chapter 4

Figure 4.1: The proposed topology……. 38
Figure 4.2: The switching mode for (a) V_1+V_2, (b) V_2 , (c) – (V_1 + V_2), (d) -V_1 , and (e)-(f) zero state…….. 39
Figure 4.3: The hybrid configuration…… 41
Figure 4.4: The hardware prototype……..... 42
Figure 4.5: The experimental testing arrangement……... 43
Figure 4.6: The (a) the schematic diagram and,
(b) the actual photo (IRG4PH50UDPbF,2004)…… 43
Figure 4.7: The actual photo of DSP..…….. 44
Figure 4.8: The gate drives that are fixed onto interface board…… 45

Chapter 5

Figure 5.1: The simulation setup for 9-level configuration…….. 48
Figure 5.2: The switching pulses for S_1, S_2, S_9, S_5, and S_6…… 49
Figure 5.3: The output voltages for *m* = (a) 1, (b) 0.8, (c) 0.5,
and (d) 0.3…..... 49-50
Figure 5.4: The harmonic orders for *m* (a) 1.0, (b) 0.8,
(c) 0.5, and (d) 0.3……. 51
Figure 5.5: The simulation setup for the 13-level configuration…….. 53
Figure 5.6: The switching pulses for S_1, S_2, S_9, S_5, and S_6…… 54
Figure 5.7: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5
and (d) 0.3……. 54-55
Figure 5.8: The harmonic orders for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 56
Figure 5.9: The simulation setup for the 17-level configuration…….. 59
Figure 5.10: The switching pulses for S_1, S_2, S_9, S_5, and S_6 ……. 59
Figure 5.11: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 60-61
Figure 5.12: The harmonic orders for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 61

Figure 5.13: The switching pulse for S_1, S_2, S_9, S_5, S_6, S_{11}, and S_{13}…….. 64-65
Figure 5.14: The voltage trains from (a) Part A and Part B,
and (b) Part C…… 65
Figure 5.15: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 66-67
Figure 5.16: The harmonic orders when *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 68
Figure 5.17: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 70-71
Figure 5.18: The voltage THD percentages for m = (a) 1.0, (b) 0.8, (c)
0.5, and (d) 0.3…….. 72
Figure 5.19: The voltage output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 73-74
Figure 5.20: The voltage THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 75
Figure 5.21: The current THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 76
Figure 5.22: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 77-78
Figure 5.23: The voltage THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 78-79
Figure 5.24: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 80-81
Figure 5.25: The voltage THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 81-82
Figure 5.26: The current THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 83
Figure 5.27: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3…….. 84-85
Figure 5.28: The voltage THD percentages for *m* = (a) 1.0, (b) 0.8, (c)
0.5, and (d) 0.3…… 85-86
Figure 5.29: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5,
and (d) 0.3……. 87-88

Figure 5.30: The voltage THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3……. 88-89
Figure 5.31: The current THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3……. 90
Figure 5.32: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3……. 91-92
Figure 5.33: The voltage THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3……. 92-93
Figure 5.34: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3……. 94-95
Figure 5.35: The output voltages for *m* = 0.4 ……. 95
Figure 5.36: The THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, (d) 0.4, and (e) 0.3……. 96-97
Figure 5.37: The THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, (d) 0.4, and (e) 0.3……. 98

Chapter 6

Figure 6.1: The comparison between the number of components and the number of voltage output level for CHB-MLI, DC-MLI, FC-MLI, and the proposed topology……. 103
Figure 6.2: STATCOM simulation flowchart…..…… 109
Figure 6.3: The voltage and current waveform at source……..... 110
Figure 6.4: The THD percentage for voltage…… 110
Figure 6.5: The voltage and current at the load…… 110
Figure 6.6: The THD percentage for voltage…… 111
Figure 6.7: The current and voltage waveform at STATCOM…… 111

List of Tables

Chapter 2

Table 2.1: The comparison of total component counts
for five-level output…….. 17
Table 2.2: The switching state for two-level inverter……... 21

Chapter 4

Table 4.1: List of components to build the prototype……... 42
Table 4.2: The electronic components used to build gate drivers…… 45

Chapter 5

Table 5.1: The switching state for 9-level configuration…….. 48
Table 5.2: The parameters obtained from 9-level configuration…….. 51
Table 5.3: The mean current and voltage for every switch…….. 52
Table 5.4: The switching states for 13-level configuration……... 53
Table 5.5: The parameters obtained from this 13-level configuration…….. 57
Table 5.6: The mean current and voltage for every switch……... 57
Table 5.7: The switching states for 17-level configuration……... 58
Table 5.8: The parameters obtained from this 17-level configuration…….. 62
Table 5.9: The mean current and voltage for every switch……... 62
Table 5.10: The switching states for 51-level configuration……. 63-64
Table 5.11: The parameters from the 51-level configuration……... 68
Table 5.12: The mean current and voltage for every switch……. 69
Table 5.13: The comparison between simulation and experimental testing
for no-load condition……. 73

Table 5.14: The comparison between experimental testing and simulation for loading condition ……..... 75
Table 5.15: The comparison between simulation and experimental testing for no-load condition……. 79
Table 5.16: The comparison between experimental testing and simulation for loading condition ……..... 82
Table 5.17: The comparison between simulation and experimental testing for no-load condition……. 86
Table 5.18: The comparison between experimental testing and simulation for loading condition ……..... 89
Table 5.19: The comparison between simulation and experimental testing for no-load condition……. 93
5Table 5.20: The comparison between experimental testing and simulation for loading condition
……..... 97

Chapter 6

Table 6.1: The comparison between conventional MLIs and the proposed topology to produce 9-level of output voltage…….. 101
Table 6.2: The comparison between conventional MLIs and the proposed topology to produce 13-level of output voltage…… 101
Table 6.3: The comparison between conventional MLIs and the proposed topology to produce 17-level of output voltage…… 102
Table 6.4: The comparison between conventional MLIs and the proposed topology to produce 51-level of output voltage……..... 102
Table 6.5: Comparison between PT-9, (Mohapatra, et al., 2020), (Vineeth, Mukundam, & Jayaprakash, 2021), and (Abdulhamed & Dr. A. H. Esuri, 2021)……. 105
Table 6.6: Comparison between PT-17 and (Vineeth, Mukundam, & Jayaprakash, 2021)…… 106
Table 6.7: Comparison between PT-51, (Shankar, Edward, Kumar, & Raglend, 2017), (Hosseinzadeh, et al., 2019), and (Mondol, Biswas, Hosain, Samad, & Rahman, 2019)…… 107
Table 6.8: The parameters used in the simulation……. 109

Abbreviation List

RES	Renewable Energy Sources
GHG	Green House Gas
AC	Alternating Current
DC	Direct Current
MLI	Multilevel Inverter
CHB-MLI	Cascaded H-Bridge Multilevel Inverter
DC-MLI	Diode Clamped Multilevel Inverter
FC-MLI	Flying Capacitor Multilevel Inverter
CCS-MLI	Cross Connected Sources Based Multilevel Inverter
SV-PWM	Space Vector Pulse Width Modulation
CB-PWM	Carrier Based Pulse Width Modulation
SHE	Selective Harmonic Elimination
THD	Total Harmonic Distortion
V_{DC}/E	Source Voltage
PV	Photovoltaic
n	Number of levels
V_{ref} / V_{REF}	Reference voltage
V_C	Carrier Signal
f	frequency
F_{ref}	Reference Voltage
m	Modulation index
NLC	Nearest Level Control
PF	Power factor
VSC	Voltage Sourced Converter
V_C	STATCOM voltage
V_S	System voltage
i	Current
L	Inductor
R	Reactor
PCC	Point of Common Coupling
DSP	Digital Signal Processor

PCB	Printed Circuit Board
V_{FND}	Fundamental voltage
V_{RMS}	RMS voltage
V_{PH-PH}	Phase to phase voltage

Chapter 1: Introduction

Electrical energy has become the driving force for today's civilization and development. Generally, electrical energy is generated from (i) non-renewable sources (Non-RES) like fossil fuels, biomass, and nuclear energy; and (ii) renewable energy sources (RES) like solar, wind, geothermal and hydro. As the population growth and the demands escalated year by year, more power plants are built to cater to energy needs.

As the name suggested Non-RES are unsustainable, depleted in the long run, and believed to cause climate change. The increase in carbon footprint from the burning of hydrocarbon is one of the contributors to the increase in greenhouse gasses (GHG). The trapped GHG in the atmosphere results in climate change, specifically global warming that melts the ice caps in the arctic, increases the sea level, causes forest fires, as well as contributes to catastrophic and unpredictable weather change ("The Effect of Climate Change", 2021). It also cripples human health and economic growth making global warming no longer something that can be taken for granted. Hence, shifting to RES needs to be done promptly so that the environmental damage could be controlled, or at least be minimized.

Unlike Non-RES, RES is sustainable, clean, and not harmful to humans and the environment. Malaysia is a tropical country blessed with abundant RES, especially solar and hydro. According to (Sivaprasaad & Kumbhare, 2021, para. 9), RES is 18% of Malaysia's energy mix, with 86% of the capacity being dominated by hydropower. Unfortunately, the use of RES is still limited and less developed. A lot of studies need to be done to ensure RES deployment is a worthy investment for alternative energy sources.

Hence, to ensure RES is not an economic burden, it needs to be equipped with components that can fully utilize its potential. The inverter is one of the core components of RES power generation. It converts the direct current (DC) to alternating current (AC) so that it is usable to consumers. In addition, the output AC shall be as close as a sinusoidal waveform (i.e., ideal AC waveform) to produce a low harmonic or high power quality. A high harmonic AC reduces the system performance by increasing the power loss.

Before multilevel inverter (MLI) was introduced, a two-level inverter was used together with a step-up transformer and an output filter. The step-up transformer was required to step up the output to a suitable AC magnitude, while the filter was to filter harmonic. This design results in a bulkier system that is not preferable for medium to high voltage applications. On the other hand, MLI can produce a waveform greater than the two-level inverter and closer to a sinusoidal waveform. In addition, MLI also does not require a step-up transformer and output filter, which makes the system compact.

The first introduced MLI was Cascaded H-Bridge (CHB)-MLI, traced back to 1970 (Alishah, Nazarpour, Hosseini, & Sabahi, 2014). It produced higher output levels compared to a single H-Bridge that can only generate three output levels. It was followed by Diode Clamped (DC)-MLI which was introduced in 1980 and Flying Capacitor (FC)-MLI in 1990. These three early MLIs are grouped as 'conventional MLIs'. Conventional MLIs has gained instant fame and are widely used in low to high power application, including RES generation (Siddique, et al., 2020). However, researchers are still actively improving the conventional MLIs in the hope to extract a pure sinusoidal AC waveform.

1.1 Building Justification

1.1.1 The Research Field

Cross-connected sources based (CCS)-MLI is a type of recently established MLI that has some resemblance with CHB-MLI. As compared to CHB-MLI, CCS-MLI uses fewer components to produce the same level of output. Hence, the size of the CCS-MLI is smaller and the production cost is expected to be smaller. This study will propose a new topology that utilized the benefits of CHB-MLI, DC-MLI, and CCS-MLI. A simple mathematical equation will also introduce to predetermine the total level of output voltage. This figure will be referred to determine the switching sequence and the appropriate magnitude for DC sources.

MLI configurations that are commonly used are symmetrical configuration, asymmetrical configuration, and hybrid configuration. The symmetrical configuration uses similar DC sources whereas the asymmetrical configuration utilizes unequal DC sources. Meanwhile, the hybrid configuration is the combination of several MLI topologies. Using these configurations can help the proposed topology yield different levels of output voltage. In addition, asymmetrical and hybrid configurations can

increase the level of output voltage without increasing the number of components used (Gupta & Jain, 2014).

The modulation technique is a method used to synthesize AC waveform from the DC supply. The modulation techniques that are commonly used are carrier-based pulse width modulation (CB-PWM), space vector pulse width modulation (SV-PWM), selective harmonic elimination (SHE), and nearest level control. As modulation techniques could affect the quality of the synthesized outputs, the techniques that give the best quality of output will be chosen.

1.1.2 The Research Gaps

Component counts are one of the major concerns in building MLI as they can affect size, complexity, system losses, and production cost. Continuous studies have been done and over the years, a lot of MLI with a reduced number of components have been introduced. Most of the presented topologies are made up of fundamental units that can be cascaded to yield a higher level of output voltage and separated parts for level generation and polarity. Despite their ability to produce a higher level of output voltage and eliminates the need for a transformer, the number of components used is still considerably high. On the contrary, unidentical DC sources (i.e., asymmetrical configuration) and hybrid configuration can be utilized to increase the level of output voltage without drastically increasing the component counts.

Harmonic problem is also a challenge in building MLI. Since MLI is widely used for non-linear loads, harmonics is unavoidable. However, like other power quality issues, failure to compensate harmonics can severely affect the whole system. Therefore, it is important to keep the total harmonic distortion (THD) percentage within the limit stipulated by IEEE standards. Theoretically, the higher the level of output voltage, the lower the THD percentage. However, not all MLI can keep the THD percentage within the stipulated standard. Hence, it may require an output filter for power quality enhancements which will add to the system size.

Modulation techniques that are commonly used to synthesize MLI output included CB-PWM, SV-PWM, SHE, and nearest-level control. These techniques can affect the synthesized output positively and negatively. Some can help to improve the quality of the synthesized output (Jani & Kapil, 2016) and solve voltage imbalance problems (Kang, Lee, Jeon, Kim, & Hyun, 2005) but some may have a difficult computation, high voltage drops, and high power loss at the switching devices.

1.1.3 Research Questions

The research questions are listed as follows:

i. Does the proposed topology able to address the limitations of the conventional MLI in terms of the number of components and the total number of voltage output levels?
ii. Does the proposed topology able to produce a THD percentage less than 5% for the application below 69 kV?
iii. Does the proposed topology capable to be hybridized to produce a higher voltage output level without significantly increasing the number of components used?

1.2 Objectives

This study aims to develop a new MLI topology with better efficiency as compared to the existing MLI. The proposed topology is expected to have lower component counts for the sake of compact and simple design. It is also expected to produce a high level of output voltage to achieve an ideal AC waveform.

The specific objectives of this research study are outlined as follows:

1. To design and develop a new single-phase MLI topology based on DC-MLI and CCS-MLI with symmetrical, asymmetrical, and hybrid.
2. To discuss the results obtained from the testing in terms of total component counts, THD percentage, and total level of output voltage.
3. To perform a comparative study between the proposed topology and the conventional MLI as well as the MLI proposed recently by other researchers.

1.3 Outcome and Significance

The outcomes of this research work are as follows:

i. A new topology that utilizes the benefit of DC-MLI is proposed. As explained in the literature review, DC-MLI is the least explored MLI as compared to its other two counterparts though it gained fame in industrial. Thus, through this study, the disadvantages of DC-MLI will be improved.
ii. As this topology produces a high number of voltage output levels, the THD percentage is low or within the allowable limit set by the IEEE standard. Thus, there is no need for an output filter or transformer.

Then, the significance of this research is listed as follows:

i. The proposed topology will improve the power quality thus resulting in a remarkable increase in the reliability of the MLI.
ii. As the proposed topology uses fewer components, the MLI size will be more compact and simpler.
iii. Compared to CHB-MLI and FC-MLI, DC-MLI is the least developed despite its advantages. The proposed topology will maximize the benefits of DC-MLI and open the path for further exploration in DC-MLI.
iv. This study also can contribute to the study of RES in Malaysia's electricity generation as a part of the effort in reducing carbon footprint.

1.4 Ethical Issue

This research does not involve any ethical issues.

1.5 Facilities and Resources

The materials for this project will include the IGBT transistor (or MOSFET) module, diodes, resistive, capacitive, and inductive load, protection elements, electrical measuring instruments, oscilloscope, real-time interface board, and real-time digital signal processing unit. The power rating of electrical and electronic components is subject to the operating power. This prototype will undergo several experimental testings.

The experiment, testing, and troubleshooting will be done in the electrical engineering laboratory of Curtin University Malaysia. The equipment that might be needed includes DC-power supplies, voltage, and current probes, oscilloscopes, digital multimeters, and micro-box controller. The equipment is readily available in Curtin Malaysia.

1.6 Data Storage

The research data that is being collected will be kept in the Network drive of Curtin Malaysia and will be retained in compliance with the Curtin Data Management Plan and the Western Australian University Sector Disposal Authority with a minimum storage of five years after the thesis is published.

1.7 Thesis Outline

This thesis is organized into 7 chapters:

1. Chapter 1 (Introduction) lists the problem statements, objectives, and the novelty of the study.
2. Chapter 2 (Literature Review on MLI, Modulation Techniques, and STATCOM) presents a brief background and the recent studies related to the topics.
3. Chapter 3 (Research Methodology) presents the research methodology in detail, including software and measuring instruments that were being used.
4. Chapter 4 (The Proposed Topology & Hardware Implementation) presents the proposed topology and the proposed topology prototype.
5. Chapter 5 (Simulation and Experimental Result Analysis) analyses the results obtained from simulation and experimental testing.
6. Chapter 6 (Comparative Analysis & STATCOM) presents the comparative study between the proposed topology with the conventional MLI and the topology proposed in the last 10 years. It also presents the proposed topology implementation in STATCOM.
7. Chapter 7 concludes the study and suggests a few recommendations that can be done in the future.

Chapter 2:
Literature Review on Multilevel Inverter & Modulation Techniques

2.1 Chapter Introduction

This chapter gives a general knowledge of multilevel inverter (MLI), modulation techniques, and STATCOM. The inverter or MLI is used to convert DC input to AC output that is useable and the consumer side. The conventional MLIs are CHB-MLI, DC-MLI, and FC-MLI. Meanwhile, modulation techniques are methods used by the inverter to synthesize the AC output and STATCOM is an example of MLI application in the industry.

2.2 Inverter Overview

The ideal AC output is a smooth sinusoidal waveform. However, the MLI produces a staircase-like waveform. The ideal AC output is achievable by increasing the number of the staircase which subsequently will increase the THD percentage. Nevertheless, increasing the staircase may also increase the number of components used in building the MLI. This results in a bulkier, more complex, and more expensive MLI. Therefore, this study is conducted to propose an MLI topology that generates a high level of output voltage (i.e., the staircases) with a reduced number of components.

2.2.1 The Two-level Inverter

In the early years, a three-phase two-level inverter was used to produce an AC output. The general structure of this inverter is shown in Figure 2.1. This inverter produced a three-level of outputs, which are $-V_{DC}$, 0, and $+V_{DC}$. The output voltage was represented by a quasi-square waveform.

A quasi-square waveform is far from the ideal AC waveform, namely the sinusoidal waveform. High-frequency switching was introduced to smoothen the output waveform. However, this produces undesirable effects like high switching losses, high dv/dt, voltage doubling effect, and electromagnetic interference. In addition, the two-level inverter requires a step-up transformer and an output filter for grid integration to achieve the desired output voltage level and a better output (Blaabjerg, Chen, & Kjaer, 2004).

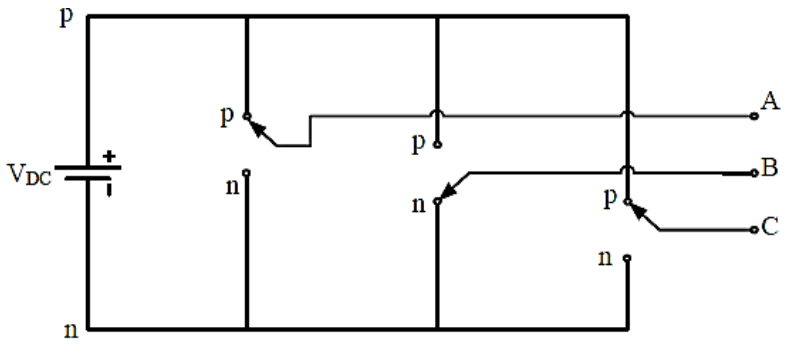


Figure 2.1: The three-phase two-level inverter

On the other hand, MLI produces a higher level of output voltage than the two-level inverter thanks to the increasing number of switches to share voltage stress. This results in the output waveform that is closer to the ideal waveform. The higher level of output voltage also increases the output quality. As a result, the step-up transformer and the output filter can be eliminated, and the switching frequency can be reduced to avoid severe electromagnetic interference to the system (Blaabjerg, Chen, & Kjaer, 2004; Welter, 1999).

The MLI gained instant fame especially in medium to high-voltage applications. High voltage applications might still need the transformer, but the size of this transformer is smaller than in the two-level inverter. Thus, the system is referred to as a 'transformerless' system (Agrawal & Jain, 2017).

2.2.2 CHB-MLI

CHB-MLI is a term given to the MLI structure with several H-MLI cascaded. Each H-MLI consists of a DC source and 4 switches (Matsumoto, Shibako, & Neba, 2016). The configuration is shown in Figure 2.2. The switches are divided into two parallel legs: the left leg (S_1 and S_3) and the right leg (S_2 and S_4). These series-connected switches are operating in a complementary manner in every switching cycle. Hence, an H-MLI can produce three-level of output voltage; $-V_{DC}$, 0, and $+V_{DC}$.

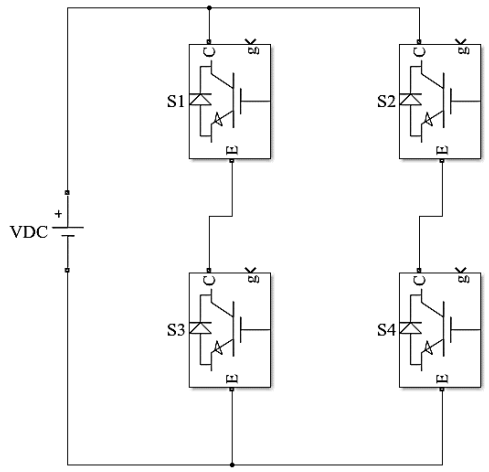


Figure 2.2: H-MLI configuration

The total level of the output voltage can be increased by cascading more H-MLI or by using unequal DC sources. The latter method is known as asymmetrical configuration. The commonly used DC sources ratio is binary (1:2) and trinary (1:3) (Raj, Dash, Dhatrak, & Nema, 2015). Asymmetrical configuration helps the MLI to achieve a higher level of output voltage without increasing the number of components used. For example, the trinary-CHB-MLI used lesser components than the binary and symmetrical configured CHB-MLI (Mohapatra, et al., 2020; Patel & Sood, 2020). Even so, not all topologies can support trinary configuration as some of the output voltage levels may be 'skipped' when synthesizing the output (Raj, Dash, Dhatrak, & Nema, 2015).

(Davis & Dey, 2016; Du, Tolbert, Ozpineci, & N.Chiasson, 2009) had suggested several examples of hybrid CHB-MLI. (Davis & Dey, 2016) suggested a hybrid of FC-MLI and CHB-MLI where FC-MLI helped in reducing the number of isolated DC sources. In return, CHB-MLI helped in mitigating the voltage imbalance in FC-MLI. However, this topology does not reduce the number of components used.

Isolated DC sources would not be an issue if the DC sources are abundant, for example in solar PV applications. The DC source can be represented by a PV module or a string of a PV module. The string is equipped with a dc-link capacitor. However, this application needs a dc-link capacitor control (Noman, Al-Sharmma'a, Addoweesh, Alabuljabbar, & Alolah, 2017). Hence, in the case where DC sources are limited, CHB-MLI will become less practical.

Numbers of MLI topologies have been proposed based on CHB-MLI topology for its output stability purpose, modularity, and cascading features (Abdulhamed, Esuri,

& Abodhir, 2021; Babaei, Laali, & Bayat, 2015; Nanda, et al., 2022; Muhammad, et al., 2017; Ponkumar, Rivera, & Kumar, 2017; Samsami, Taheru, & Samanbakhsh, 2017; S, Peddapati, & Naresh, 2020; Vineeth, Mukundam, & Jayaprakash, 2021). Generally, all these topologies consist of two parts: (i) the level generation part and (ii) the polarity part, as shown in Figure 2.3. A unit of H-MLI is normally used for the polarity part.

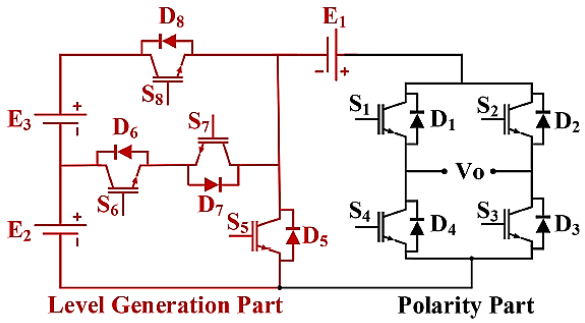


Figure 2.3: The basic suggested MLI unit for topology presented in (Samsami, Taheru, & Samanbakhsh, 2017)

As the name suggested, the level generation part generates the desired level of output voltage with a positive magnitude. Meanwhile, the polarity of the outputs is determined by the polarity part. Most of the presented topologies have a 'fundamental unit' that can be cascaded to yield a higher level of output voltage. Although these fundamental units have a reduced the number of components, the figure is still skyrocketed as the desired output level increase (Abdoli, Khorsandi, Ekandari, & Moghani, 2020; Babaei, Laali, & Bayat, 2015; Muhammad, et al., 2017; Ponkumar, Rivera, & Kumar, 2017; Samsami, Taheru, & Samanbakhsh, 2017).

Nevertheless, there is also topology with fixed designs for the level generation part like in (Nanda, et al., 2022; K., Pedapati, & Naresh, 2020; Vineeth, Mukundam, & Jayaprakash, 2021). These topologies normally have fixed levels of output voltage that they can achieve and are impractical to be cascaded. However, the level of output voltage can be increased by introducing asymmetrical configurations like in (Vineeth, Mukundam, & Jayaprakash, 2021).

(Barah & Bahera, 2021) has introduced a sub-multilevel structure that was derived from CHB-MLI. It consists of one DC source and two switches. The sub-multilevel structures need to be cascaded to achieve the desired level of output voltage.

This topology used lesser components than conventional CHB-MLI to produce the same level of output voltage.

2.2.3 FC-MLI

One of the disadvantages of using CHB-MLI is it requires multiple isolated DC sources to synthesize the output voltage level. As the level increases, the number of required DC sources will also increase. This increases the number of components and the complexity of the topology. Therefore, FC-MLI and DC-MLI are used to replace CHB-MLI when the availability of the DC sources is a concern. FC-MLI and DC-MLI used capacitors and diodes to maintain the voltage at presided voltage levels. In other words, they can use a single DC source and generate multiple output voltage levels by clamping the voltage.

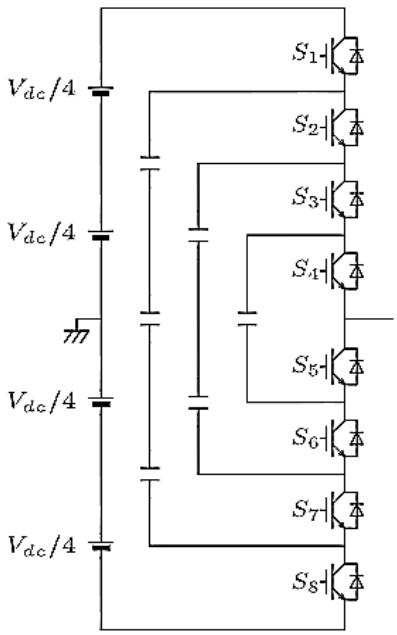


Figure 2.4: Five-level capacitor clamped converter (Fujita, 2012)

Figure 2.4 shows a typical five-level capacitor clamped inverter (Fujita, 2012). This converter can produce five-level of output voltage. Meanwhile, Figure 2.5 shows *n*-level FC-MLI. The numbers of power switches in the upper and lower half of the system are donated by (*n*-1), respectively. The (*n*-2) FC holds voltages that are varied by *E*/(*n*-1). The output voltage level is generated by combining the capacitor voltages and the source voltages which is by manipulating the switching state of the *2*(*n*-1) power devices (Mochidate, Matsuo, Obara, & Sato, 2016).

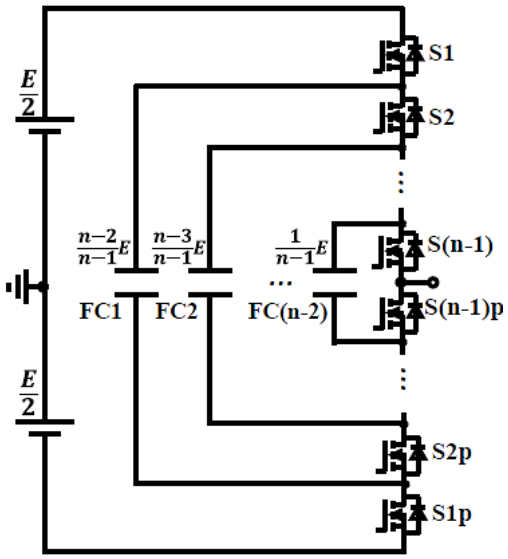


Figure 2.5: Circuit configuration per phase for n-level FC-MLI (Mochidate, Matsuo, Obara, & Sato, 2016)

As reported in (Amini & Abedini, 2013; Rohner, Bernet, Hiller, & Sommer, 2010), FC-MLI addresses DC-MLI and CHB-MLI limitations. Its design has eliminated the requirement for isolated DC sources and clamping diodes. Plus, it does not need a snubber circuit to function and has the very least loss among the three conventional MLIs. Furthermore, the presence of a large number of capacitors provides extra ride-through capability during system imperils (Amini, Viki, Radan, & Moallem, 2016).

However, the presence of capacitors will significantly increase the size of the system as the desired level of output voltage increases. This results in a bulkier and more complex topology. In addition, it is demanding to maintain the voltage of floating capacitors at the appropriate level. Due to these undesirable conditions, FC-MLI becomes less attractive in the power industry despite its admirable improvement (Amini, Viki, Radan, & Moallem, 2016; Ohmer, Kumar, & Surjan, 2020).

(Huang & Corzine, 2006) introduced a prototype of a three-cell inverter to minimize the component counts. This prototype used a redundant switching state to generate more voltage steps by a definite number of components. The prototype had successfully reduced the THD percentage and the switching loss, but the conduction losses were fairly constant. Despite the noticeable merits, this method is less attractive due to its complex control scheme.

Meanwhile in 2020, (Chen, Fong, & Loh, 2020) cascaded two FC-cells are being cascaded to build a novel five-level inverter for PV systems. This topology reduced the total number of capacitors used, discard the use of the high voltage-rating capacitor, and provide a solution for voltage imbalance. It has significantly reduced the number of components, but the application is limited to five-level of output.

The voltage imbalance problem in FC-MLI is due to the difficulty in fixing the capacitor voltage at the appropriate level (Muhammad, et al., 2017). This problem can be solved by (i) the open-loop control, and (ii) the closed-loop control (Amini, Viki, Radan, & Moallem, 2016).

(Feng, Liang, & Agelidis, 2007; Kang, Lee, Jeon, Kim, & Hyun, 2005) introduced a few examples of open-loop control. This method is said to be simpler than the closed-loop control but it has a poor dynamic response in transients and a high inductive load (Rohner, Bernet, Hiller, & Sommer, 2010). In order to improve the dynamic response, requires additional components that will subsequently increase the cost and the power loss. Moreover, all the power devices are required to have the same characteristics as the switching cells operating at a similar duty cycle. Since this ideal condition is hard to compromise, the open-loop method is hopeless when using unequal DC sources (Beig, Kumar, & Ranganathan, 2004).

The control scheme that was presented in (Choi & Saeedifard, 2012; Defay, Llor, & Fadel, 2010; Khazraei, Sepahvand, Corzine, & Ferdowsi, 2012) for the closed-loop control method provides better performance than the open-loop method. However, the operation becomes more complex and tangled when the system is expanded to a higher level. The complicated algorithm and look-up table also may be necessary for this method. (Amini, Viki, Radan, & Moallem, 2016) has proposed a reliable solution for this problem but the method is still complicated.

(Mochidate, Matsuo, Obara, & Sato, 2016) stated that the FC-MLI performance can be improved by manipulating the modulation technique. For such, voltage ripple can be mitigated by introducing a high switching frequency. In addition, FC-MLI is not only restricted to power industry use. (Modeer, et al., 2017) suggested FC-MLI's active involvement in the aircraft industry. A new design of FC-MLI with a low inductance layout has been proposed to increase the performance of FC-MLI in the aircraft industry.

2.2.4 DC-MLI

DC-MLI or also known as neutral point clamped (NPC)-MLI was first introduced in 1981 (Nabae, Takhashi, & Akagi, 1981). The structure of DC-MLI is inspired by the classical two-level inverter with the addition of a pair of semiconductors (Franquello, et al., 2008). The basic structure for the three-phase three-level DC-MLI is shown in Figure 2.6.

A pair of diodes is located in between the two switches. When the diode is reverse biased, the reverse bias voltage clamps the source voltage to generate the output voltage level. The diodes share the voltage stress with the switches when are in series with the applied voltage (Bhattacharya, Saha, Khan, & Nag, 2017; Boussada, Elbeji, & Benhamed, 2017).

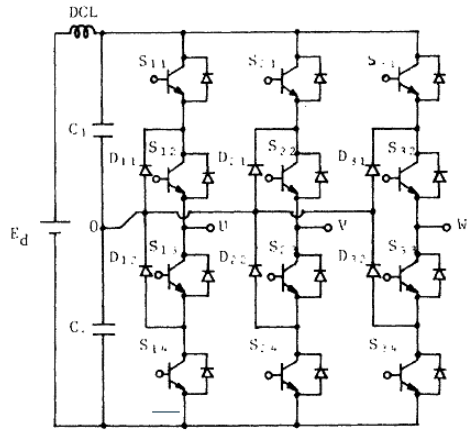


Figure 2.6: The presented topology in (Franquello, et al., 2008)

The perk of using DC-MLI is the voltage sources sharing among the existing phases. This eliminates the need for additional voltage sources. As the result, the topology is practical to be used in high voltage applications (HVA) and the capacitors also can be pre-charged as a group (Boussada, Elbeji, & Benhamed, 2017). In (Dave & Bhagdev, 2016), a comparison has been made between the CHB-MLI topologies presented in (Beig, Kumar, & Ranganathan, 2004; Cui, Ge, Zhou, & Yang, 2017; Kang, Park, Cho, & Cheul U-Kim, 2005; Valderrama-Blavi, M.Munoz-Ramirez, J.Maixe, & Calvente, 2005) with the DC-MLI. In their papers, the authors believed that voltage source sharing mitigates the need for cabling and power losses at the input side. This can improve the reliability of the system.

However, DC-MLI is far from perfect. Among the three conventional MLIs, DC-MLI uses the greatest number of components. The figure skyrocket as the desired

output level increases. This results in design, conduction, and switching losses. In addition, the voltage balancing problem might occur in a higher level DC-MLI (Wang, Kou, Liu, & Sen, 2017). Despite the superiority of common DC sources, DC-MLI is not feasible as the desired level of output voltage increases (Ohmer, Kumar, & Surjan, 2020).

(Cui, Ge, Zhou, & Yang, 2017) suggested several methods for voltage balancing. (Cui, Ge, Zhou, & Yang, 2017) classified the method into three types: using improved SV-PWM, using modified CB-PWM, and adding a voltage balance circuit. It can be concluded that the balance voltage can be achieved by modifying the modulation techniques that are used in the presented topologies (Lange & Piepenbreier, 2017; Li, et al., 2017; Tamasas, Saleh, Shaker, & Hammoda, 2017).

(Valderrama-Blavi, M.Munoz-Ramirez, J.Maixe, & Calvente, 2005) presented two DC-MLI topologies with a fewer number of components. The configuration is shown in Figure 2.7. The DC-MLI was coupled with FC-MLI to increase modularity and increase the level of output voltage. It is also believed to improve the voltage balance at the DC-link capacitor. Nevertheless, there is no significant improvement in the number of components and complexity.

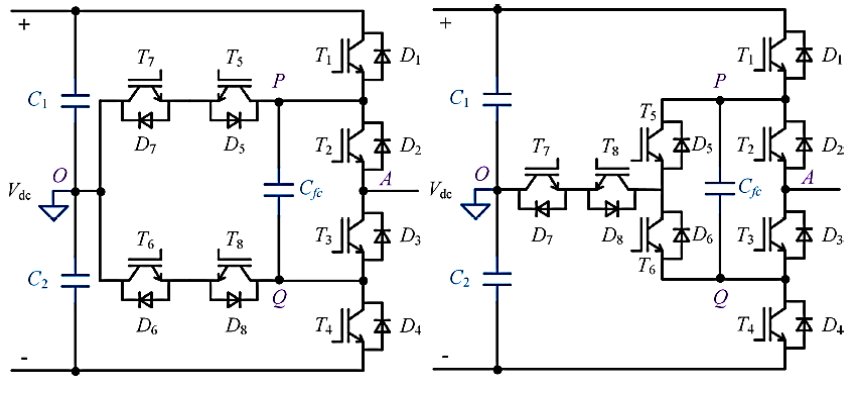


Figure 2.7: (Left) The type 1 and (Right) type 2

Examples of DC-MLI with a reduced number of components are suggested in (Zolfaghar, Najafi, & Hasanzadeh, 2018), (Goopta, Dhar, & Bhattacharya, 2020) and (Jacobo-Palmer, Garridor, Escobedo-Trujillo, & Revuelta-Acosta, 2021).

Topology presented in (Zolfaghar, Najafi, & Hasanzadeh, 2018) attached a unit H-MLI to the upper and the lower switch of DC-MLI as shown in Figure 2.8. The H-Bridge acted as a polarity changer. Since the presented topology is modular, it can be extended to yield a higher level of output voltage.

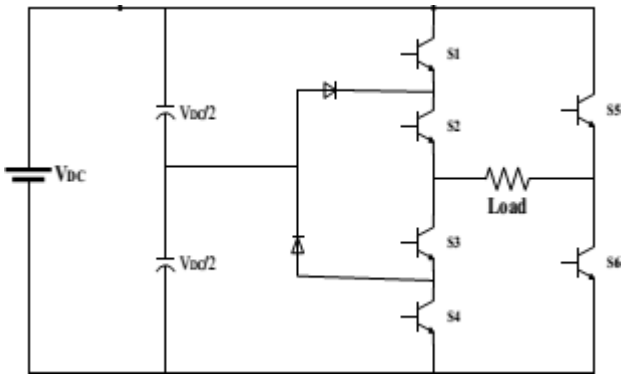


Figure 2.8 : Topology presented in (Zolfaghar, Najafi, & Hasanzadeh, 2018)

Topology in (Goopta, Dhar, & Bhattacharya, 2020) is divided into 2 portions; the upper portion is used for the positive level generation, and the lower portion for the negative level generation. Although it is proven to reduce the components, it may have a problem with voltage imbalance due to the DC-link capacitor.

Meanwhile, (Jacobo-Palmer, Garridor, Escobedo-Trujillo, & Revuelta-Acosta, 2021) used feedback diodes to reduce the number of components. The feedback diodes return the stored energy from the inductive loads to the sources instead of the switching gate. The drawback of this topology is the high number of isolated DC sources and the lack of flexibility.

2.2.5 CCS-MLI

Years later, (Gupta & Jain, 2014) presented CCS-MLI, a novel topology with reduced components. The name is given likewise due to the presence of floating input DC sources that connect the higher potential terminal of the preceding source to the lower potential of the succeeding sources. CCS-MLI had successfully addressed the disadvantage of conventional MLIs in terms of component counts. The topology also has a simple design (Gupta & Jain, 2014).

The CCS-MLI topology is illustrated in Figure 2.9. This topology produces five-level of output voltage which are, +2*E*, +*E*, 0, -*E*, and -2*E*. Similar to the H-bridge cell; the switches in each cell operate in a complementary manner to avoid short-circuit. Plus, the CCS-MLI structure also closely resembles CHB-MLI. They do not require any clamping devices and they can be cascaded to achieve a higher level of output voltage.

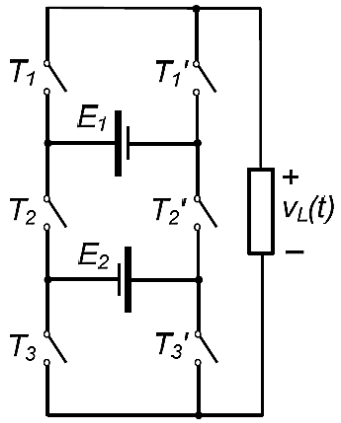


Figure 2.9: A five-level CCS-MLI as being presented in (Gupta & Jain, 2014)

CCS-MLI used fewer components than the other conventional MLIs. The comparison between the components used to produce a 5-level of output voltage between CCS-MLI and conventional MLIs is tabulated in Table 2.1. The number of components can be further reduced with the use of unequal DC sources or simply an asymmetrical configuration. However, using the asymmetrical configuration will eliminate the modularity of CCS-MLI. In this case, it is demanding to cascade. On the contrary, a symmetrical configuration can retain the modularity but the number of components will soar (Kangarlu, Babaei, & Sabahi, 2013).

Table 2.1: The comparison of total component counts for five-level output

Type of MLI / Components	**DC-MLI**	**FC-MLI**	**CHB-MLI**	**CCS-MLI**
No. of switches	24	24	24	18
No. of clamping diodes	16	0	0	0
No. of DC sources	4	4	6	6
No. of flying capacitor	0	18	0	0
Total component counts	88	70	54	42

(Dewangan, Gurjar, Ullah, & Zafar, 2014) has suggested a way to improvise CCS-MLI by adding the additional switches known as the bidirectional-conducting-unidirectional blocking (BCUB) and the bidirectional-conducting-bidirectional-blocking (BCBB). The configuration is shown in Figure 2.10. This topology is known as Level Doubling Network (LDN). It produced a 12-level of output voltage with less number of components than a standard CCS-MLI and the conventional MLIs.

However, this topology failed to reduce the number of DC sources. Plus, as the level increase, the link network will increase the complexity of the circuit.

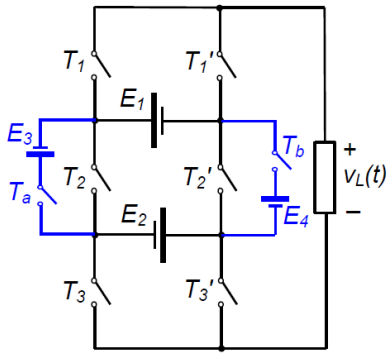


Figure 2.10: The proposed CCS-MLI in (Dewangan, Gurjar, Ullah, & Zafar, 2014)

Meanwhile, a new topology called Packed U-Cell (PUC) was also introduced in (Ounejjar, Al-Haddad, & Gregoire, 2011). This topology consists of DC sources and flying capacitors. It is said to be successfully reduced the number of components. PUC has almost a similar structure as CCS-MLI apart from the capacitors. Although PUC is a good candidate to reduce the component counts, its undesirable features like lack of modularity, disability to produce the summation of DC link voltage, difficulty to maintain the DC capacitors voltage as well as the high switch rating had significantly reduced the competency of PUC.

To improve the reliability of PUC, two crossed switches were added for DC input summation (Kangarlu, Babaei, & Sabahi, 2013). (Babadi, Salari, Mojibian, & Bina, 2017) suggested a topology that utilizes asymmetrical configuration and cascading features. This topology is said to be capable to address the limitations of PUC in (Ounejjar, Al-Haddad, & Gregoire, 2011). As compared to PUC, CCS-MLI is somehow more attractive as it has a simpler structure and a straightforward operation. A complex topology will be less attractive as it will indirectly increase the size and complexity of the inverter.

2.3 Modulation Techniques

Modulation techniques are methods used to synthesize the AC output from the DC input. Examples of modulation techniques that are commonly used are CB-PWM, SV-PWM, SHE, and Nearest Control Method. It is important to choose an appropriate modulation technique as it may affect the quality of the output.

2.3.1 CB-PWM

Generally, the gating signals of CB-PWM are generated by comparing the sinusoidal reference signal, V_{ref} with the carrier signal, V_c. The output frequency and the amplitude are given by the reference frequency, $F_{ref,}$ and the modulation index, m. There are three categories of modulation: (i) ideal modulation where m = 1, (ii) overmodulation where m>1, and (iii) undermodulation where m < 1. Overmodulation can help to boost the output voltage. However, this method is rarely used due to the presence of low-order harmonics. Meanwhile, undermodulation can deteriorate the reliability of the system.

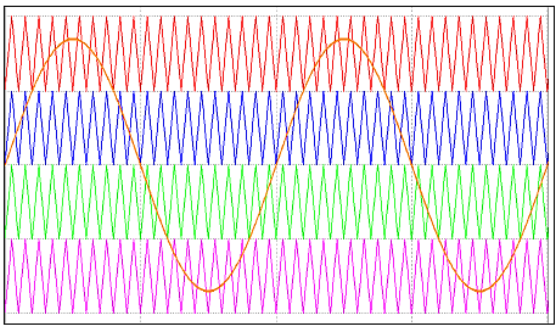
In general, an MLI with n-levels of output requires (n-1)V_c. The PWM can be generated either using analog control or digital control. However, digital control provides better stability, noise immunity, and flexibility.

CB-PWM can be further divided into phase-shifted modulation and level-shifted modulation. As for the phase-shifted modulation, V_c and V_{ref} have similar frequencies and peak-to-peak amplitude. The level-shifted modulation shared a similar trait. However, in phase-shifted modulation, a phase shift between any two adjacent V_c by φ_{cr} = 360°/(m-1) is required to determine the gating pulse.

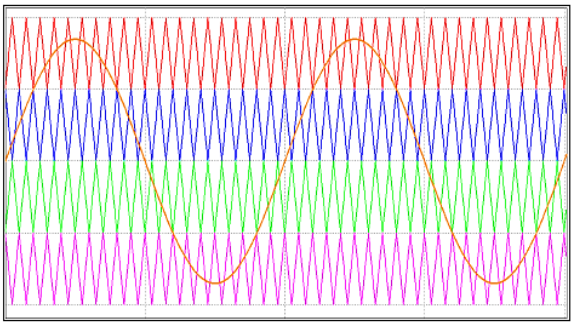
In level-shifted modulation, carrier signals are vertically disposed of such that the bands that they are occupied become contagious. There are three common types of level-shifted modulation namely;

i. Phase/in-phase disposition (PD): all the carrier signals are in phase.
ii. Alternative phase opposite disposition (APOD): all the carrier signals are alternatively in opposite disposition.
iii. Phase opposite disposition (POD): the carrier signals are opposite above the zero references and the zero references.

The gating pulse of level-shifted modulation is gained by comparing the reference signal, V_{ref} with the carrier signals, V_c. V_{ref} must be greater than V_c to generate a signal above zero references and vice versa for the signal below zero references. Figure 2.11 (a) to Figure 2.11 (c) show the different types of level-shifted modulation. The sinusoidal waveform indicates the V_{ref} whereas the multicolours triangular waveforms indicate V_c (Jani & Kapil, 2016).



(a)



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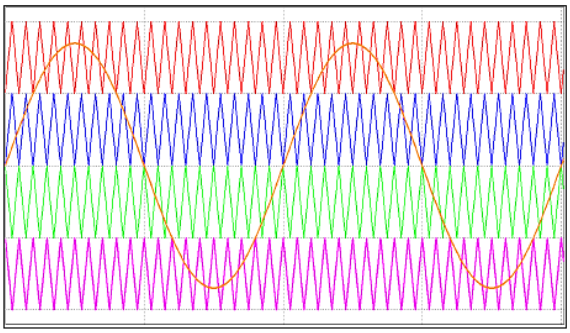


(c)

Figure 2.11: (a) Phase/in-phase disposition, (b) Alternative phase opposite disposition, and (c) Phase opposite disposition.

2.3.2 SV-PWM

SV-PWM is the most preferable real-time modulation technique. The switching state for SV-PWM is denoted by n^3 where n is the level of output voltage. For example, a two-level inverter will have a total of eight switching states. Six of the total states are considered active states or simply, the ON state. Meanwhile, the remaining two are known as the zero states or simply OFF states. The switching states of the two-level inverter are tabulated in Table 2.2. The zero states are given by [PPP]

or [OOO]. This redundancy can be utilized to minimize the switching frequency or to perform other functions.

Table 2.2: The switching state for a two-level inverter

Space vectors		Switching states
Zero vector	$\overrightarrow{V_O}$	[PPP] [OOO]
Active vectors	$\overrightarrow{V_1}$	[POO]
	$\overrightarrow{V_2}$	[PPO]
	$\overrightarrow{V_3}$	[OPO]
	$\overrightarrow{V_4}$	[OPP]
	$\overrightarrow{V_5}$	[OOP]
	$\overrightarrow{V_6}$	[POP]

. The switching diagram is shown in Figure 2.12. The active vectors form a regular hexagon with six equal vectors while the zero vectors lie at the center of the hexagon. Both active and zero vectors are stationary, and the switching state is determined by the reference voltage, V_{ref} rotation. Although SV-PWM is preferable in real-time modulation, this method is less favorable as it becomes more complex as the level of output voltage increases. Thus, it is only preferable for a low level of output voltage.

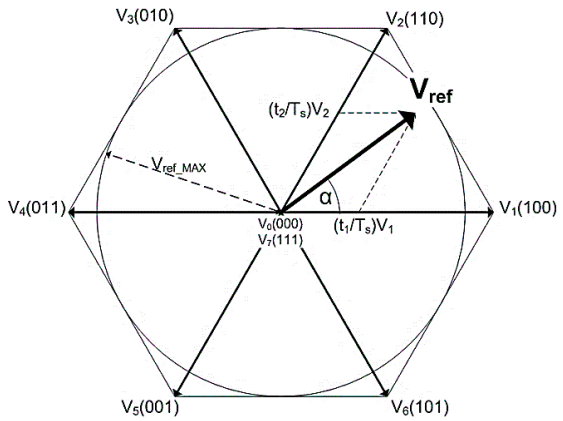


Figure 2.12: The switching diagram for a two-level inverter (Space Vector Modulation, 2017)

2.3.3 SHE

SHE is introduced to improve the quality of the classical pulse width modulation method. This idea was proposed by Turnbull in 1964. In this technique, harmonic components are explained in terms of switching angles in the trigonometric components. Figure 2.13 shows the switching angles of PWM (Ahmadi, Zou, Li, Huang, & Wang, 2011).

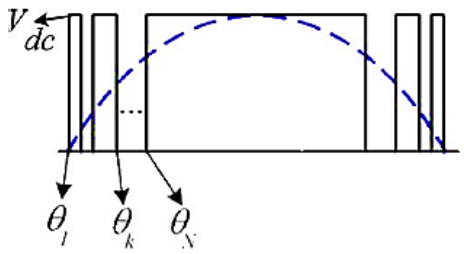


Figure 2.13: Multiple switching angles of PWM (Ahmadi, Zou, Li, Huang, & Wang, 2011)

While referring to Figure 2.13, given *S* is the total number of switching transitions, the Fourier series expansion of the PWM waveform can be expressed in (1);

$$V\ (\omega t) = \sum_{m=1,3,5}^{\infty} \frac{4V_{DC}}{m\pi}\ (\cos(m\theta_1) - \cos(m\theta_2) \ldots + \cos(m\theta_2)\sin(m\omega t) \qquad (1)$$

Where *m* is the order of the harmonics and θ_k are the k^{th} switching angle. A group of polynomial equations, such as (2) can be utilized to calculate the *N* switching angles. It also can realize the selective elimination up to m^{th} order of harmonics (Ahmadi, Zou, Li, Huang, & Wang, 2011). Hence, by calculating the *S* switching angles, *S*-1 number of harmonics can be eliminated. V_F in (2) is defined as the fundamental amplitude.

$$\begin{Bmatrix} \frac{4V_{DC}}{\pi}\ (\cos\theta_1 - \cos\theta_2 \ldots + \cos\theta_s) = V_F \\ \cos 5\theta_1 - \cos 5\theta_2 \ldots + \cos 5\theta_s = 0 \\ \cos 7\theta_1 - \cos 7\theta_2 \ldots + \cos 7\theta_s = 0 \\ \ldots \\ \cos m\theta_1 - \cos m\theta_2 \ldots + \cos m\theta_s = 0 \end{Bmatrix} \qquad (2)$$

However, the drawback of using SHE is the longer computation time to solve the transcendental equation as soft computing methods are used to obtain the optimized switching angle. It is demanding as it is not doable in real-time computation.

2.3.4 Nearest Control Method

The nearest control method is capable to cater the problem faced in SHE. The nearest control method can be classified into two types: (i) nearest vector control (NVC) and (ii) nearest level control (NLC). This technique operates with low fundamental frequency and produces less distorted output.

NVC is an advanced adaptation of SV-PWM with a similar logical approach with the switching pulses manipulated only based on the vector duration. Thus, NVC will generate pulses by comparing the reference vector position with the existing vectors. NLC shares a similar approach with NVC, but instead of comparing the vectors, NLC compares the actual output voltage level with the rounded reference output voltage level. The NLC computational is very straightforward and easier to be comprehended than NVC (Jonnala, Eluri, & Choppavarapu, 2016).

The nearest voltage level selection in NLC is based on the simple expression per phase. It is determined using (3) where V_{RN} is the nearest voltage level, V_{DC} is the voltage source, V_{ref} is the reference voltage, and *f-round* is the rounded function (Jonnala, Eluri, & Choppavarapu, 2016).

$$V_{RN} = V_{DC} \text{ x } f\text{-}round\ (V_{ref}) \tag{3}$$

The output voltage is rounded to the lower voltage level when the output voltage is less than 0.5. Meanwhile, when the output voltage is greater than 0.5 or equal; the voltage output is rounded to the nearest higher level. Hence, the power loss for this technique is equal to $0.5V_{DC}$. Despite its simple computational, NLC is only suitable to produce a level of output voltage as it cannot eliminate the low-order harmonics. The low-order harmonic is naturally eliminated when the level of the output voltage is high.

2.4 STATCOM

Static compensator or STATCOM is an example of MLI application. This section briefly explains STATCOM and its control scheme.

2.4.1 STATCOM Overview

The development in the power industry has increased the dependency on induction loads, induction motors, and power electronic devices. These devices have positive impacts on the power industry, but they also contribute to the power quality problem (Hingorani & Gyugyi, 2000; Tummakuri, Kasari, Das, & Chakraborti, 2018). Power quality problems like voltage imbalance, voltage sag/swell, harmonic distortion, flickering, and low power factor (PF) can reduce the systems' performance if left untreated (Lian-gui, 2016). Hence, they need to be swiftly compensated to maintain the reliability of the system at the optimum rate (Subramaniam, Ramkumar, Amudha, & Kuppusamy, 2017; Hui, 2014).

STATCOM is an advanced version of the VAR compensator. It was introduced in the 1990s. STATCOM is significantly different from the conventional VAR (i.e., thyristor switched capacitor (TSC), thyristor switched reactor (TSR), and the manually switched capacitor) as STATCOM does not have any rotating part. It is also equipped with a new generation high power force commutated semiconductor valve-based inverters, DC capacitors, and an output transformer. Other merits of STATCOM include quick and accurate dynamic response, minimum construction cost due to small size, wide operating range, high efficiency, and high decoupling ability (Haw, Dahidah, & Mariun, 2011). It is widely used for reactive power compensation, voltage regulation like in D-STATCOM, and harmonic compensation like in active power filters (Moran, Dixon, Espinoza, & Wallace, 1999; Pezeshki, .Arefi, Ledwich, & Wolfs, 2018; Zhu, Jiang, & Lian, 2011).

Generally, STATCOM is a shunt-connected voltage sourced converter or simply VSC (Subramaniam, Ramkumar, A.Amudha, & Kuppusamy, 2017) that is commonly used to control the reactive power in the power line; either by injecting or absorbing the reactive power (Kumar & Nagaraju, 2007; Rode, Gaigowal, & Patil, 2018). The single-phase equivalent circuit of a STATCOM is presented in Figure 2.14. From Figure 2.14, V_C is defined as the generated voltage of the STATCOM, V_S is the system voltage and i is the current drawn by the STATCOM. L and R are defined as the AC inductance and reactance, respectively (Sharma & Gidwani, 2018).

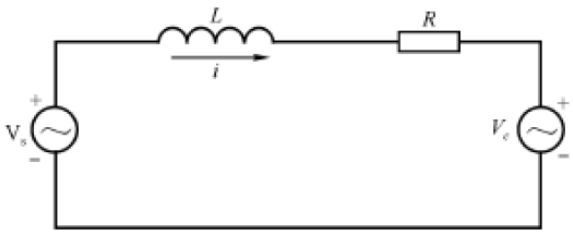


Figure 2.14: The single-phase equivalent circuit of the STATCOM system (Subramaniam, Ramkumar, A.Amudha, & Kuppusamy, 2017)

The STATCOM operation can be divided into 3 modes which are the capacitive mode, the inductive mode, and unity. When V_S is lower than V_C (i.e., the capacitive mode), the STATCOM will generate and inject reactive current into the electric line. On the contrary, when V_S is greater than V_C (i.e., the inductive mode), STATCOM will absorb the reactive current. The system is said to be in unity when V_S is equal to V_C. At this point, the net flow of reactive current is zero (Kadu, Jawale, & Muni, 2020; Sharma & Gidwani, 2018).

According to (Sharma & Gidwani, 2018), the first STATCOM manufactured in China was equipped with a multi-pulse inverter and zig-zag transformer. This technology is still widely used today. However, the credibility of the zig-zag transformer is questionable as the said transformer is bulky, high loss, spacy, and difficult to control.

The MLI's ability to produce a high level of output voltage has eliminated the need for a transformer. Furthermore, the MLIs' power quality improves as the level of output voltage increases. This also eliminates the need for the filter as the output enhancer. MLI is also convenient for STATCOM applications due to low semiconductor voltage stress, electromagnetic interference, and switching loss. These advantages made MLI for power systems and power quality enhancement applications like STATCOM. MLI-based STATCOM is convenient for high power applications (Gultekin & Ermis, 2013; Kangarlu, Babaei, & Sabahi, 2013; Kangarlu & Babaei, 2013).

2.4.2 The Control Scheme

STATCOM output voltage control method can be classified into (i) phase angle control where the phase angle is varied while the modulation index and pulse width modulated VSC are kept constant, and (ii) hybrid control where both phase angle and modulation index are varied (Chatterjee & Joshi, 2010).

The typical double loop method in (C.Schauder & Mehta, 2002) is an example of hybrid control. The two loops are the outer loop and the inner loop. The outer loop is responsible to give the desired active and reactive currents to the control point of common coupling (PCC). Meanwhile, the inner loop controls the inverter currents in zero steady-state error. This control scheme required a total of four PI controllers, resulting in a complex and demanding realization.

The direct output voltage (DOV) control that utilized only two PI controllers was introduced to reduce the former's complexity. This control scheme was designed based on the instantaneous power theory proposed by (Chen & Hsu, 2003). DOV can be divided into direct control and indirect control. For direct control, STATCOM utilizes a constant DC-link voltage that is high enough to produce output voltage at any desirable value. Meanwhile, the indirect control varies the magnitude of the output voltage by shifting the switching pattern to partially charge and discharge the DC-link capacitor.

Although this control method is less complex, dealing with the non-linear characteristics of the STATCOM like the accuracy and the speed of voltage control is demanding. Thus, more advanced controllers like fuzzy PI control scheme, particle swarm optimization based self-tuning PI control scheme, and genetic algorithm-based PI controlled were introduced (Ajami & Hosseini, 2006; Eshterhardiha, Poodeh, & Kiyoumarsi, 2007; Wang, Zheng, Li, Wang, & Yao, 2011).

Among the advanced method, particle swarm optimization has successfully achieved a satisfactory dynamic response under the balance load. In addition, the control strategy is simpler than the formal fuzzy approach. The strategy also does not depend on the evaluation function to determine the control gain. Instead, it used Runge-Kutta, a numerical method to specify the performance in real-time. Even so, the fuzzy method and particle swarm optimization require complex formulation that will be troublesome to deploy into DSP (Haw, Dahidah, & Almurib, 2014).

2.5 Conclusion

This literature study is to facilitate the understanding of MLIs. In this study, CHB-MLI, FC-MLI, and DC-MLI are regarded as conventional MLIs. They have their fair share of pros and cons, but their common limitation is the number of components used. In order to produce the output voltage close to the ideal waveform, the MLI must have the ability to produce a high level of output voltage. This will become a liability

to conventional MLIs. Therefore, a lot of new topologies had been proposed over the years to reduce the number of components.

The literature study also includes modulation techniques and STATCOM. Modulation techniques are used to synthesize the AC output from the DC input. Each technique has its pros and cons. It also can affect the reliability and complexity of the MLI. Meanwhile, STATCOM is an example of MLI application in the power industry. The topology proposed in this study will be implemented into a STATCOM to demonstrate its usability in the industry.

Chapter 3:
Research Methodology

3.1 Chapter Introduction

This chapter provides an outline of the research methodology to propose a new topology of cross-switched MLI. It includes the designing process, data collection process, data analysis techniques used, and the limitation of the chosen research method.

3.2 Research Methodology

The goal of this study is to propose a new MLI topology that is capable to produce a higher level of output voltage with a reduced number of components. These are the major concern in the MLI industry. Therefore, a depth understanding of MLI was created through a literature study. This process provided guidelines to design the proposed topology. The literature study also included modulation techniques and STATCOM that related to MLI.

The design was based on CHB-MLI, DC-MLI, and CCS-MLI. It used isolated DC sources like in CHB-MLI to eliminate voltage imbalance, clamping diodes like in DC-MLI, and cross-connected switches like in CCS-MLI to increase the level of output voltage with a reduced number of components. Plus, the use of isolated DC sources allowed the application of unequal DC sources. This method helped to further increase the level of output voltage. The designing process was carried out in Matlab/Simulink.

With the symmetrical (i.e., equal DC sources) and asymmetrical (i.e., unequal DC sources) configurations, the proposed topology yielded 9-level, 13-level, and 17-level of output voltage with only 18 components. This study also hybridized the proposed topology with a unit of H-MLI. The hybrid configuration used 23 components and produced a 51-level of voltage output.

The switching gate was generated using Nearest Level Control (NLC). This modulation technique was chosen due to its low switching and operating frequency (Siddique, Mekhilef, Shah, Tayyab, & Ansari, 2019). The NLC modulator setup is shown in Figure 3.1. The m is the modulation index, V_{DC} is the voltage supplied by the voltage source to the proposed topology and n is the total level of output voltage. The

modulator setup was used for all configurations. This modulator produced a normalized positive reference voltage that was rounded off to the nearest integer. The output was compared with the switching state of the respective configuration.

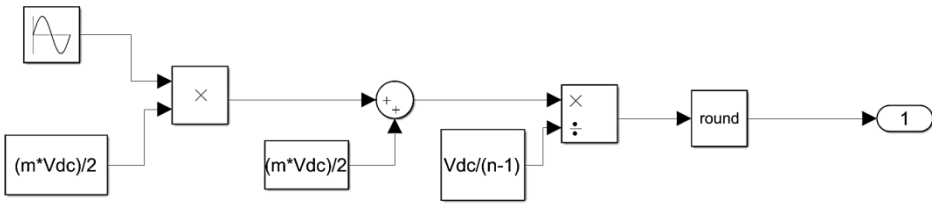


Figure 3.1: The NLC modulator setup

Once the design was completed, the proposed topology was simulated in Matlab/Simulink. The simulation was meant to observe the relationship between the THD percentage, the RMS voltage, and the number of voltage output levels with the modulation index, *m*. The simulation was conducted with voltage capped at 240 V (single-phase voltage) and at a power line frequency of 50 Hz. The proposed topology was verified in no-load condition and loading condition. For the loading condition, an inductive-resistive load of 217.4 Ω and 556.5 mH was added to the proposed topology. The value of *m* was set to 1.0 (the ideal modulation index), 0.8, 0.5, and 0.3.

The simulation result was supported by the experimental testing that was conducted in Curtin Electrical Power Laboratory. A prototype was built for this purpose. The experimental testing was conducted with the same conditions as the simulation, except that the capped voltage was stepped down for safety purposes. For 9-level, 13-level, and 17-level configurations, the voltage was stepped down to 24 V whereas, for the 51-level configuration, the voltage was stepped down to 37.5 V as it was difficult to distribute the voltage source evenly to get 24 V.

The experimental testing also required software like Code Composer Studio V5.5 and TI control suite. Code Composer Studio V5.5 and TI control suite were used to compile the switching pulse that was produced in Matlab/Simulink into a 'language' that is understandable by the prototype. The signal was uploaded into a DSP, that acted as the interface between the computer and the prototype. The process is explained in detail in the next section.

To ensure the switching pulse was successfully supplied to the switches, an oscilloscope was used to check the pulse waveform at all the switches. Once this was confirmed, the data collection was conducted immediately to ensure an accurate result.

Connecting the prototype to DSP and power supply for a long time can distort the voltage output. Thus, they were disconnected from the prototype after every testing. It is best to take the measurements as soon as possible.

The data obtained from the simulation and experimental testing were compared and analyzed. The simulation was repeated using the same capped voltage as the experimental testing. The simulation results were used as a reference as they were conducted in a controlled condition. However, it is impossible to get similar results as the inductive-reactive load, power supplies, power switches (IGBT), and DSP can cause external disturbances to the prototype. Hence, the performance of the proposed topology was determined by analyzing the output trend. Generally, the value of *m* affects the RMS voltage and the number of voltage output levels. Meanwhile, the THD percentage was solely affected by the number of voltage output levels. As the THD percentage reflects the quality of the MLI, the lower the THD percentage, the better the inverter.

However, if the experimental result does not have a similar trend as the simulation, there might be an error either in the circuit connection, switching pulse, or components failure. To solve this, all the possibilities of failure need to be checked. This process might require some time and is very meticulous. Thus it is important to adhere closely to the datasheets and ensure every component is functioning before building the prototype. Furthermore, be sure to practice proper working procedures while using the DC power supplies or measuring instruments to avoid accidentally damaging the components that are connected to them. Measuring instruments used in this study were oscilloscope, multilevel inverter, and Fluke 43B.

After the result analysis, the proposed topology was compared with a few MLI topologies presented recently and the conventional MLIs. The MLIs were compared in terms of the number of components, the total level of output voltage, and the THD percentage. This discussion is to demonstrate the novelty of the proposed topology. The proposed topology was also implemented into a STATCOM as an example of its industrial application.

3.3 TI Control Suite and Code Composer Studio

To proceed with the experimental testing, besides Matlab/Simulink, software like the TI control suite and Code Composer Studio were also required.

Code Composer Studio works as the mean of communication between the Matlab/Simulink and the DSP controller. It can be downloaded from the Texas Instruments website. There are several versions available, but for this testing, Code Composer Studio v5.5 was chosen. As for the Matlab/Simulink, Matlab/Simulink R2018a was chosen to be used in this study. The rationale for using version R2018a is that the later version can not execute some command like 'xmakefilesetup' that was needed to link Code Composer Studio to the Matlab/Simulink.

TI suite controller and Embedded Coder Support Package for TI C2000 were also required to link the Code Composer Studio to the Matlab/Simulink. TI Suite can be downloaded from the Texas Instruments website while the latter is available in Matlab/Simulink add-on. The process was done by executing the command 'xmakefilesetup' in the command prompt of Matlab as shown in Figure 3.2. This process was conducted with the DSP controller connected to the laptop.

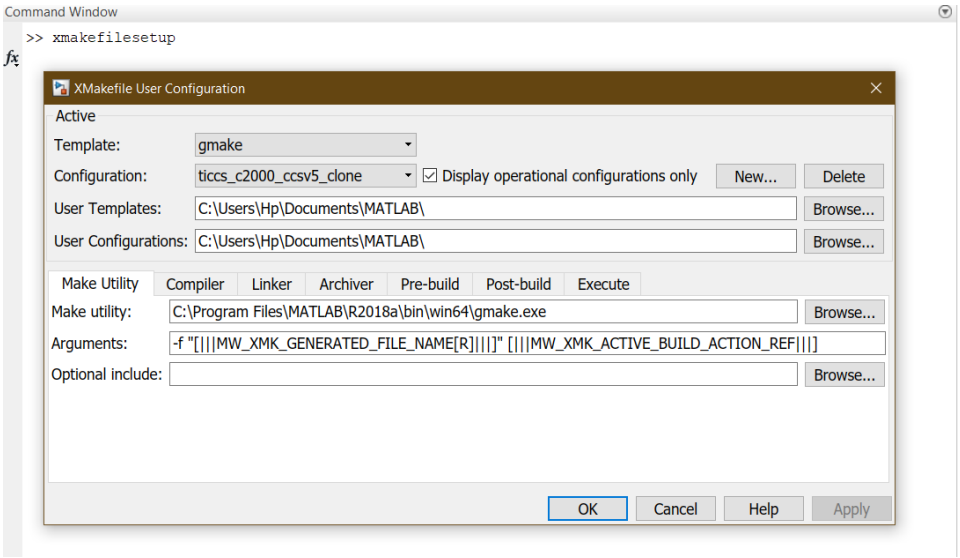
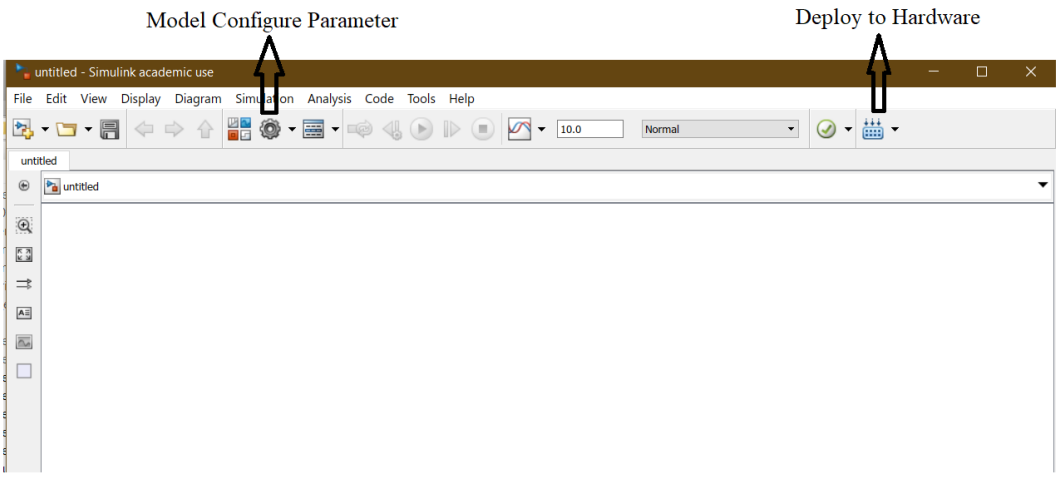


Figure 3.2: The "xmakefilesetup" configuration

Then, Simulink model parameters were configured according to the conditions required for the compilation in "Model Configuration Parameter" as shown in Figure 3.3 (a). The parameters were set according to the setup as shown in Figure 3.3 (b) – Figure (e).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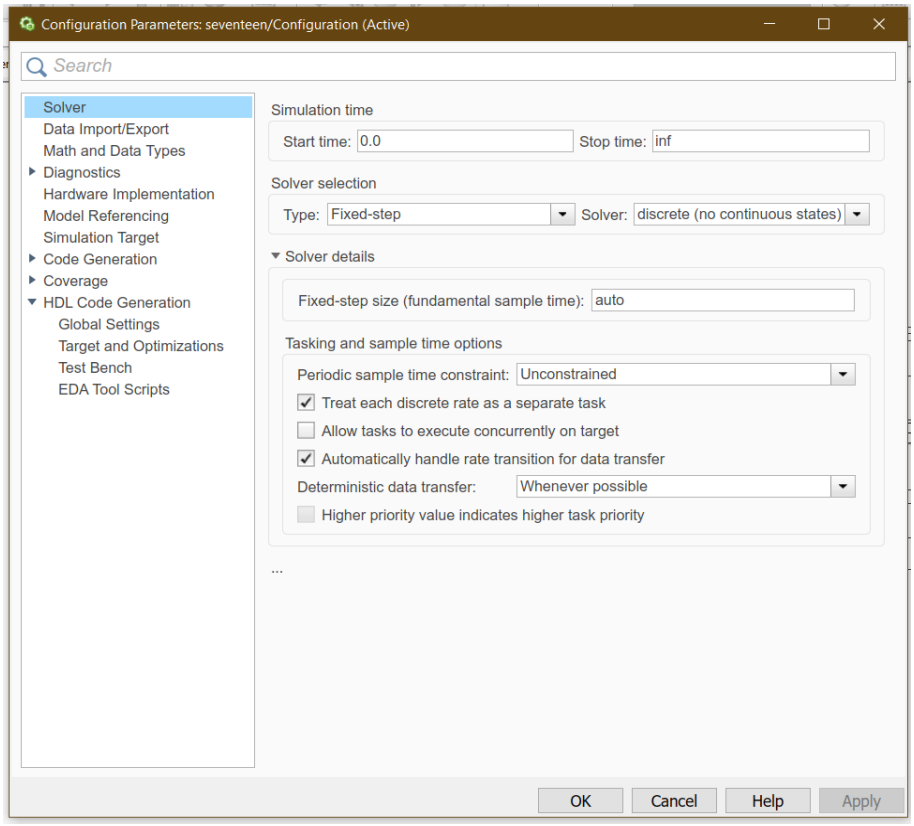
(a)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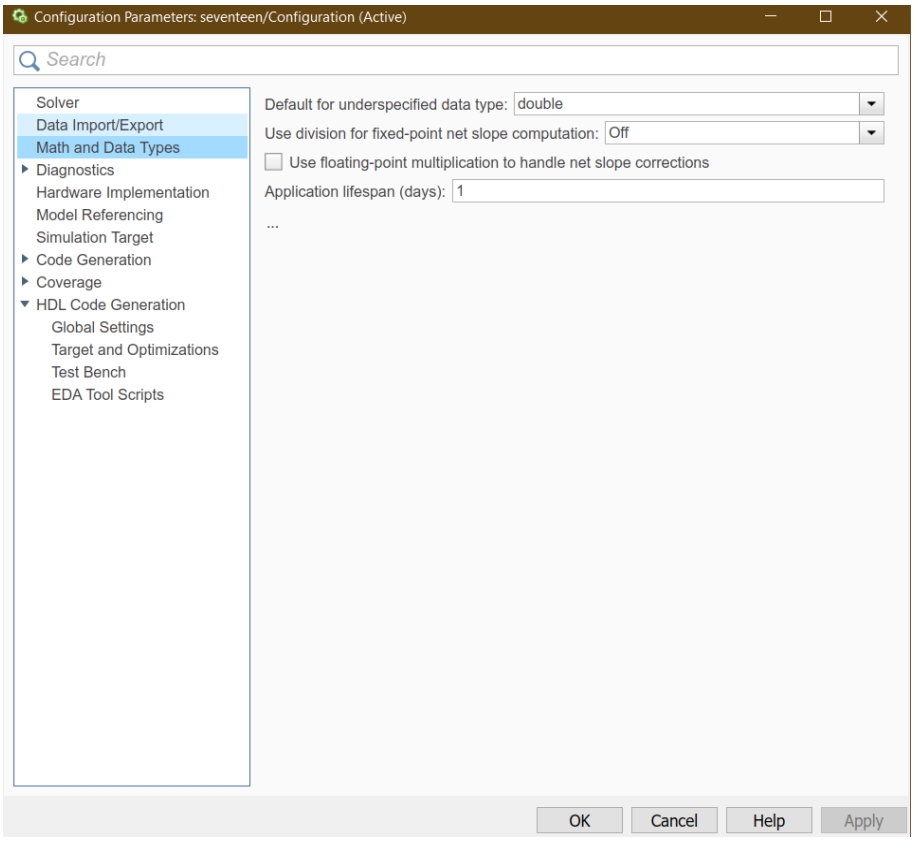
Solver
Data Import/Export
Math and Data Types
Diagnostics
Hardware Implementation
Model Referencing
Simulation Target
Code Generation
Coverage
HDL Code Generation
Global Settings
Target and Optimizations
Test Bench
EDA Tool Scripts
Simulation time
Start time: 0.0
Stop time: inf
Solver selection
Type: Fixed-step
Solver: discrete (no continuous states)
Solver details
Fixed-step size (fundamental sample time): auto
Tasking and sample time options
Periodic sample time constraint: Unconstrained
Treat each discrete rate as a separate task
Allow tasks to execute concurrently on target
Automatically handle rate transition for data transfer
Deterministic data transfer: Whenever possible
Higher priority value indicates higher task priority
...
OK
Cancel
Help
Apply

(b)


Configuration Parameters: seventeen/Configuration (Active)
Search
Solver
Data Import/Export
Math and Data Types
Diagnostics
Hardware Implementation
Model Referencing
Simulation Target
Code Generation
Coverage
HDL Code Generation
Global Settings
Target and Optimizations
Test Bench
EDA Tool Scripts
Default for underspecified data type: double
Use division for fixed-point net slope computation: Off
Use floating-point multiplication to handle net slope corrections
Application lifespan (days): 1
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OK
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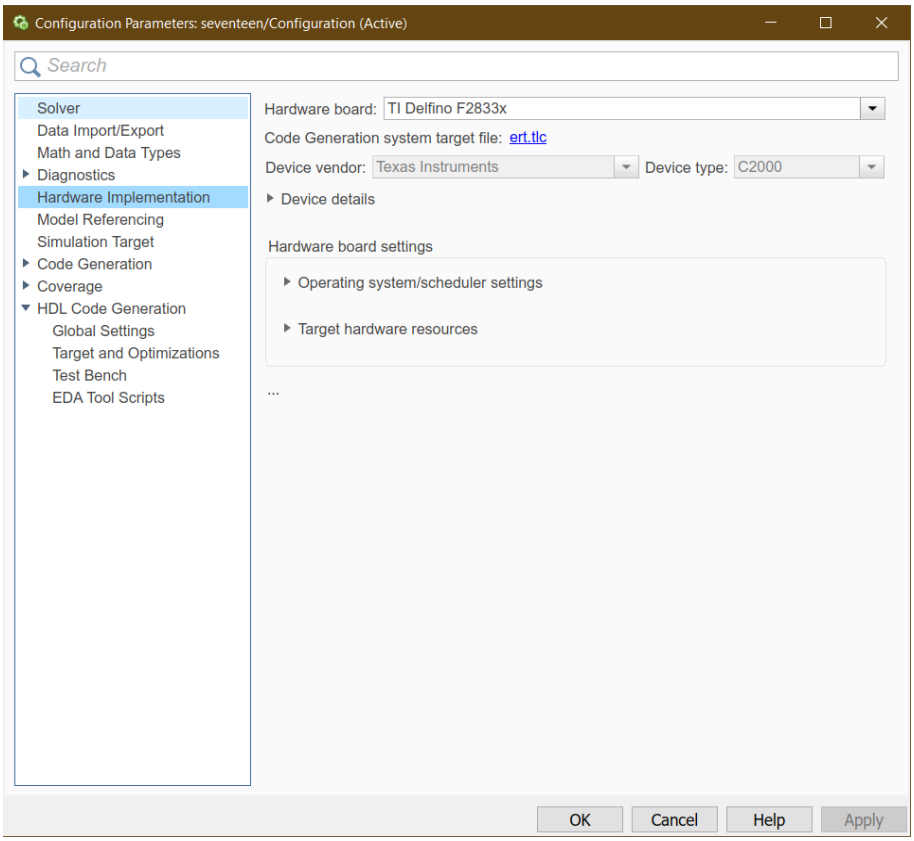
(c)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Diagnostics
Hardware Implementation
Model Referencing
Simulation Target
Code Generation
Coverage
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Target and Optimizations
Test Bench
EDA Tool Scripts
Hardware board: TI Delfino F2833x
Code Generation system target file: ert.tlc
Device vendor: Texas Instruments
Device type: C2000
Device details
Hardware board settings
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Target hardware resources
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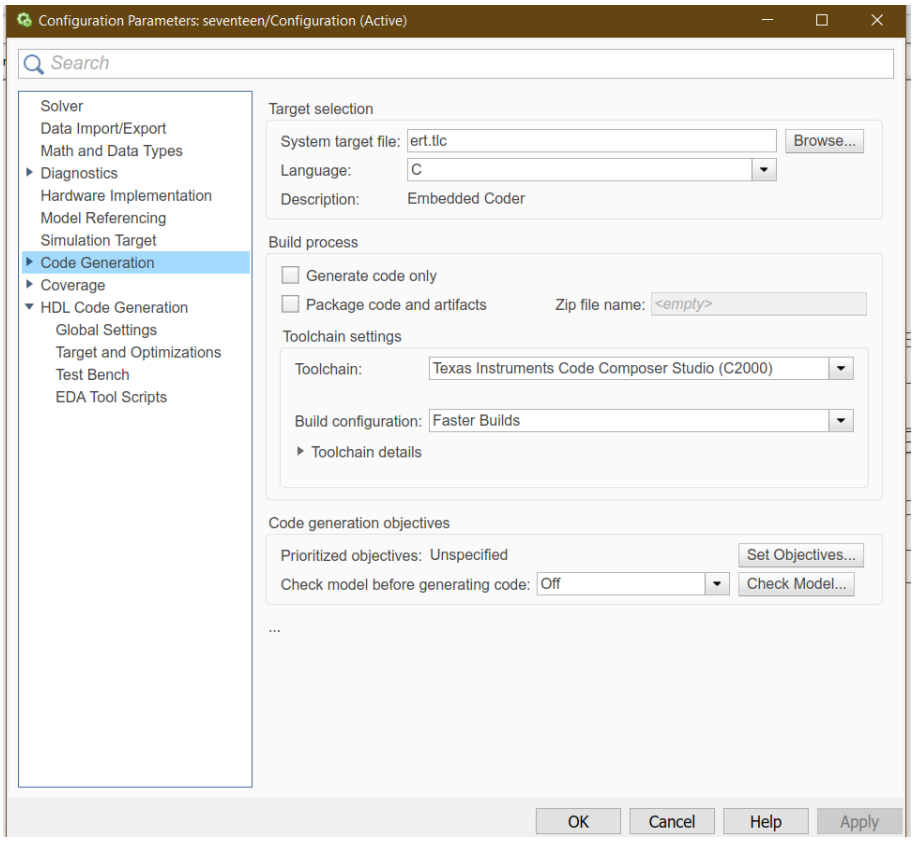
(d)



(e)

Figure 3.3 (a-e): The parameter configuration

By clicking the "Deploy to hardware", the switching pulses simulated in the Simulink model were converted into .OUT files. Briefly, the switching signals were generated in Matlab/Simulink, deployed into a Code Composer Studio, and finally uploaded into the DSP. Then, from the DSP, the switching signals fed into the gate driver that interfaced the control signal from DSP with the power switches. The process is summarized in Figure 3.4.

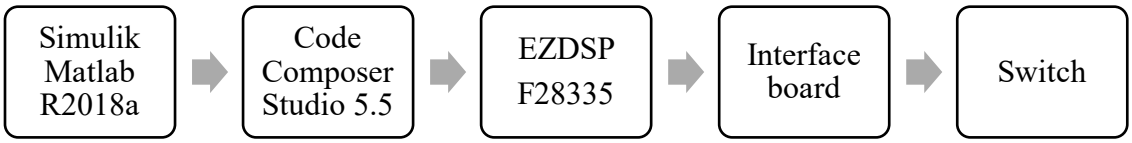


Figure 3.4 The flow of switching signal

3.4 Measuring Instruments

The parameters – (i) voltage and current THD percentage, (ii) the total level of output voltage, and (iii) the RMS voltage/current were measured using appropriate measuring instruments.

FLUKE 43B was used to measure THD percentage, RMS voltage/current, and frequency. FLUKE 43B is a hand-held power quality analyzer that works primarily to maintain power systems, troubleshoot power failures as well as diagnose equipment failures. It is equipped with FlukeView® software that can log harmonics and measurements in real-time and can be remotely viewed on a laptop (Fluke, 2001). Thus, it is easier to compile the recorded data for thesis writing. This device is also capable to act as an ordinary multimeter, however, it was not being used for that purpose. An actual photo of Fluke 43B is shown in Figure 3.5.

Figure 3.5: A photo of Fluke 43B (Fluke, 2001)

Notice that in Figure 3.5, there are two inputs labelled on the Fluke 43B Figure 3.5. This measuring device can measure the current and voltage simultaneously. This device requires current and voltage probes to interface it and the prototype to avoid damage. Meanwhile, the output waveform was recorded using a digital oscilloscope. The oscilloscope used was InfiniVision MSOX2012A from Keysight. The perk of using this type is the presence of a USB port, which is very convenient for data collection. In addition, it is also easy to handle. The oscilloscope was also used to check the switching pulse.

3.5 Conclusion

This chapter detailed the whole process taken to conduct this research study. The process includes a literature study, the designing phase, data collection, and data analysis. The designing process was carried out in Matlab/Simulink and the data were collected from simulation and experimental testing. Then, the data were analyzed to investigate the performance of the proposed topology. Then, the outcome was discussed and compared with the other topologies to demonstrate its novelty. This chapter also includes the process to execute switching signals to the prototype and the measuring tools used for collecting data.

Chapter 4:
The Proposed Topology & Hardware Implementation

4.1 Chapter Introduction

The proposed topology is aimed to increase the level of the output voltage by utilizing a lesser number of components. This chapter will detail the structure of the proposed topology as well as its operation. It also includes explanations of the proposed topology and H-MLI hybrid. This hybrid is believed to further increase the level of output voltage. As experimental testing was also required in evaluating the topology performance, this chapter also elaborates on the prototype structure.

4.2 The Proposed Topology

The proposed topology is shown in Figure 4.1. Generally, the topology is divided into two parts; Part A and Part B. Part A (lined in blue) and part B (lined in green) were designed based on DC-MLI structures. These parts are connected with a pair of floating switches S_9 and S_{10}, which were based on the cross-connected switches in CCS-MLI. The use of isolated DC sources, which were based on CHB-MLI, eliminates the voltage imbalance problem. It also made it easier for the proposed topology to be configured symmetrically and asymmetrically.

Since Part A and Part B are separated from each other, they produce their own 'voltage train' – a term used to explain the voltage output waveform. The voltage train depends on the voltage ratio assigned to the proposed topology. For example, in a symmetrical configuration, the ratio assigned to the proposed topology is 1:1. Hence, every DC source at Part A as well as Part B will be equal to the voltage at DC sources, V_{DC}. On the contrary, in an asymmetrical configuration, given the voltage ratio is 1:3, every DC source in Part A will be equal to V_{DC} and every DC source in Part B is equal to $3V_{DC}$. The total level of the output voltage is the summation of the voltage trains from Part A and Part B.

As for the switches, they are divided into upper legs; S_1, S_2, S_5, and S_6, and lower legs; S_3, S_4, S_7, and S_8. Switches in the upper legs and the lower legs operate in a complementary manner to avoid short-circuit. Similarly, the floating switches, S_9 and S_{10} are also operating in a complementary manner. S_2, S_3, S_6, and S_7 are also known as the "inner switch" that divides the total voltage sources at each part.

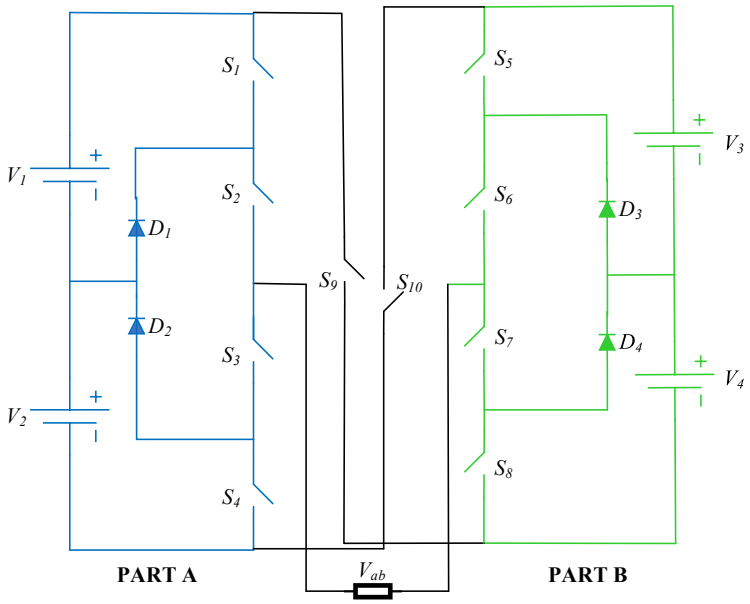


Figure 4.1: The proposed topology

$$n = 2h + 1 \tag{4}$$

Where;

n is the total number of output voltage level

h is the summation of V_{DC}

The total number of output voltage levels can be calculated using (4). The value of h is the summation of V_{DC} – for example in a symmetrical configuration, the summation is $V_{DC} + V_{DC} + V_{DC} + V_{DC} = 4V_{DC}$. Hence, $h = 4$. The value of h is multiplied by 2 as the output voltages produced by the proposed topology exist in both positive and negative waveforms. Meanwhile, '1' refers to the zero-state level. By using (1), the proposed topology is expected to produce 9-level, 13-level, and 17-level of output voltage under symmetrical and asymmetrical configurations.

The switching operation can be divided into 5 modes of operation, which are (i) V_1+V_2, (ii) V_2, (iii) 0, (iv) – ($V_1 + V_2$), and (v) -V_1. The modes of operation are presented in Figure 4.2 (a) to Figure 4.2 (f). These are taken from Part A for the topology shown in Figure 4.1. Since part B has similar switching operations as Part A.

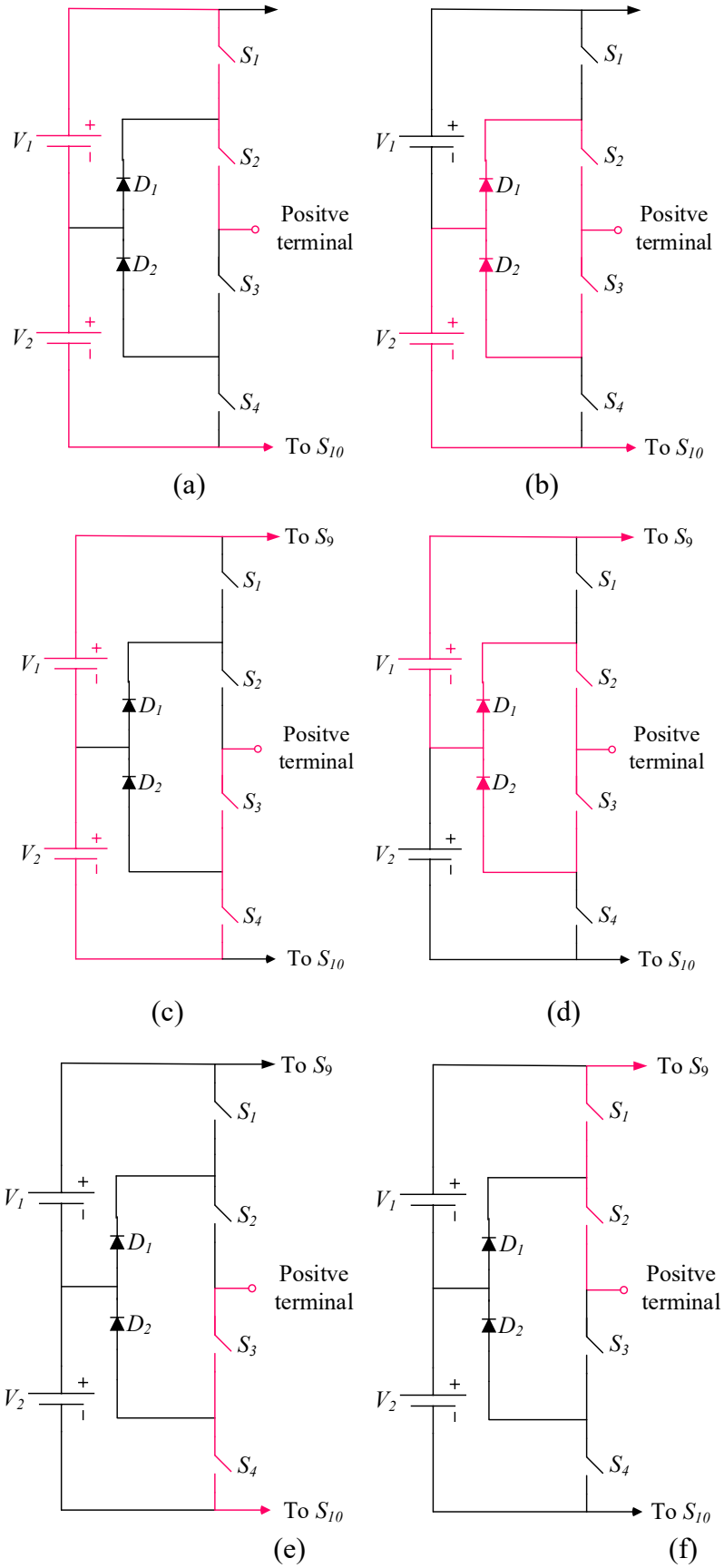


Figure 4.2: The switching mode for (a) V_1+V_2, (b) V_2, (c) $-(V_1 + V_2)$, (d) $-V_1$, and (e)-(f) zero state.

Figure 4.2 (a) and Figure 4.2 (b) show the switching operation to generate a positive waveform. The switching operation in Figure 4.2 (a) allows the current to flow through the switches in the upper legs and both DC sources. Hence, it will produce $V_1+V_2 = V_{DC}+V_{DC} = 2V_{DC}$. On the contrary, the switches at the lower legs are turned off. Meanwhile in Figure 4.2 (b), the current flows through "inner switches", which are S_2 and S_3, the clamping diodes D_1 and D_2, and V_2. Thus, $V_2 = V_{DC}$ is yielded from this cycle. S_1, S_4, and S_9 are switched off during this period.

Figure 4.2 (c) and Figure 4.2 (d) show the switching operations to generate negative waveforms. The switching operation in Figure 4.2 (c) allows the current to flow through the switches in the lower legs and both DC sources. Hence, this operation produces $-V_1+(-V_2) = -V_{DC}+(-V_{DC}) = -2V_{DC}$ whereas the switches at the upper legs are turned off. Meanwhile, in Figure 4.2 (d), the current flows through the S_2 and S_3, D_1 and D_2, and V_1, producing $V_1 = -V_{DC}$. S_1, S_4, and S_{10} are turned off during this cycle.

Figure 4.2 (e) and Figure 4.2 (f) show the switching operations for the zero-state level. As these options are interchangeable; they can help to reduce the switching frequency of the switches. During this switching period, the current will not flow through any of the two voltage sources.

4.3 Hybrid Configuration

The proposed topology is hybridized with a unit of H-MLI to further increase the voltage output levels. It is common for the new topology to be hybridized with a conventional MLI. Among all the conventional MLIs, H-MLI seems to be the best choice as it uses the least number of components.

The hybrid structure is shown in Figure 4.3. Notice that the configuration is divided into 3 parts, namely Part A (lined in blue), Part B (lined in green), and Part C (lined in purple). Part A and Part B are the proposed topology whereas Part C is the H-MLI. Every part is supplied by isolated DC sources, producing their own voltage trains according to their assigned ratio.

The switching operations for Part A and Part B are shown in Figure 4.2 (a) to Figure 4.2 (f). Meanwhile, the switches in H-MLI are divided into the upper legs switches, S_{11} and S_{13}, and the lower switches, S_{12} and S_{14}. These switches are operated in a complementary manner to avoid short-circuit. The positive waveform is generated by switching on S_{11} and S_{14} whereas the negative waveform is generated by turning on

S_{12} and S_{13} The zero-state level is generated with the combination of S_{11} and S_{13} or S_{12} and S_{14}.

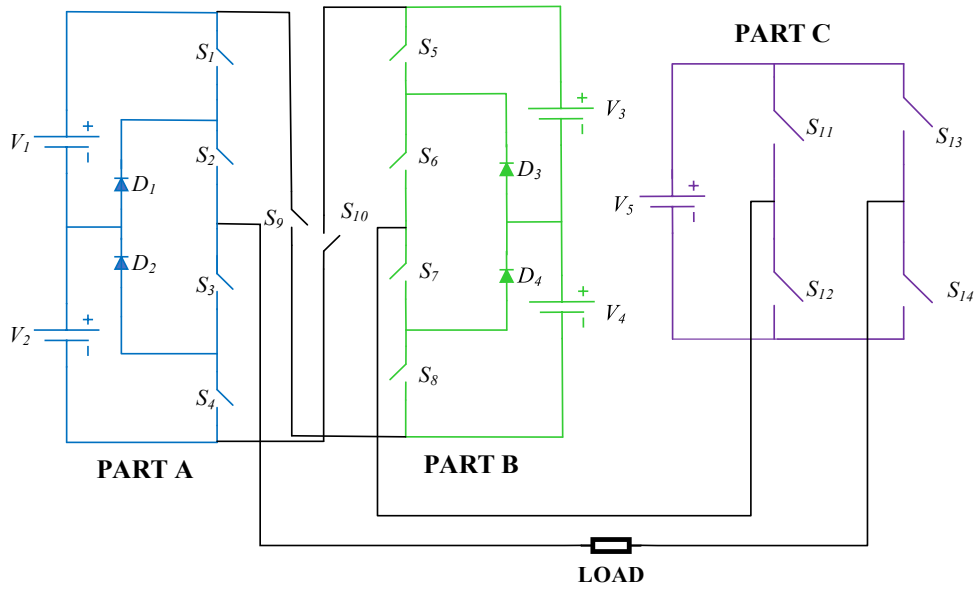


Figure 4.3: The hybrid configuration

Due to the isolated DC sources, this hybrid can be configured symmetrically (1:1:11) and asymmetrically (1:2:13 and 1:3:17). However, this study only focuses on trinary asymmetrical (1:3:17) configuration as it produced the highest total number of output voltage levels. Unlike Part A and Part B, the ratio for Part C is calculated using (5) to maximize output voltage levels. In addition, (6) is used to calculate the total number of output voltage levels, *n*.

$$V_{DC\text{-}C} = 2h+1 \quad (5)$$

Where;

$V_{DC\text{-}C}$ in the DC ratio assign to Part C

h is the summation of V_{DC}

$$n = 2\,(V_{DC\text{-}C} + h) + 1 \quad (6)$$

4.4 The Prototype Overview

The prototype was built for experimental testing and modelled based on the structure presented in Figure 4.3. It is shown in Figure 4.4. The prototype can be divided into 4 parts; the proposed topology (consists of Part A and Part B), the H-MLI cell (Part C), the DSP controller, and the gate driver. The list of components used to build this prototype is presented in Table 4.1.

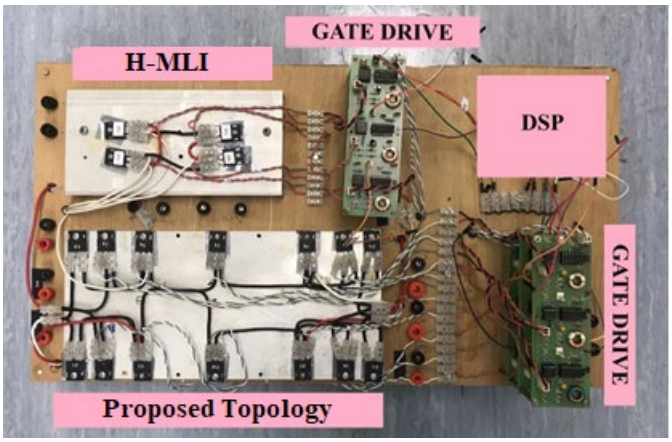


Figure 4.4: The hardware prototype

Table 4.1: List of the components to build the prototype.

No.	Name of the components	Quantity
1	DSDP controller (TMS320F28335)	1
2	Gate Drivers	14
3	IGBT switches	14
4	Diode	4
5	RL load bank	1
6	Heat sinks	2

In general, the arrangement for the experimental testing is illustrated in Figure 4.5. The purple arrows refer to the flow of the input signal that was fed into the prototype, while the green arrows refer to the flow of the output signal out from the prototype. The DC voltage was supplied by the DC power supply and as a precaution step, every power input was supplied with a DC power supply. Hence, at least 5 DC power supplies were used in the experimental testing.

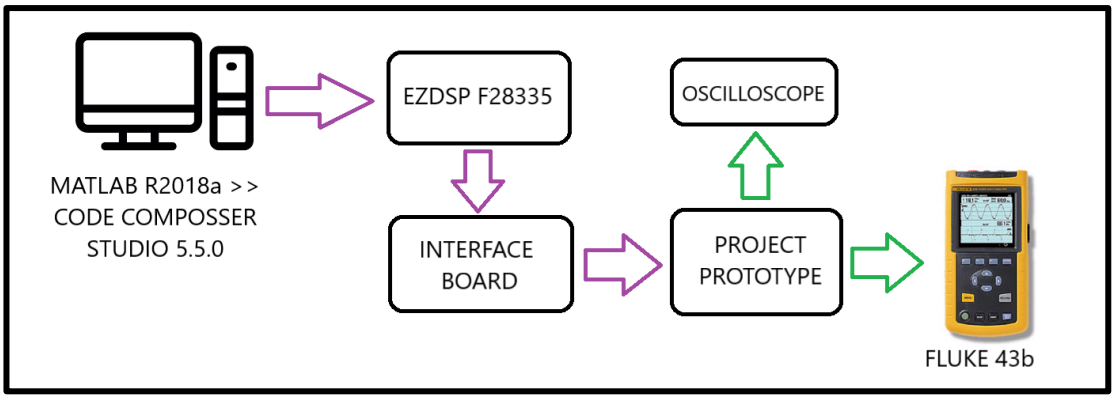
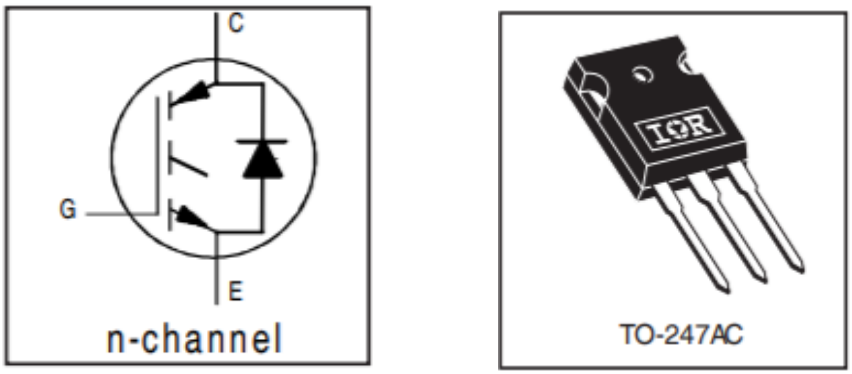


Figure 4.5: The experimental testing arrangement

As presented in Table 4.1, this prototype used 14 power switches, 4 diodes, and 5 isolated DC sources to generate up to 51-level of output voltage. The power switches can be either MOSFET or IGBT as long as it has an anti-parallel diode. The anti-parallel diode serves as the "return path" for the inductive load current when the output voltage changes in its polarity.

The IGBT that was used to build the prototype has a minimum gate to emitter voltage, V_{GE} = 15 V (IRG4PH50UDPbF, 2004). Figure 4.6 (a) and Figure 4.6 (b) show the schematic diagram of the IGBT and its actual photo, respectively. A diode with a forward bias of 0.3 V – 0.7 V was also used. Since these components are delicate, it is advisable to ensure the reading of DC source supplies is zero before switching on the power supply. This is to avoid voltage spikes that can damage the components. It is also advisable to test the components before assembling them. Accidentally using a broken component can damage other components that are connected to it.



(a) (b)

Figure 4.6: The (a) the schematic diagram and, (b) the actual photo (IRG4PH50UDPbF, 2004)

All these components were fixed onto a heatsink that acts as a temperature regulator. Switches tend to heat up during multiple switching. Therefore, using a

heatsink can minimize the power loss due to heat thus increasing the quality of the output. It also can increase the components' lifespan.

To supply the switching pulse to the prototype, DSP was used as means of communication between a computer and the prototype. In experimental testing, DSP was used to effectively convert the digital signals that are fed into it, to an analog signal that was fed into the gate driver. DSP is also known as a filter due to its ability to filter noise. Hence, this significantly increases the quality of the converted signal. This study used the TMS320F28335 EZDSP starter kit as shown in Figure 4.7. This is a type of floating-point controller that is capable to integrate JTAG emulation, operating at 150 MHz and has 256 kb on-chip flash memory (TMS320F28335, 2021).

Figure 4.7: The actual photo of DSP

Meanwhile, the gate drivers carry the switching signal (in form of an analog) from DSP to the switches. The gate driver acted as the interface between DSP and the prototype – nicknamed the 'interface board'. A gate driver was a set of different power electronic components that are assembled and soldered together onto a printed circuit board (PCB). The electronic components that were used to build a gate driver were an IC controller, 4 capacitors of different ratings, 3 resistors of different ratings, 4 rectifier diodes, a Zener diode, and an optocoupler. Each PCB had three sets of gate drivers that were soldered onto it. The construction of the gate driver is shown in Figure 4.8 whereas the total number of components used is tabulated in Table 4.2. The unlabelled components are the diodes, the resistors, and the capacitors.

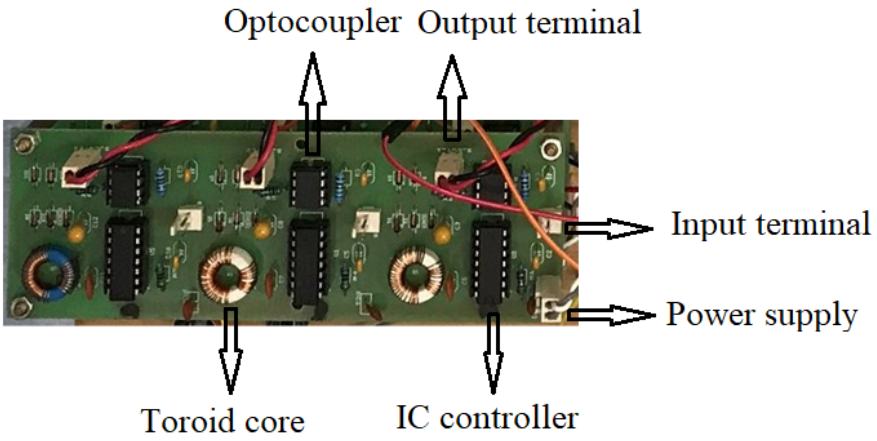


Figure 4.8: The gate drives that are fixed onto the interface board

Table 4.2: The electronic components used to build gate drivers

Name of the components	Rating/Type	Quantity
Capacitor	47 pF	14
	100 pF	14
	100 nF	14
	10 µF	14
Resistor	100 Ω	14
	680 Ω	14
	10 kΩ	14
Diode	Rectifier	56
	Zener	14
IC controller	74HCO4	14
Optocoupler	A3120	14
Toroid transformer	10 :30	14

Each interface board was supplied with 5 V. This voltage is enough to operate the IC controller that was connected to it. However, to operate IGBT, the voltage needs to be stepped up to at least 15 V. This task was fulfilled by the toroid core, which acted as a step-up transformer with a turn ratio of 1:3.

The amplified voltage was rectified by the four pieces of the diode rectifier to produce a 15 V DC signal. A Zener diode that was soldered next to it acts as a voltage stabilizer. The optocoupler acts as the common-mode noise transient suppressor. From this point, the switching signal finally left the interface board through the output terminal in form of a square wave voltage pulse.

The interface board was also used to isolate the power switches and the DSP controller. In case of unexpected error occurs, the interface board will protect the DSP controller and IGBTs by burning the IC controller. This option is reasonable as the IC controller is easily replaceable and cheaper as compared to DSP.

4.5 Conclusion

In nutshell, this chapter explains the structure of the proposed topology. The proposed topology used clamping diodes like DC-MLI, isolated DC sources like CHB-MLI, and floating switches like CCS-MLI. With this structure, it can be configured symmetrically and asymmetrically to produce 9-level, 13-level, and 17-level of output voltage with 14 components. The hybrid of the proposed topology and H-MLI is capable of yielding 51-level of output voltage with 23 components.

The prototype of the proposed MLI was built for experimental testing. It was modelled based on the proposed topology with DSP and gate drivers added to it. The DSP controller is the mean of communication between the computer and the prototype whereas the gate driver interfaced switches and the DSP.

Chapter 5:
Simulation and Experimental Results Analysis

5.1 Chapter Introduction

This chapter discusses and compares the simulation and the experimental results. Detailed explanations of these results will be given for each of the configurations. The first test was the simulation. It was carried out in Matlab/Simulink with the voltage capped at 240 V (single-phase voltage), at the power line frequency of 50 Hz, and connected to an inductive-resistive load. Since the simulations were performed under a controlled condition, the simulated results were treated as references and validated by the experimental results. The experimental testing was conducted with the output voltage of 240 V stepped down (capped) to 24 V for 9-, 13- and 17-level configurations whereas 37.5 V for the 51-level configuration. The simulations were repeated at the same capped input voltages with experimental testing to get more reliable and accurate results for comparison.

5.2 Simulation Analysis

The simulations were performed with an inductive-resistive load of 227.6 Ω and 0.55 H. The frequency was set at the power line frequency of (50 Hz) and the output voltage was capped at 240 V (single-phase voltage). The simulations were repeated for modulation index (m) equal to 1.0 (the ideal modulation), 0.8, 0.5, and 0.3. The results are presented with output waveform and the harmonic order, which explains the fundamental voltages, and the THD percentages.

5.2.1 9-level Configuration

9-level is symmetrical configuration (i.e. 1:1 ratio) with $V_{DC} = V_1 = V_2 = V_3 = V_4$. Hence, each part produced the same set of voltage trains of $2V_{DC}$, V_{DC}, 0, $-V_{DC}$, and $-2V_{DC}$. The highest output voltage was $4V_{DC}$ and the lowest was $-4V_{DC}$. The total output voltage was equal to 9. The voltage train for this configuration was $4V_{DC}$, $3V_{DC}$, $2V_{DC}$, V_{DC}, 0, $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, and $-4V_{DC}$. The switching states for this configuration are shown in Table 5.1 while the switching operations are enclosed in Appendix A.

Table 5.1: The switching state for 9-level configuration

State level	S_1	S_2	S_9	S_5	S_6	V_{ab}
1	1	1	0	0	0	$+4V_{DC}$
2	1	1	0	0	1	$+3V_{DC}$
3	0	0	0	0	0	$+2V_{DC}$
4	0	0	0	0	1	$+1V_{DC}$
5	0	0	0	1	1	0
6	1	1	1	0	1	$-1V_{DC}$
7	0	0	1	0	0	$-2V_{DC}$
8	0	0	1	0	1	$-3V_{DC}$
9	0	0	1	1	1	$-4V_{DC}$

Since the total output voltage was capped at 240 V, each V_{DC} = 60 V. The simulation was performed with a resistive-inductive load of 227.6 Ω and 0.55 H. The simulation was arranged as shown in Figure 5.1 and the switching signals for S_1, S_2, S_9, S_5, and S_6 are shown in Figure 5.2. The switching signals for S_3, S_4, S_{10}, S_7, and S_8 were complementary to those in Figure 5.2.

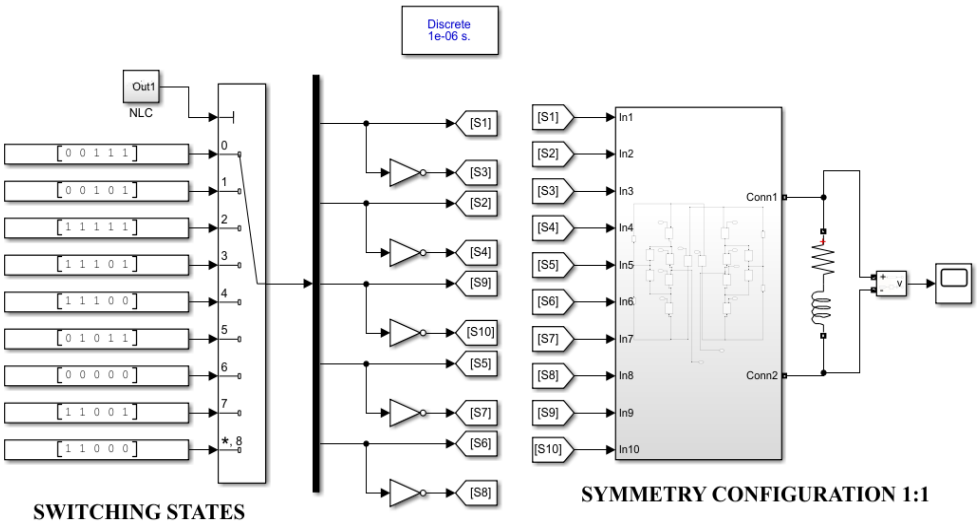


Figure 5.1: The simulation setup for the 9-level configuration

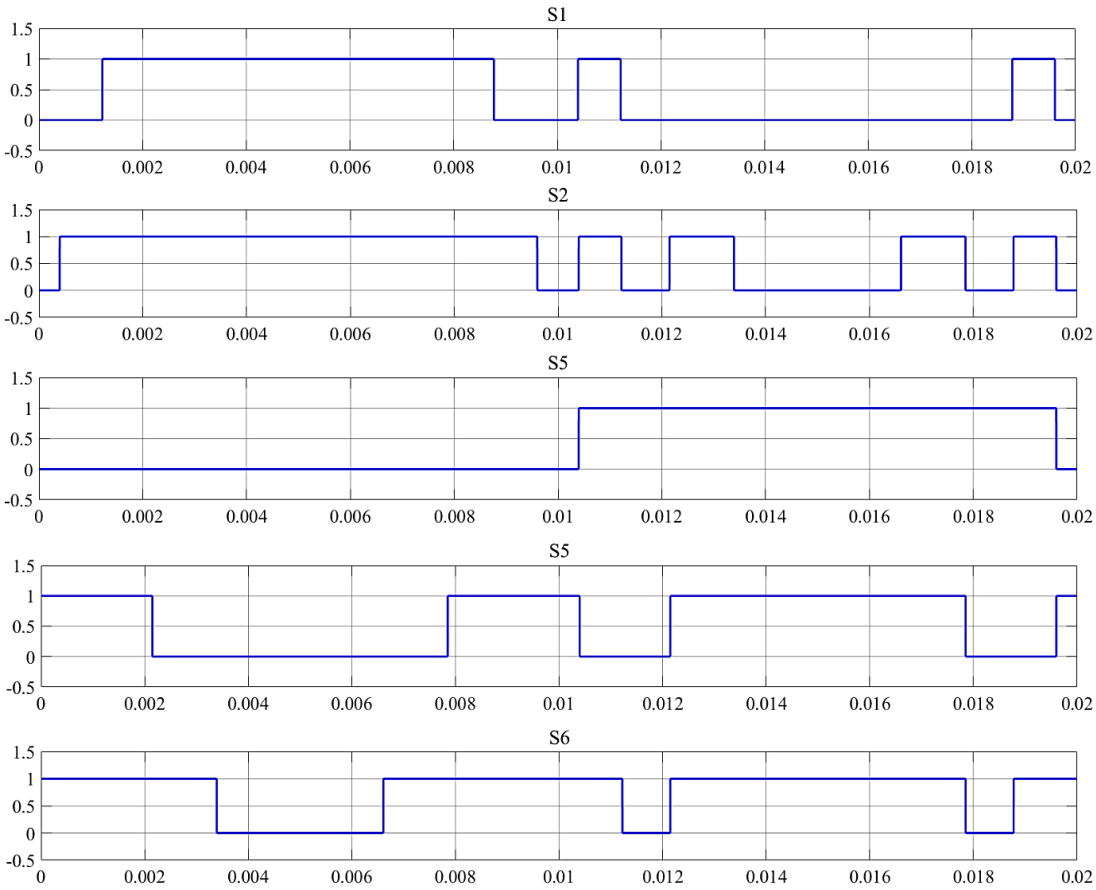
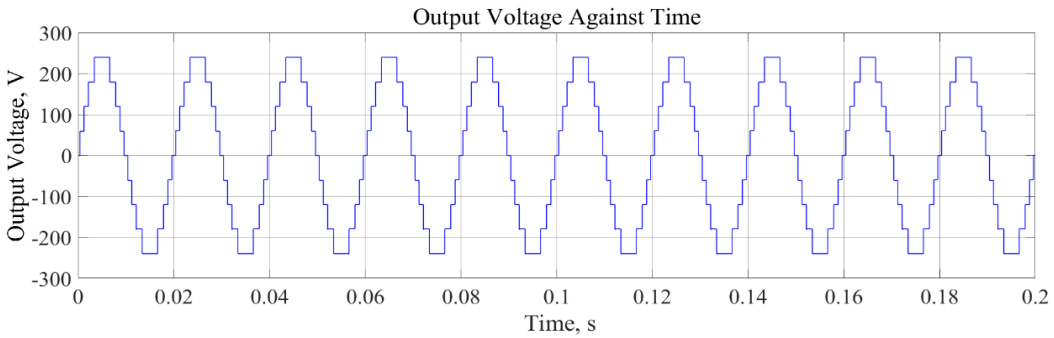
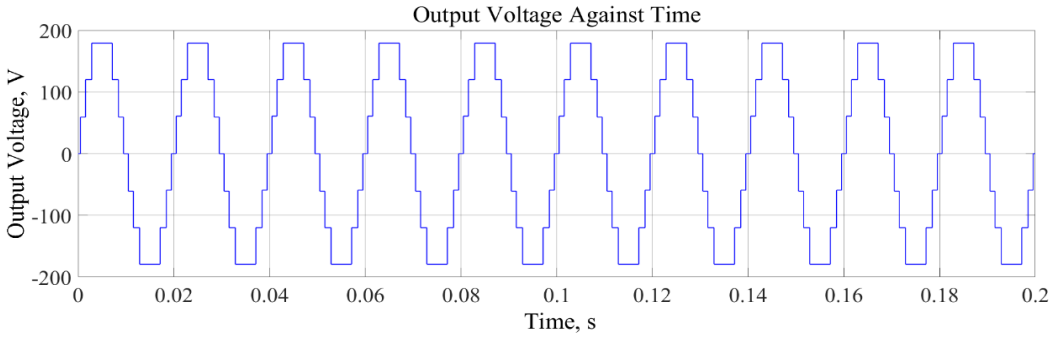


Figure 5.2: The switching pulses for S_1, S_2, S_9, S_5, and S_6

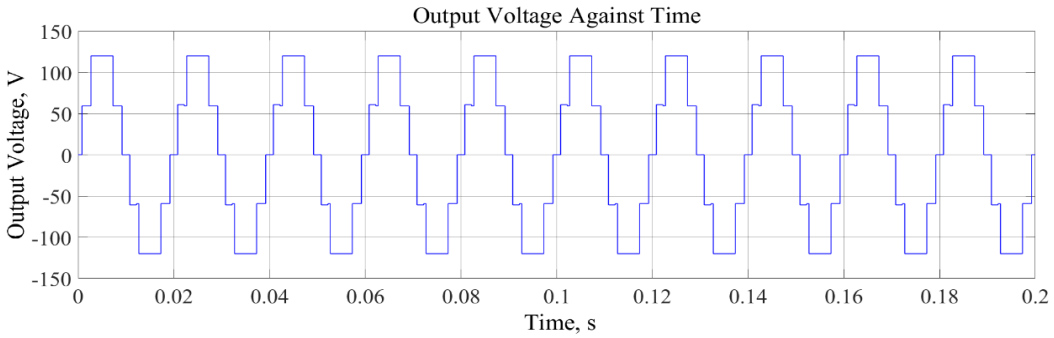
Figure 5.3 (a) to Figure 5.3(d) show the simulated output voltages when m is equal to 1.0, 0.8, 0.5, and 0.3, respectively. In figure 5.3 (a), a 9-level output voltage was produced when m = 1, which is the ideal modulation index. The output voltage level dropped to 7 when m = 0.8 (shown in Figure 5.3 (a)) and halved the initial value when m = 0.5 (shown in Figure 5.3 (c)). The number decreased further to 3 when m lowered to 0.3 (shown in Figure 5.3 (d)) which is equivalent to the total number of output levels produced by a two-level inverter.



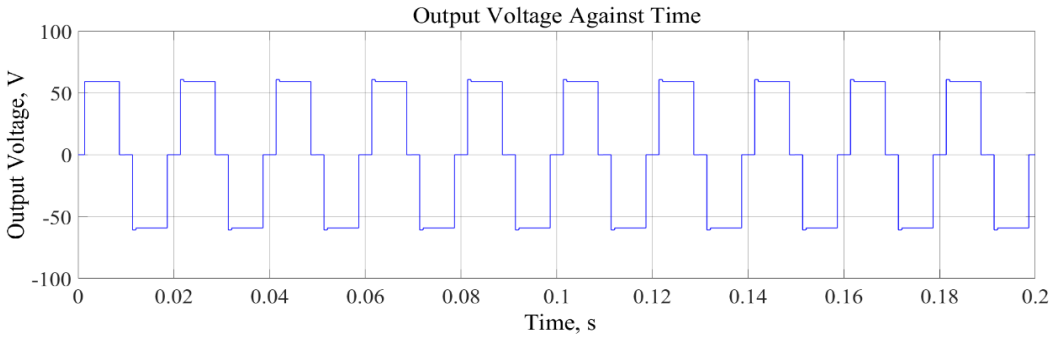
(a)



(b)



(c)

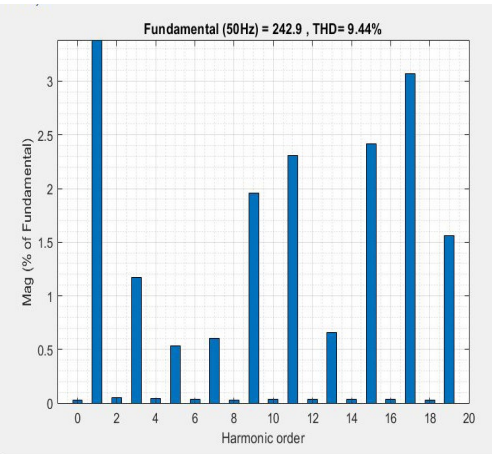


(d)

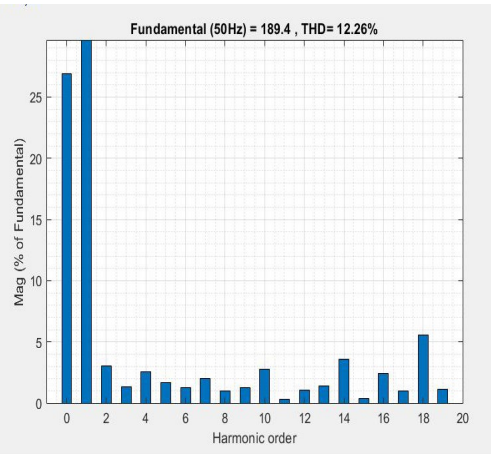
Figure 5.3: The output voltages for *m* (a) 1, (b) 0.8, (c) 0.5, and (d) 0.3

Figure 5.4 (a) to Figure 5.4 (d) show the harmonic order obtained from the simulation. When m = 1.0, the fundamental voltage, V_{FND} was 242.9 V (V_{RMS} = 171.8 V) and the THD percentage of 9.49%. The V_{FND} dropped with the modulation index but the THD percentage increased gradually. When m = 0.8, the THD percentage was 12.26 % and V_{FND} = 189.4 V. When m = 0.3, the THD percentage was almost 4 times the value when m = 1.0. With only three-level of output voltages and a THD percentage equal to 32.12%, it can be concluded that during m = 0.3, the 9-level configuration is no longer practical. Since the THD percentage during m = 1.0 is more than 5% (i.e.,

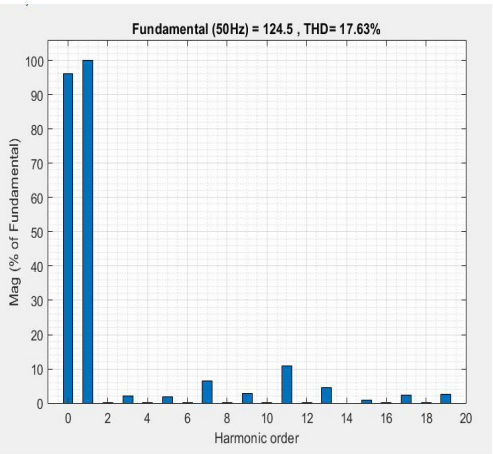
the standard set by IEEE for every application below 69 kV), this configuration might require an output filter. The results are tabulated in Table 5.2.



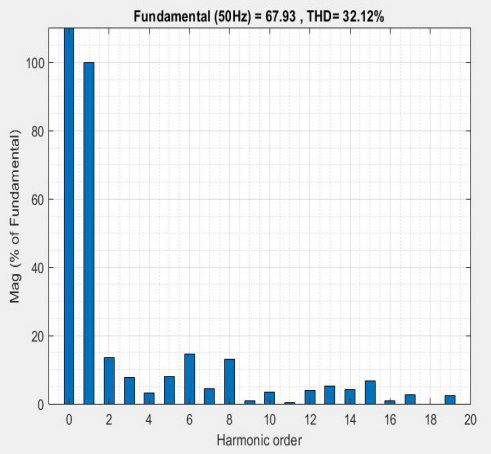
(a)



(b)



(c)



(d)

Figure 5.4: The harmonic orders for *m* (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

Table 5.2: The parameters obtained from a 9-level configuration

Modulation index, *m*	**Total number of voltage output levels, *n***	**THD Percentage**	**RMS Voltage, (V_{RMS}), V**	**Fundamental Voltage (V_{FND}), V**
1.0	9	9.44	171.8	242.9
0.8	7	12.26	133.9	189.4
0.5	5	17.63	88.03	124.5
0.3	3	32.12	48.03	67.93

Table 5.3 shows the mean voltage and the mean current of all switches. Note that the mean currents were higher at the inner switches — S_2, S_3, S_6, and S_7. The higher currents at the inner switches were believed caused by the diodes. The voltage was

said to be evenly distributed when the summations of the voltages were almost the same at the upper legs and the lower legs. From the table, the mean voltages were shown to be evenly distributed in Part A, but in Part B (S_5, S_6, S_7, and S_8), the voltages were concentrated at the lower legs – the S_7 and S_8. The switching frequency for this configuration was 800 Hz.

Table 5.3: The mean current and voltage for every switch

Switch	Mean Current, A ($x10^{-2}$)	Mean Voltage, V
S_1	19.20	27.30
S_2	22.01	24.99
S_3	21.32	32.19
S_4	13.73	35.52
S_5	12.12	24.71
S_6	14.98	18.01
S_7	15.64	46.30
S_8	7.63	30.98

5.2.2 13-level Configuration

The voltage ratio for this configuration was 1:2. Therefore, $V_1 = V_2 = V_{DC}$ and $V_3 = V_4 = 2V_{DC}$ The highest values for output voltage for Part A and Part B were $2V_{DC}$ and $4V_{DC}$, respectively. The maximum number of output voltage levels for this configuration was 13. The voltage train produced by Part A was $2V_{DC}$, V_{DC}, 0, $-V_{DC}$, and $-2V_{DC}$ while for Part B was $4V_{DC}$, $3V_{DC}$, $2V_{DC}$, V_{DC}, 0, $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, and $-4V_{DC}$. The switching states were as tabulated in Table 5.4 and the switching operations were as enclosed in Appendix B.

Table 5.4: The switching states for 13-level configuration

State level	S_1	S_2	S_9	S_5	S_6	V_{ab}
1	1	1	0	0	0	$6V_{DC}$
2	0	1	0	0	0	$5V_{DC}$
3	0	0	0	0	0	$4V_{DC}$
4	0	1	0	0	1	$3V_{DC}$
5	0	0	0	0	1	$2V_{DC}$
6	0	1	0	1	1	$1V_{DC}$
7	0	0	0	1	1	0
8	0	1	1	0	0	$-1V_{DC}$
9	1	1	1	0	1	$-2V_{DC}$
10	0	1	1	0	1	$-3V_{DC}$
11	1	1	1	1	1	$-4V_{DC}$
12	0	1	1	1	1	$-5V_{DC}$
13	0	0	1	1	1	$-6V_{DC}$

As the total voltage was capped at 240 V, each V_{DC} = 40 V. A resistive-inductive loads of 227.6 Ω and 0.55 H were added to the configuration. The simulation setup is presented in Figure 5.5. The switching signals for S_1, S_2, S_9, S_5, and S_6 are indicated in Figure 5.6. The switching signals for S_3, S_4, S_{10}, S_7, and S_8 are complementary to the switching signals shown in Figure 5.6.

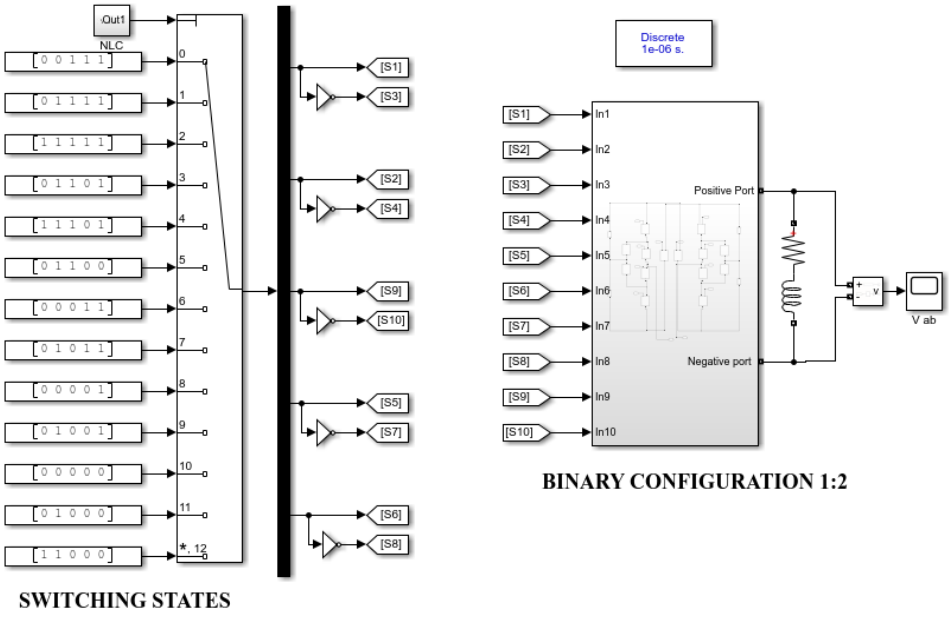


Figure 5.5: The simulation setup for the 13-level configuration

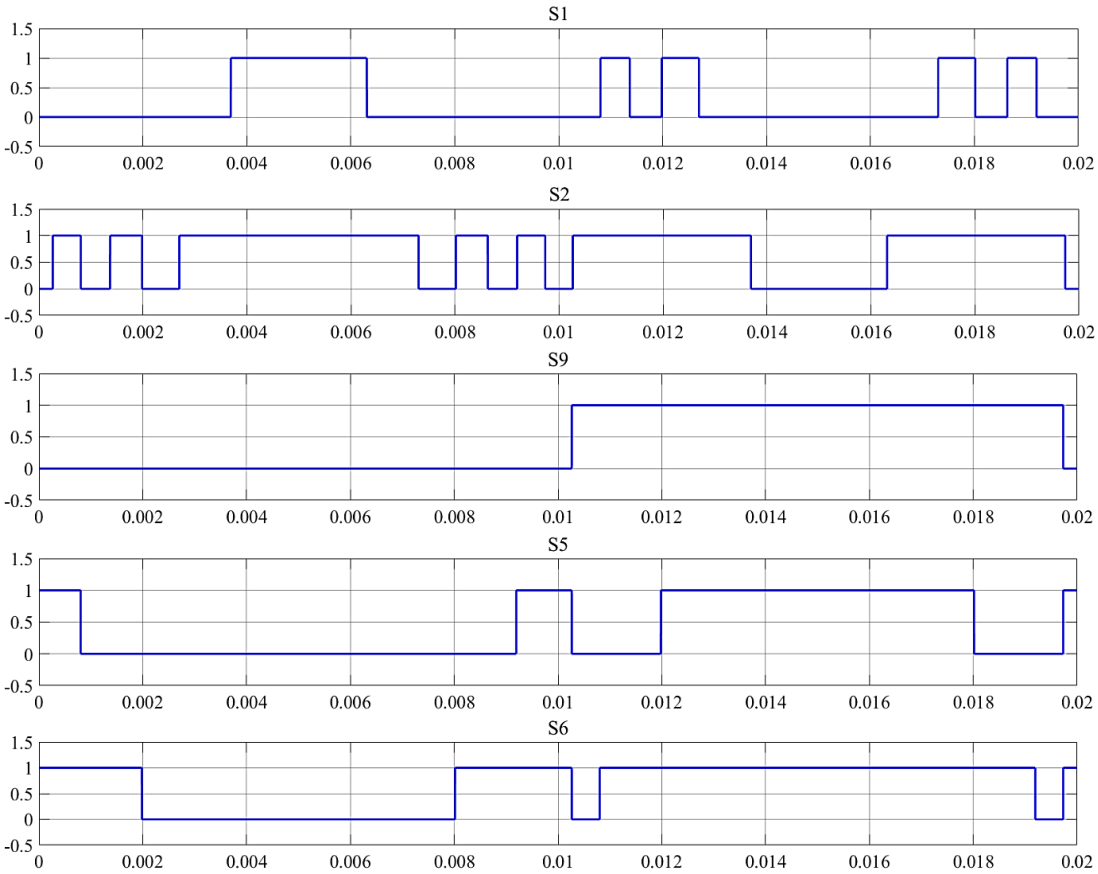
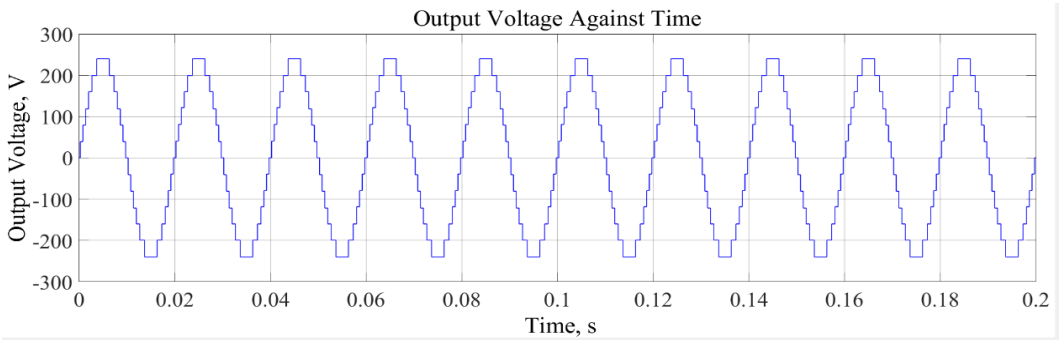
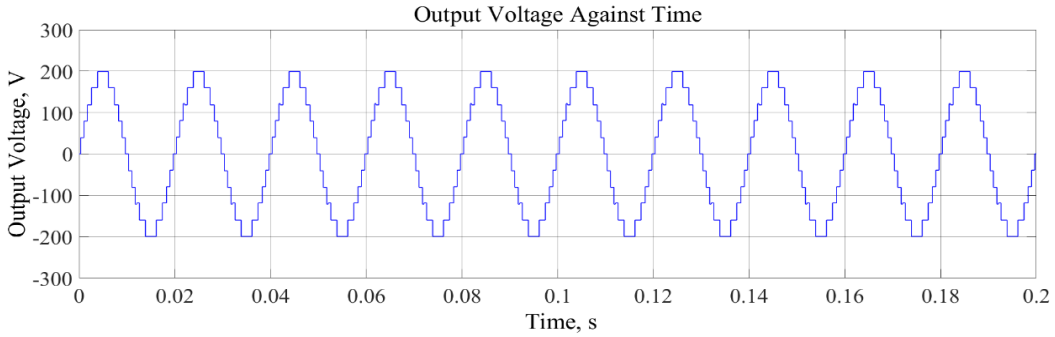


Figure 5.6: The switching pulses for S_1, S_2, S_9, S_5, and S_6

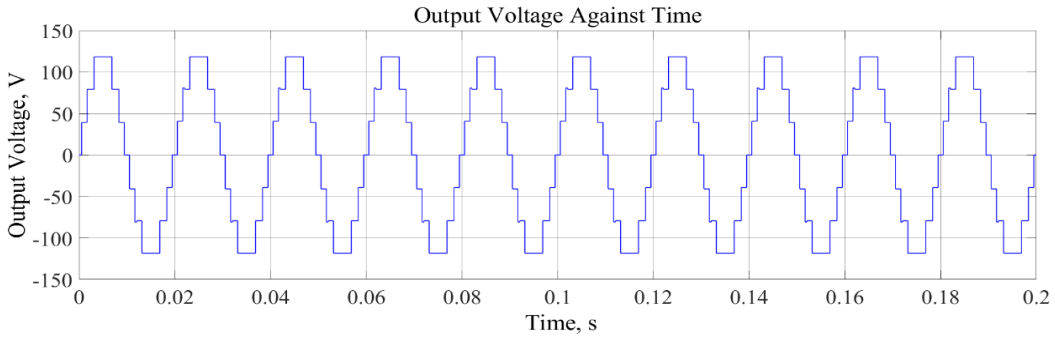
The output waveforms for m = 1.0, 0.8, 0.5, and 0.3 are shown in Figure 5.7 (a) to Figure 5.7 (d). This configuration produced 13-level of output voltage when m = 1.0. The number of output levels decreased to 11, 7 and 5 when m = 0.8, 0.5 and 0.3, respectively. Figure 5.8 (a) to Figure 5.8 (d) respectively show the THD percentages for m = 1.0, 0.8, 0.5, and 0.3.



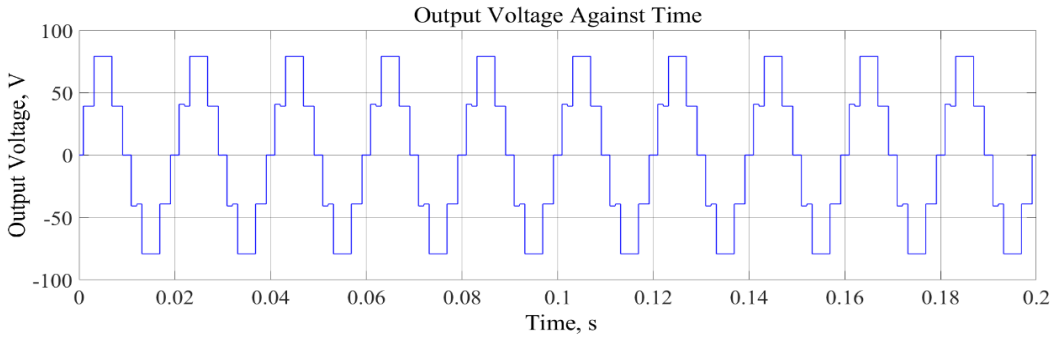
(a)



(b)

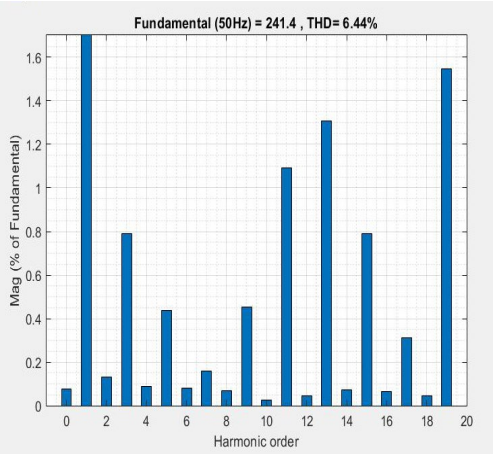


(c)

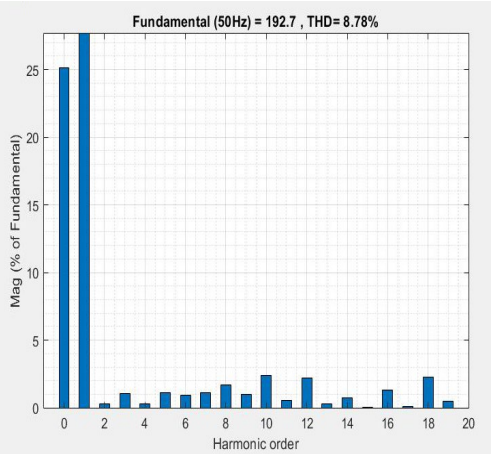


(d)

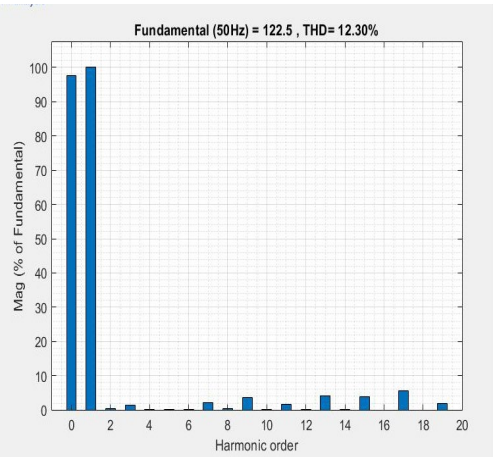
Figure 5.7: The output voltages for m = (a) 1.0, (b) 0.8, (c) 0.5 and (d) 0.3



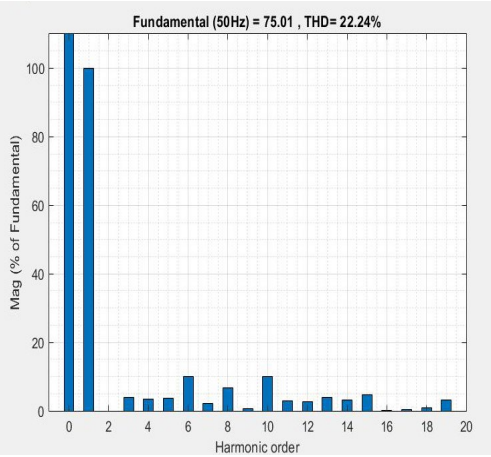
(a)



(b)



(c)



(d)

Figure 5.8: The harmonic orders for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

As shown in Figure 5.8 (a), the THD percentage during ideal modulation was 6.44%, which was greater than the allowable limit. Thus, an output filter is required to enhance the quality. The THD percentages were 8.78%, 12.30%, and 22.40% when m = 0.8, 0.5, and 0.3. When m = 0.3, the THD percentage was three times the value when m = 1.0. The odd harmonic was noticeably high when m = 1.0, as shown in Figure 5.8 (a).

On the contrary, the total number of output levels and the fundamental voltage decreased with the modulation index. The V_{FND} when m = 1.0 was 241.4 V and dropped to 75.01 V when m = 0.3. With the 5-level output voltage, V_{FND} = 75.01 V, and the THD percentage = 22.24%, it can be concluded that this operation is no longer

practicable when m = 0.3. The simulated results from this 13-level configuration are tabulated in Table 5.5.

Table 5.5: The parameters obtained from this 13-level configuration

Modulation index, *m*	**Number of voltage levels, *n***	**THD Percentage, %**	**RMS Voltage, (V_{RMS}), V**	**Fundamental Voltage (V_{FND}), V**
1.0	13	6.44	170.7	241.4
0.8	11	8.78	136.3	192.7
0.5	7	12.30	86.6	122.5
0.3	5	22.24	53.04	75.01

Table 5.6 shows the mean current and the mean voltage for every switch. Note that the currents were higher at the inner switches - S_2, S_3, S_6, and S_7 and the floating switches – S_9, and S_{10}. The existence of the clamping diodes is believed to be the cause. Meanwhile, a high current at the floating switches might be due to the high voltage shared by the floating switches. The voltage distributions were almost even between switches at the upper legs and switches at the lower legs. The switching frequency for this 13-level configuration was 1.2 kHz.

Table 5.6: The mean current and voltage for every switch

Switch	**Mean Current, A ($x10^{-2}$)**	**Mean Voltage, V**
S_1	4.44	29.53
S_2	15.70	12.61
S_3	15.09	10.47
S_4	4.21	27.40
S_5	17.00	45.37
S_6	22.18	30.37
S_7	27.78	36.34
S_8	17.41	47.92
S_9	21.49	126.40
S_{10}	22.11	113.60

5.2.3 17-level configuration

The voltage ratio for this configuration was 1:3. Hence, $V_1 = V_2 = V_{DC}$ and $V_3 = V_4 = 3V_{DC}$. Given that value, Part A produced a voltage train of $2V_{DC}$, $1V_{DC}$, 0, $-1V_{DC}$, and $-2V_{DC}$, while Part B produced a voltage train of $6V_{DC}$, $5V_{DC}$, 4 V_{DC}, $3V_{DC}$, $2V_{DC}$, $1V_{DC}$, 0, $-1V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, $-4V_{DC}$, $-5V_{DC}$, and $-6V_{DC}$. The summation of Part A and Part B produced output voltage between $8V_{DC}$ and $-8V_{DC}$; with each switching state differing by $1V_{DC}$. The switching states are shown in Table 5.7 and the switching operations are as attached in Appendix C.

Table 5.7: The switching states for the 17-level configuration

State Level	S_1	S_2	S_9	S_5	S_6	V_{ab}
1	1	1	1	0	0	$+8V_{DC}$
2	0	1	1	0	0	$+7V_{DC}$
3	0	0	1	0	0	$+6V_{DC}$
4	1	1	1	0	1	$+5V_{DC}$
5	0	1	1	0	1	$+4V_{DC}$
6	0	0	1	0	1	$+3V_{DC}$
7	1	1	1	1	1	$+2V_{DC}$
8	0	1	1	1	1	$+1V_{DC}$
9	0	0	1	1	1	0
10	0	1	0	0	0	$-1V_{DC}$
11	0	0	0	0	0	$-2V_{DC}$
12	1	1	0	0	1	$-3V_{DC}$
13	0	1	0	0	1	$-4V_{DC}$
14	0	0	0	0	1	$-5V_{DC}$
15	1	1	0	1	1	$-6V_{DC}$
16	0	1	0	1	1	$-7V_{DC}$
17	0	0	0	1	1	$-8V_{DC}$

As the output voltage was capped at 240 V, each V_{DC} = 30 V. A resistive-inductive loads of 227.6 Ω and 0.55 H were also included in the simulation. Figure 5.9 and Figure 5.10 respectively show the simulation setup and the switching pulses for S_1, S_2, S_9, S_5, and S_6, whereas switching pulses for S_3, S_4, S_{10}, S_7, and S_8 were complementary to the former pulses.

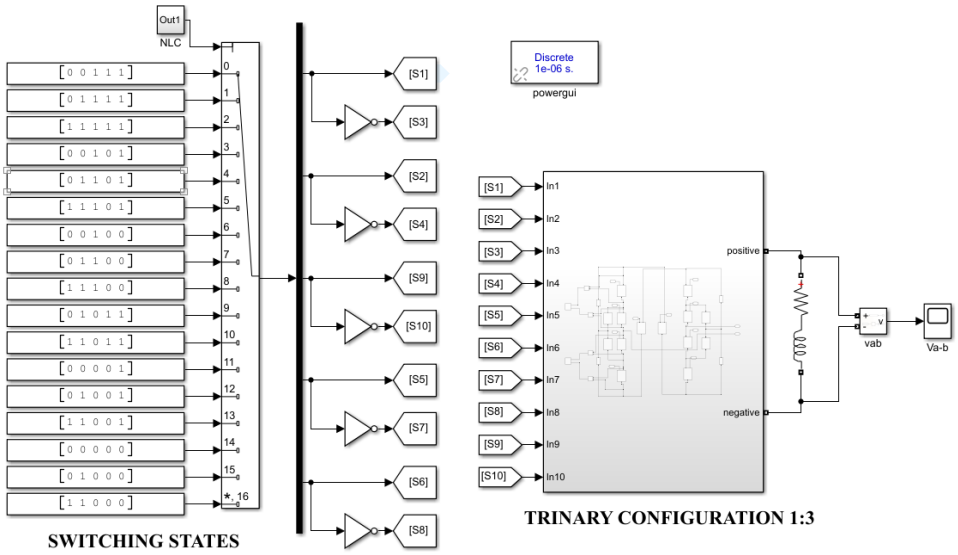


Figure 5.9: The simulation setup for the 17-level configuration

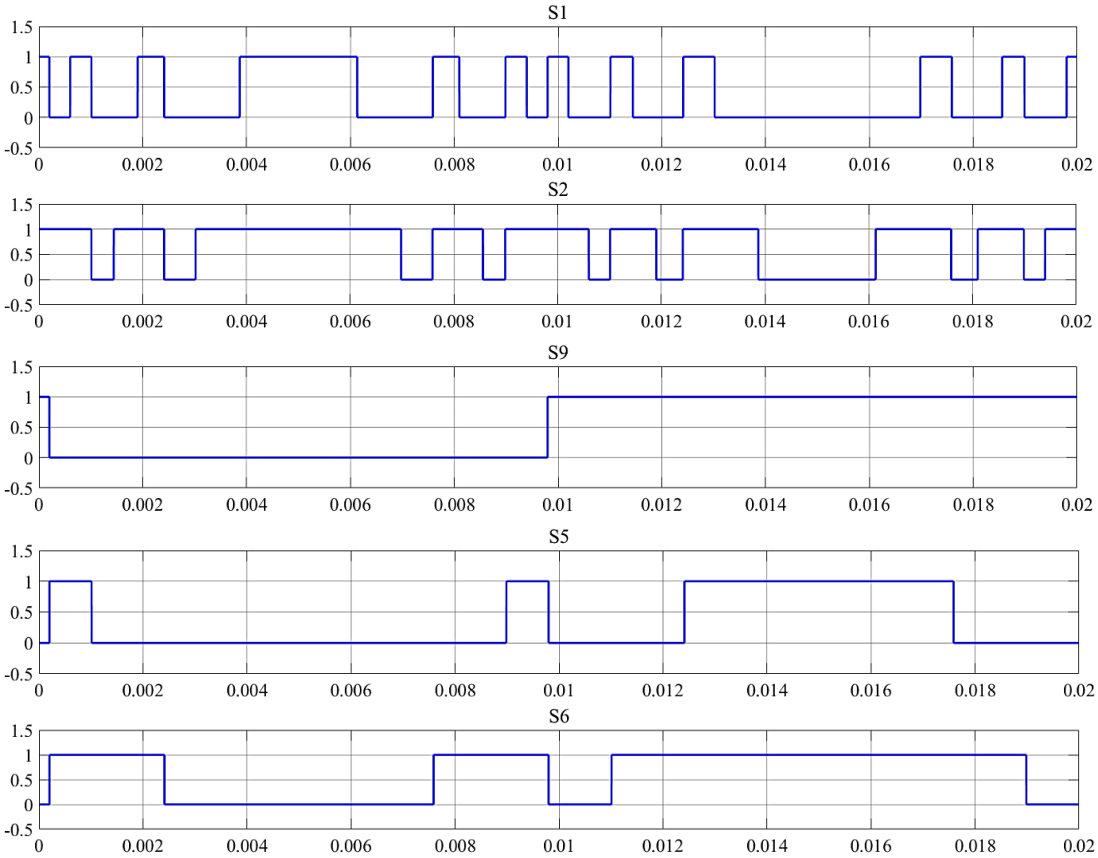
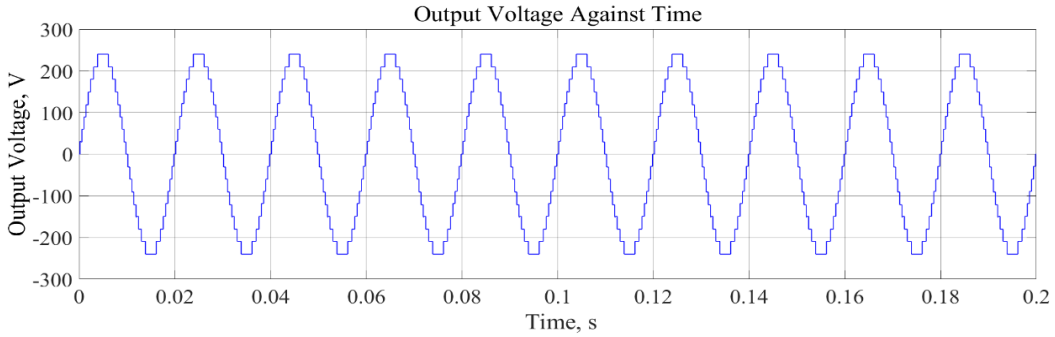


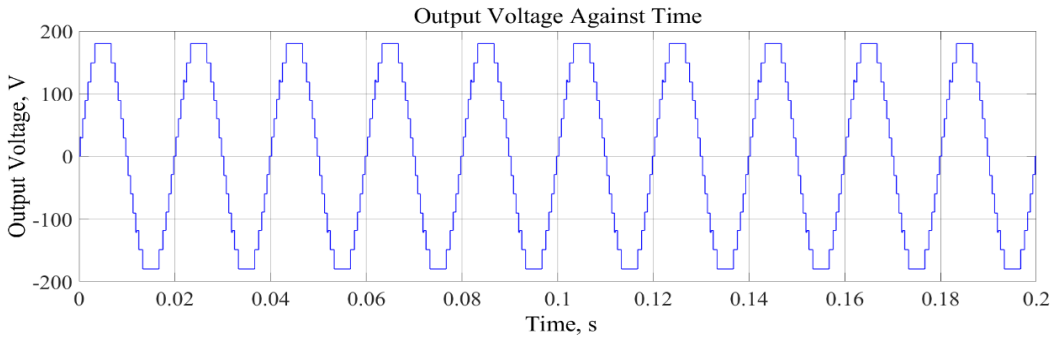
Figure 5.10: The switching pulses for S_1, S_2, S_9, S_5, and S_6

The simulations were conducted with m = 1.0, 0.8, 0.5, and 0.3. Figure 5.11 (a) to Figure 5.11 (d) show the respective output voltage waveform for m = 1.0, 0.8, 0.5, and 0.3. From the simulated results, a specific trend can be observed. Similar to the 9-level and 13-level configurations, the number of output voltage levels decreased with

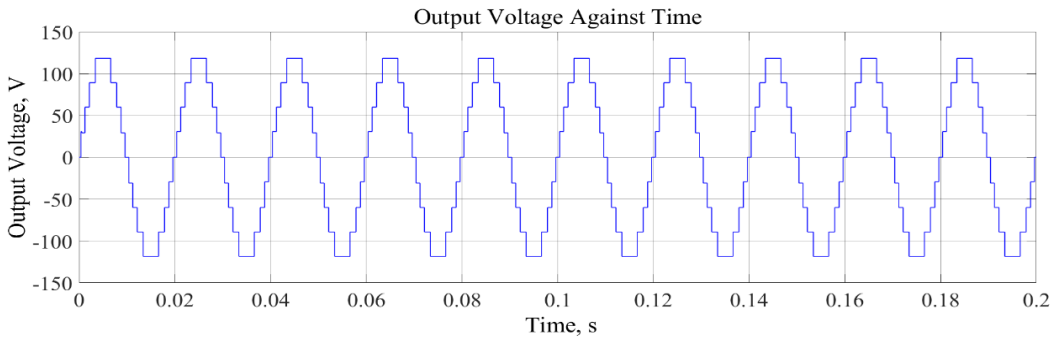
the values of *m*. The output voltage level was 17 when *m* = 1, but dropped to 14, 9, and 6 as the value of *m* was respectively reduced to 0.8, 0.5, and 0.3. The THD percentages are shown in Figure 5.12 (a) to Figure 5.12 (d).



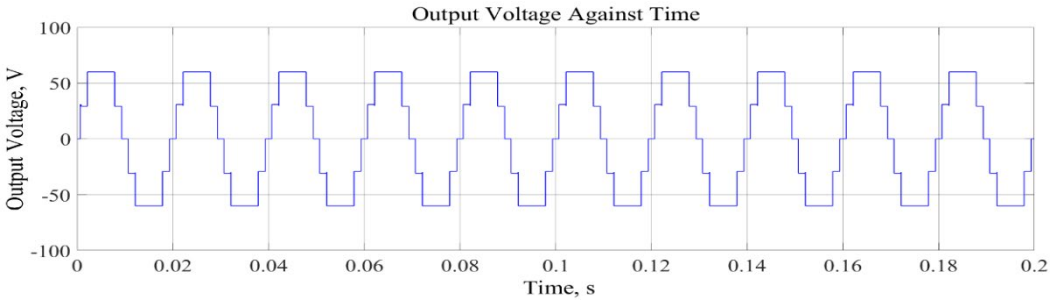
(a)



(b)

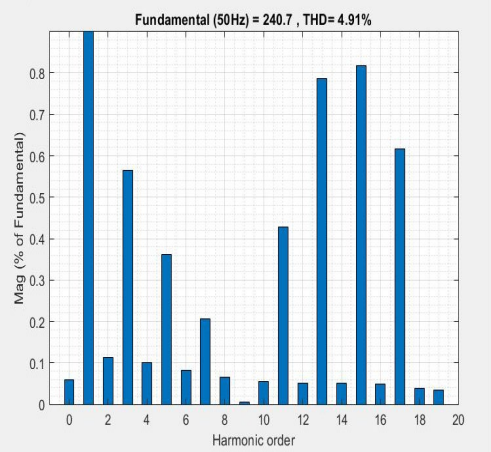


(c)

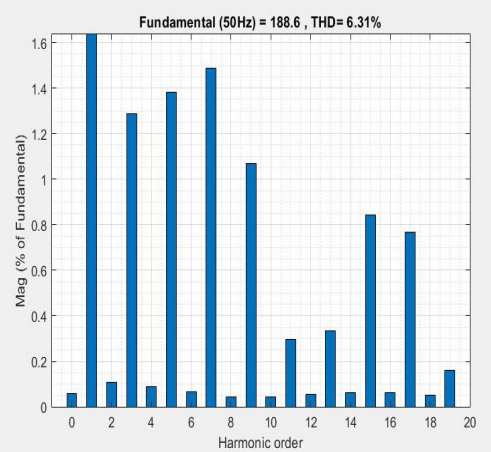


(d)

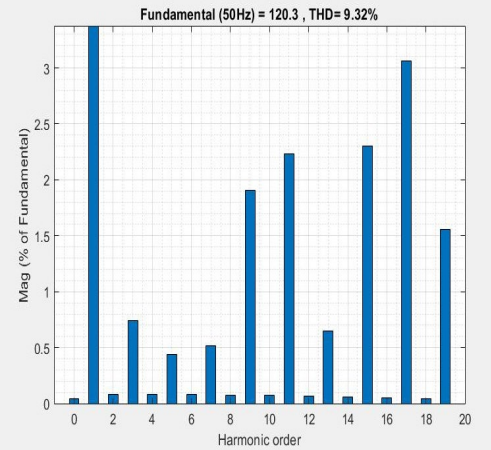
Figure 5.11: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3



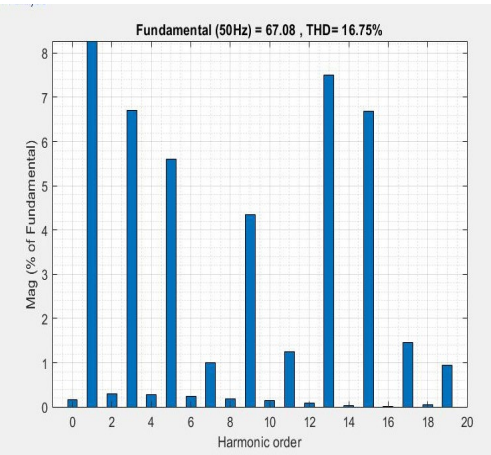
(a)



(b)



(c)



(d)

Figure 5.12: The harmonic orders for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

As indicated in Figure 5.12 (a) to Figure 5.12 (d), it was observed that the THD percentage increased as *m* decreased. The increment in THD percentage reflected the drop in the power quality of the inverter. The lowest THD percentage obtained from this 17-level configuration was 4.9%, which is within the IEEE standard limit When

m = 0.8, the THD percentage was just 1.29% greater than the allowable limit and it was lesser than 10% when m = 0.5. The percentage was 15.72% when m = 0.3. Certainly, a filter is needed to enhance the power quality, but the filter size would be smaller than the one being used for the THD percentage greater than 20%. In addition, the odd harmonic for every value of m is also noticeably higher as compared to other configurations. Simulation results were shown in Table 5.8.

Table 5.8: The parameters obtained from this 17-level configuration

Modulation index, *m*	**Number of voltage levels, *n***	**THD Percentage, %**	**RMS Voltage, (V_{RMS}), V**	**Fundamental Voltage (V_{FND}), V**
1.0	17	4.90	170.20	240.7
0.8	14	6.29	136.40	192.8
0.5	9	9.44	85.99	121.60
0.3	6	15.72	53.20	75.23

The mean voltage and the mean current for every switch are shown in Table 5.9. Note that the mean currents were higher at S_2, S_3, S_6, S_7, S_9, and S_{10}. This was most likely due to the existence of clamping diodes at the inner switches - S_2, S_3, S_6, and S_7. The voltage distribution between the upper legs and the lower legs was almost even. The switching frequency for this 17-level configuration was 1.6 kHz.

Table 5.9: The mean current and voltage for every switch

Switch	**Mean Current, A ($x10^{-2}$)**	**Mean Voltage, V**
S_1	6.82	16.68
S_2	15.91	12.13
S_3	15.31	13.37
S_4	6.36	17.82
S_5	14.72	54.11
S_6	20.76	39.47
S_7	21.38	34.18
S_8	15.15	52.24
S_9	21.42	115.20
S_{10}	22.02	124.80

5.2.4 51- level Configuration

The hybrid of the proposed topology and H-MLI can be configured symmetrically and asymmetrically. However, this study focused on the asymmetrical configuration with the voltage ratio of 1:3:17. Therefore, $V_1 = V_2 = V_{DC}$, $V_3 = V_4 = 3V_{DC}$, and $V_5 = 17V_{DC}$.

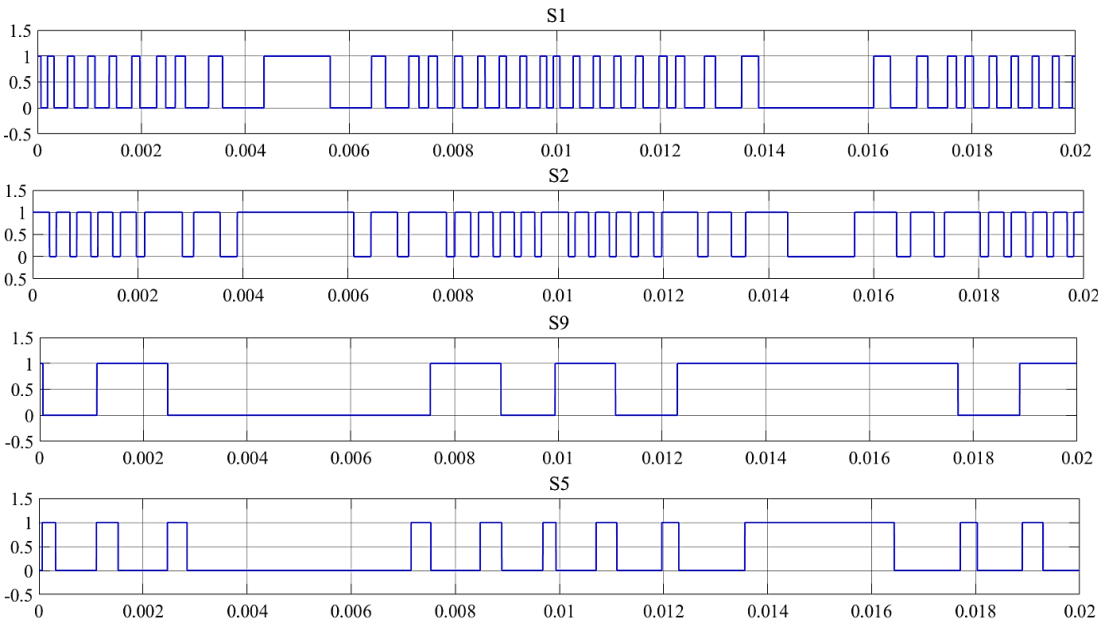
Part A produced a voltage train of $+V_{DC}$, 0, and $-V_{DC}$, Part B produced a voltage train of $+6V_{DC}$, $+5V_{DC}$, $+4V_{DC}$, $+3V_{DC}$, $+2V_{DC}$, $+1V_{DC}$, 0, $-1V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, $-4V_{DC}$, $-5V_{DC}$, and $-6V_{DC}$, and Part C produced a voltage train of $+17V_{DC}$, 0, and $-17V_{DC}$. The summation produced a voltage train between $+25V_{DC}$ to $-25V_{DC}$ with each switching state differing by $1V_{DC}$. The state levels are shown in Table 5.10 and the switching operations are attached in Appendix D.

Table 5.10: The switching states for 51-level configuration

State Level	S_1	S_2	S_9	S_5	S_6	S_{11}	S_{13}	V_{ab}
1	1	1	0	0	0	1	0	$+25V_{DC}$
2	1	0	0	0	0	1	0	$+24V_{DC}$
3	0	0	0	0	0	1	0	$+23Vdc$
4	1	1	0	1	0	1	0	$+22Vdc$
5	1	0	0	1	0	1	0	$+21V_{DC}$
6	0	0	0	1	0	1	0	$+20V_{DC}$
7	1	1	0	1	1	1	0	$+19V_{DC}$
8	1	0	0	1	1	1	0	$+18V_{DC}$
9	0	0	0	1	1	1	0	$+17V_{DC}$
10	1	0	1	0	0	1	0	$+16V_{DC}$
11	0	0	1	0	0	1	0	$+15V_{DC}$
12	1	1	1	1	0	1	0	$+14V_{DC}$
13	1	0	1	1	0	1	0	$+13V_{DC}$
14	0	0	1	1	0	1	0	$+12V_{DC}$
15	1	1	1	1	1	1	0	$+11V_{DC}$
16	1	0	1	1	1	1	0	$+10V_{DC}$
17	0	0	1	1	1	1	0	$+9V_{DC}$
18	1	1	0	0	0	1	1	$+8V_{DC}$
19	1	0	0	0	0	1	1	$+7V_{DC}$
20	0	0	0	0	0	1	1	$+6V_{DC}$
21	1	1	0	1	0	1	1	$+5V_{DC}$
22	1	0	0	1	0	1	1	$+4V_{DC}$
23	0	0	0	1	0	1	1	$+3V_{DC}$
24	1	1	0	1	1	1	1	$+2V_{DC}$
25	1	0	0	1	1	1	1	$+1V_{DC}$
26	0	0	0	1	1	0	0	0
27	1	0	1	0	0	1	1	$-1V_{DC}$
28	0	0	1	0	0	1	1	$-2V_{DC}$
29	1	1	1	0	0	1	1	$-3V_{DC}$
30	1	0	1	0	0	1	1	$-4V_{DC}$
31	0	0	1	1	0	1	1	$-5V_{DC}$
32	1	1	1	1	1	1	1	$-6V_{DC}$
33	1	0	1	1	1	1	1	$-7V_{DC}$
34	0	0	1	1	1	1	1	$-8V_{DC}$
35	1	1	0	0	0	0	1	$-9V_{DC}$
36	1	0	0	0	0	0	1	$-10V_{DC}$

37	0	0	0	0	0	0	1	$-11V_{DC}$
38	1	1	0	1	0	0	1	$-12V_{DC}$
39	1	0	0	1	0	0	1	$-13V_{DC}$
40	0	0	0	1	0	0	1	$-14V_{DC}$
41	1	1	0	1	1	0	1	$-15V_{DC}$
42	1	0	0	1	1	0	1	$-16V_{DC}$
43	1	1	1	0	0	0	1	$-17V_{DC}$
44	1	0	1	0	0	0	1	$-18V_{DC}$
45	0	0	1	0	0	0	1	$-19V_{DC}$
46	1	1	1	1	0	0	1	$-20V_{DC}$
47	1	0	1	1	0	0	1	$-21V_{DC}$
48	0	0	1	1	0	0	1	$-22V_{DC}$
49	1	1	1	1	1	0	1	$-23V_{DC}$
50	1	0	1	1	1	0	1	$-24V_{DC}$
51	0	0	1	1	1	0	1	$-25V_{DC}$

For this simulation, the voltage was capped at 240 V, therefore each V_{DC} = 9.6 V. A resistive – inductive load of 227.6 Ω and 0.55 H was also added at the load side. The switching pulses for S_1, S_2, S_9, S_5, S_6, S_{11}, and S_{13} are stated in Figure 5.13 whereas the-switching pulses for S_3, S_4, S_{10}, S_7, S_8, S_{12}, and S_{14} were complementary to these switching. Figure 5.14 (a) shows the voltage train at Part A and Part B (i.e. the proposed topology), while Figure 5.14 (b) shows the voltage train at Part C (i.e. a unit of H-MLI).



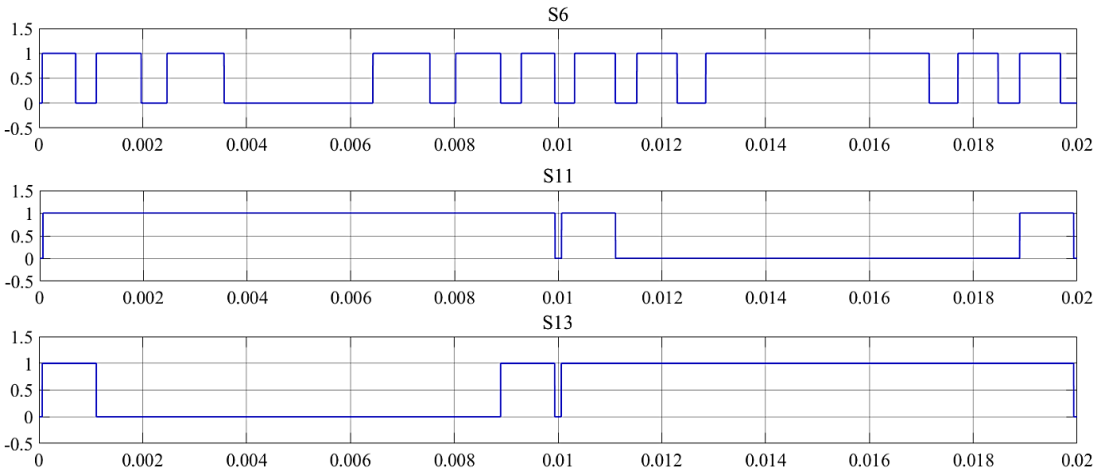
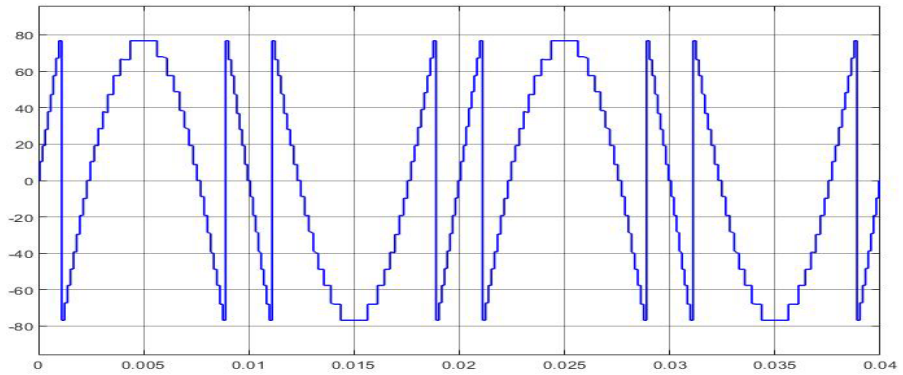
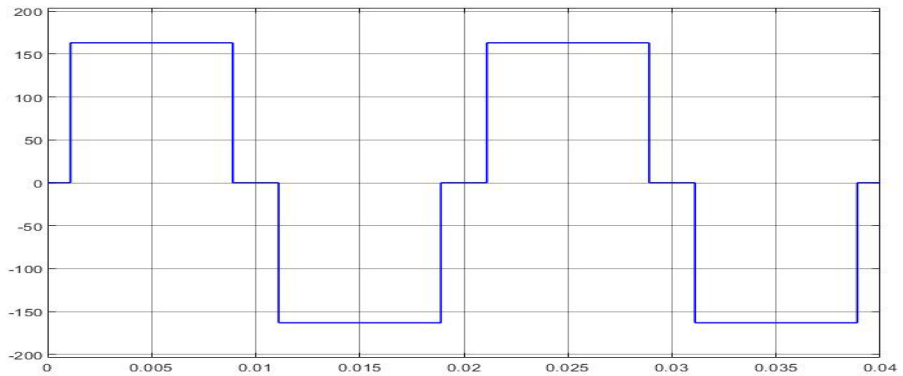


Figure 5.13: The switching pulses for S_1, S_2, S_9, S_5, S_6, S_{11}, and S_{13}.



(a)

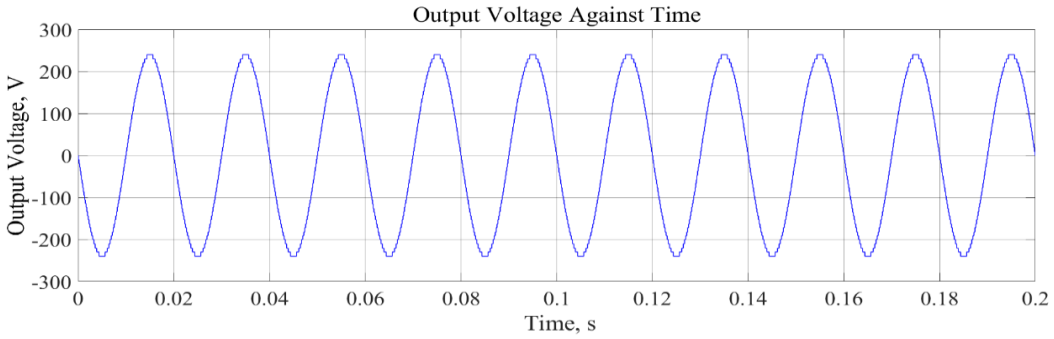


(b)

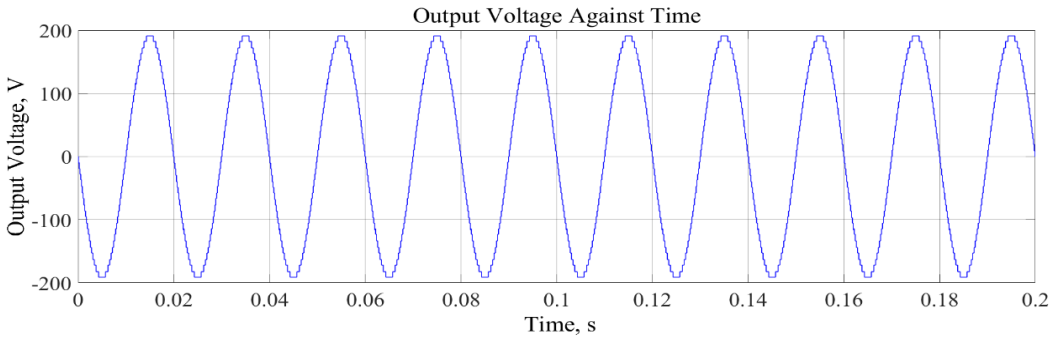
Figure 5.14: The voltage trains from (a) Part A and Part B, and (b) Part C

Figure 5.15 (a) to Figure 5.15 (d) show the voltage output for m = 1.0, 0.8, 0.5 and 0.3, respectively. Note that, in Figure 5.15 (a), the waveform was almost sinusoidal, which is the ideal form of the AC output. However, like the results from the previous configurations, the number of output levels (but for this case, the output level was less visible) decreased with m. The total level of the output voltage was 51-

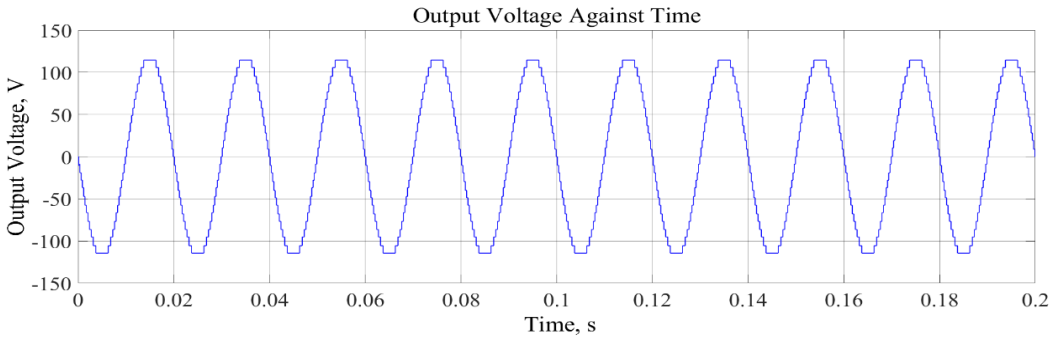
level when $m = 1.0$ *and* dropped to 41, 26, and 16 when m = 0.8, 0.5, and 0.3, respectively. Even though the number was diminishing, the total number of output voltage levels was still high even when m = 0.3. The THD percentage for every value of m is respectively shown in Figure 5.16 (a) to Figure 5.16 (d).



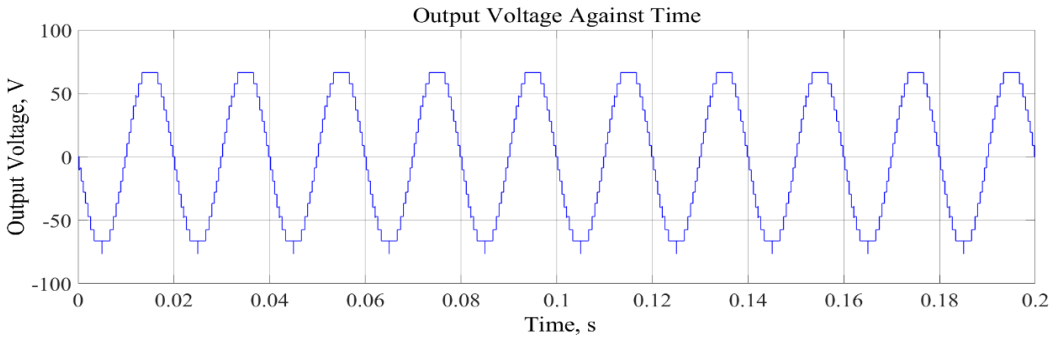
(a)



(b)



(c)

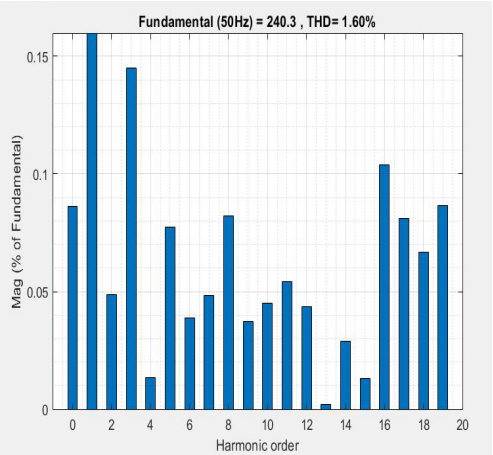


(d)

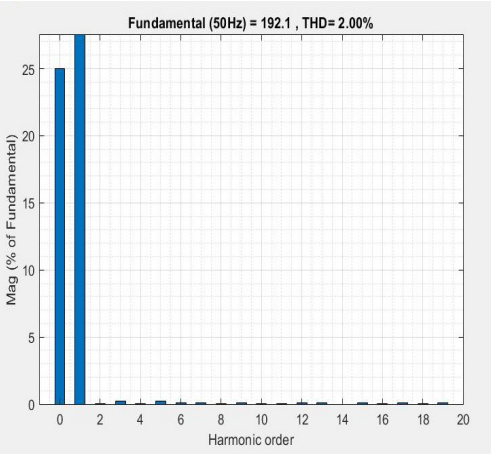
Figure 5.15: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

As indicated in Figure 5.16 (a) to Figure 5.16 (d), the THD percentage for every value of m was very small. THD percentage was 1.60% when *m* = 1.0, which is lesser than the allowable THD stipulated by IEEE. The THD did increase as *m* decreased, but the increment was still lesser than the allowable limit. When *m* = 0.3, however, the value was slightly higher than the limit by 0.7%. Additionally, during *m* = 0.3, the total output voltage was 16-level, which was almost comparable to the 17-level configuration when *m* = 1.0. Hence, it is worth assuming that this configuration is still efficient even when *m* = 0.3.

On the contrary, the fundamental voltage dropped with the modulation index. The fundamental voltage when *m* = 1.0 was 240.3 V and dropped gradually to 72.47 V when *m* = 0.3. The fundamental voltage (and the RMS voltage) and the THD percentage for every value of *m* are shown in Table 5.11.



(a)



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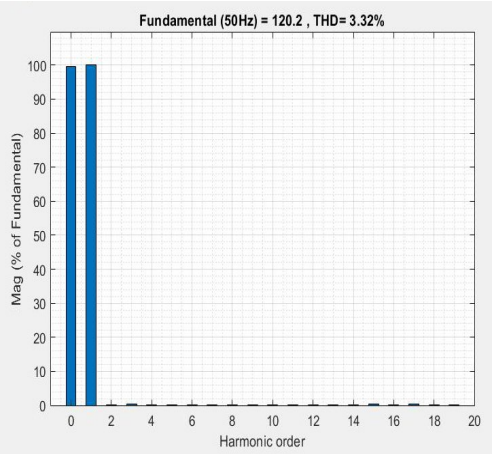
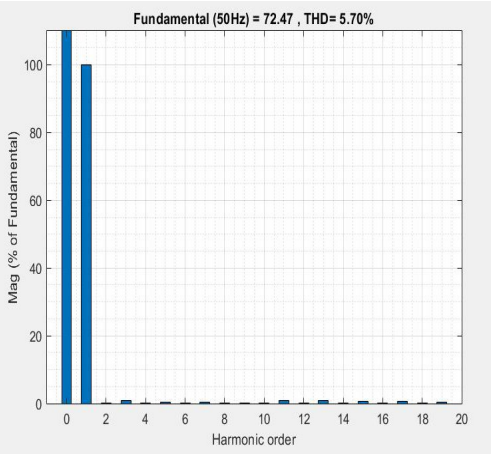


(c)



(d)

Figure 5.16: The harmonic orders when m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

Table 5.11: The parameters from the 51-level configuration

Modulation index, *m*	**Number of voltage levels, *n***	**THD Percentage, %**	**RMS Voltage, (V_{RMS}), V**	**Fundamental Voltage (V_{FND}), V**
1.0	51	1.60	169.90	240.30
0.8	41	2.00	135.90	192.10
0.5	26	3.32	85.00	120.20
0.3	16	5.70	51.24	72.47

The mean voltage and the mean current at all the switches are shown-in Table 5.12. Note that a higher mean current was observed at S_2, S_3, S_6, S_7, S_9, S_{10}, S_{11}, S_{12}, S_{13}, and S_{10}. These were the inner and floating switches. The higher current for inner switches might be caused by the clamping diode. As for the floating switches, it is unavoidable since the voltage share between these switches was greater as compared to the others. The voltage distribution was almost even between the lower and the

upper legs. It is worth noting that the voltage stress is equal for the parallel switches in H-bridge. The switching frequency for this configuration was 5 kHz.

Table 5.12: The mean current and voltage for every switch

Switch	Mean Current, A ($x10^{-2}$)	Mean Voltage, V
S_1	3.93	5.09
S_2	13.17	4.06
S_3	12.56	4.57
S_4	3.51	5.49
S_5	8.49	16.47
S_6	16.27	13.69
S_7	16.88	11.77
S_8	8.91	15.67
S_9	12.28	36.58
S_{10}	12.88	40.22
S_{11}	20.71	65.65
S_{12}	20.07	97.55
S_{13}	19.19	65.65
S_{14}	20.48	97.55

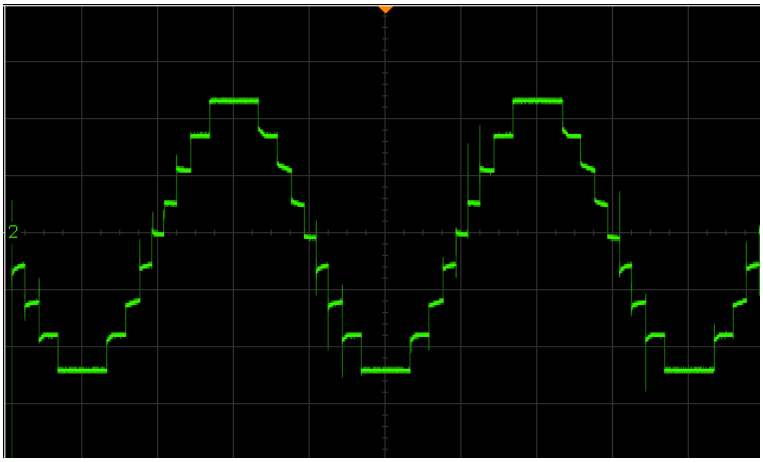
5.3 Experimental Testings Analysis

The experimental testings were carried out to validate the results obtained from those of the simulation. During this experimental validation test, for safety reasons, the output voltage was stepped down to 24 V for 9-level, 13-level, and 17-level configurations and to 37.5V for 51-level configuration (because of the difficulty of achieving 24 V precisely. The frequency was maintained at 50 Hz.

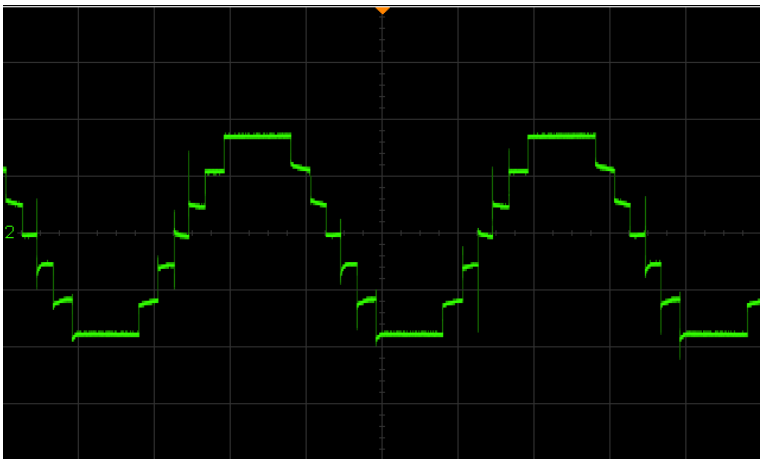
The experiments were conducted under no-load and loading conditions – where inductive-resistive load banks of 227.6 Ω and 0.55 H were added to the topology. Like in the simulations, they were repeated for every value of m = 1.0, 0.8, 0.5, and 0.3. The output voltage waveforms were captured using a digital oscilloscope while the THD percentage, RMS voltage, and RMS current were recorded using Fluke 43B (the value displayed is an RMS value). For an accurate comparison, the simulation was repeated using the same parameter as the experimental testing. The results from the experiments were recorded and compared with those obtained from the simulations.

5.3.1 9-level Configuration

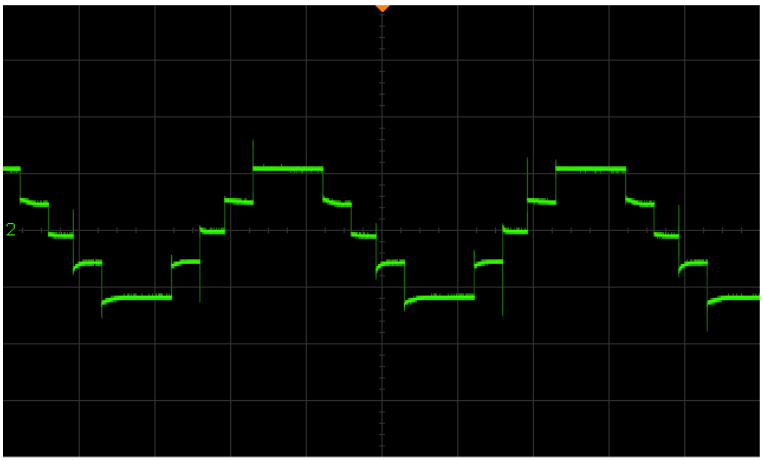
With the output voltage capped at 24 V, $V_1 = V_2 = V_3 = V_4 = 6$ V. Under the no-load condition, the current flow at the output was zero. The output voltage waveform for m = 1.0, 0.8, 0.5, and 0.3 are respectively shown in Figure 5.17 (a) to Figure 5.17 (d), respectively. Like in the simulation, the waveforms seemed to follow the same characteristic. The simulation result was therefore verified. The waveform was however not as smooth as that in the former. The roughness could be due to the harmonic interference from the DSP.



(a)



(b)



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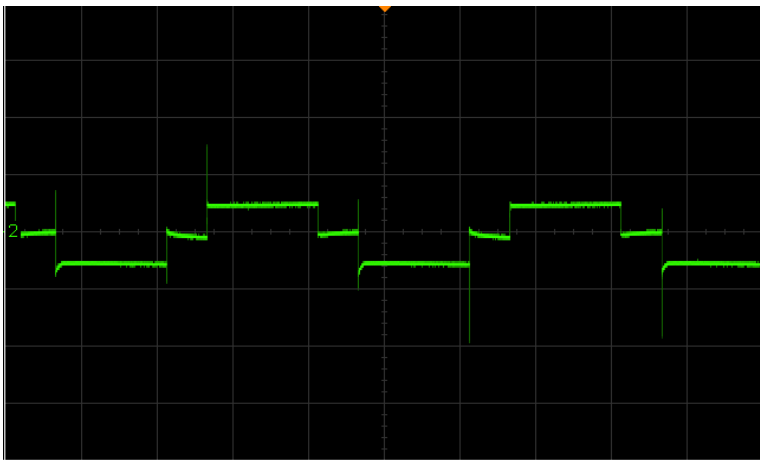


(d)

Figure 5.17: The output voltages for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

The THD percentages, frequencies, and RMS voltages for every value of m = 1.0, 0.8, 0.5, and 0.3 are respectively shown in Figure 5.18 (a) to Figure 5.18 (d). The THD percentage obtained during the experimental testing shared the same trend with those in the simulation, namely, as the value of m decreased, the THD percentage increased. RMS voltage however decreased with the value of m.

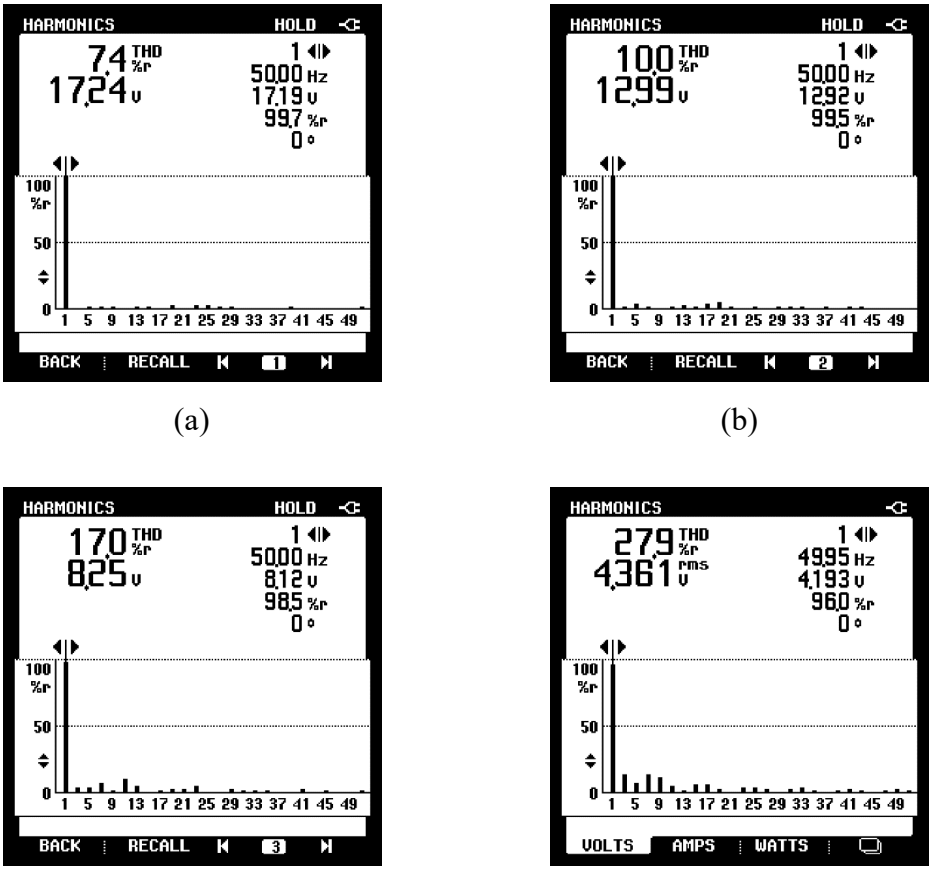


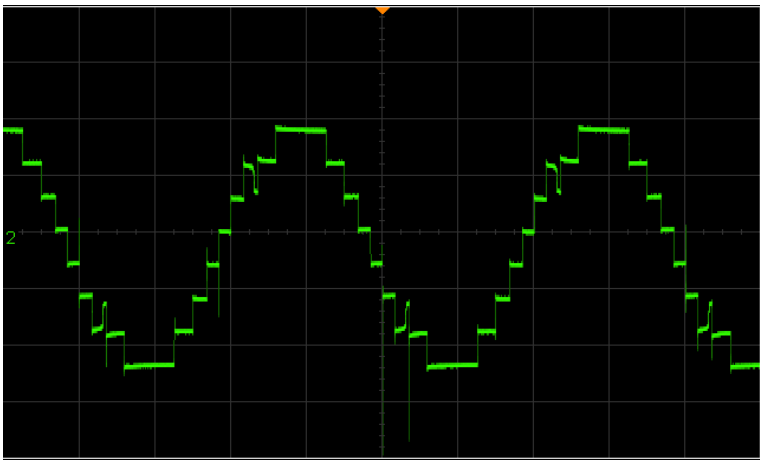
Figure 5.18: The voltage THD percentage for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

The results from the simulations and experiments are shown in Table 5.13. The experimental results were found to be lower than those from the simulation. This could be due to the type of switches being used in the experiments. -THD percentages showed higher percentage errors than the RMS voltages. On average, the percentage error for THD percentage and RMS Voltage was 13.01 and 5.10% respectively. The highest and lowest percentage error for THD percentage was 22.10% and 6.31% respectively, whereas for RMS Voltage, the highest was 11.20% and the lowest was 0.17%.

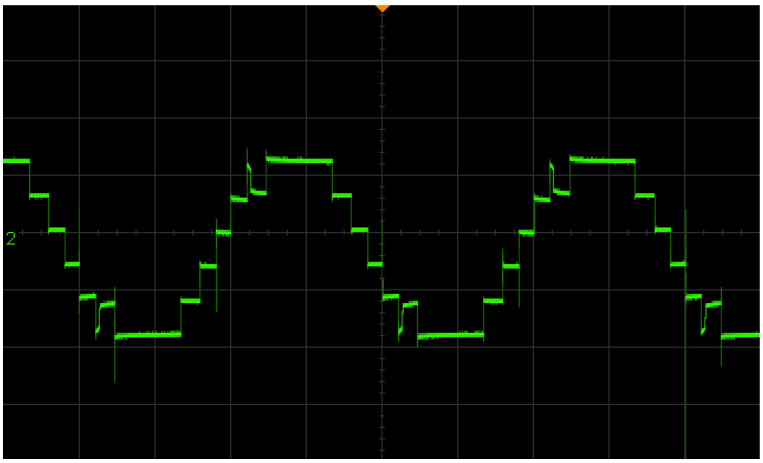
Table 5.13: Comparison between the results from the experiment and simulation for no-load condition

	THD Percentage			RMS Voltage, V_{RMS}		
Modul-ation index, *m*	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**
1.0	7.4	9.5	22.10	17.24	17.27	0.17
0.8	10.0	11.8	15.83	12.99	13.36	2.77
0.5	17.0	18.4	7.81	8.25	8.80	6.25
0.3	27.9	29.8	6.31	4.36	4.91	11.20

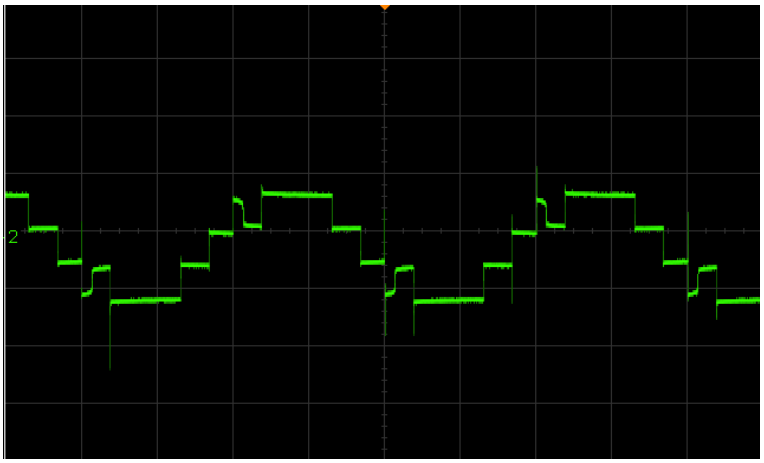
For loading conditions, the prototype was connected in parallel with 217.4 Ω and 556.5 mH resistive-inductive load (the output current was measured at the load side). The output voltage waveform for m = 1.0, 0.8, 0.5, and 0.3 are shown in Figure 5.19 (a) to Figure 5.19 (d).



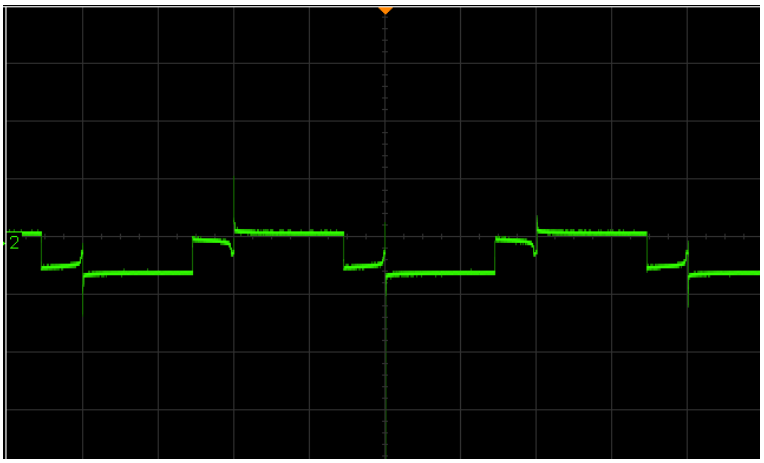
(a)



(b)



(c)



(d)

Figure 5.19: The voltage output voltages for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

As shown in Figure 5.19, the same pattern was exhibited in the output voltages for both loading and no-load conditions for every value of m, i.e. as the values of m decreased, the number of output voltage levels were also decreased. Unlike under no-load conditions, the shape of the waveform in the loading condition is a bit rougher. This roughness reflects the deterioration in the power quality.

Figure 5.20 (a) to Figure 5.20 (d) show the THD percentage and the RMS voltage for every value of m. Both seemed to share a similar trend to those from the simulation and when under no-load condition. As shown in Table 5.14, the THD percentages recorded were slightly higher than those in the simulation. This could be due to the harmonic coming from the loads and the DSP.

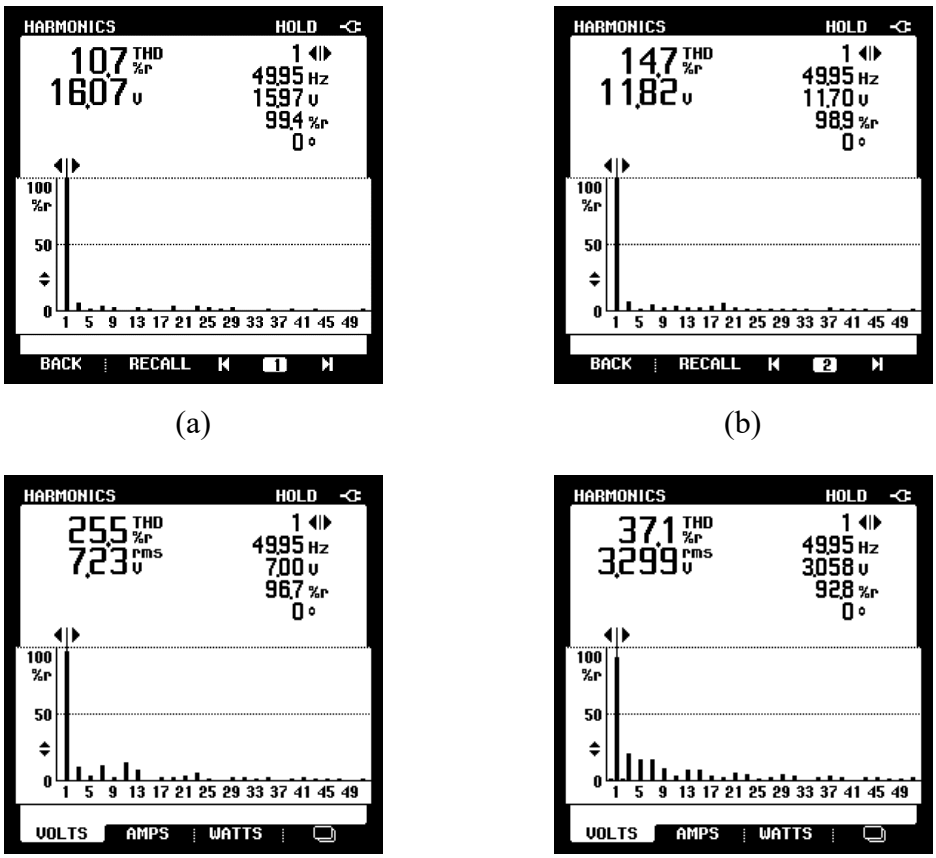


Figure 5.20: The voltage THD percentage for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

From Table 5.14, the THD percentage error average was 13.03%; the highest and lowest were 28.1% and 4.9% respectively. RMS voltage average was 17.28%, having the highest at 32.78% and the lowest at 6.95%.

Table 5.14: The comparison between experimental testing and simulation loading condition

	THD Percentage			**RMS Voltage, V_{RMS}**		
Modul-ation index, *m*	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**	**Experi-mental (V)**	**Simul-ation (V)**	**% Error (%)**
1.0	10.7	10.2	4.9	16.07	17.27	6.95
0.8	14.7	11.8	24.6	11.82	13.36	11.53
0.5	25.5	19.9	28.1	7.23	8.80	17.84
0.3	37.1	31.5	17.8	3.30	4.91	32.78

Figure 5.21 (a) to Figure 5.21 (d) show the respective RMS current for m = 1.0, 0.8, 0.5, and 0.3. The RMS current was smaller than the RMS voltage, but both have a similar trend; the RMS values increased when the value of m decreased.

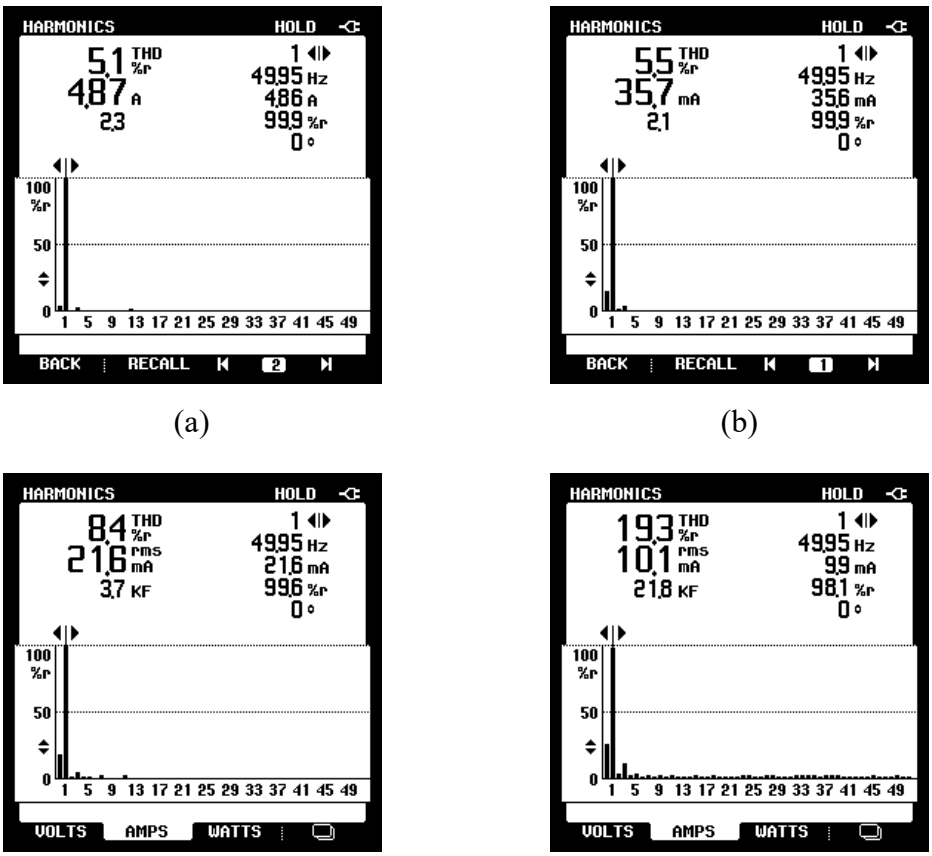
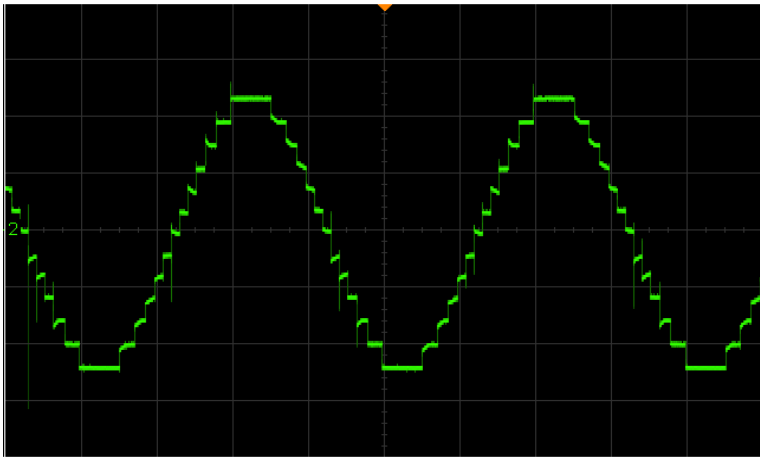


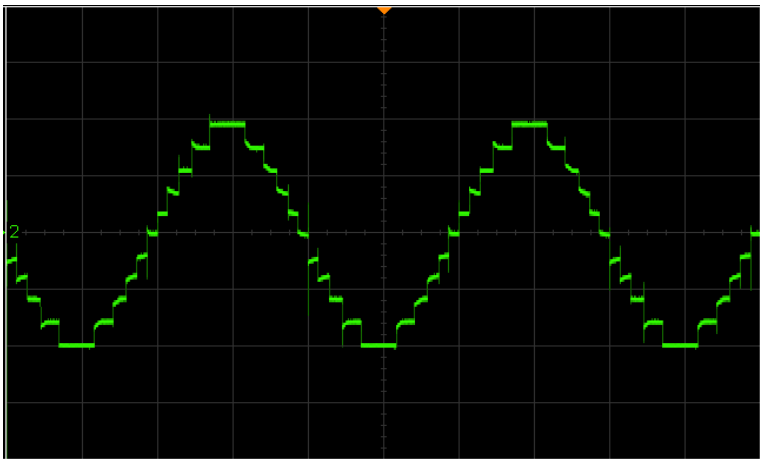
Figure 5.21: The current THD percentage for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

5.3.2 13-level Configuration

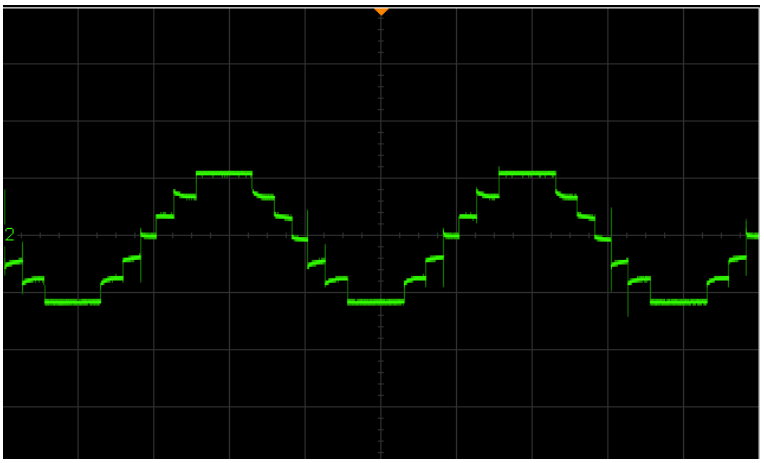
Given that the nominal voltage was 24 V, $V_1 = V_2 = 4$ V and $V_3 = V_4 = 8$ V. For the no-load condition, the current flow was zero. The voltage output waveforms observed for m = 1.0, 0.8, 0.5, and 0.3 are respectively shown in Figure 5.22 (a) to Figure 5.22 (d). The output waveforms exhibited the same trend as those in the simulation, where the total output voltage levels decreased with m.



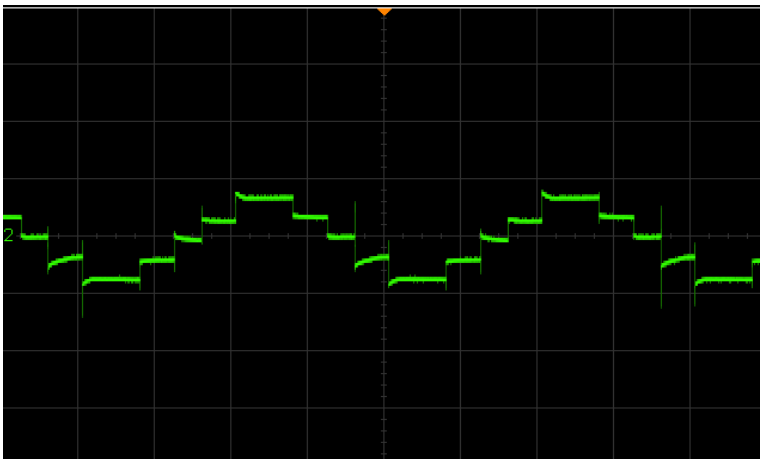
(a)



(b)



(c)

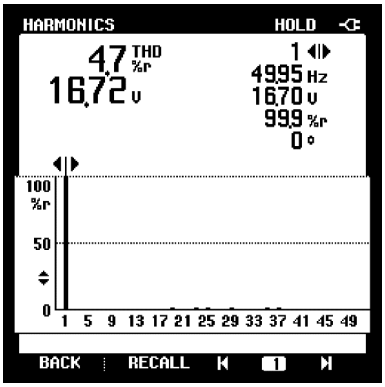


(d)

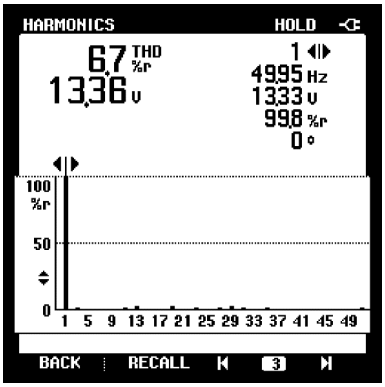
Figure 5.22: The output voltages for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

The THD percentage and the RMS voltage for every value of m are indicated in Figure 5.23 (a) to Figure 5.23 (d). Note that, as the value of m decreased, the THD percentage increased, but V_{RMS} decreased concurrently with m. The trend was similar to those of the simulation results, but the values were smaller.

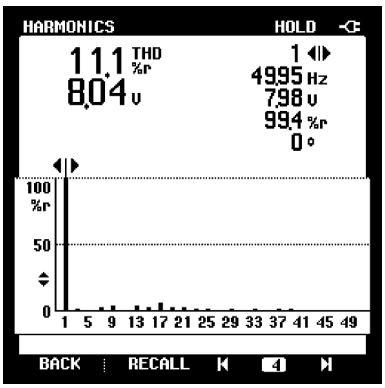
The THD percentage was 4.7% when m = 1, which was smaller than the allowable limit, but 1.7% higher than the allowable limit at 6.7% when m = 0.8. At m = 0.3, the THD percentage was the highest at 18.4%. At this point, the proposed MLI might require an output filter, but given that the V_{RMS} = 5.03 V, this configuration is no longer practical to be used.



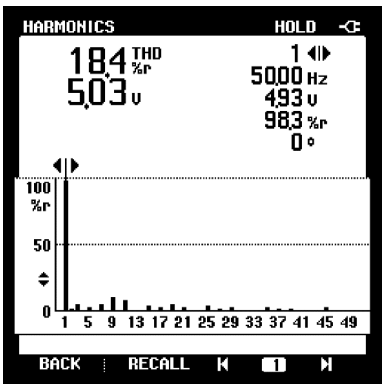
(a)



(b)



(c)



(d)

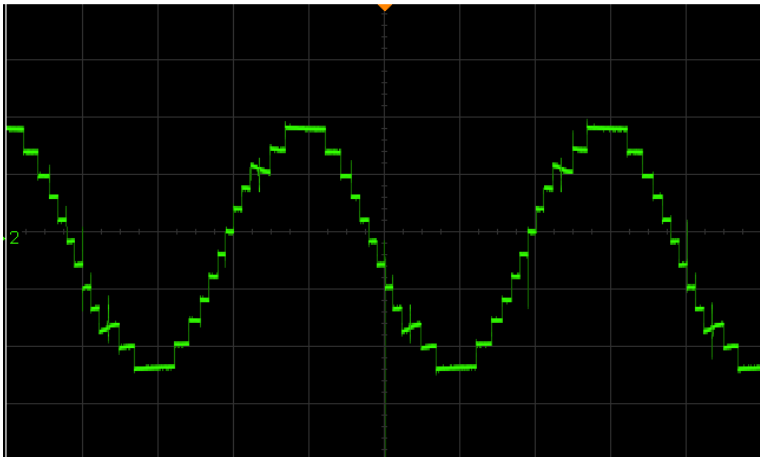
Figure 5.23: The voltage THD percentage for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

The results from the simulation and experiment are tabulated in Table 5.15. THD percentage average error was 21.75%, having the highest and the lowest at 34.4% and 10.3% respectively. V_{RMS} percentage average error was 1.53%, having the highest at 2.55% and the lowest at 0.67%.

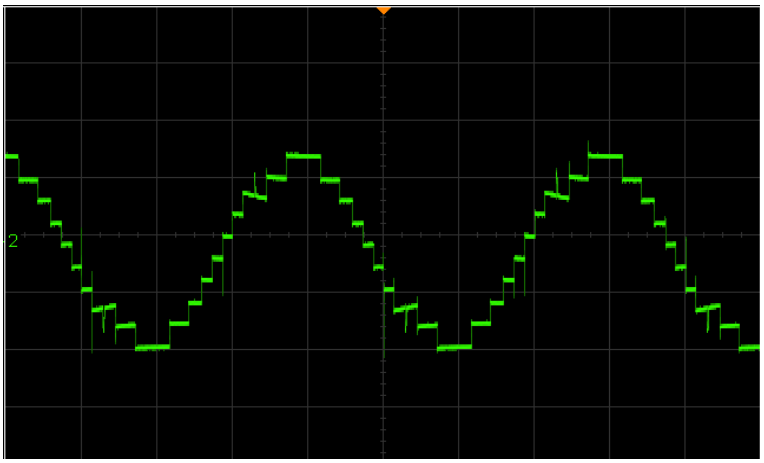
Table 5.15: The comparison between simulation and experimental testing for no-load condition

	THD Percentage			**RMS Voltage, V_{RMS}**		
Modul-ation index, *m*	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**	**Experi-mental (V)**	**Simul-ation (V)**	**% Error (%)**
1.0	4.7	7.2	34.4	16.72	17.04	1.88
0.8	6.7	8.8	23.4	13.36	13.45	0.67
0.5	11.1	12.4	10.3	8.04	7.84	2.55
0.3	18.4	22.6	18.7	5.02	4.97	1.01

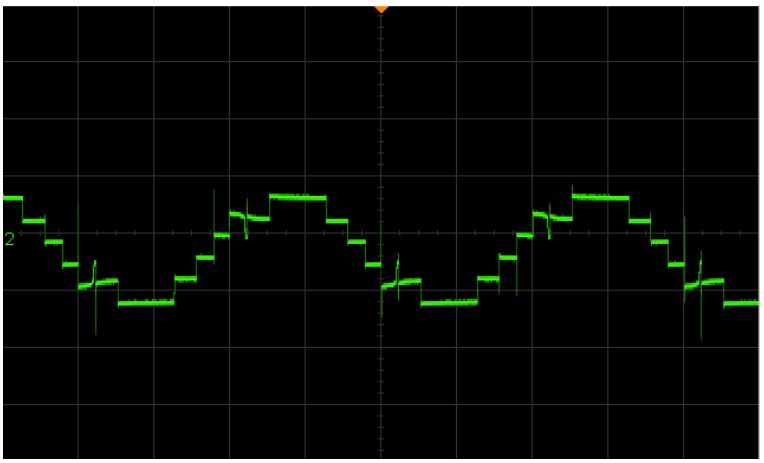
The output voltage waveforms for each value of m = 1.0, 0.8, 0.5, and 0.3 for loading condition are shown in Figure 5.24 (a) to Figure 5.24 (d) below. From Figure 5.24, it was observed that the output waveforms decreased along with the value of m. The waveforms were however not as smooth as those under no-load conditions. This might be due to the harmonic interference from DSP, load banks, or the switches.



(a)



(b)



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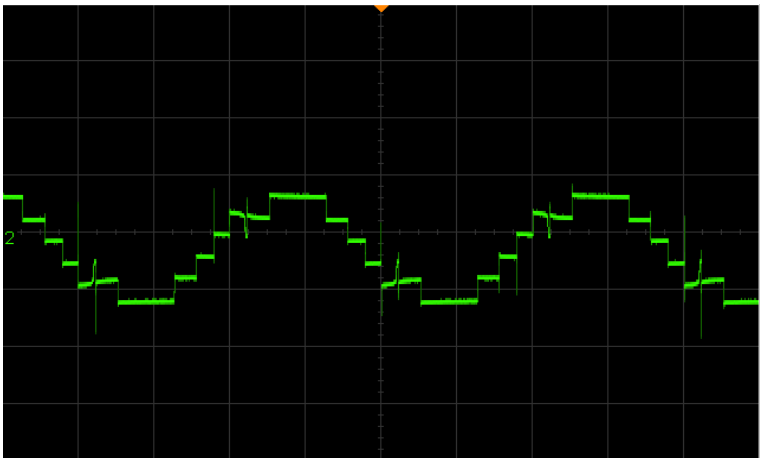
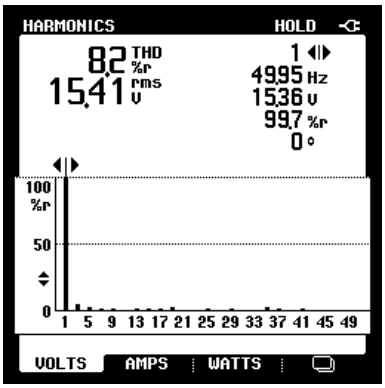


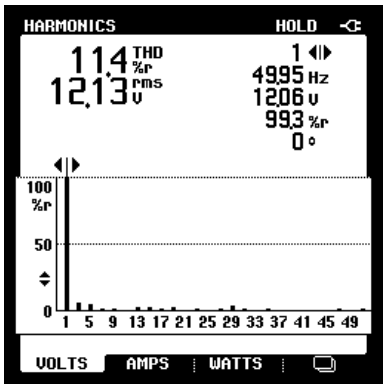
(d)

Figure 5.24: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

Figure 5.25 (a) to Figure 5.25 (d) show the THD percentage and the RMS voltage for every value of *m*. The THD percentage when *m* = 1.0 was 8.2%, 3.2% greater than the allowable limit. The THD percentage increased to 11.4%, 18.7%, and the highest was 35.9% which was when *m* = 0.3. At *m* = 0.3 and RMS voltage 3.9 V and THD percentage = 35.9%, this configuration was comparable to 9-level configuration when *m* = 0.3.



(a)



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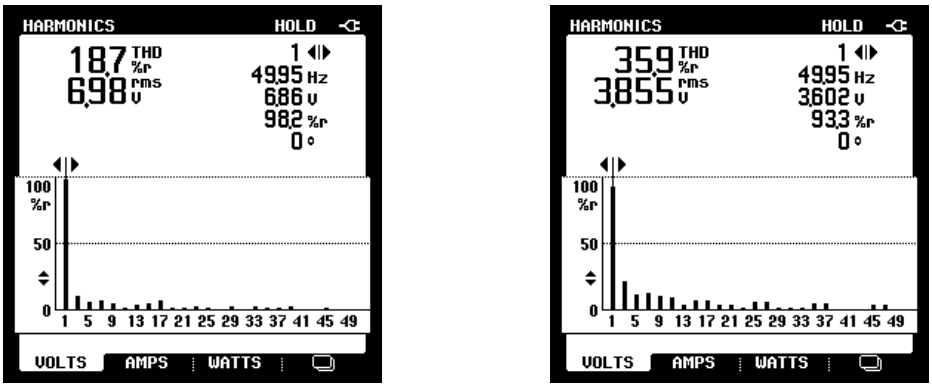


(c) (d)

Figure 5.25: The voltage THD percentage for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

Table 5.16 tabulated and compared the results from the simulation and experiment. The highest THD percentage error was 45.2% and the lowest was 4.73% with an average of 27.93%. Whereby the average error for V_{RMS} was 11.29%, having the highest at 19.96% and the lowest at 8.28%.

Table 5.16: The comparison between experimental and simulation for loading condition

	THD Percentage			**RMS Voltage, V_{RMS}**		
Modul-ation index, *m*	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**	**Experi-mental (V)**	**Simul-ation (V)**	**% Error (%)**
1.0	8.2	7.8	4.73	15.41	16.81	8.33
0.8	11.4	9.7	17.3	12.13	13.27	8.59
0.5	18.7	12.9	45.2	6.98	7.61	8.28
0.3	35.9	24.9	44.5	3.85	4.81	19.96

The RMS current and THD percentage current for every value of *m* were shown in Figure 5.26 (a) to Figure 5.26 (d). The THD percentage for the current was slightly lower than the THD percentage for voltage. The lowest THD percentage was 4.5% when *m* = 1.0 and the highest was 14.9% when *m* = 0.3. The RMS current was very small, but it is worth noting that the value decreases with the value *m*.

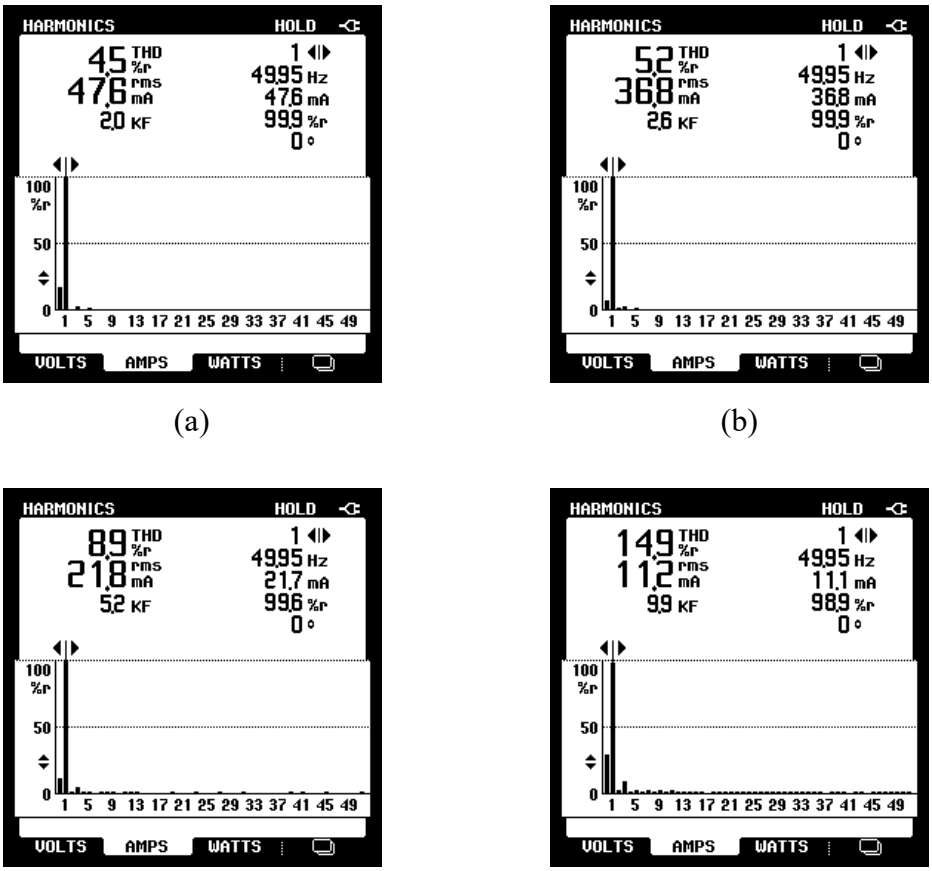
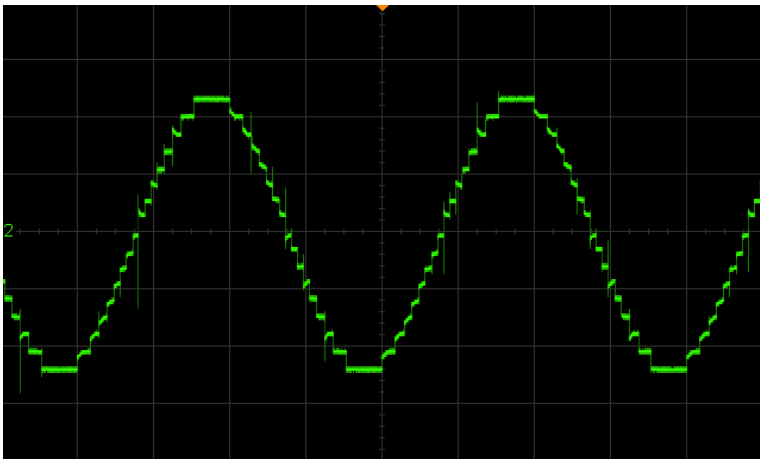


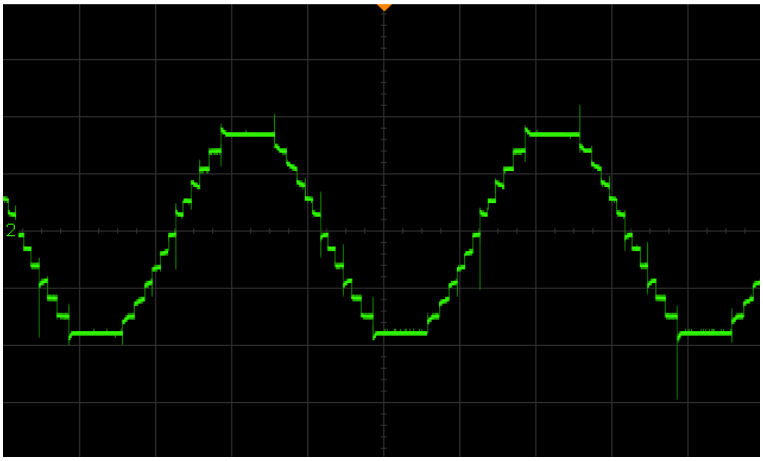
Figure 5.26: The current THD percentages for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

5.3.3 17-level Configuration

Having the output voltage capped at 24 V, $V_1 = V_2 = 3$ V and $V_3 = V_4 = 9$ V. The current was zero in the no-load condition. The output voltage waveform for m = 1.0, 0.8, 0.5, and 0.3 are shown in Figure 5.27 (a) to Figure 5.27 (d). Notice that the output waveform decreased from 17-level when m = 1.0, to 13-level, 9-level, and 5-level when m = 0.8, 0.5, and 0.3, respectively. This trend was similar to that of the simulation.



(a)



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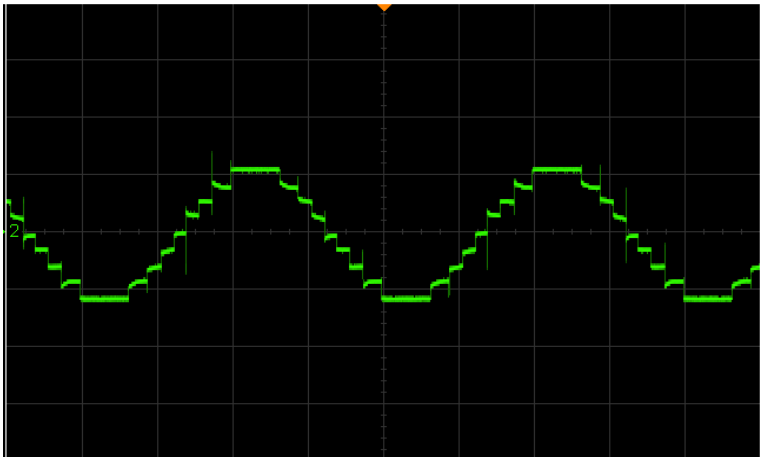
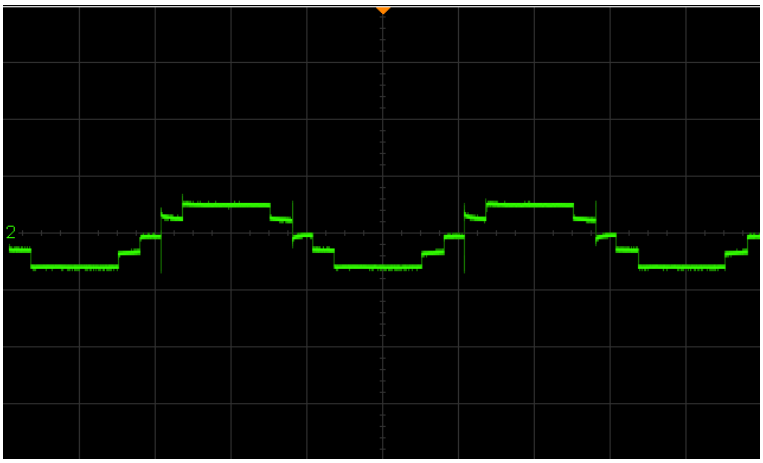


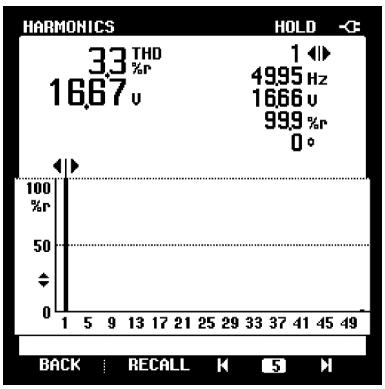
(c)



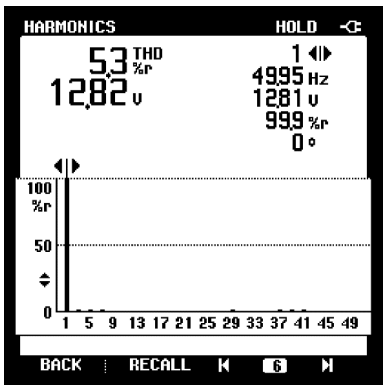
(d)

Figure 5.27: The output voltage for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

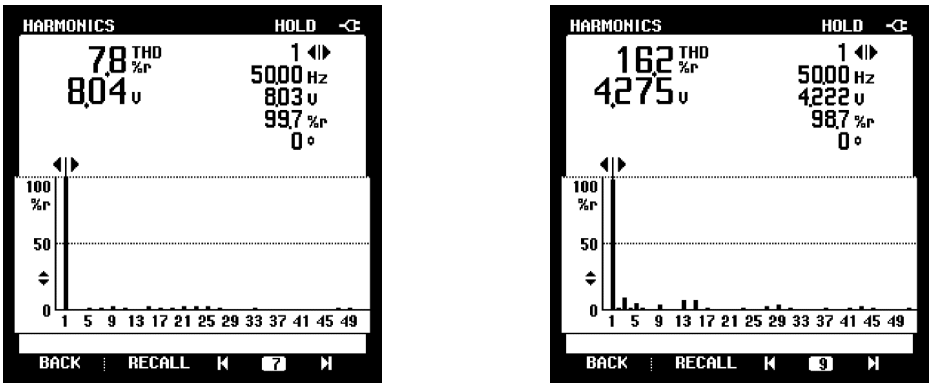
Figure 5.28 (a) to Figure 5.28 (d) show the THD percentage and the V_{RMS} for every value of m. The THD percentage increased as m decreased while RMS voltage increased with m. The THD percentage when m = 1.0 was 3.3%, smaller than the allowable limit. When m = 0.8, the THD percentage was 0.3% which was greater than the allowable limit. The highest THD percentage for this configuration is 16.2% which is when m = 0.3. When m = 0.5, topology performance was almost comparable to the 9-level configuration when m =1.0.



(a)



(b)



(c) (d)

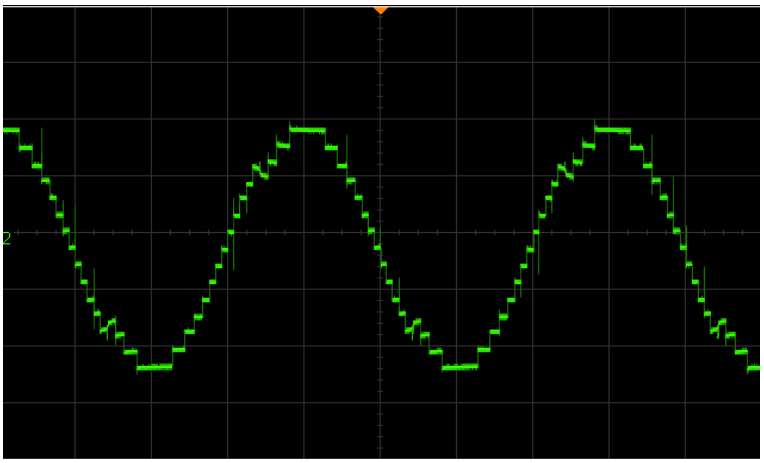
Figure 5.28: The voltage THD percentage for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

A detailed comparison between the simulation and experiment is shown in Table 5.17. THD percentage average error was 22.9%, having the highest and lowest at 35.3% and 12.9% respectively. V_{RMS} highest and lowest average errors were 11.2% and 0.50%, with an average of 4.73%.

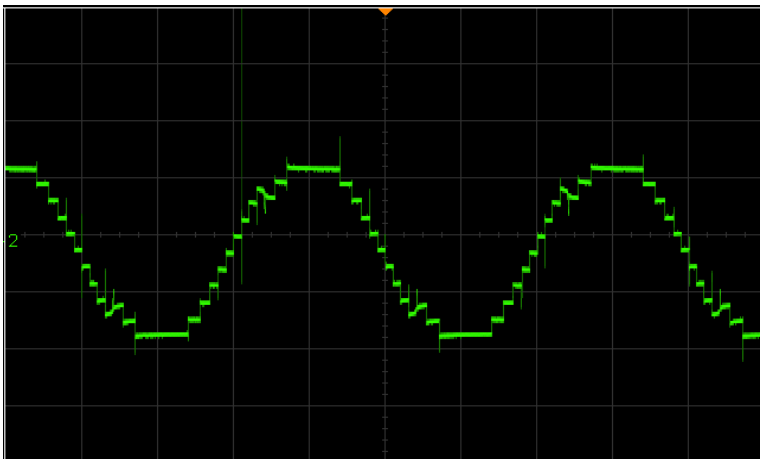
Table 5.17: The comparison between simulation and experimental testing for no-load condition

	THD Percentage			**RMS Voltage, V_{RMS}**		
Modul-ation index, *m*	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**	**Experi-mental (V)**	**Simul-ation (V)**	**% Error (%)**
1.0	3.3	5.10	35.3	16.67	17.15	2.80
0.8	5.3	6.87	19.1	12.82	13.41	4.40
0.5	7.8	9.82	24.3	8.04	8.08	0.50
0.3	16.2	18.59	12.9	4.28	4.82	11.2

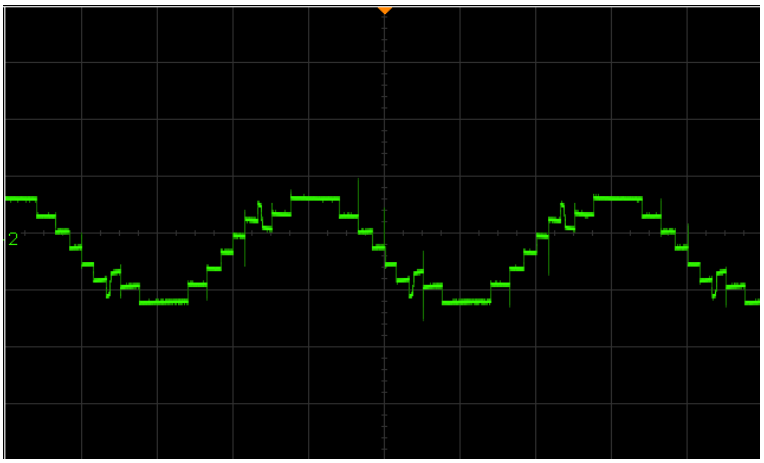
Figure 5.29 (a) to Figure 5.29 (d) show the output voltage waveforms when experimented with a resistive-inductive load that was connected in parallel to the prototype. The RMS current was also recorded.



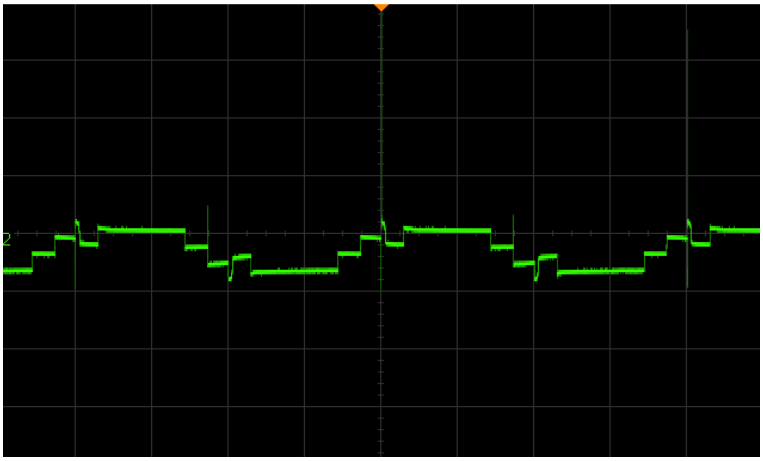
(a)



(b)



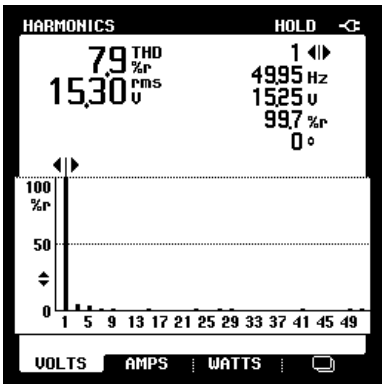
(c)



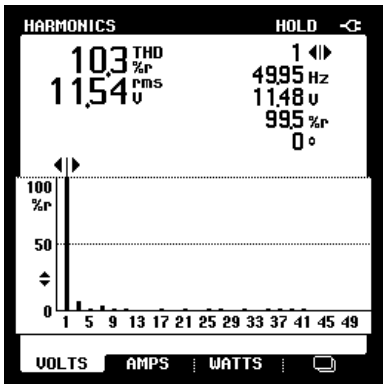
(d)

Figure 5.29: The output voltages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

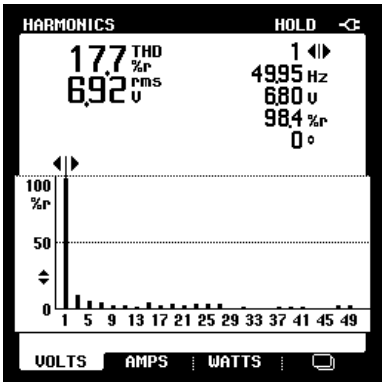
In Figure 5.29 (a) to Figure 5.29 (d), note that the output voltage levels decreased as *m* increased. This was similar to those in the simulation and from the no-load condition. However, the output waveform in the loading condition was slightly rougher than the one in the no-load condition. The roughness is the deterioration in the output quality. This can be seen from the THD percentage shown in Figure 5.30 (a) to Figure 5.30 (d).



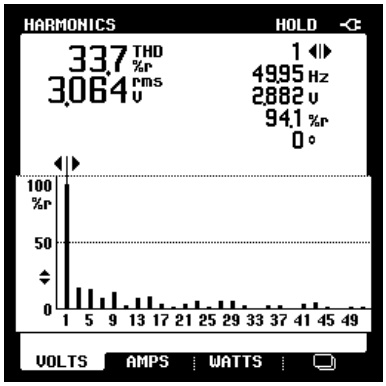
(a)



(b)



(c)



(d)

Figure 5.30: The voltage THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

The THD percentage shown in Figure 5.30 (a) to Figure 5.30 (d) is slightly higher compared to the THD percentage in the no-load condition. For example, the THD percentage when *m* =1.0 was 7.9% whereas for the no-load condition was 3.3%. Since 7.9% is more than 5.0% (the allowable limit), this configuration requires an output filter during the loading condition. Even so, the trend was similar to simulation and the no-load condition. There is also a huge difference between the loading and no-load V_{RMS}.

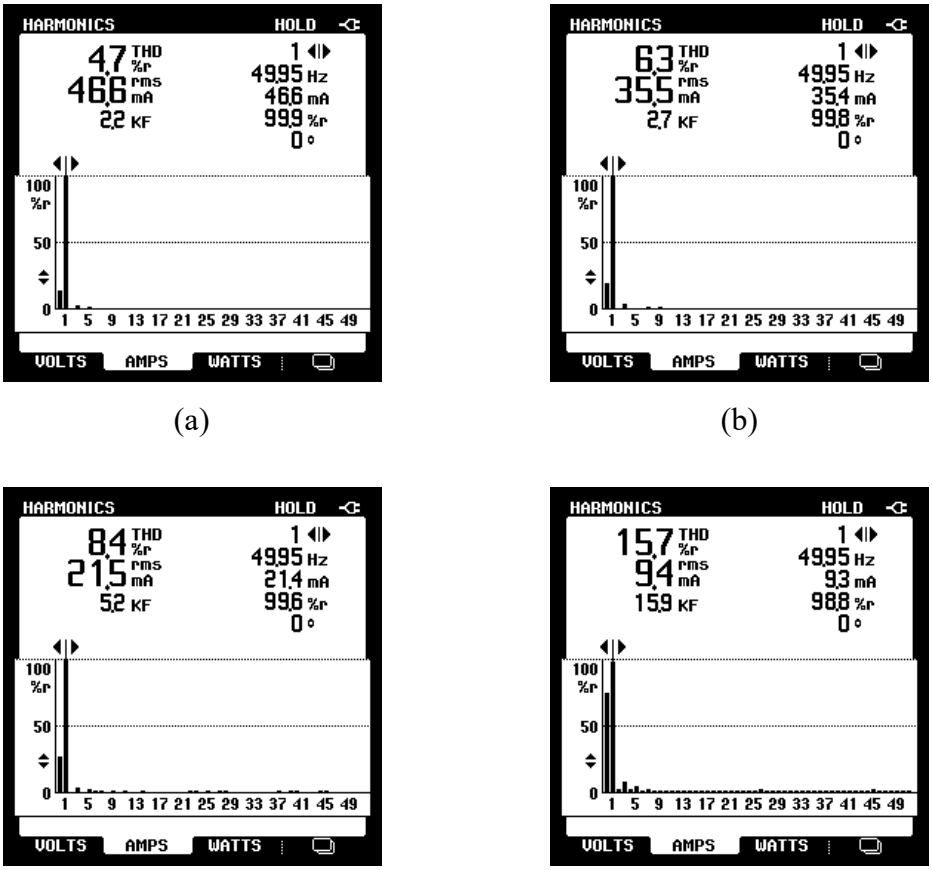
The results from the experimental and simulation are compared in Table 5.18. The average error for THD percentage was 50.5% with the highest being 77.2% and the lowest being 23.1%. Meanwhile, the average error for V_{RMS} was 16.13% with the highest being 34.62% and the lowest being 8.66%. Notice that during *m* = 0.3, the percentage error for THD percentage was 77.2%.

Table 5.18: The comparison between experimental testing and simulation for loading condition

	THD Percentage			**RMS Voltage, V_{RMS}**		
Modul-ation index, *m*	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**	**Experi-mental (V)**	**Simul-ation (V)**	**% Error (%)**
1.0	7.9	6.4	23.1	15.30	16.75	8.66
0.8	10.3	7.9	29.9	11.54	13.03	11.44
0.5	17.7	10.3	71.8	6.92	7.67	9.78
0.3	33.7	19.0	77.2	3.06	4.68	34.62

Figure 5.31 (a) to Figure 5.31 (d) show the THD percentage for the current. Notice that the THD percentage for current also increased as *m* decreased, similar to

the THD percentage for voltage. However, as compared to the voltage, the THD percentage for the current was smaller. The RMS current also decreased with *m* similar to the RMS voltage.



(a) (b)

(c) (d)

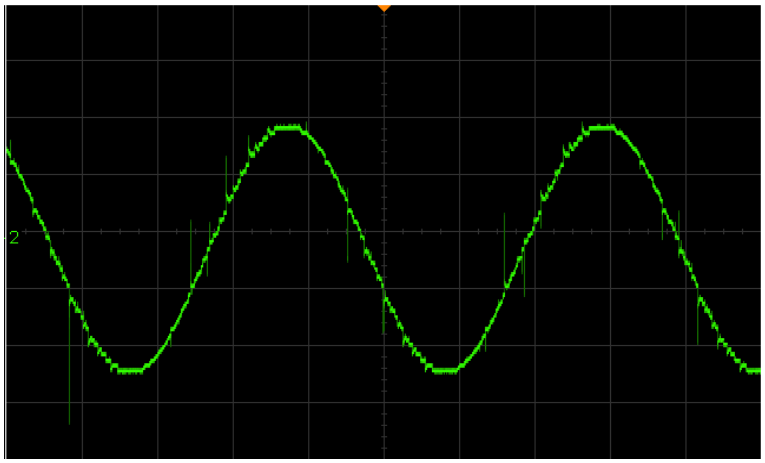
Figure 5.31: The current THD percentages for *m* = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

5.3.4 51-level Configuration

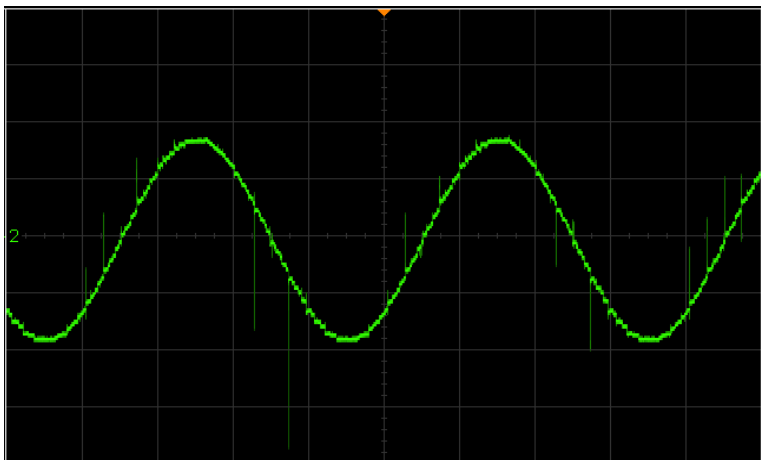
The total voltage was capped at 37.5 V resulted in $V_1 = V_2 = 1.5$ V, $V_3 = V_4 = 4.5$ V, and $V_5 = 25.5$ V. In the no-load condition, the current flow is zero. Hence, only RMS voltage was recorded using FLUKE 43B.

The output voltage waveform for *m* = 1.0, 0.8, 0.5, and 0.5 are shown in Figure 5.32 (a) to Figure 5.32 (d). The output voltage waveform was almost sinusoidal when *m* = 1.0. Unlike in the previous configuration, the staircase shape was not visible which make it difficult to count the total number of output levels. However, the effect of the decreasing *m* can be seen from the amplitude of output voltage. The output voltage

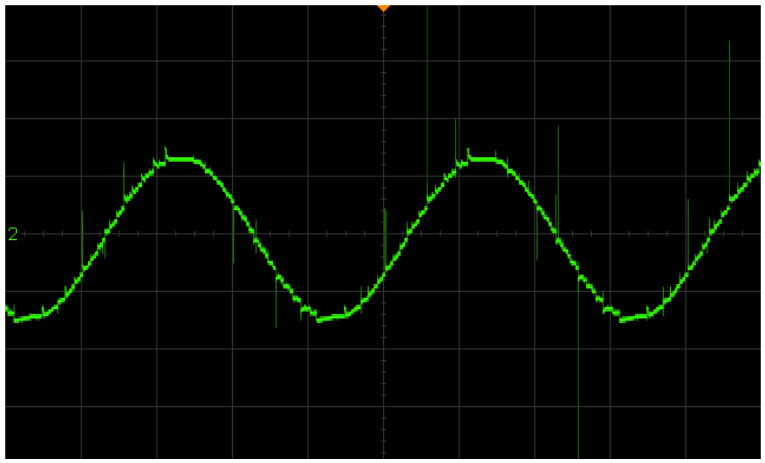
waveform in Figure 5.32 (a) to Figure 5.32 (d) show that the amplitude of the output voltage decreased with *m*. This was supported by the decreasing value of RMS voltage.



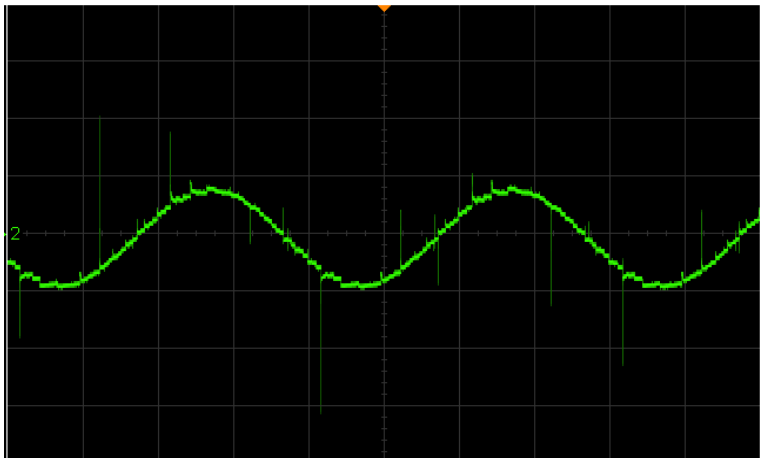
(a)



(b)



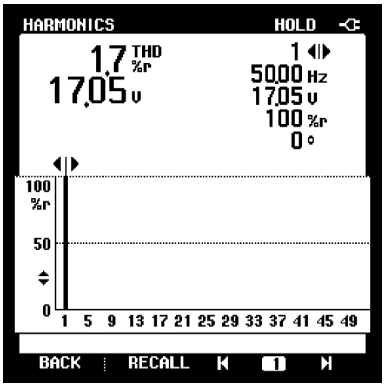
(c)



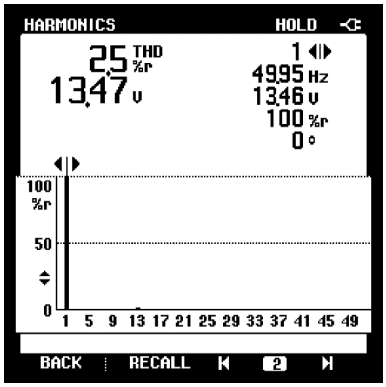
(d)

Figure 5.32: The output voltages for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

The THD percentage for every value of m is shown in Figure 5.33 (a) to Figure 5.33 (d). The experimented THD percentage was generally lesser than the allowable limit. The THD percentage showed a similar trend to the simulation; the smaller the value of m, the greater the THD percentage. The experimental and the simulation results are compared in Table 5.19.



(a)



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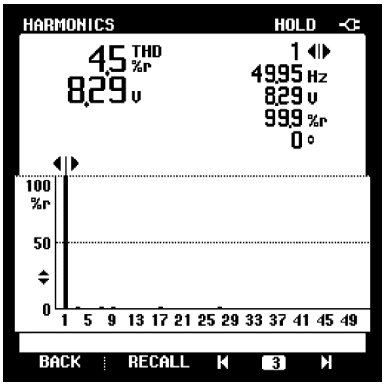

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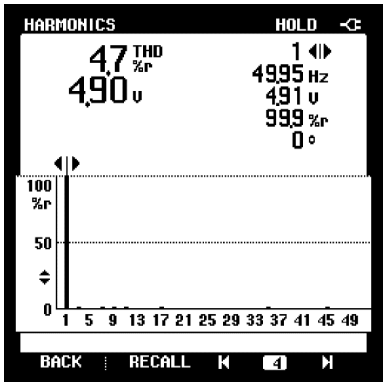


(d)

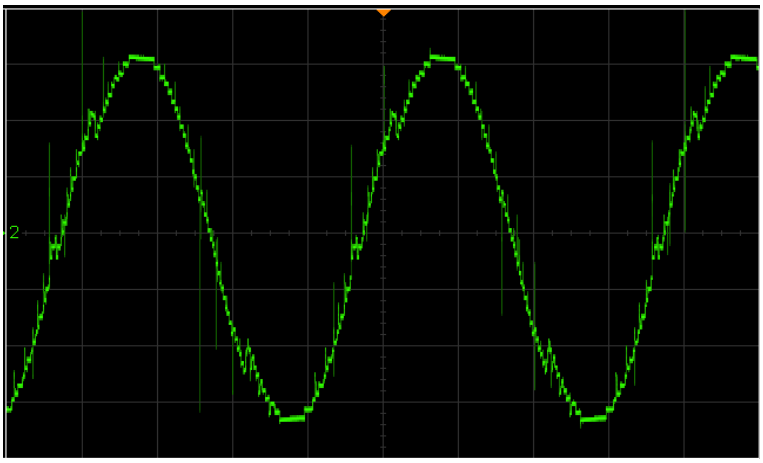
Figure 5.33: The voltage THD percentages for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

Notice that the THD percentage in experimental testing was smaller than in the simulation. However, it was the other way round for the RMS voltage. This might be caused by the harmonic interference from the switches and the DSP. The average error for THD percentage is 20.4% with the lowest being 7.1% and the highest being 31.1%. Averagely, the RMS voltage error is 36.6% with 36.0% being the lowest and 37.6% being the highest.

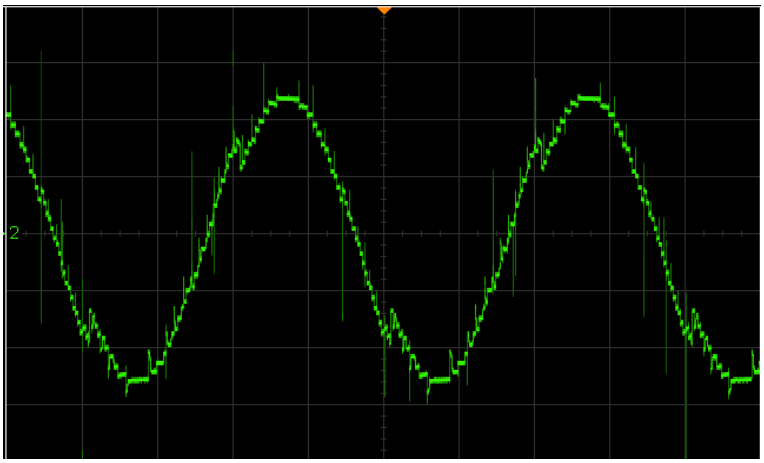
Table 5.19: The comparison between experimental and simulation results for no-load condition

	THD Percentage			**RMS Voltage, V_{RMS}**		
Modul-ation index, *m*	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**	**Experi-mental (V)**	**Simul-ation (V)**	**% Error (%)**
1.0	1.7	1.8	7.1	17.05	26.64	36.0
0.8	2.5	2.1	18.5	13.47	21.19	36.4
0.5	4.5	3.6	25.0	8.29	13.06	36.5
0.3	4.7	6.8	31.1	4.90	7.85	37.6

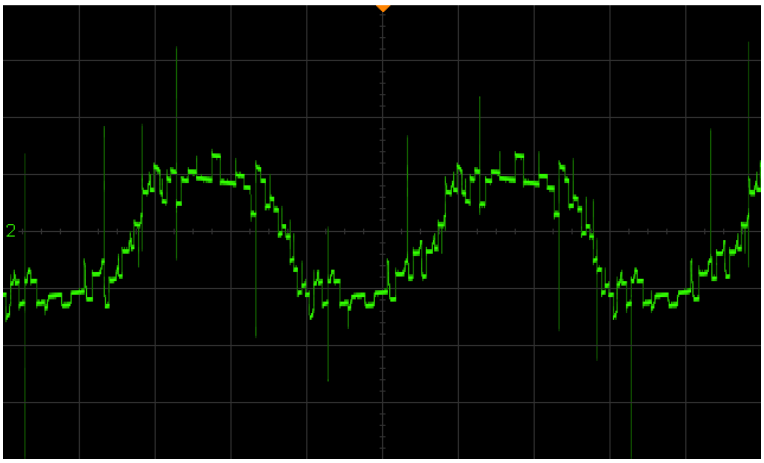
An inductive-resistive load was added to the prototype for the loading condition. The output voltage waveform for m = 1.0, 0.8, 0.5, and 0.3 are respectively shown in Figure 5.34 (a) to Figure 5.34 (d).



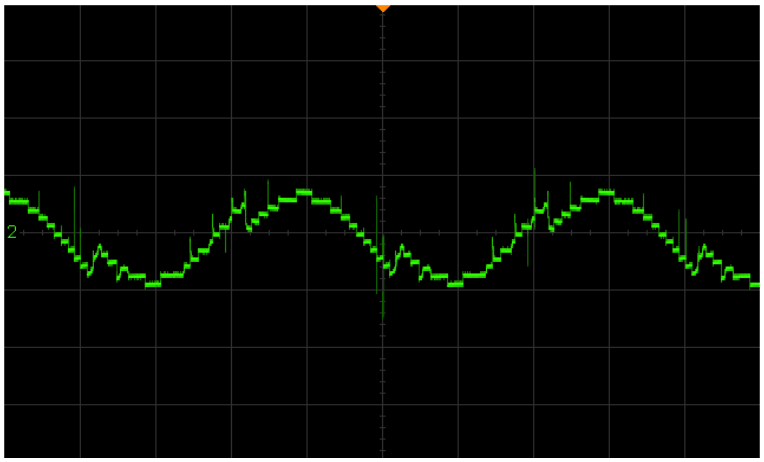
(a)



(b)



(c)



(d)

Figure 5.34: The output voltages for m = (a) 1.0, (b) 0.8, (c) 0.5, and (d) 0.3

Notice the output voltage waveforms in Figure 5.34 (a) to Figure 5.34 (d) were more distorted than those in simulation and in the no-load condition. However, they all shared a similar trend. Like in the no-load condition, the staircase shape is not noticeable and the waveform is almost sinusoidal. The amplitude of the waveform decreases gradually with m, except when m = 0.5, where the waveform distorted heavily and lost its sinusoidal form. This might be caused by harmonic interference.

Since m = 0.5 had ruined the trend, the experimental testing was repeated with m = 0.4. The output waveform is shown in Figure 5.35. Unlike Figure 5.34 (c), the waveform shown in Figure 5.35 was as anticipated. Therefore, when m = 0.5 was excluded from the analysis, the trend appeared to be similar to the no-load condition; the total output voltage levels (the output voltage waveform) decreased with m.

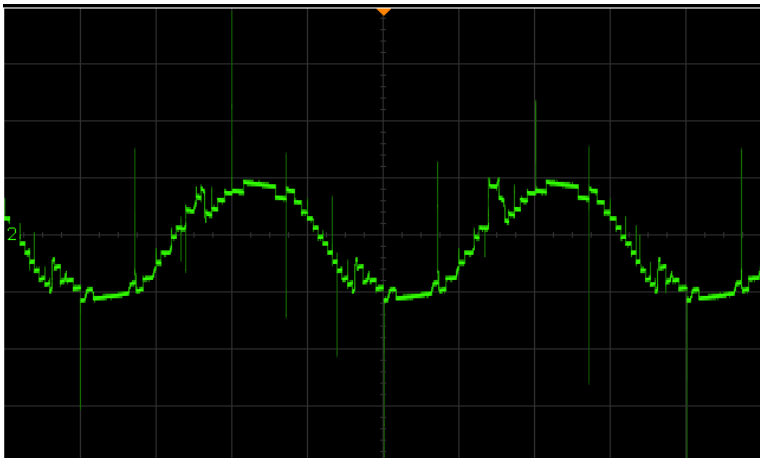
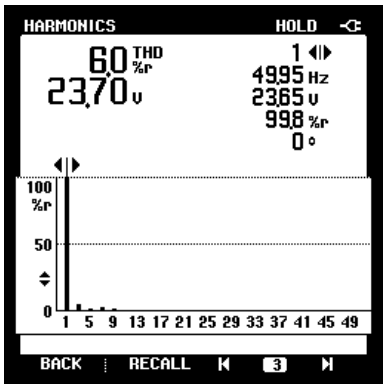
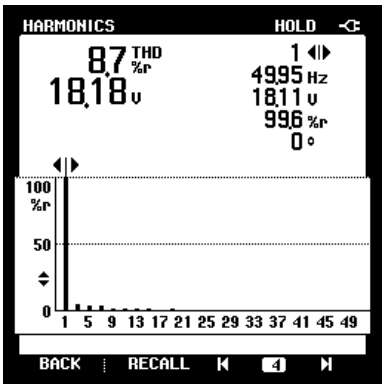


Figure 5.35: The voltage output for m = 0.4

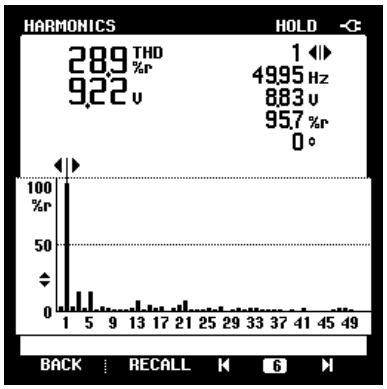
The THD percentage and the RMS voltage for m = 1.0, 0.8, 0.5, 0.4, and 0.3 are shown in Figure 5.36 (a) to Figure 5.36 (e). The THD percentage increased as m decreased. The distortion in the output waveform shown in Figure 5.34 (a) to Figure 5.34 (d) is reflected in the THD percentage. Generally, the THD percentage is higher in the loading condition. Notice that when m = 1.0 the THD percentage is almost 5 times the percentage of the value in the no-load condition. When m = 0.3, the THD percentage is comparable to the value from the other configurations even though the total voltage output level is high. The THD percentage for m = 0.5 is 28.9% which is higher than when m = 0.3 and m = 0.4.



(a)



(b)



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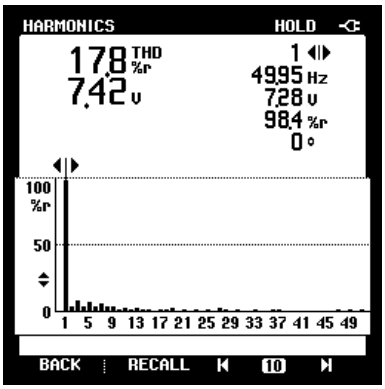

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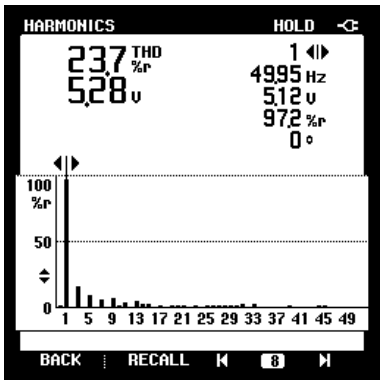

(e)

Figure 5.36: The THD percentages for m = (a) 1.0, (b) 0.8, (c) 0.5, (d) 0.4, and (e) 0.3

The results from the simulation and experiment are tabulated and compared in Table 5.20. The percentage error was extremely big in THD percentage, having the highest at 436.18% which was when m = 0.5. This explains the output voltage waveform shown in Figure 5.34 (c). However, the percentage error is also high for the other value of m. The average error is 208.18% with the highest being 436.18% and the lowest being 109.6%. As for the RMS voltage, the average error is 20.94% with the highest being 27.82% and the lowest being 9.37%.

Table 5.20: The comparison between experimental and simulation for loading condition

	THD Percentage			**RMS Voltage, V_{RMS}**		
Modul-ation index, *m*	**Experi-mental (%)**	**Simul-ation (%)**	**% Error (%)**	**Experi-mental (V)**	**Simul-ation (V)**	**% Error (%)**
1.0	6.0	2.87	109.6	23.70	26.15	9.37
0.8	8.7	3.23	169.4	18.18	20.80	12.57
0.5	28.9	6.39	436.2	9.22	12.73	27.57
0.4	17.3	6.33	173.3	7.42	10.28	27.82
0.3	23.7	9.39	152.4	5.28	7.27	27.37

Figure 5.37 (a) to Figure 5.37 (e) showed the RMS current (in milliampere, taken using Fluke 43B) for the value of m = 1.0, 0.8, 0.4, and 0.3 and its THD percentage. The THD percentage seemed to increase as m decreased but RMS current dropped with m decreased. Compared to the voltage, the THD percentage and the RMS current were smaller.

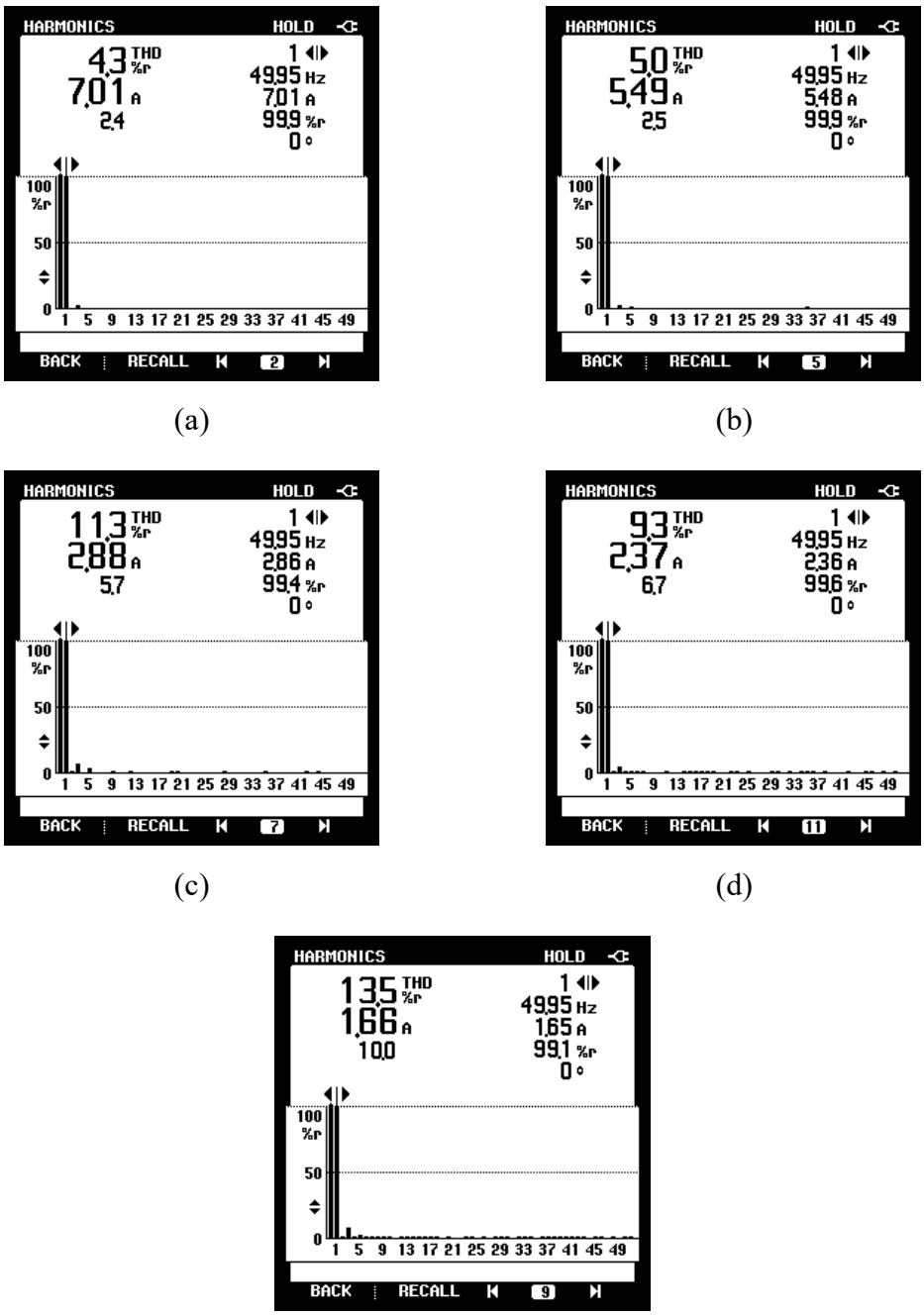

Figure 5.37: The THD percentage for m = (a) 1.0, (b) 0.8, (c) 0.5, (d) 0.4, and (e) 0.3

5.4 Conclusion

Two trends can be observed in the data analysis; (i) the THD percentage increased as modulation decreased and (ii) the output voltage decreased with the modulation index. Both simulation and experimental results satisfied these trends despite having a high percentage error.

THD percentage indicates the quality of the output (voltage or current). Hence, the smaller the THD percentage the better the output voltage. Theoretically, the THD percentage can be improved by producing a higher level of output voltage. As the level of output voltage increases, the staircase-like waveform becomes more like an ideal AC waveform. This can be seen from the 51-level output voltage. In some configurations, the percentage error between the simulated THD percentage and the experimental THD percentage was very high. This might be due to the harmonic interference from the power supplies, switches, DSP, or load banks (Pinyol, 2015).

Meanwhile, the output voltage waveform described the output voltage and the total number of output voltage levels. The number of levels decreased with *m* but was somehow related to the THD percentage. The THD percentage for the same level of the output voltage is comparable despite the value of *m*. For example, the THD percentage for 17-level configuration and 9-level configuration when they produced a 9-level of the output voltage are both equal to 9.44%.

In the case of output voltage (fundamental and RMS voltage), it was solely varied with the value of *m*. The values are almost the same in every configuration given the same value of *m*. The slight difference was due to the DC offset. The percentage error between the simulation and experimental was also smaller than the THD percentage. This might be caused by the accuracy of the measuring instruments or the DC supplies.

Similar trends were also observed in the output current. However, the THD percentage in the output voltage was lesser than in the output voltage. The RMS current was also small and recorded in milliampere.

Chapter 6:
Comparative Analysis & STATCOM

6.1 Chapter Introduction

The operation of the proposed topology has been verified through simulations and experimental testings. Both of these verification methods performed showed that the proposed topology had successfully produced 9-level, 13-level, and 17-level of output voltage with 18 components, and 23 components for a 51-level configuration. This proposed topology achieved a THD percentage below 5% (IEEE standard for applications below 69 kV) from 17-level and 51-level configurations. This chapter includes a comparative analysis of the proposed topology with the conventional MLIs and the topologies presented by other researchers in previous years. It also details the proposed topology implementation in STATCOM as an example power industry application.

6.2 Comparative Analysis

This comparative analysis demonstrates the novelty of this study by comparing the proposed topology against the conventional MLIs and the topologies presented by other researchers in previous years. The comparison is made in terms of the total number of output voltage levels, the design complexity, and the THD percentage.

6.2.1 Comparison with Conventional MLI

This comparison is to demonstrate the superiority of the proposed topology over the conventional MLIs. Conventional MLIs include CHB-MLI, DC-MLI, and FC-MLI. CHB-MLI was the earliest MLI and its distinct feature is the isolated DC sources. The isolated DC source gives the MLI its modularity and high immunity to failure. However, CHB-MLI is unfavorable to use if the DC source is limited. Hence, DC-MLI was introduced.

DC-MLI uses a capacitor bus to distribute voltage instead of using multiple DC sources. Clamping diodes are also utilized by DC-MLI to enhance the output voltage level. Hence, a significant number of components are used to yield higher output voltage levels. This high component usage issue was solved by FC-MLI, in which the

clamping diodes are replaced by capacitors to induce a higher level of output voltage. This results in a simpler topology.

The comparison between the proposed topology with the conventional MLIs is tabulated in Table 6.1, Table 6.2, Table 6.3, and Table 6.4 for 9-level, 13-level, 17-level, and 51-level of output voltage, respectively. The proposed topology is abbreviated to PT-9 for 9-level configuration, PT-13 for 13-level configuration, PT-17 for 17-level configuration, and PT-51 for 51-level configuration for tabulation purposes.

Table 6.1: The comparison between conventional MLIs and the proposed topology to produce 9-level of output voltage.

	CHB-MLI	**DC-MLI**	**FC-MLI**	**PT-9**
DC sources	4	1	1	4
Capacitor bus	0	8	8	0
Power switches	16	16	16	10
Clamping diode	0	56	0	4
Flying capacitor	0	0	28	0
Total components	20	81	53	18

Table 6.2: The comparison between conventional MLIs and the proposed topology to produce 13-level of output voltage.

	CHB-MLI	**DC-MLI**	**FC-MLI**	**PT-13**
DC sources	6	1	1	4
Capacitor bus	0	12	12	0
Power switches	24	24	24	10
Clamping diode	0	132	0	4
Flying capacitor	0	0	66	0
Total components	30	169	103	18

Table 6.3: The comparison between conventional MLIs and the proposed topology to produce 17-level of output voltage.

	CHB-MLI	**DC-MLI**	**FC-MLI**	**PT-17**
DC sources	8	1	1	4
Capacitor bus	0	16	16	0
Power switches	32	32	32	10
Clamping diode	0	240	0	4
Flying capacitor	0	0	120	0
Total components	40	289	169	18

Table 6.4: The comparison between conventional MLIs and the proposed topology to produce 51-level of output voltage.

	CHB-MLI	**DC-MLI**	**FC-MLI**	**PT-51**
DC sources	25	1	1	5
Capacitor bus	0	50	50	0
Power switches	100	100	100	14
Clamping diode	0	2450	0	4
Flying capacitor	0	0	1225	0
Total components	125	2601	1375	23

From Table 6.1, CHB-MLI, DC-MLI, and FC-MLI require 20, 81, and 53 components, respectively to produce a 9-level of output voltage. From Table 6.2, they require 30, 169, and 103 components, respectively to produce a 13-level of output voltage. From Table 6.3, they require 40, 289, and 169 components, respectively to produce a 17-level of output voltage. Finally, from Table 6.4, they require 125, 2601, and 1375 components, respectively to produce a 51-level output voltage.

On the contrary, the proposed topology maintains 18 components for 9-level, 13-level, and 17-level configurations whereas 23 components are used to yield 51-level of output voltage. The comparison is simplified in Figure 6.1.

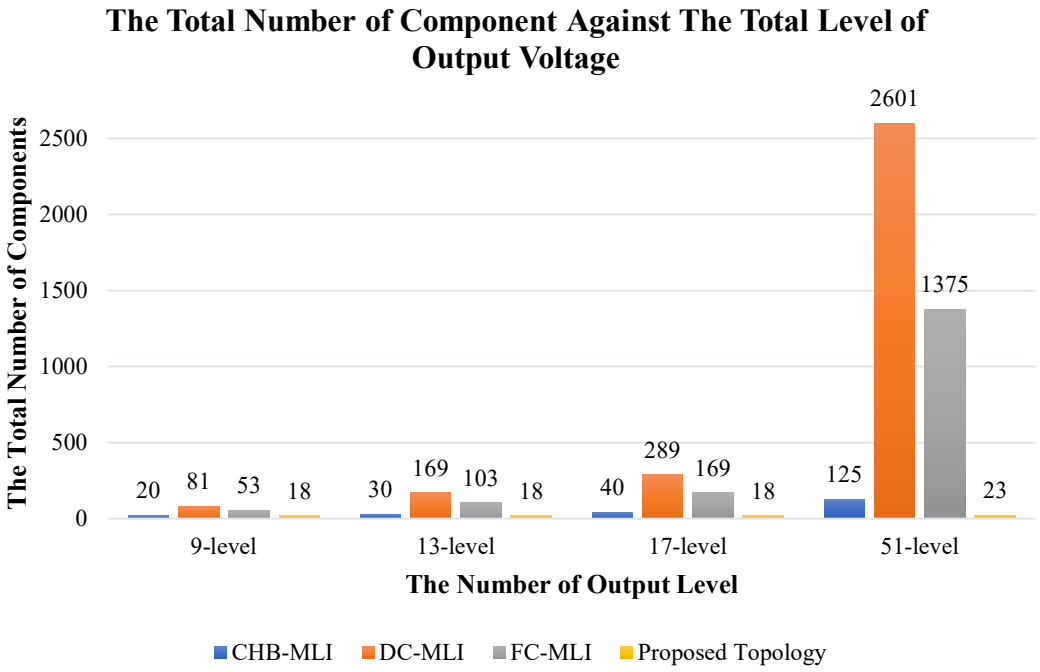

Figure 6.1: The comparison between the number of components and the number of voltage output levels for CHB-MLI, DC-MLI, FC-MLI, and the proposed topology.

From the tabulation made in Table 6.1 to Table 6.4, notice that the conventional MLIs were utilizing the same number of switches to yield the same voltage output level. The overall total number of components used varied due to the inclusion of capacitors and/or diodes. DC-MLI had the highest due to the presence of both capacitors and diodes, followed by FC-MLI which only had capacitors installed. CHB-MLI employed neither capacitor nor diode. The number of components used to generate a 9-level of output voltage was comparable to the proposed topology.

The number of components utilized by the conventional MLIs (including CHB-MLI) to produce 13-level, 17-level, and 51-level increased tremendously. DC-MLI, the highest, increased by more than 100%, reaching 2601 at 51-level configuration. FC-MLI were having the same trend, exceeding 1000 at 51-level configuration. Having more components used would result in a much bulkier design, complex system, and more costly to produce. These drawbacks make the conventional MLI less convenient for application.

However, due to the isolated DC source, CHB-MLI can be configured asymmetrically (Gupta & Jain, 2014), reducing the number of components utilized. For example, (Mohapatra, et al., 2020) used asymmetric CHB-MLI to produce a 9-level of output voltage. It used only 10 components — 8 switches and 2 DC sources

instead of 20 components in a symmetrical configuration. Despite the reduction in the component counts, it is somewhat difficult for the configuration to be cascaded to increase the level of output voltage.

6.2.2 Comparison with Recently Presented MLI

Unlike conventional MLI, recently presented MLIs undoubtedly have lessened the number of components used. They are more compact than the conventional MLIs and have a low THD percentage due to their ability to produce a higher level of output voltage.

Most of the recently presented topologies have a basic unit that can be further cascaded to achieve a higher level of output voltage. They also opt for an isolated DC source instead of DC-link capacitors to avoid voltage imbalance problems. Isolated DC sources also make it easier for the topologies to be configured asymmetrically to increase the level of output voltage.

The basic unit (i.e., not cascaded) for the recently presented topologies has component counts that are comparable to the proposed topology. However, unlike the proposed topology, some presented topologies need an H-bridge attached to determine the polarity of the output (Abdulhamed & Dr. A. H. Esuri, 2021; Mondol, Biswas, Hosain, Samad, & Rahman, 2019; Roodmajan, Monfared, & Ashan, 2017; Shankar, Edward, Kumar, & Raglend, 2017; Vineeth, Mukundam, & Jayaprakash, 2021). The downside of this design is the H-bridge inverter increases the total standing voltage (Sarebanzadeh, et al., 2021).

An additional circuit is also required when implementing asymmetrical configuration as presented in (Roodmajan, Monfared, & Ashan, 2017). The topologies in (Alishah, Nazarpour, Hosseini, & Sabahi, 2014) and (Babadi, Salari, Mojibian, & Bina, 2017) need different calculations to determine the voltage sources for asymmetrical configuration. On the contrary, the asymmetrical voltage sources for the proposed topology are either binary (1:2) or trinary (1:3) that generate up to 17-level of output voltage.

Table 6.5 shows a comparison between the proposed topology and the topologies presented in (Abdulhamed, Esuri, & Abodhir, 2021), (Vineeth, Mukundam, & Jayaprakash, 2021), and Hybrid Cascaded Multilevel Inverter (HCHB) presented in (Mohapatra, et al., 2020). These topologies produce 9-level of output voltage. For tabulation purposes, the proposed topology is abbreviated as PT-9, PT-13, PT-17, and

PT-51 for 9-level configuration, 13-level configuration, 17-level configuration, and 51-level configuration, respectively.

Table 6.5: Comparison between PT-9, (Mohapatra, et al., 2020), (Vineeth, Mukundam, & Jayaprakash, 2021), and (Abdulhamed, Esuri, & Abodhir, 2021)

Topology	**HCHB** (Mohapatra, et al., 2020)	(Vineeth, Mukundam, & Jayaprakash, 2021)	(Abdulhamed, Esuri, & Abodhir, 2021)	**PT-9**
Number of DC sources	2	4	2	4
Number of switches	8	12	7	10
Number of diodes	0	0	3	4
Number of capacitors	0	0	0	0
Total components	10	16	12	18
THD percentage	10.40%	-not mentioned-	13.53%	9.44%

All topologies in Table 6.5 used isolated DC sources. This allows the topologies to be cascaded and configured asymmetrically. Generally, (Mohapatra, et al., 2020), (Vineeth, Mukundam, & Jayaprakash, 2021), and (Abdulhamed, Esuri, & Abodhir, 2021) used fewer components than in the proposed topology.

(Abdulhamed, Esuri, & Abodhir, 2021) used 2 DC sources, 7 switches, and 3 diodes. This topology used fewer components than the proposed topology but the THD percentage for the same level of the output voltage is higher in the former. This topology used an asymmetrical configuration and the ability to further increase the level of output voltage was however not discussed in the paper.

As for (Mohapatra, et al., 2020), the topology presented is a conventional CHB-MLI with an asymmetrical (voltage ratio 1:3) configuration. It used 10 components, which halved the component counts of CHB-MLI in a symmetrical configuration. It has a higher THD percentage despite having fewer components than the proposed topology. This paper also did not mention its ability to further increase the level of output voltage. However, it is possible to increase the level of output voltage by cascading the symmetrical configuration CHB-MLI.

(Vineeth, Mukundam, & Jayaprakash, 2021) used 4 DC sources and 12 switches in its configuration. 4 of the switches were connected in an anti-series connection to build two sets of bidirectional switches. Bidirectional switches are

convenient to control but they have high conduction loss. In some applications, they require snubbers for safe commutation (Bland, Wheeler, Clare, & Empringham, 2001; Klumpner, Blaabjerg, & Nielsen, 2001; Klumpner & Blaabjerg, 2006). In addition, this topology can be configured asymmetrically to produce a higher level of output voltage. The same number of components was used to generate 13-level and 17-level output voltage.

Table 6.6 shows the comparison between (Vineeth, Mukundam, & Jayaprakash, 2021) and the 17-level configuration. The number of components for both topologies is similar to Table 6.5. These topologies used trinary asymmetrical configurations. Although (Vineeth, Mukundam, & Jayaprakash, 2021) used fewer components than the proposed topology, it has a higher THD percentage than the latter.

Table 6.6: Comparison between PT-17 and (Vineeth, Mukundam, & Jayaprakash, 2021)

Topology	(Vineeth, Mukundam, & Jayaprakash, 2021)	**PT-17**
Number of DC sources	4	4
Number of switches	12	10
Number of diodes	0	4
Number of capacitors	0	0
Total components	16	18
THD percentage	5.79%	4.91%

PT-51 is compared with (Shankar, Edward, Kumar, & Raglend, 2017), (Hosseinzadeh, et al., 2019), and (Mondol, Biswas, Hosain, Samad, & Rahman, 2019). The topologies were chosen because their structures are almost similar to the proposed topology despite having different total levels of output voltages. The comparison is tabulated in Table 6.7.

Table 6.7: Comparison between PT-51, (Shankar, Edward, Kumar, & Raglend, 2017), (Hosseinzadeh, et al., 2019), and (Mondol, Biswas, Hosain, Samad, & Rahman, 2019)

Topology	(Shankar, Edward, Kumar, & Raglend, 2017)	(Hosseinzadeh, et al., 2019)	(Mondol, Biswas, Hosain, Samad, & Rahman, 2019)	**PT-51**
Number of DC sources	4	5	1	5
Number of switches	12	10	22	14
Number of diodes	4	4	17	4
Number of capacitors	0	0	18	0
Total components	20	19	58	23
Number of output voltage	31	31	37	51
THD percentage	10.22%	-not mention-	2.25%	1.78%

(Shankar, Edward, Kumar, & Raglend, 2017) introduced as sub-MLI that utilized 4 DC sources, 8 switches, and 4 diodes. The sub-MLI was connected to one H-bridge for polarity generation. With the H-bridge in place, the number of components used to produce a 31-level of output voltage is higher than those used by the proposed topology to produce 51-level of output voltage. This topology has successfully produced a higher level of output but the THD percentage is also high. The figure is almost equivalent to the THD percentage obtained from the 9-level configuration.

The topology presented in (Hosseinzadeh, et al., 2019) is a cell that consists of 5 DC sources, 10 switches, and 4 diodes. It used a binary algorithm (1:2:4) for asymmetric configuration and can be cascaded to achieve a higher level of output voltage. The asymmetric topology presented in this paper produced 31-level of output voltage. The number of components used is comparable to those used by the proposed topology to produce 51-level of output. The THD percentage is not mentioned in the paper.

(Mondol, Biswas, Hosain, Samad, & Rahman, 2019) used 1 DC source, 22 switches, 17 diodes, and 18 capacitors to produce 37-level of output voltage. This topology is the extension of a simple cell. It used an H-bridge inverter for polarity generation. The number of components used by this topology is greater than those in the 51-level configuration. To produce 51-level of output voltage, the quantity of components used is also expected to increase.

In conclusion, the proposed topology (9-level, 13-level, 17-level, and 51-level configurations) has successfully reduced the number of components compared to the conventional MLIs. This results in a compact and less complicated MLI topology. However, when compared with the topologies proposed recently, the number of components to produce the same level of output voltage is comparable.

Nonetheless, the proposed topology aces in terms of its structure. It does not require a complicated calculation to determine unequal voltage sources (Babadi, Salari, Mojibian, & Bina, 2017), additional circuits for asymmetrical configuration (Roodmajan, Monfared, & Ashan, 2017), bidirectional switches that have a high conduction loss (Vineeth, Mukundam, & Jayaprakash, 2021), an H-bridge inverter for polarity generation output (Mondol, Biswas, Hosain, Samad, & Rahman, 2019; Roodmajan, Monfared, & Ashan, 2017; Shankar, Edward, Kumar, & Raglend, 2017, Abdulhamed & Dr. A. H. Esuri, 2021, Vineeth, Mukundam, & Jayaprakash, 2021). This results in a simple mechanism that is easy to use.

6.3 STATCOM as an Example of Industrial Application

This study implemented a 51-level configuration into a STATCOM using the control method proposed in (Haw, Dahidah, & Almurib, 2014). The advantages of using this method are the design simplicity and the ability to improve the transient response of the STATCOM. It also provides PF correction. Furthermore, it utilizes the availability of the variables (i.e., the grid PCC voltage and STATCOM voltage V_{PCC} and STATCOM voltage, V_C) to achieve good transient without forsaking the dynamic performance. According to (Haw, Dahidah, & Almurib, 2014), the proposed method can be used with any kind of topology. Hence, this method was used to verify the functionality of the proposed MLI when it is implemented into a STATCOM.

6.3.1 The Simulation Result

The application of the proposed topology in STATCOM is verified using the parameters tabulated in Table 6.8.

Table 6.8: The parameters used in the simulation

	Parameters	Value
Power source	Phase-to-Phase Voltage, V_{PH-PH}	104 V_{RMS}
	Frequency, f	50 Hz
NLC Modulator	Frequency, f	50 Hz
	Voltage source, V_{DC}	6.7 V
	Modulation index, m	1.0
	Number of output voltage level, n	51
STATCOM	Inductive load	122.61 x 10^{-3} H
	Resistive load	3.852 Ω

From this simulation, the voltage and current readings were recorded at the power source, STATCOM, and at the load. The phase difference between the voltage waveform and the current was observed and the simulation was conducted according to the block diagram illustrated in Figure 6.2.

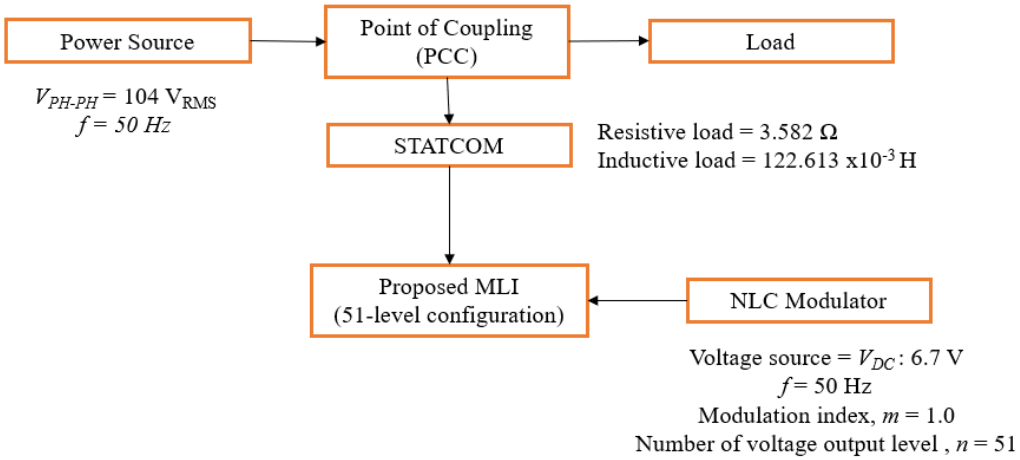

Figure 6.2: STATCOM simulation flowchart

Figure 6.3 shows the current and voltage reading obtained at the power source. The two inputs are in phase and reach a steady-state after 0.04 s. The waveform plotted in bold red line represents the voltage output while the waveform plotted in the dashed blue line is representing the current output. The THD percentage for the voltage is shown in Figure 6.4.

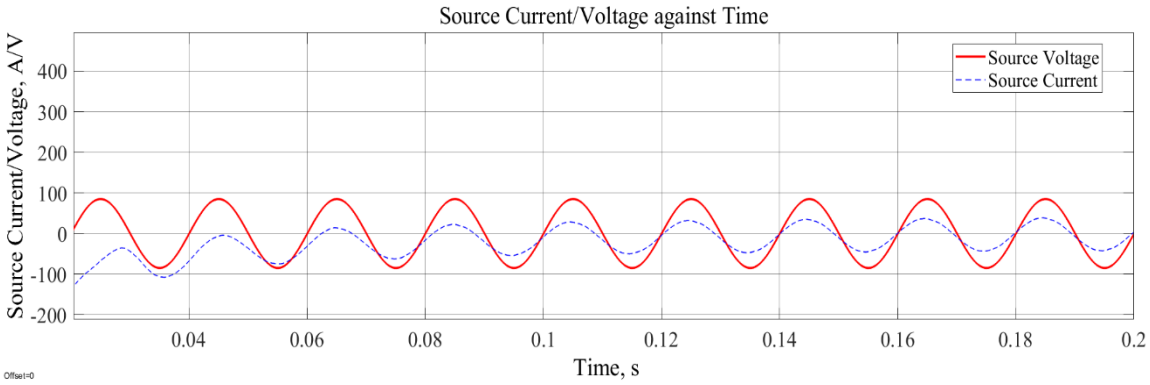

Figure 6.3: The voltage and current waveform at the source.

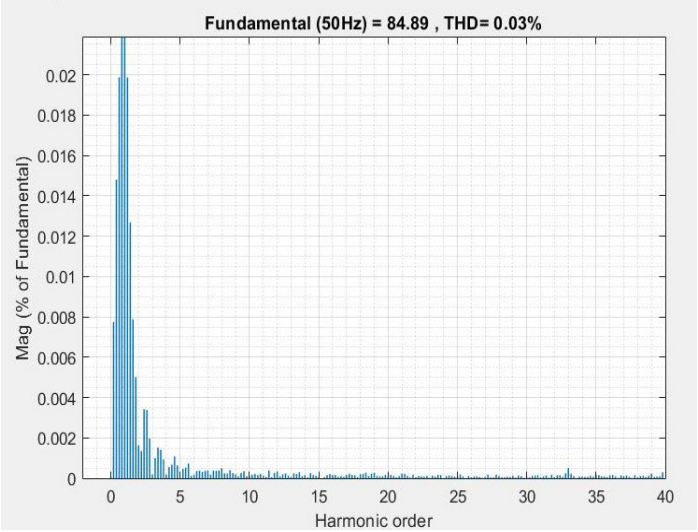

Figure 6.4: The THD percentage for voltage

Meanwhile, Figure 6.5 shows the voltage and the current waveform taken from the load. Note that the current (dotted blue waveform) is lagging the voltage (bold red waveform). This indicates the presence of inductive load. The THD voltage percentage is shown in Figure 6.6.

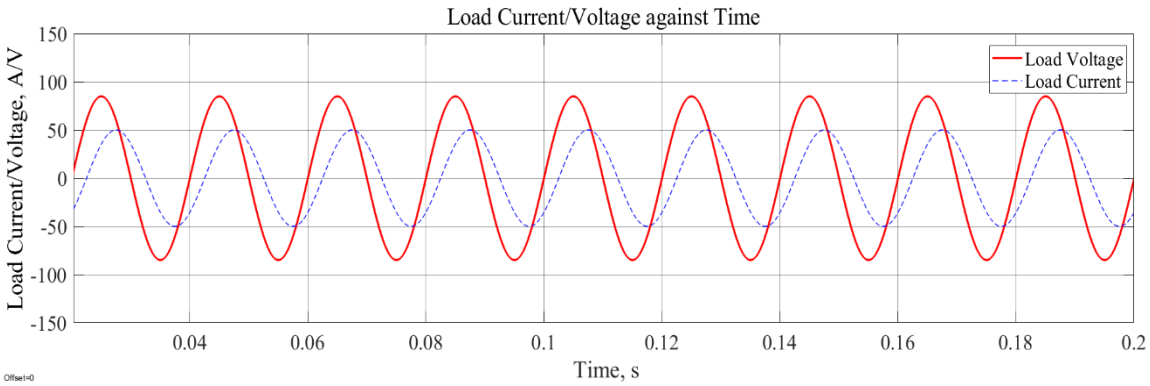

Figure 6.5: The voltage and current at the load

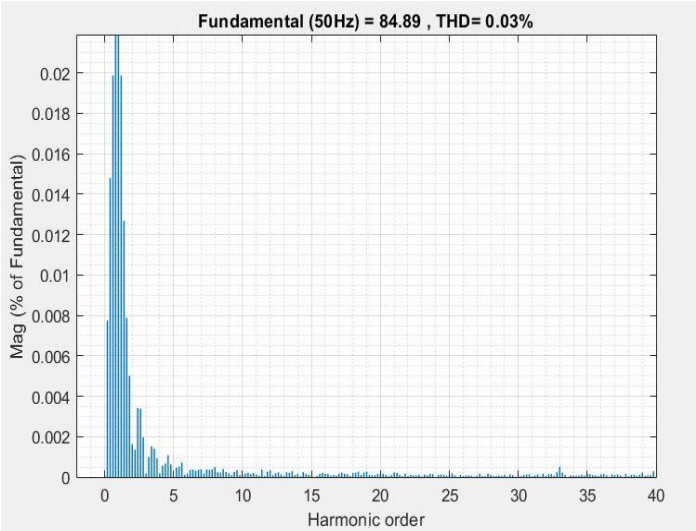

Figure 6.6: The THD percentage for voltage

Since it is impossible to control what the load is consumed, STATCOM was implemented to maintain the stability of the system by injecting the necessary reactive current to ensure only active current exists in the power source. This is reflected in Figure 6.3 where the current and voltage waveform is in phase. This is equal to a unity PF.

The voltage and current waveform at STATCOM is shown in Figure 6.7. The step-like waveform is given by the 51-level configuration that was implemented in this system. Note that the current is lagging the voltage. This indicates the reactive current.

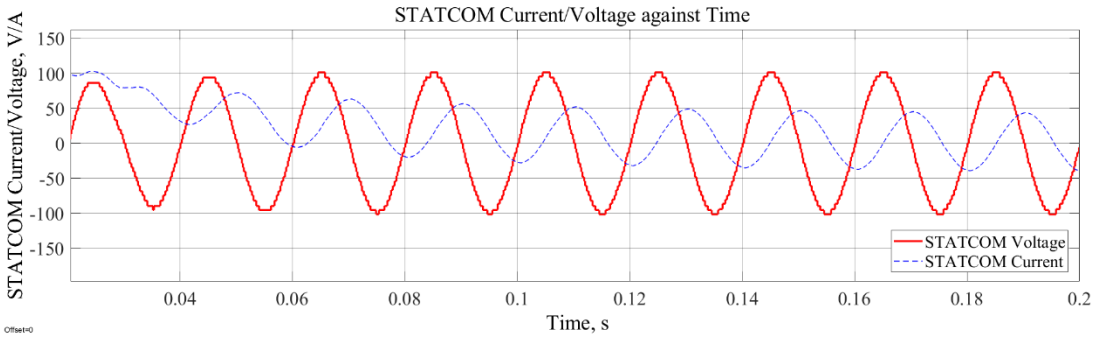

Figure 6.7: The current and voltage waveform at STATCOM

6.4 Conclusion

In summary, the proposed topology also has catered to the limitations of the conventional MLIs and has improved the limitations found in the recently presented topology, especially in terms of complexity. The component counts of the proposed topology are relatively lower than the others. It does not need to be cascaded to achieve a 51-level of voltage output or require any additional circuit when configured asymmetrically.

The asymmetrical implementation does not require complicated calculations. As cascading is not required, the complexity and the system size can be reduced. It is easy to comprehend, implement, and troubleshoot. Using the isolated DC source also makes it possible for the circuit to be cascaded like other recently presented topologies but that area is yet to be verified in this study.

The proposed topology is also proved to be capable to be implemented in a STATCOM and has been verified by the simulation. It is worth noting that its ability to produce a high level of voltage output (i.e., 51-level) has significantly reduced the THD percentage. Plus, the high level of voltage output also has eliminated the need for a transformer.

Chapter 7:
Conclusion & Recommendation

7.1 Chapter Introduction

This chapter presents the conclusion of this research study. The study is to propose a topology that produces a higher level of output voltage with a reduced number of components. This results in a compact configuration, a simple operation, and a high-quality output. The proposed topology was verified with simulations and experimental testing. It also was compared with the conventional MLIs and recently proposed topologies to demonstrate the novelty of the study.

7.2 Conclusion

This study is to propose a topology that produces a higher level of output voltage with a reduced number of components. It used isolated DC sources like CHB-MLI to eliminate the problem with voltage balancing, clamping diodes like in DC-MLI to induce more voltage steps, and floating switches like being applied in CCS-MLI. The MLI was verified with simulation and experimental testing.

The topology consists of 4 isolated DC sources, 4 diodes, and 10 switches. It was configured with equal (symmetrical) and unequal (asymmetrical) DC sources. This results in 9-level, 13-level, and 17-level of output voltage. The proposed topology was also hybridized with a unit of H-MLI. This configuration consists of 5 isolated DC sources, 4 diodes, and 14 switches. It can be configured with equal and unequal DC sources but this study only focused on asymmetrical configuration. The configuration produced 51-level of output voltage with an output waveform close to sinusoidal.

The performance of the proposed topology was verified using Matlab/Simulink simulation and experimental testing. Overall, the proposed topology has successfully increased the level of output voltage which results in a better quality of output. In the ideal modulation, the THD percentage for 9-1evel and 13-level configurations is over 5%. It is over the standard limit set by IEEE but the figure is somehow lower than the other topologies. The THD percentage for 17-level and 51-level configurations, the THD percentage is below 5%. It is important to keep the THD percentage below 5% as this is the standard set by IEEE for applications below 69 kV. An output filter is

required to lessen the THD percentage beyond the stipulated level. This additional component will increase the number of components.

To ensure the novelty of this study, the proposed topology was compared with the conventional MLI and recently proposed MLI. The comparison was made in terms of the total number of components, the total level of output voltage, and the THD percentage. Generally, the proposed topology used fewer components than the conventional MLIs. But, the number of components used by CHB-MLI is comparable to the proposed topology to produce a 9-level of output voltage. The number of components was further reduced when using unequal voltage sources (Sangram, 2021).

As for the recently proposed topology, the number of component counts is comparable to the proposed topology. The purposed topology is aced in terms of the structure, operation, and THD percentage. As compared to the others, the proposed topology's operation and its structure are simpler. This makes it user-friendly. But, the proposed topology is not convenient to cascade to increase the level of output voltage, unlike the others. The number of components will increase drastically if it is cascaded. Thus, a new and detailed algorithm needs to cascade it.

In summary, the merits of the proposed topology are listed as follows;

- Used less number of components to yield up to 51-level of output voltage. The output voltage has a waveform close to a sinusoidal waveform (i.e., ideal AC waveform). Hence, the system does not require a transformer.
- The higher level of output voltage leads to a lower THD percentage (i.e., within the stipulated IEEE standard for 17-level and 51-level configuration) that reflects an improvement in power quality. Therefore, the output filter does not require in the system.

Reduced component counts, transformerless systems, and the elimination of output filters decrease the system size, complexity, and production cost. These features are attractive especially when it is designed for public use. In addition, a compact system will also reduce losses like conduction losses, switching losses, and cabling losses. This increase the reliability and the stability of the proposed topology, thus making it a favorable solution for consumer applications such as electrical vehicles (EV), air conditioners, water pump, and inverters for off-grid RES generations.

7.3 Recommendation for Improvement

There are a few parts of the proposed topology that need to be improved to increase its performance and effectiveness. The limitations found in this study are listed as follows;

1. The voltage stress in the 9-level configuration is not evenly distributed especially for switches in Part B that are S_5, S_6, S_7, and S_8.
2. The voltage stress at S_9 and S_{10} (cross-connected switches) and switches in H-bridge MLI are higher compared to other switches.
3. The number of isolated DC sources required is still high.
4. The THD percentage recorded for experimental testing in loading condition is higher than in simulation.

It is important to ensure the voltage stress is evenly distributed to avoid the switch from overwork and increasing the power loss. Using different modulation techniques might be possible to improve the voltage distribution and reduce the voltage stress. In addition, using a capacitor bus also can help in distributing the voltage stress evenly. As for S_9 and S_{10}, the high voltage stress is unavoidable since these switches shared the voltage stress from Part A and Part B of the proposed topology. The same goes for the switches in H-bridge MLI where the voltage ratio assigned to the DC voltage source is way higher than those in the proposed topology. Hence, power switches with higher rated voltage are required for these switches.

The use of isolated DC sources will be convenient when the DC voltage source is readily available like solar PV. In this situation, the proposed topology also can be cascaded to further increase the total number of voltage output levels. The structure will surely expand, thus more calculations will be needed to calculate the increasing the components' counts. Hence, a set of mathematical formulas is required to ease the calculation. In the case where the DC source is limited, a capacitor bus can be used. However, a proper study needs to be done before introducing the capacitor bus as it comes with a voltage balancing problem that may threaten the reliability of the system.

Meanwhile, the THD percentage can be improved by using an output filter. This is a classical method to deal with this problem. It is effective but adding a filter might increase the system size. Another approach is by using different modulation techniques. THD percentage varies with modulation technique, but the modulation

technique itself has its share of pros and cons. Hence, a proper study needs to be done to determine which modulation technique is the best to improve the THD percentage.

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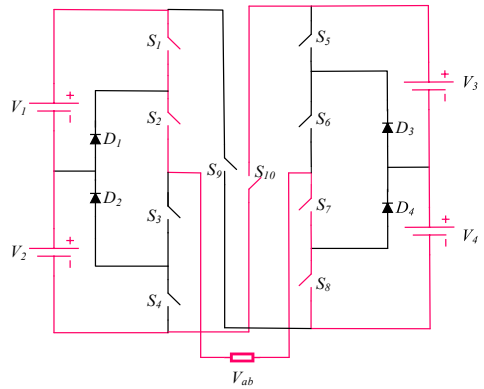
Appendix A – *Switching Modes for 9-level Configuration*



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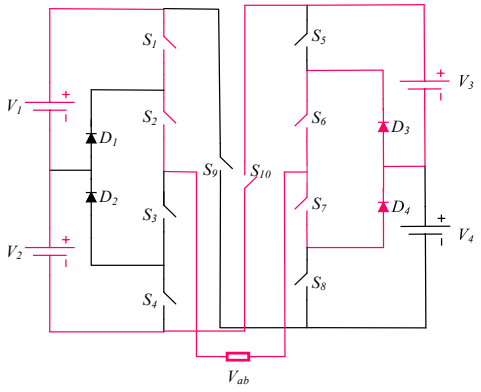

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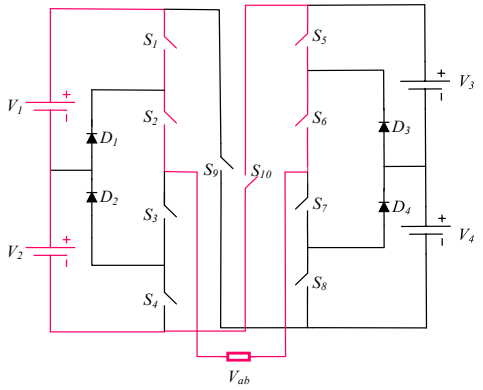

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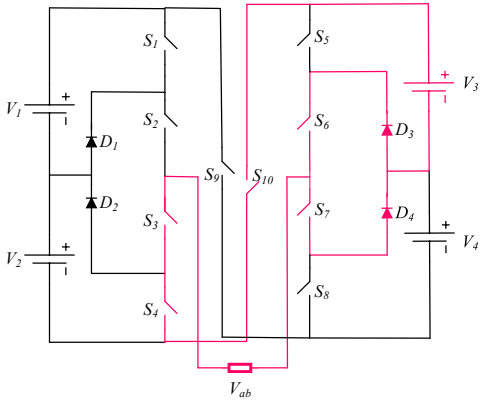
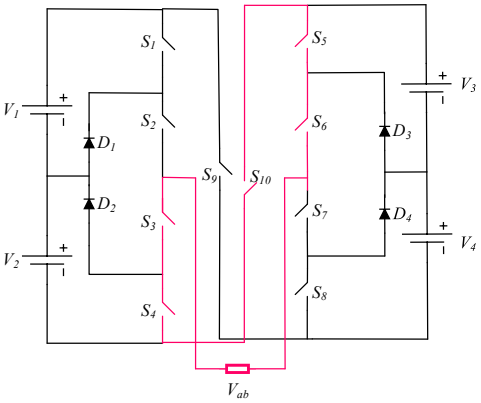


$+V_{DC}$



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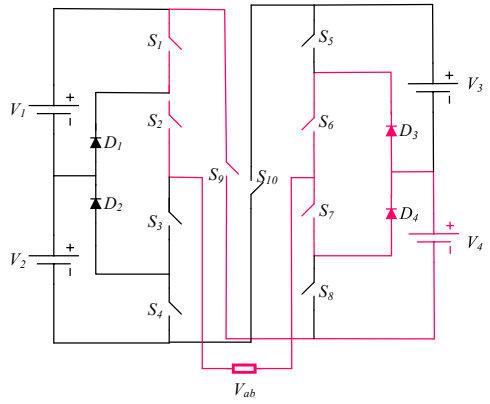
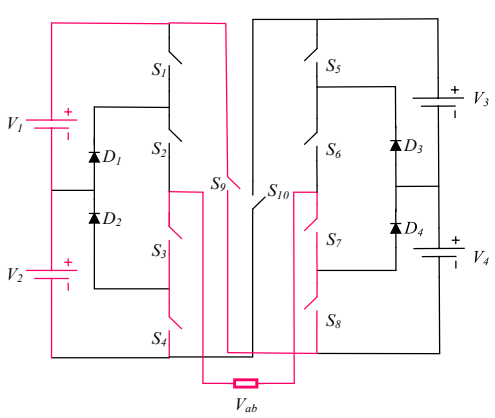


$-V_{DC}$



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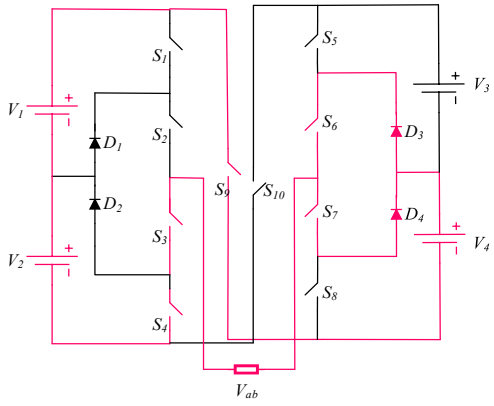

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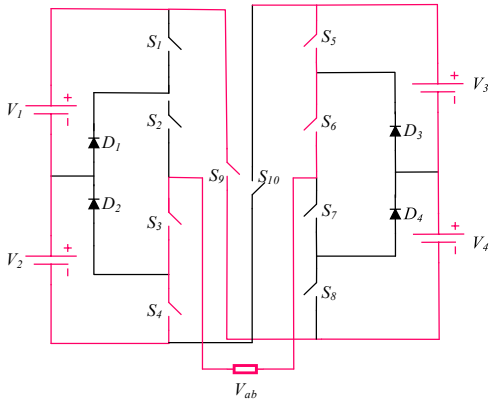

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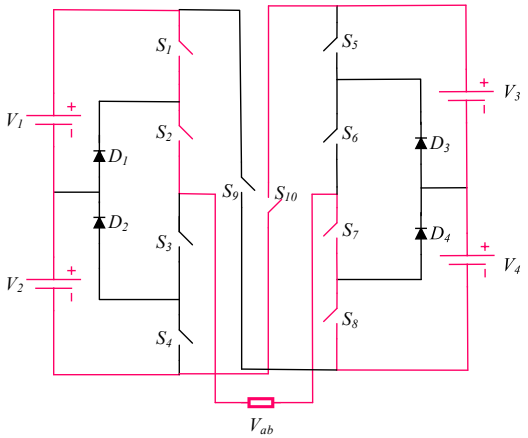
Appendix B – *Switching Modes for 13-level Configuration*



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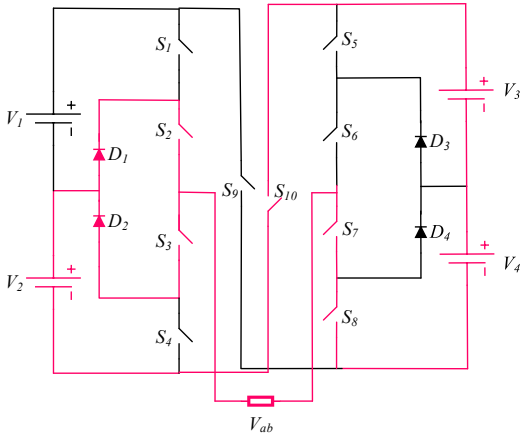
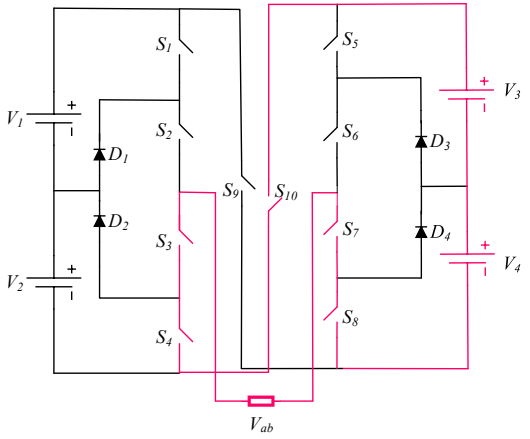
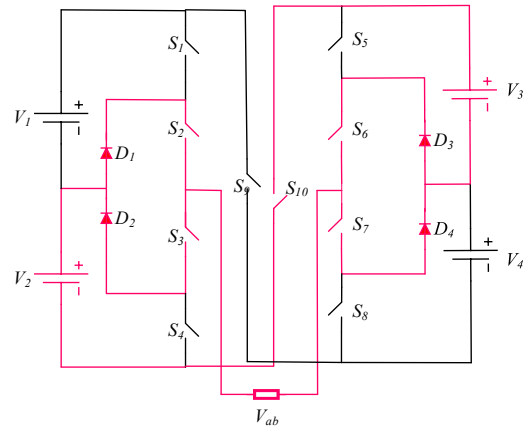


$+5V_{DC}$



$+4V_{DC}$



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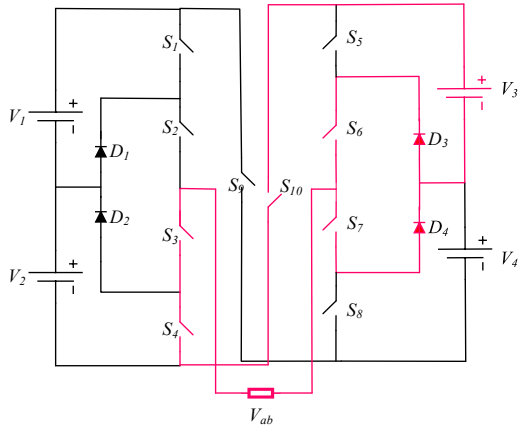

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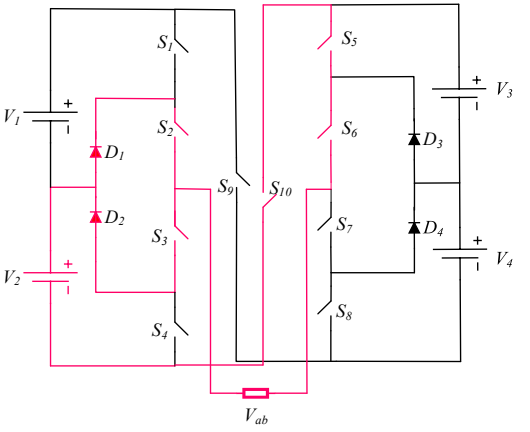

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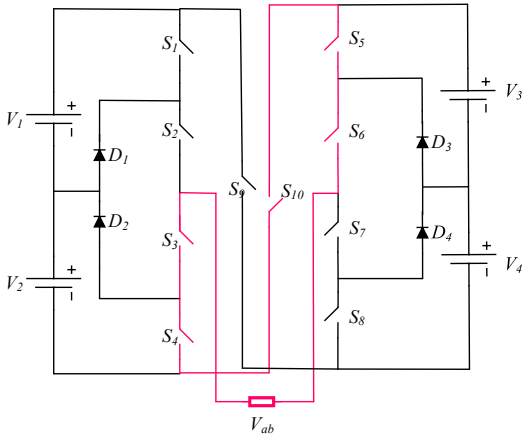

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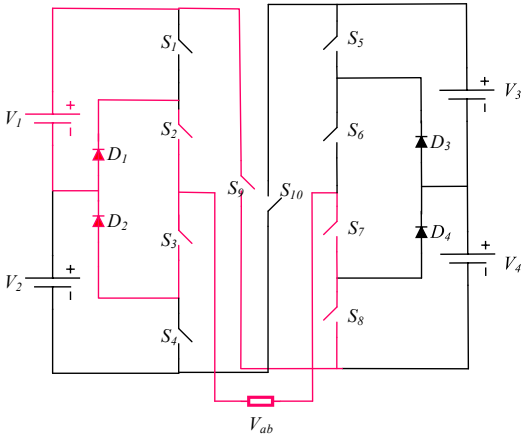
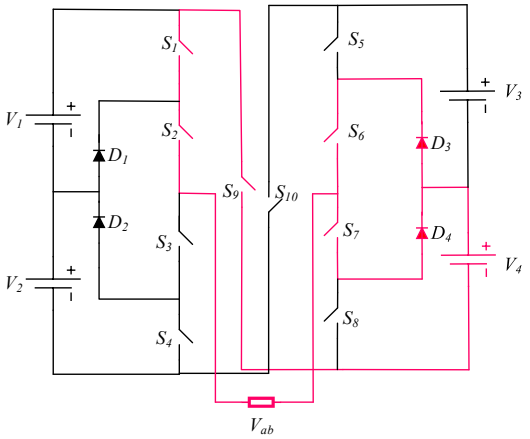
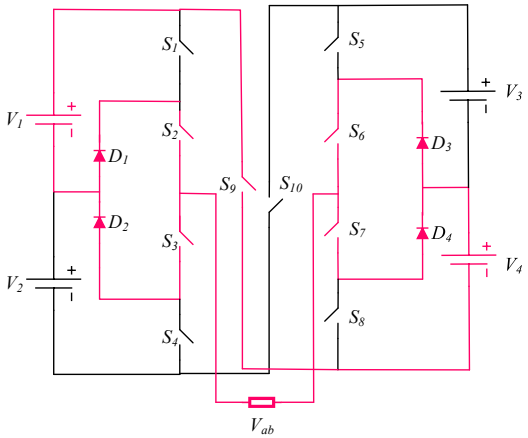


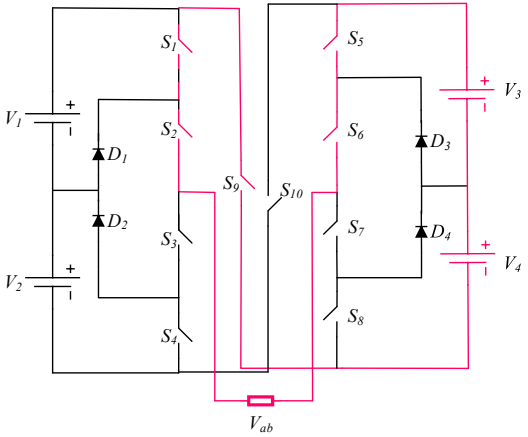
$-V_{DC}$



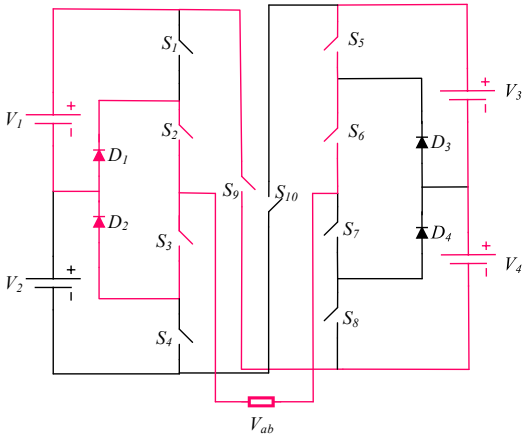
$-2V_{DC}$



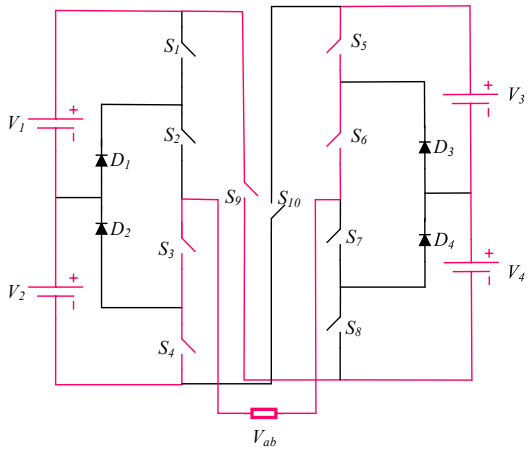
$-3V_{DC}$



$-4V_{DC}$

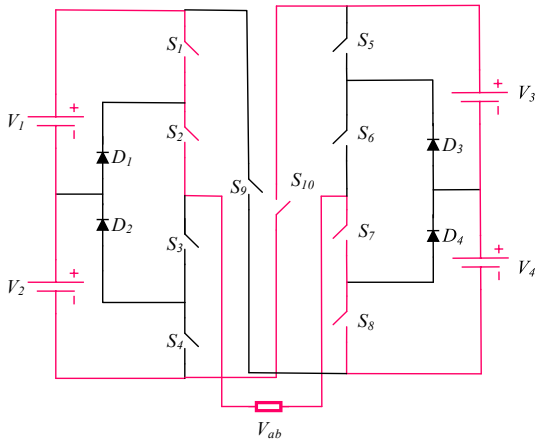


$-5V_{DC}$

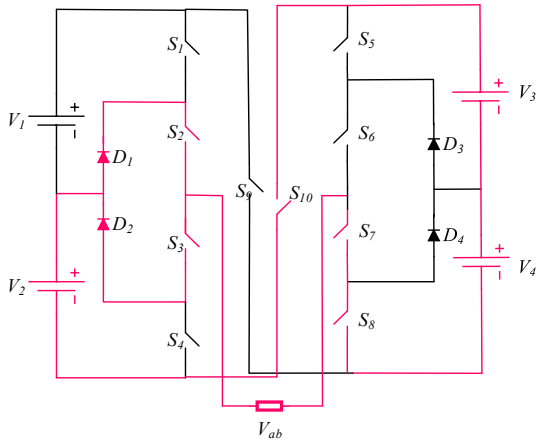


$-6V_{DC}$

Appendix C – *Switching Modes for 17-level Configuration*



$+8V_{DC}$



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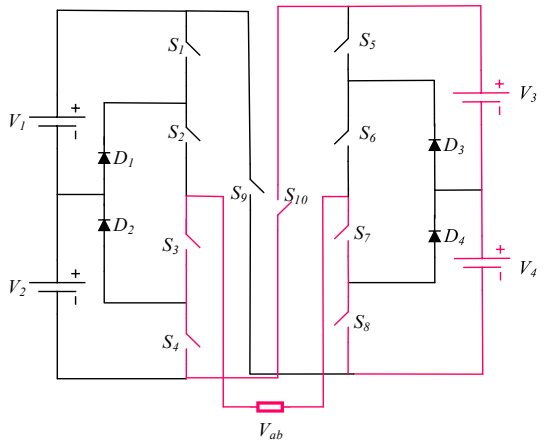
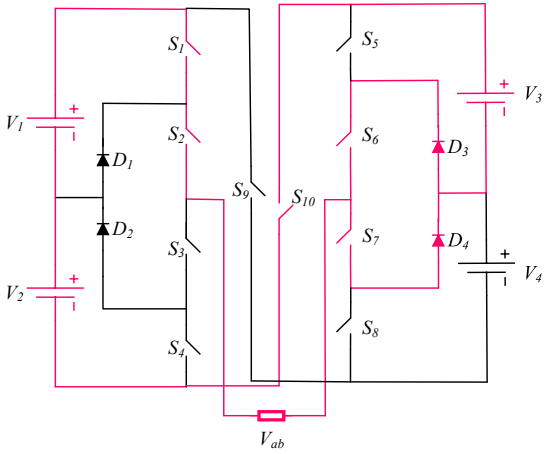
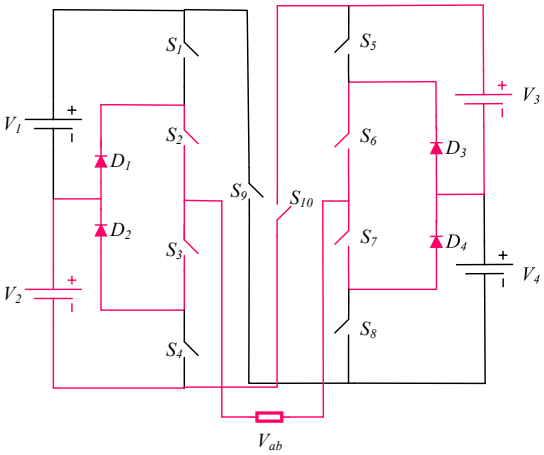


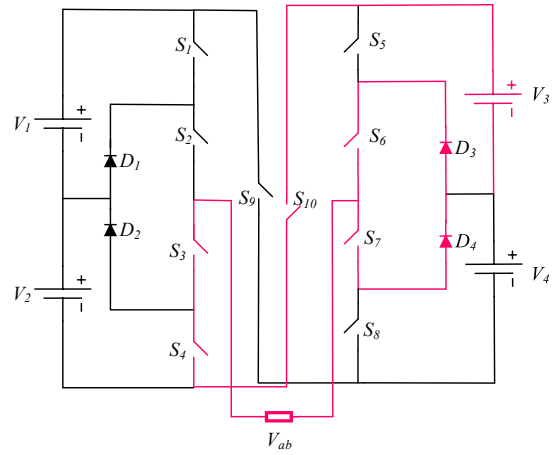
$+6V_{DC}$



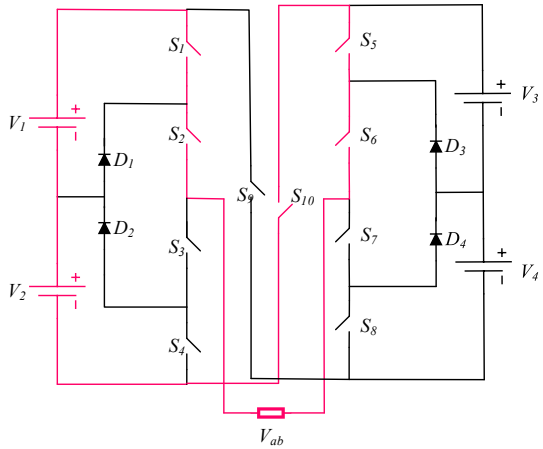
$+5V_{DC}$



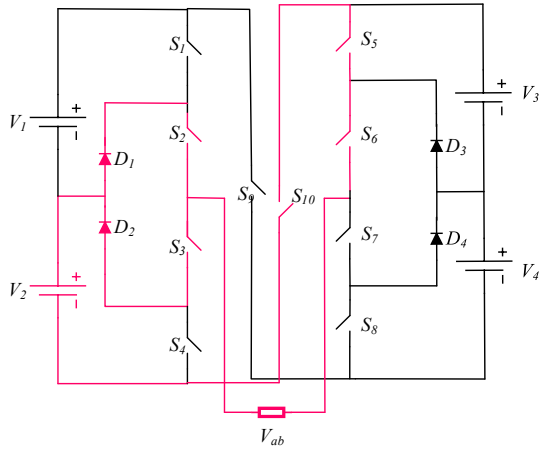
$+4V_{DC}$



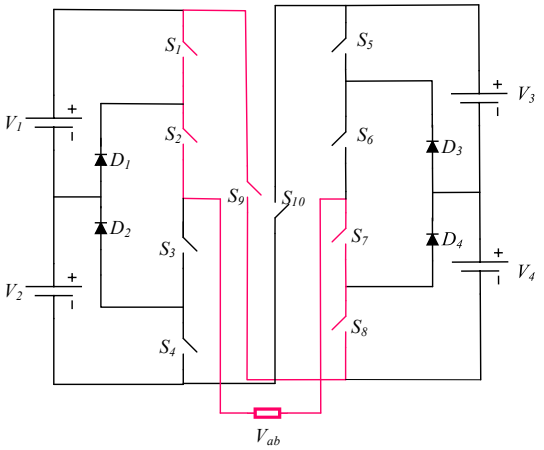
$+3V_{DC}$



$+2V_{DC}$



$+V_{DC}$



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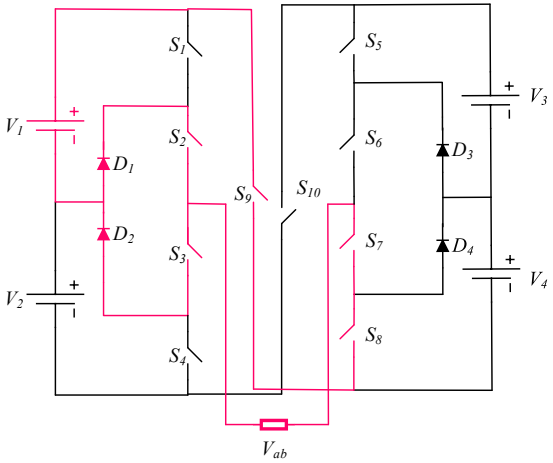

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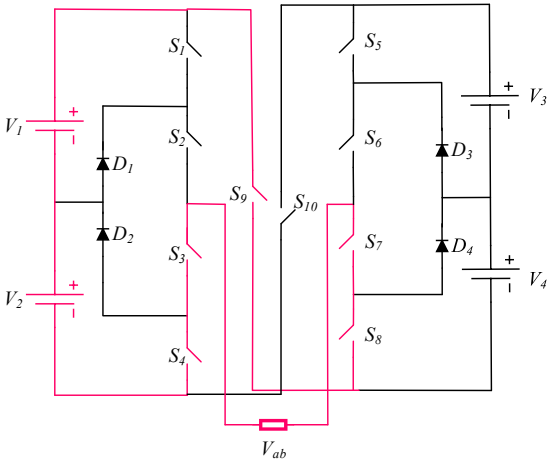

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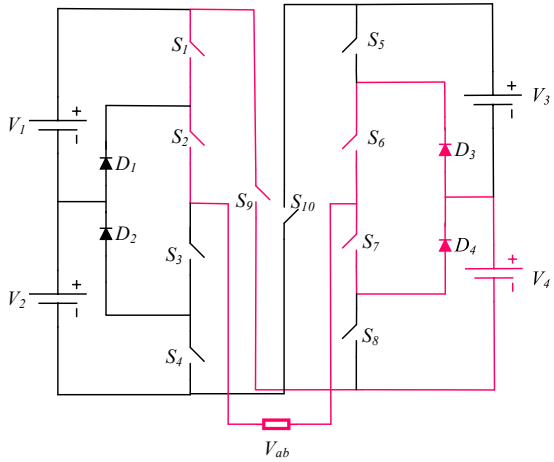

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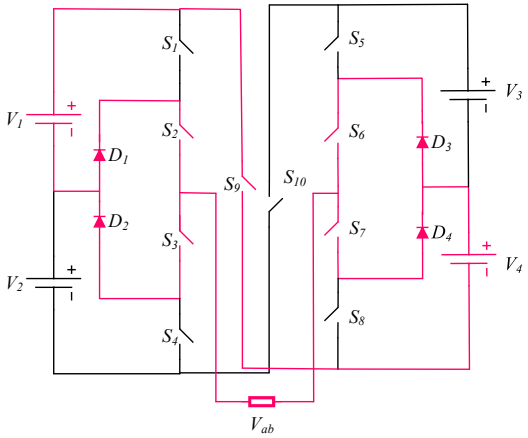

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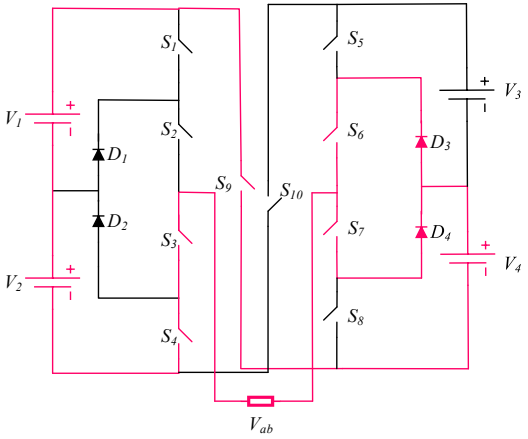
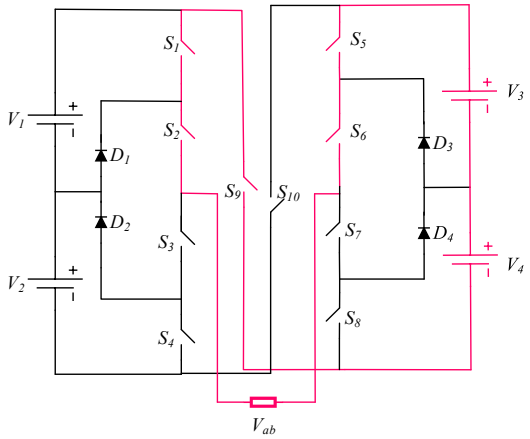
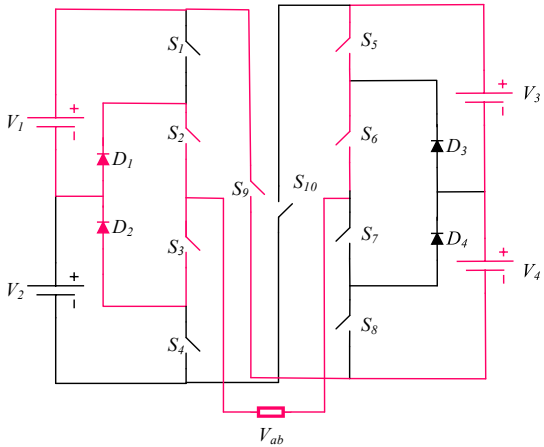


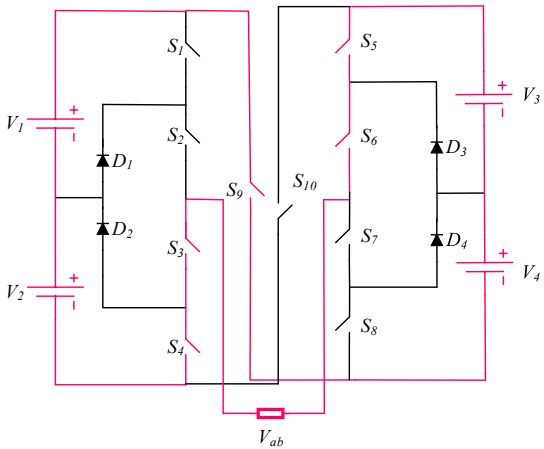
$-5V_{DC}$



$-6V_{DC}$

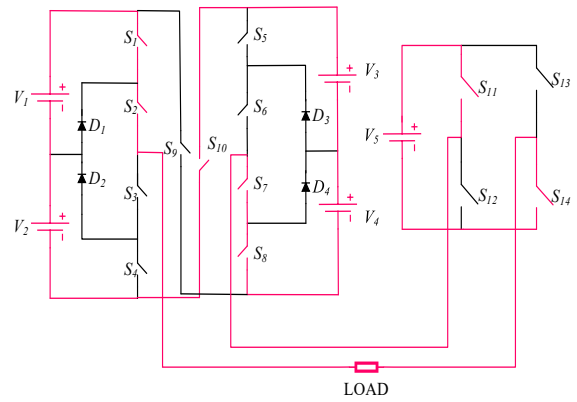


$-7V_{DC}$



$-8V_{DC}$

Appendix D – *Switching Modes for 51-level Configuration*



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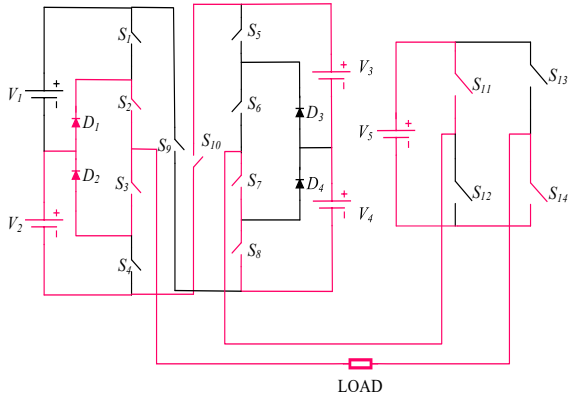
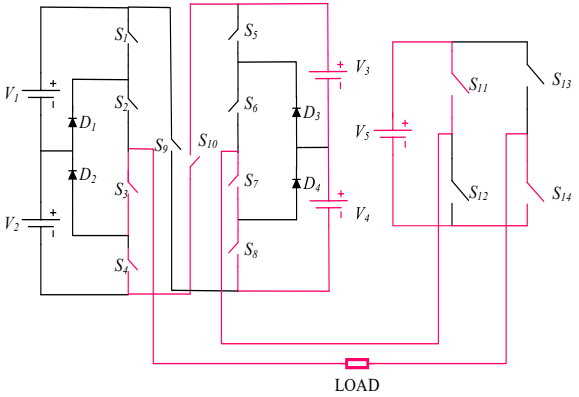
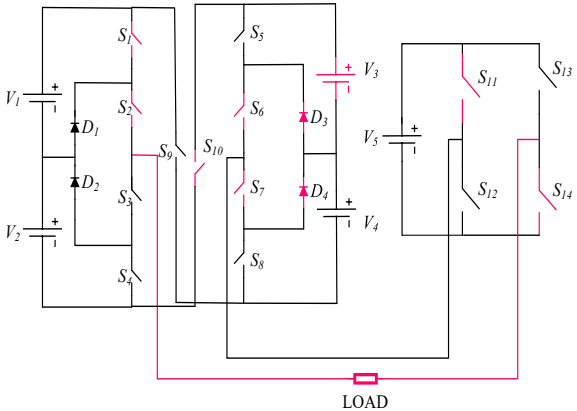


$+24V_{DC}$



$+23V_{DC}$



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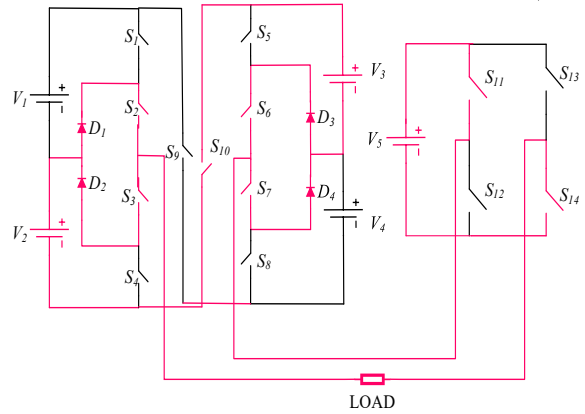
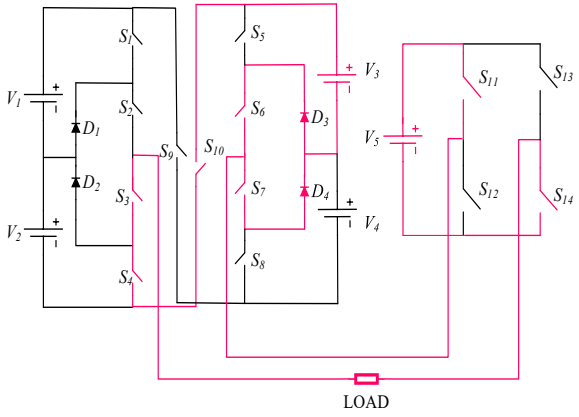
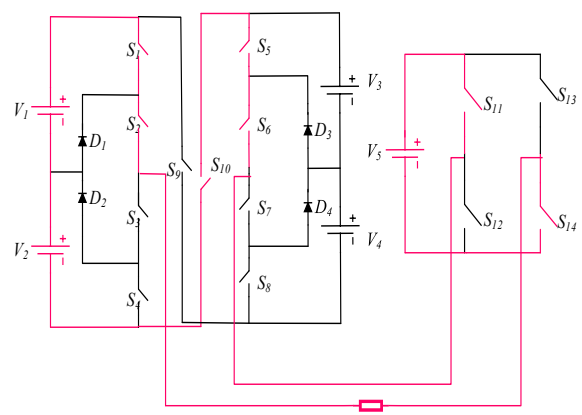


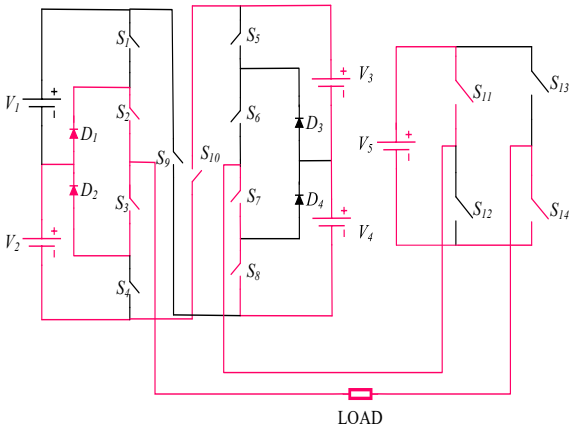
$+21V_{DC}$



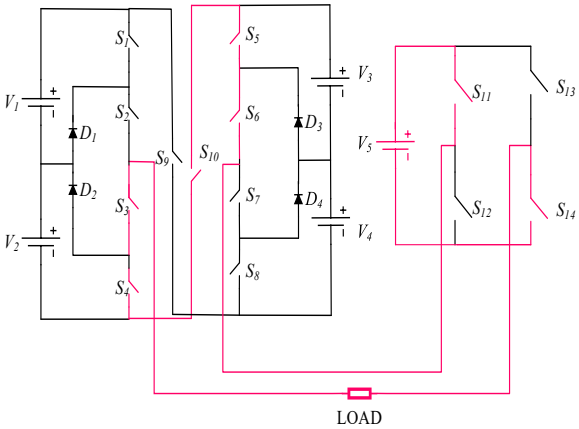
$+20V_{DC}$



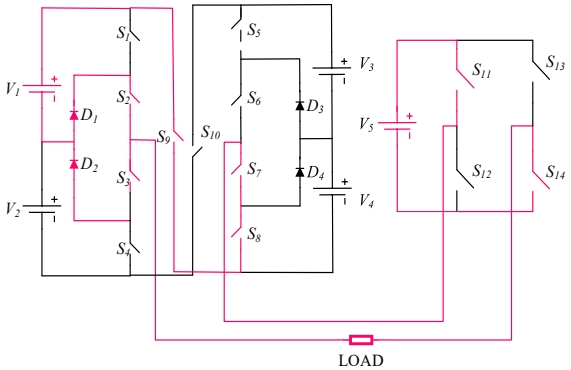
$+19V_{DC}$



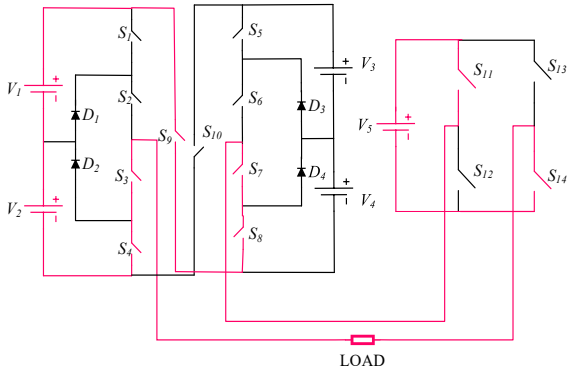
$+18V_{DC}$



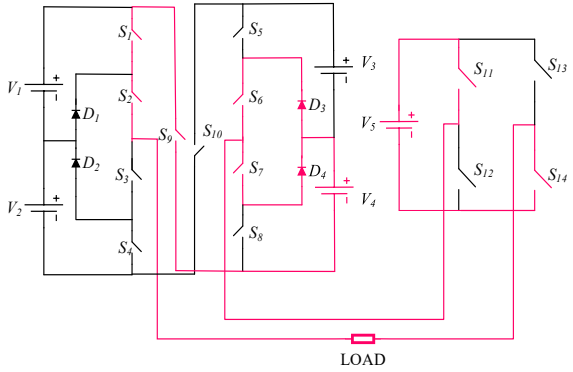
$+17V_{DC}$



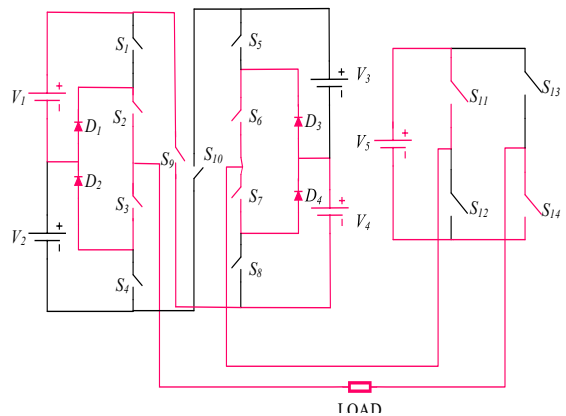
$+16V_{DC}$



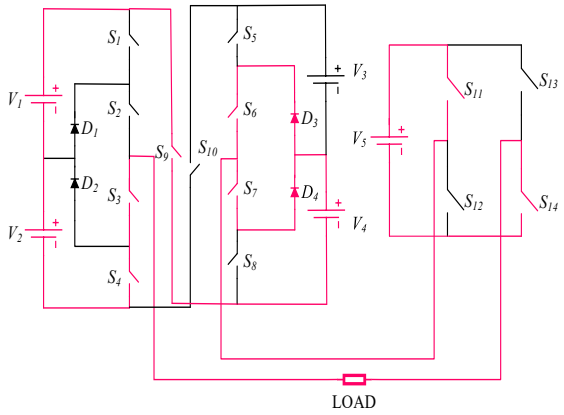
$+15V_{DC}$



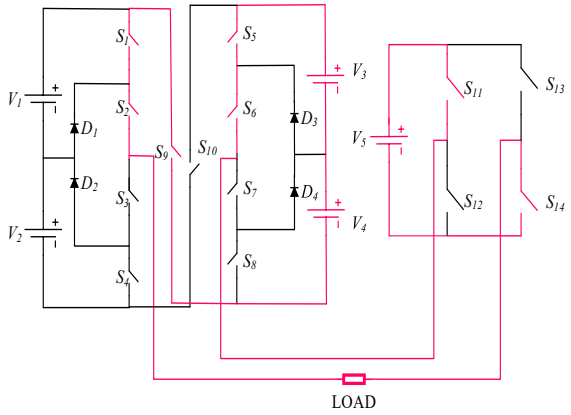
$+14V_{DC}$



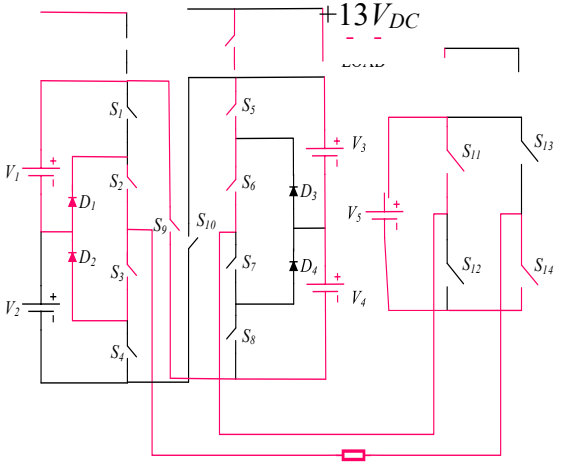
$+13V_{DC}$



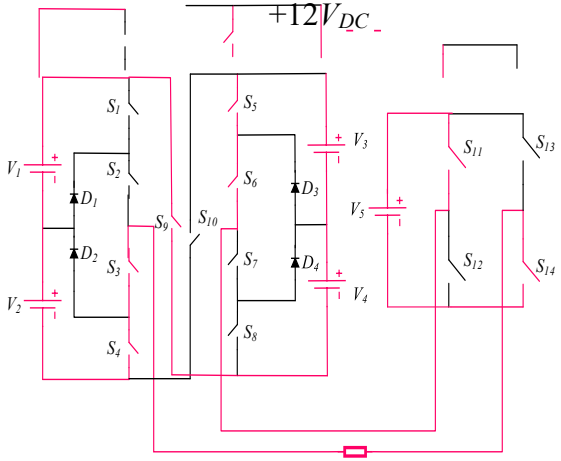
$+12V_{DC}$



$+11V_{DC}$



$+10V_{DC}$



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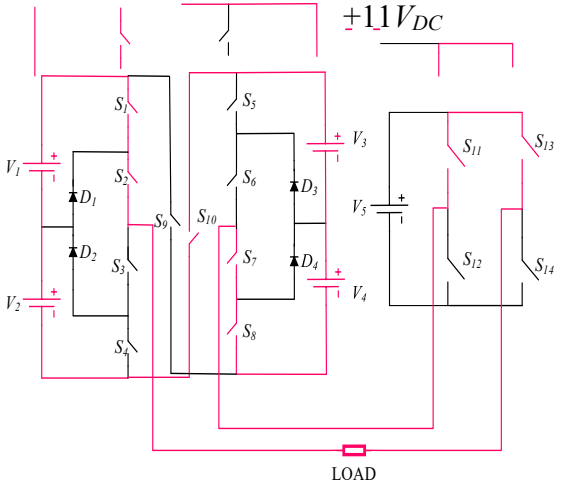

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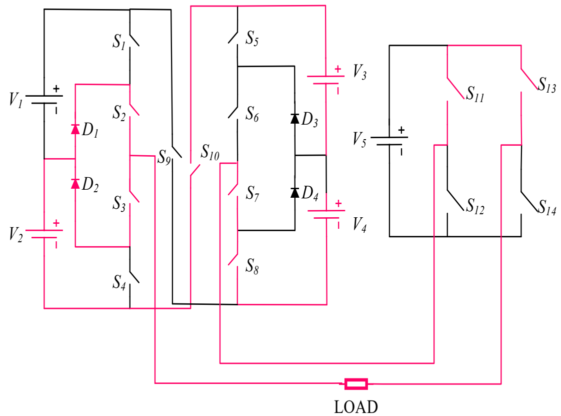
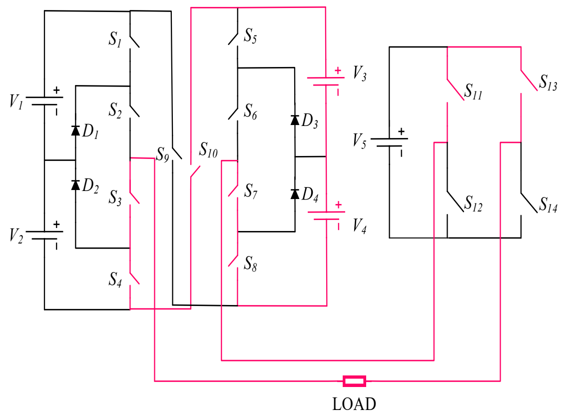
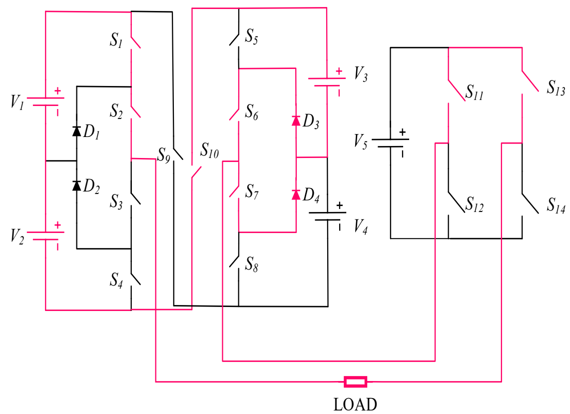


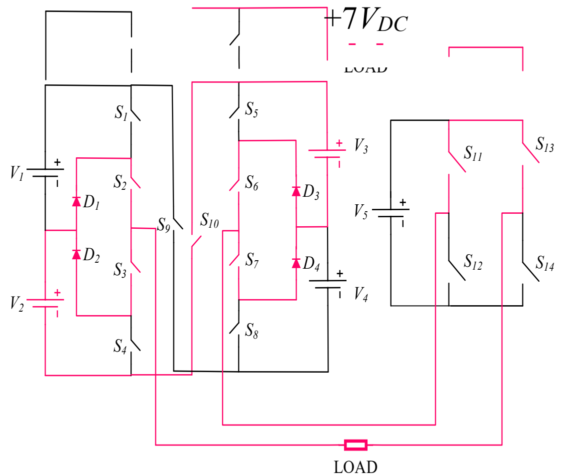
$+7V_{DC}$



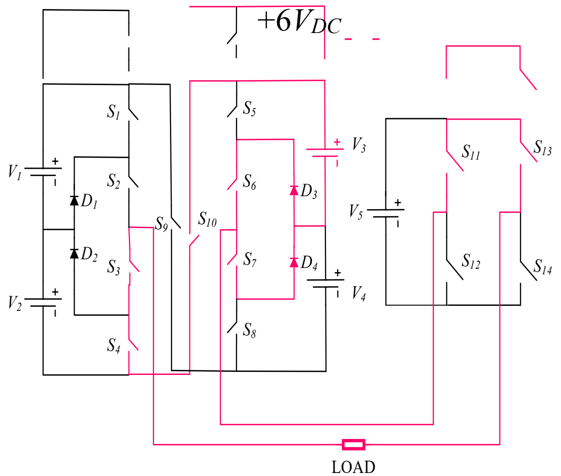
$+6V_{DC}$



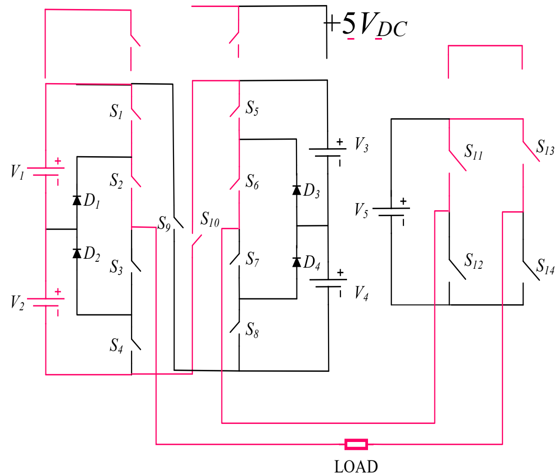
$+5V_{DC}$



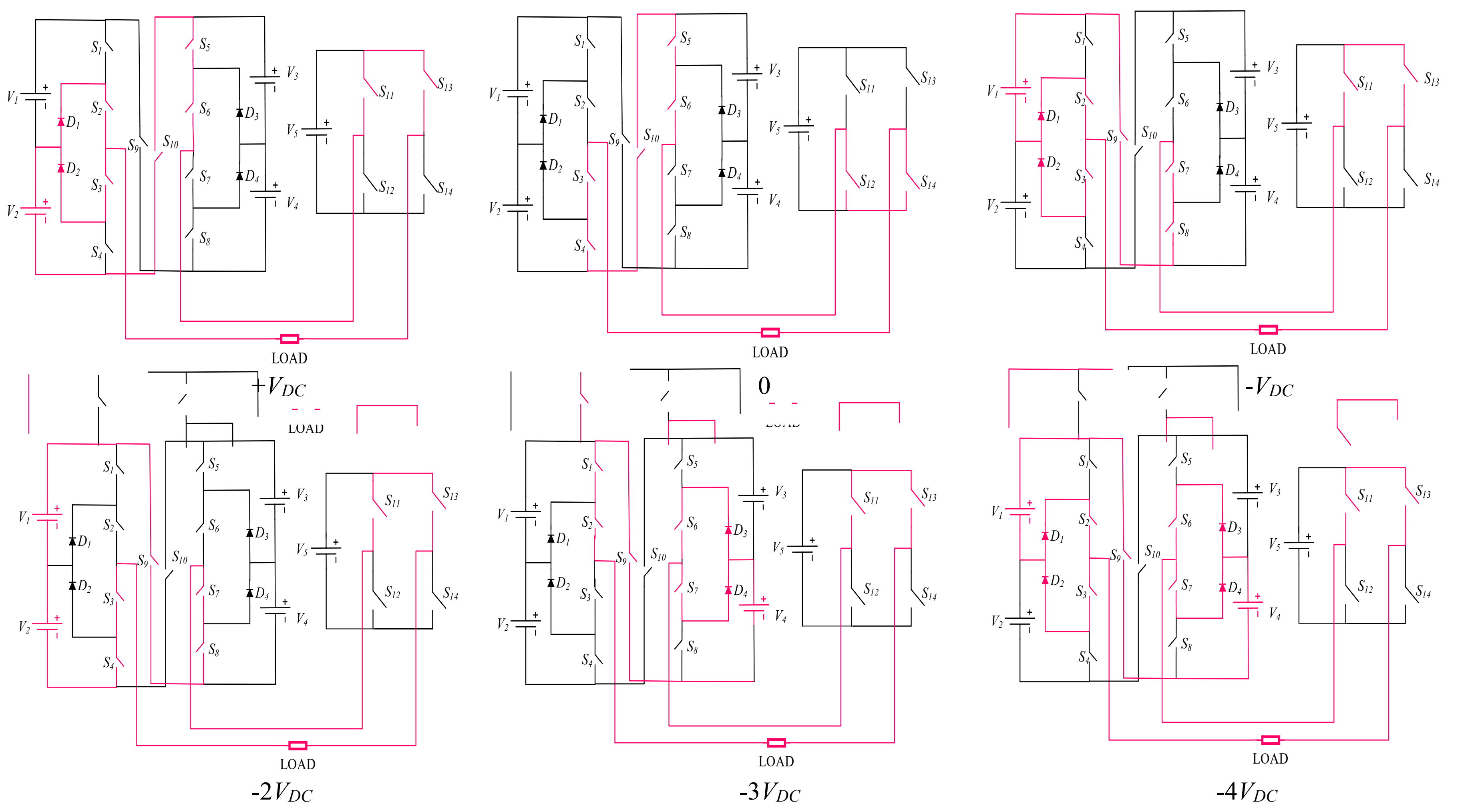
$+4V_{DC}$



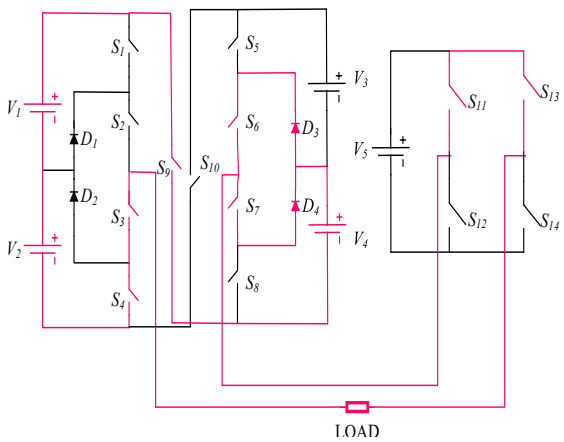
$+3V_{DC}$



$+2V_{DC}$



V_1 V_2 V_3 V_4 V_5
D_1 D_2 D_3 D_4
S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8 S_9 S_{10} S_{11} S_{12} S_{13} S_{14}
LOAD
$+V_{DC}$
LOAD
0
LOAD
$-V_{DC}$
LOAD
$-2V_{DC}$
LOAD
$-3V_{DC}$
LOAD
$-4V_{DC}$



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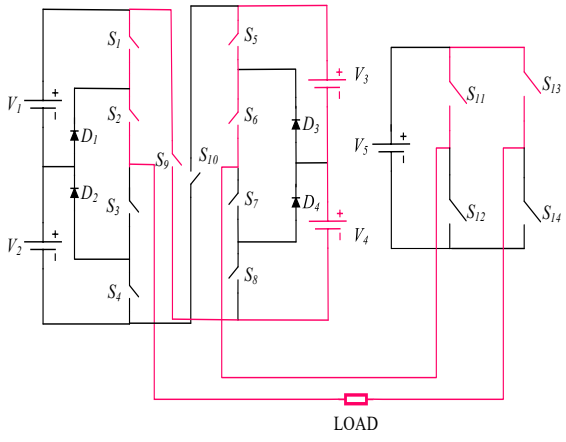

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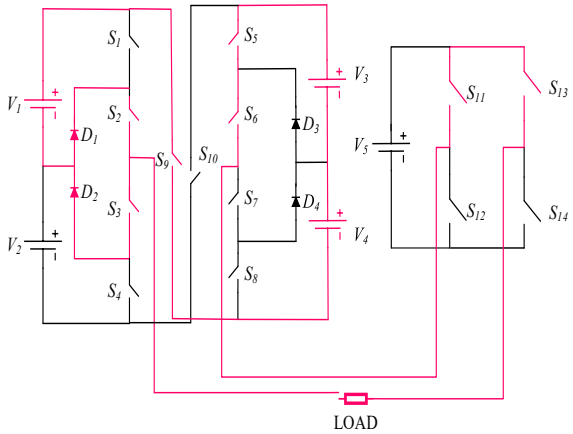

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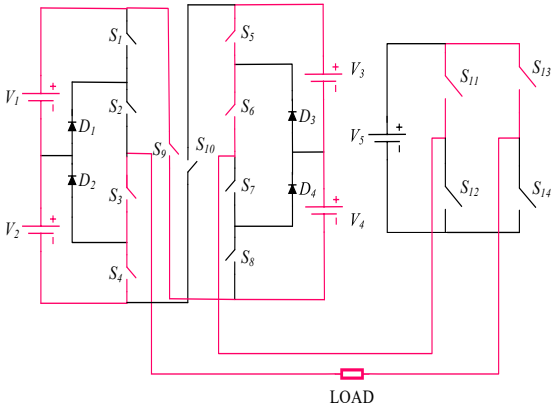

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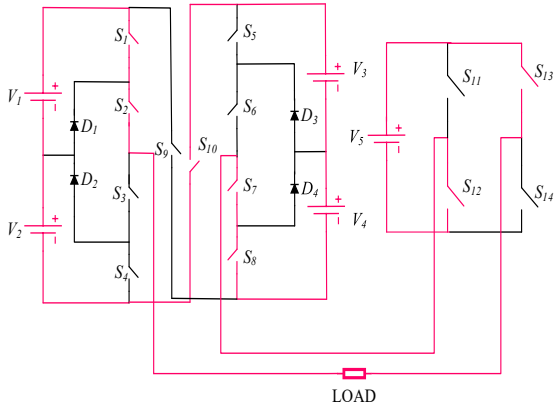

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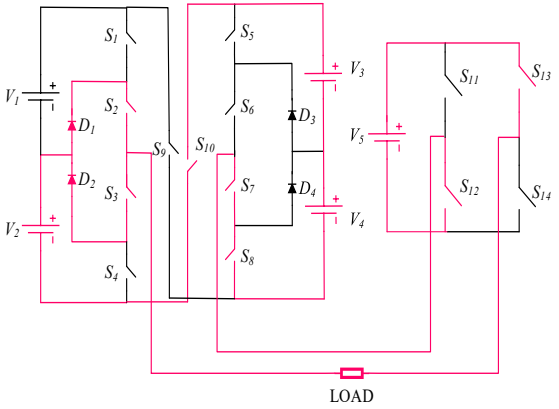

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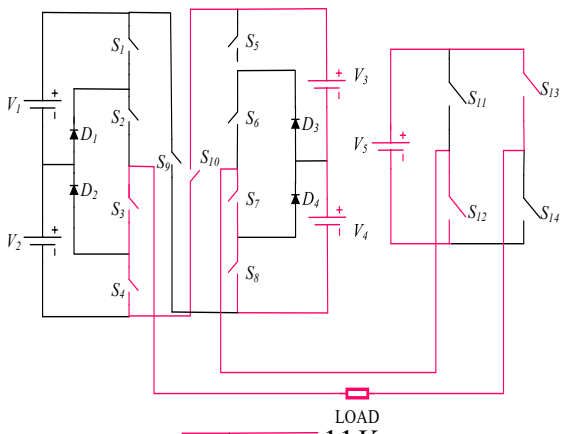
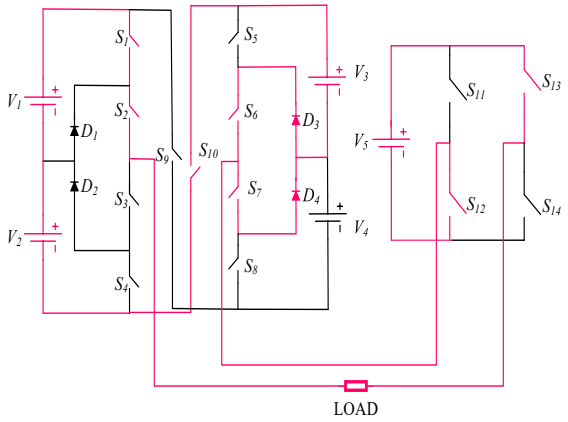
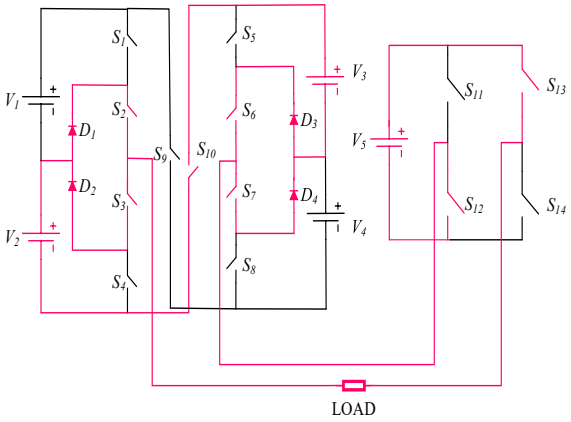


-11V_{DC}



-12V_{DC}



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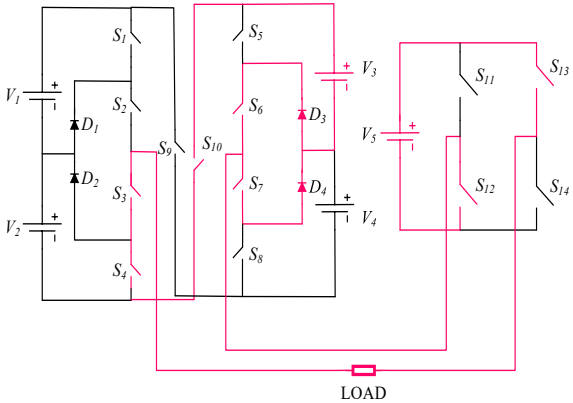

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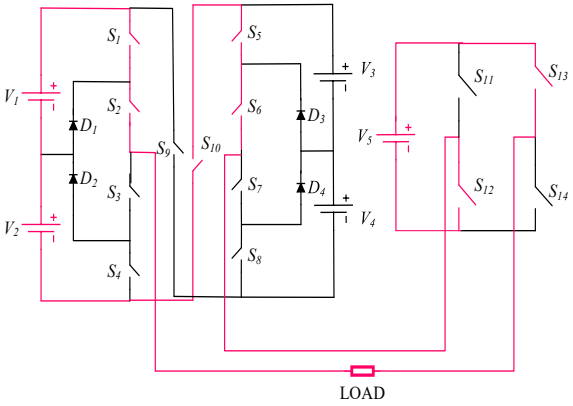
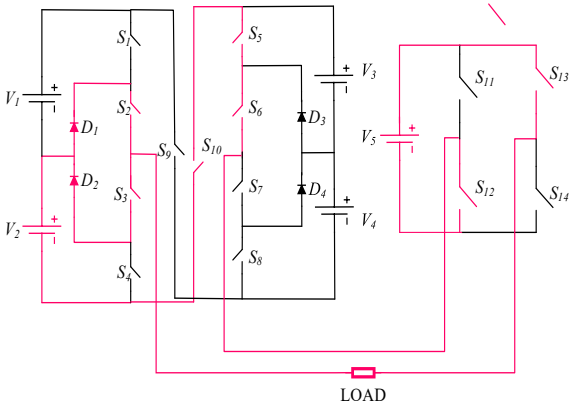
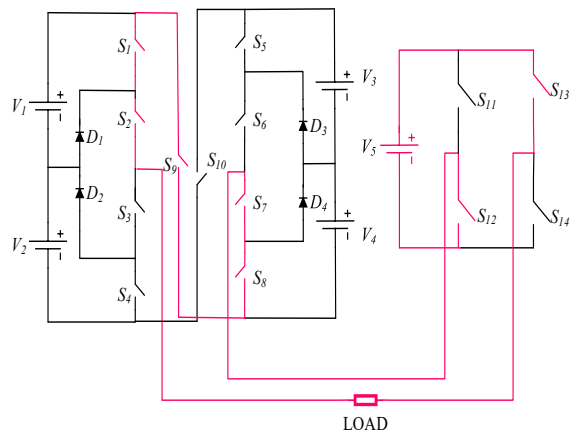


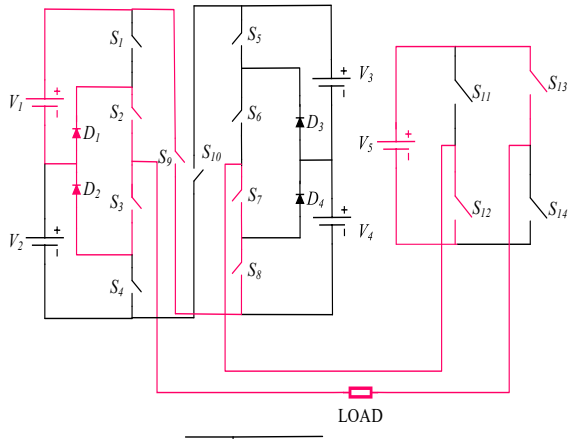
-15V_{DC}



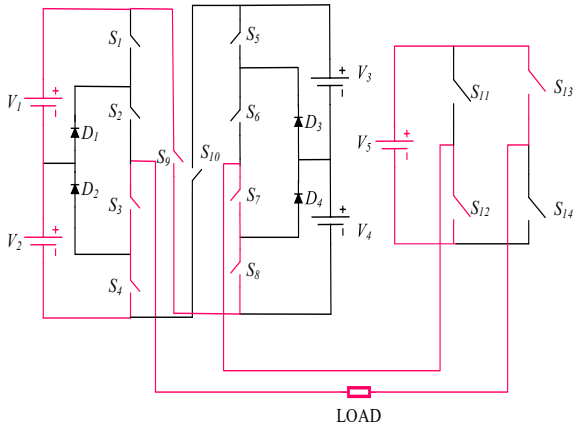
-16V_{DC}



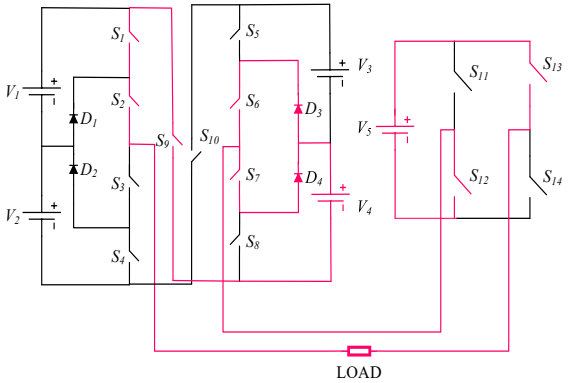
$-17V_{DC}$



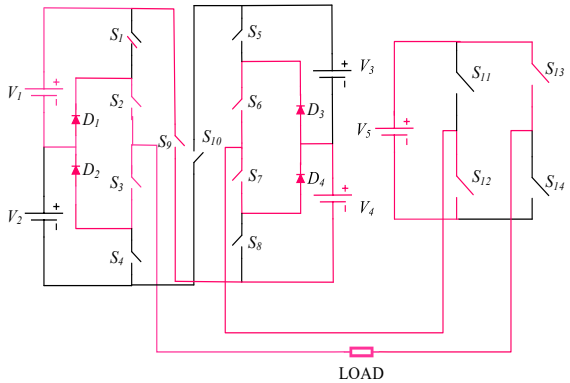
$-18V_{DC}$



$-19V_{DC}$



$-20V_{DC}$



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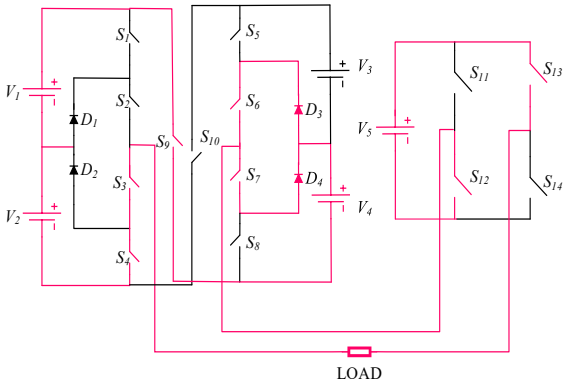
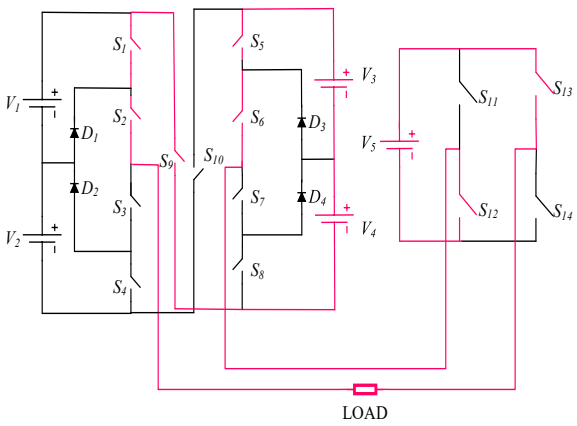


$-22V_{DC}$



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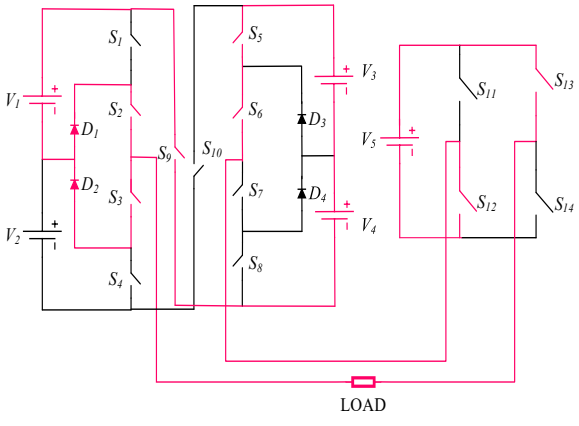
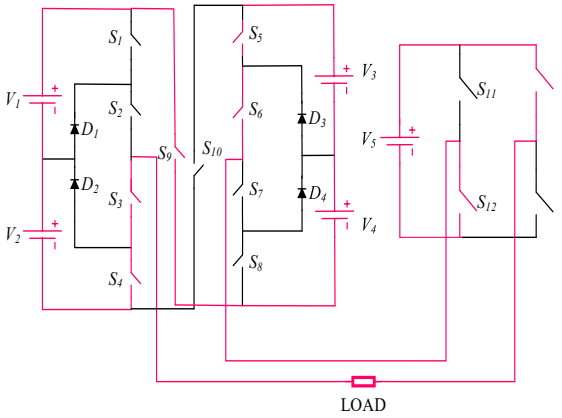


$-24V_{DC}$



$-25V_{DC}$